MX28F1000C

1M-BIT (128K x 8) CMOS FLASH MEMORY

FEATURES

- 131,072 bytes by 8-bit organization
- Fast access time: 90/120/150 ns
- Low power consumption
  - 50mA maximum active current
  - 100μA maximum standby current
- Programming and erasing voltage 12V ± 5%
- Command register architecture
  - Byte Programming (15μs typical)
  - Auto chip erase 5 seconds typical
    (including preprogramming time)
- Auto Chip Erase and Auto Program
  - DATA polling
  - Toggle bit

- 10,000/1,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1 to VCC+1V
- Advanced CMOS Flash memory technology
- Compatible with JEDEC-standard byte-wide 32-pin EPROM pinouts
- Package type:
  - 32-pin plastic DIP
  - 32-pin PLCC
  - 32-pin TSOP (Type 1)

GENERAL DESCRIPTION

The MX28F1000C is a 1-mega bit Flash memory organized as 128K bytes of 8 bits each. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX28F1000P is packaged in 32-pin PDIP, PLCC and TSOP. It is designed to be reprogrammed and erased in-system or in-standard EPROM programmers.

The standard MX28F1000C offers access times as fast as 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX28F1000C has separate chip enable (CE) and output enable (OE) controls.

MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX28F1000C uses a command register to manage this functionality, while maintaining a standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 10,000/1,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX28F1000C uses a 12.0V ± 5% VPP supply to perform the Auto
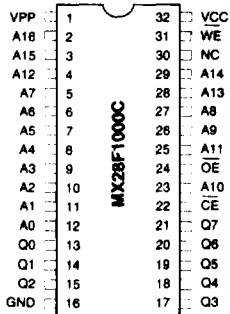
Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.
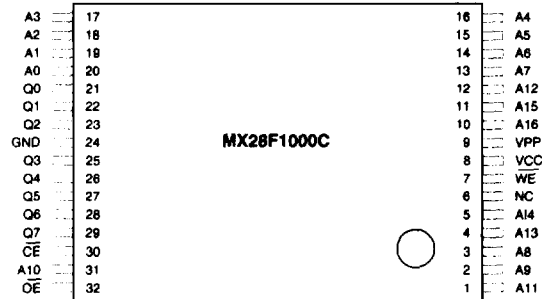

NOTICE:

MX28F1000C-XXC3(1,000 erase/program cycles) might exhibit an in-system failure rate of less than 1%.
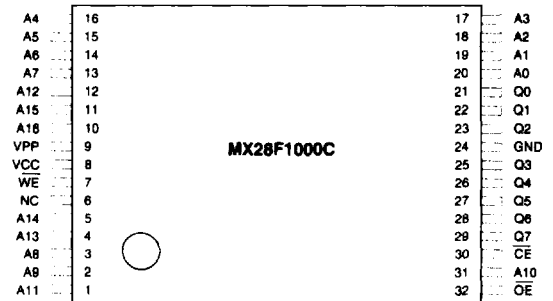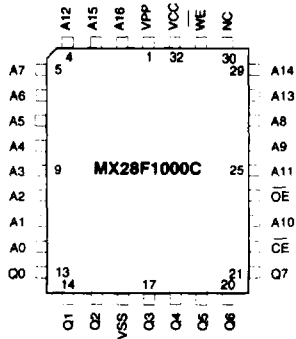

PIN CONFIGURATIONS

32 PDIP

VPP	1	32	VCC
A16	2	31	WE
A15	3	30	NC
A12	4	29	A14
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	OE
A2	10	23	A10
A1	11	22	CE
A0	12	21	Q7
Q0	13	20	Q6
Q1	14	19	Q5
Q2	15	18	Q4
GND	16	17	Q3

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32 PLCC

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Top pins: A12, A15, A16, VPP, VCC, WE, NC (4, 1, 32, 30)

Left		Right	
A7	5	29	A14
A6			A13
A5			A8
A4			A9
A3	9	25	A11
A2			OE
A1			A10
A0			CE
Q0	13	21	Q7

Bottom pins (14, 17, 20): Q1, Q2, VSS, Q3, Q4, Q5, Q6

TSOP (TYPE 1)

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A3	17	16	A4
A2	18	15	A5
A1	19	14	A6
A0	20	13	A7
Q0	21	12	A12
Q1	22	11	A15
Q2	23	10	A16
GND	24	9	VPP
Q3	25	8	VCC
Q4	26	7	WE
Q5	27	6	NC
Q6	28	5	AI4
Q7	29	4	A13
CE	30	3	A8
A10	31	2	A9
OE	32	1	A11

(NORMAL TYPE)

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A4	16	17	A3
A5	15	18	A2
A6	14	19	A1
A7	13	20	A0
A12	12	21	Q0
A15	11	22	Q1
A16	10	23	Q2
VPP	9	24	GND
VCC	8	25	Q3
WE	7	26	Q4
NC	6	27	Q5
A14	5	28	Q6
A13	4	29	Q7
A8	3	30	CE
A9	2	31	A10
A11	1	32	OE

(REVERSE TYPE)

PIN DESCRIPTION:

SYMBOL	PIN NAME
A0~A16	Address Input
Q0~Q7	Data Input/Output
CE	Chip Enable Input
OE	Output Enable Input
WE	Write enable Pin
VPP	Program Supply Voltage
VCC	Power Supply Pin (+5V)
GND	Ground Pin