November 2001 Advance Information



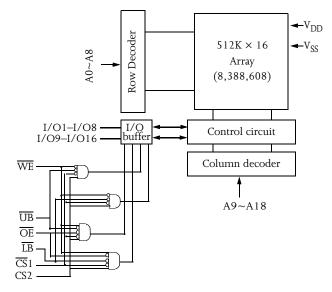
1.65V to 2.2V 512K × 16 IntelliwattTM Super Low-Power CMOS SRAM

Features

- AS6YB51216
- IntelliwattTM active power circuitry
- Industrial temperature range $(-40^{\circ} +85^{\circ} \text{ C})$
- Organization: 524,288 words x 16 bits
- 1.65V to 2.2V power supply range
- Fast access time of 70 ns
- Low power consumption: ACTIVE
- 33 mW max at 2.2 V and 70 ns

- Low power consumption: STANDBY
- 33 μW max at 2.2V
- 1.0V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{\text{CS}1}$, CS2, $\overline{\text{OE}}$ inputs
- Smallest footprint package
- 48-ball FBGA; 7.0 x 9.0 mm
- ESD protection ≥ 2000 volts
- Latch-up current \geq 200 mA

Logic block diagram



Pin arrangement (top view)

	48-CSP Ball-Grid-Array Package									
	1	2	3	4	5	6				
А	LB	OE	A0	A1	A2	CS2				
В	I/O9	UB	A3	A4	CS1	I/O1				
С	I/O10	I/O11	A5	A6	I/O2	I/O3				
D	V _{SS}	I/O12	A17	A7	I/O4	V _{CC}				
Е	V _{CC}	I/O13	V _{SS}	A16	I/O5	V _{SS}				
F	I/O15	I/O14	A14	A15	I/06	I/07				
G	I/O16	DNU	A12	A13	WE	I/08				
Η	A18	A8	A9	A10	A11	DNU				

Note: DNU = Do Not Use

Selection guide

	V _{CC} Range				Power Di	ssipation
	Min	Тур	Max	Speed	Operating (I _{CC1})	Standby (I _{SB1})
Product	(V)	(V)	(V)	(ns)	Max (mA)	Max (µA)
AS6YB51216	1.65	1.8	2.2	70/85	2	15

Functional description

The AS6YB51216 is a low-power CMOS 8,388,608-bit Static Random Access Memory (SRAM) device organized as 524,288 words x 16 bits. It is designed for memory applications where slow data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA} , t_{RC} , t_{WC}) of 70/85 ns are ideal for low-power applications. Active high and low chip enables ($\overline{CS}1$ and CS2) permit easy memory expansion with multiple-bank memory systems.

When $\overline{CS1}$ is high or CS2 is low, or \overline{UB} and \overline{LB} are high, the device enters standby mode. The AS6YB51216 is guaranteed not to exceed 33 μ W at 2.2V. The device also retains data when V_{CC} is reduced to 1.0V for even lower power consumption.

The device can also be put into standby mode when deselected ($\overline{CS1}$ is high or CS2 is low). The input/output pins (I/O0 through I/O15) are placed in a high-impedance state when deselected ($\overline{CS1}$ is high or CS2 is low), outputs are disabled (\overline{OE} High), \overline{UB} and \overline{LB} are disabled (\overline{UB} , \overline{LB} High), or during a write operation ($\overline{CS1}$ is low or CS2 is high and \overline{WE} Low).

Writing to the device is accomplished by taking Chip Enables $\overline{CS1}$ Low, CS2 High and Write Enable (\overline{WE}) input Low. If Byte Low Enable (\overline{LB}) is Low, then data from I/O pins (I/O0 through I/O7), is written into the location specified on the address pins (A0 through A18). If Byte High Enable (\overline{UB}) is Low, then data from I/O pins (I/O8 through I/O15) is written into the location specified on the address pins (A0 through A18). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable (\overline{OE}) or write enable (\overline{WE}).

Reading from the device is accomplished by taking Chip Enable $\overline{CS1}$ Low, CS2 High and Output Enable (\overline{OE}) Low while forcing the Write Enable (\overline{WE}) High. If Byte Low Enable (\overline{LB}) is Low, then data from the memory location specified by the address pins will appear on I/O0 to I/O7. If Byte High Enable (\overline{UB}) is Low, then data from memory will appear on I/O8 to I/O15.

These devices provide multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. LB controls the lower bits, I/O1–I/O8, and UB controls the higher bits, I/O9–I/O16.

All chip inputs and outputs are CMOS-compatible, and operation is from a single 1.65V to 2.2V supply. Device is available in the JEDEC 48-ball FBGA packages.

Parameter	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to V_{SS}	V _{tIN}	-0.5	V _{CC} + 0.5	V
Voltage on any I/O pin relative to GND	V _{tI/O}	-0.5		V
Power dissipation	P _D	_	1.0	W
Storage temperature (plastic)	T _{stg}	-65	+150	°C
Temperature with V _{CC} applied	T _{bias}	-55	+125	°C
DC output current (low)	I _{OUT}	_	20	mA

Absolute maximum ratings

Note: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



Truth table

CS1	CS2	WE	ŌĒ	LB	UB	Supply Current	I/O1–I/O8	I/O9–I/O16	Mode
Н	Х	Х	Х	Х	Х				
Х	L	Х	Х	Х	Х	I_{SB}	High Z	High Z	Standby (I _{SB})
Х	Х	Х	Х	Н	Н				
L	Н	Н	Н	L	Х	T	I _{CC} High Z	High Z	Output disable (I _{CC})
L	Н	Η	Н	Х	L	I _{CC}			Output disable (I _{CC})
				L	Н		D _{OUT}	High Z	
L	Н	Н	L	Н	L	I _{CC}	High Z	D _{OUT}	Read (I _{CC})
				L	L		D _{OUT}	D _{OUT}	
				L	Н		D _{IN}	High Z	
L	Н	L	Х	Н	L	I _{CC}	High Z	D _{IN}	Write (I_{CC})
				L	L		D _{IN}	D _{IN}	

Key: X = Don't care, L = Low, H = High.Recommended operating condition (over the operating range)

DC Recommended operating condition (over the operating range)

-			~ 11.1			•
Parameter	Description	Test	Conditions	Min	Max	Unit
Vcc	Supply voltage	-	-	1.65	2.2	V
V _{OH}	Output HIGH Voltage	$I_{OH} = -0.1 mA$	$V_{CC} = 1.65V$	1.4		V
V _{OL}	Output LOW Voltage	$I_{OL} = 0.1 mA$	$V_{\rm CC} = 1.65 V$		0.2	V
V _{IH}	Input HIGH Voltage		$V_{CC} = 2.2V$	1.4	$V_{CC} + 0.2$	V
V _{IL}	Input LOW Voltage		$V_{CC} = 1.65V$	-0.2	0.4	V
I _{IX}	Input Load Current	GND <u>-</u>	$\leq V_{\rm IN} \leq V_{\rm CC}$	-1	+1	μA
I _{OZ}	Output Load Current	$GND \le V_O \le V_O$	V _{CC;} Outputs High Z	-1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	$I_{OUT} = 0 mA,$ f = 0	$V_{CC} = 2.2 V$		1	mA
I _{CC1} @ 1 MHz	Average V _{CC} Operating Supply Current at 1 MHz	I _{OUT} = 0mA, f =1MHz	$V_{CC} = 2.2V$		2	mA
I _{CC2}	Average V _{CC} Operating Supply Current	$I_{OUT} = 0$ mA, f = f _{Max}	$V_{CC} = 2.2V$		15 mA at 70ns 10 mA at 85ns	mA
I _{SB}	CS Power Down Current; TTL Inputs		$V_{CC} = 2.2V$		100	μΑ
I _{SB1}	CS Power Down Current; CMOS Inputs	$\label{eq:cs1} \begin{split} \overline{\text{CS1}} \geq \text{V}_{\text{CC}} & -0.2 \text{V or} \\ \overline{\text{CS2}} \leq 0.2 \text{V} \\ \overline{\text{UB}} = \overline{\text{LB}} \geq \text{V}_{\text{CC}} - 0.2 \text{V} \\ \text{other inputs} & = 0 \text{V} - \\ \text{V}_{\text{CC}}, \ f = f_{\text{Max}} \end{split}$	V _{CC} = 2.2V		15	μΑ



Capacitance (f = 1 MHz, T_a = Room temperature, V_{CC} = NOMINAL)²

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C _{IN}	A, $\overline{\text{CS}}$ 1, CS2, $\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$	$V_{IN} = 0V$	5	pF
I/O capacitance	C _{I/O}	I/O	$V_{\rm IN} = V_{\rm OUT} = 0V$	7	pF

Read cycle (over the operating range)^{3,9}

		-70/85			
Parameter	Symbol	Min	Max	Unit	Notes
Read cycle time	t _{RC}	70/85	_	ns	
Address access time	t _{AA}	_	70/85	ns	3
Chip select to output access time	t _{ACS}	_	70/85	ns	3
Output enable (\overline{OE}) access time	t _{OE}	_	35/40	ns	
Output hold from address change	t _{OH}	10	_	ns	5
Chip select to low Z output	t _{CLZ}	10	_	ns	4, 5
Chip disable to high Z output	t _{CHZ}	_	20	ns	4, 5
OE low to low Z output	t _{OLZ}	5	_	ns	4, 5
UB/LB access time	t _{BA}	_	70/85	ns	
$\overline{\text{UB}}/\overline{\text{LB}}$ low to low Z	t _{BLZ}	10	_	ns	4, 5
UB/LB high to high Z	t _{BHZ}	_	20	ns	4, 5
OE high to output in high Z	t _{OHZ}	_	20	ns	4, 5
Power up time	t _{PU}	0	_	ns	4, 5
Power down time	t _{PD}	-	55	ns	4, 5

Key to switching waveforms

Rising input

Sealling input

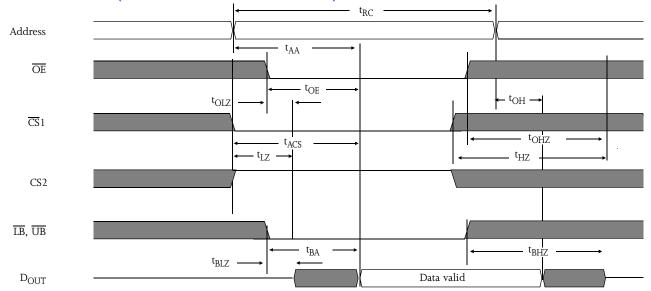
Undefined/don't care

Read waveform 1 (address controlled)^{3,6,7,9}

		<u>← t</u>	RC	
Address				
		$\leftarrow t_{AA} \longrightarrow$	│	^t OH ←───
D _{OUT}	Previous data valid		Data valid	



Read waveform 2 (\overline{CS} 1, CS2, \overline{OE} , \overline{UB} , \overline{LB} controlled)^{3,6,8,9}

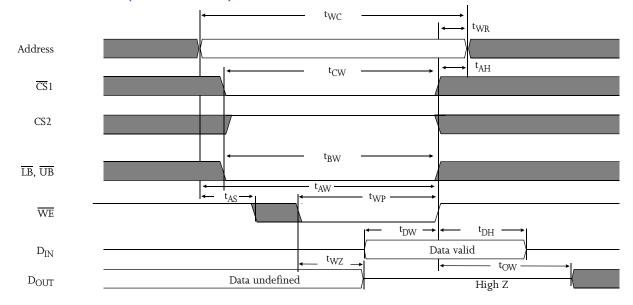


Write cycle (over the operating range)¹¹

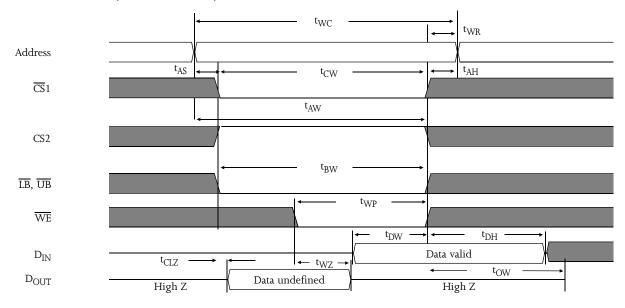
		-70/85			
Parameter	Symbol	Min	Max	Unit	Notes
Write cycle time	t _{WC}	70/85	_	ns	
Chip enable to write end	t _{CW}	60/70	_	ns	12
Address setup to write end	t _{AW}	60/70	_	ns	
Address setup time	t _{AS}	0	_	ns	12
Write pulse width	t _{WP}	50/60	_	ns	
Write recovery time	t _{WR}	0	_	ns	
Address hold from end of write	t _{AH}	0	_	ns	
Data valid to write end	t _{DW}	30/35	_	ns	
Data hold time	t _{DH}	0	_	ns	4,5
Write enable to output in high Z	t _{WZ}	_	20	ns	4,5
Output active from write end	t _{OW}	5	_	ns	4,5
UB/LB low to end of write	t _{BW}	60/70	_	ns	



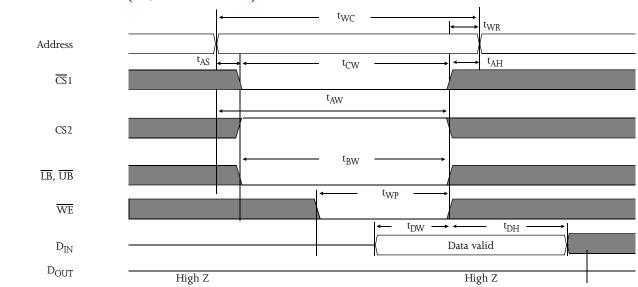
Write waveform 1 ($\overline{\text{WE}}$ controlled)^{10,11}



Write waveform 2 (\overline{CS} 1controlled)^{10,11}







Write waveform 3 (\overline{LB} , \overline{UB} controlled)



Data retention characteristics (over the operating range)^{13,5}

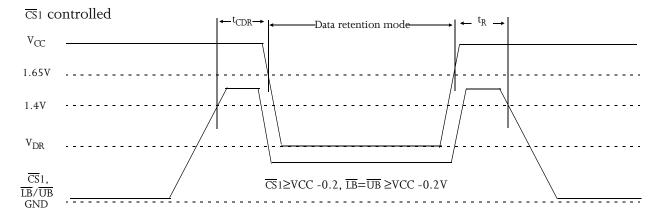
Parameter	Symbol	Test conditions	Min	Max	Unit
V _{CC} for data retention	V _{DR}	$V_{CC} = 1.0V$	1.0V	2.2	V
Data retention current	I _{CCDR}	Chip select controlled ^{A B}	-	8	μΑ
Chip deselect to data retention time	t _{CDR}	or $\overline{\text{LB}} / \overline{\text{UB}}$ controlled ^C	0	-	ns
Operation recovery time	t _R	$V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$	t _{RC}	_	ns

A : $\overline{\text{CS}1}$ controlled: $\overline{\text{CS}1} \ge \text{Vcc-0.2V}$; $\text{CS2} \le 0.2\text{V}$

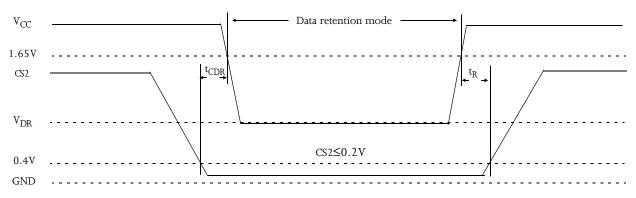
B : CS2 controlled: CS2 $\leq 0.2V$

C : $\overline{\text{LB}}$ / $\overline{\text{UB}}$ controlled: $\overline{\text{LB}}$ = $\overline{\text{UB}}$ ≥ Vcc - 0.2V, CS2 ≥ Vcc - 0.2V

Data retention waveform

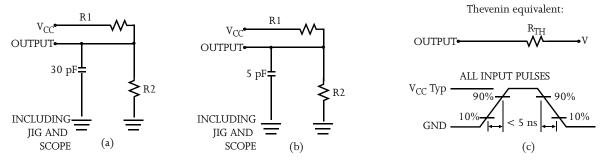


CS2 controlled





AC test loads and waveforms



Parameters	$V_{CC} = 1.8V$	Unit
R1	13500	Ohms
R2	10800	Ohms
R _{TH}	6000	Ohms
V _{TH}	0.8V	Volts

Notes

- 1 During V_{CC} power-up, a pull-up resistor to V_{CC} on \overline{CS} is required to meet I_{SB} specification.
- 2 This parameter is sampled, but not 100% tested.
- 3 For test conditions, see AC Test Conditions.
- 4 t_{CLZ} and t_{CHZ} are specified with $C_L = 5pF$ as in Figure C. Transition is measured ± 500 mV from steady-state voltage.
- 5 This parameter is guaranteed, but not tested.
- $\overline{\text{WE}}$ is HIGH for read cycle.
- 7 $\overline{\text{CS}}1$ and $\overline{\text{OE}}$ are LOW for read cycle.
- 8 Address valid prior to or coincident with $\overline{\text{CS}1}$ transition LOW.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 CS1 or WE must be HIGH during address transitions. Either CS1 or WE asserting high terminates a write cycle.
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.

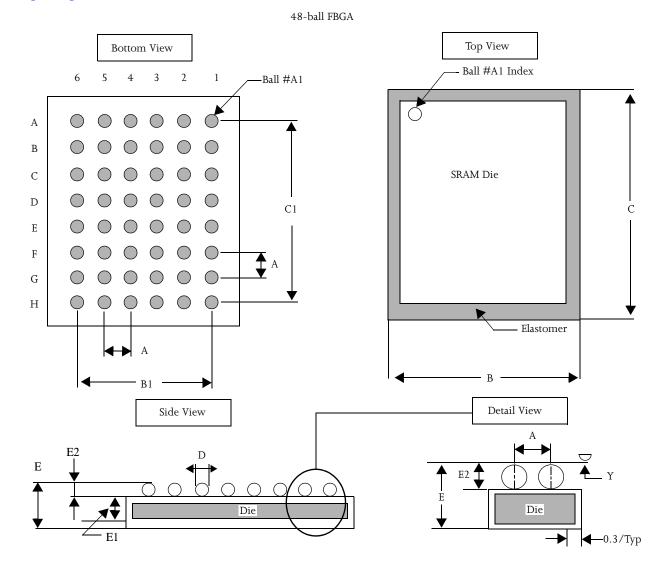
12 N/A.

- 13 1.0V data retention applies industrial temperature range operations.
- 14 C = 30pF, except at high Z and low Z parameters, where C = 5pF.

AS6YB51216



Package diagrams and dimensions



	Minimum	Typical	Maximum
А	-	0.75	-
В	6.90	7.00	7.10
B1	-	3.75	-
С	8.4	9.0	8.6
C1	-	5.25	-
D	0.30	0.35	0.40
E	_	_	1.20
E1	-	0.68	-
E2	0.22	0.25	0.27
Y	_	-	0.08

Notes

- 1. Bump counts: $48 (8 \text{ row} \times 6 \text{ column})$.
- 2. Pitch: $(x,y) = 0.75 \text{ mm} \times 0.75 \text{ mm}$ (typ).
- 3. Units: millimeters.
- 4. All tolerance are \pm 0.050 unless otherwise specified.
- 5. Typ: typical.
- 6. Y is coplanarity: 0.08 (max).

AS6YB51216



Ordering codes

Speed (ns)	Ordering Code	Package Type	Operating Range
70	AS6YB51216-70BI	48-ball fine pitch BGA	Industrial
85	AS6YB51216-85BI	48-ball fine pitch BGA	Industrial
70	AS6YB51216-70BC	48-ball fine pitch BGA	Commercial
85	AS6YB51216-85BC	48-ball fine pitch BGA	Commercial

Part numbering system

AS6YA	51216	В	C orI
SRAM Intelliwatt™ prefix	Device number	Package: B: CSP / BGA	Temperature range: C: Commercial: 0° C to 70° C I: Industrial: -40° C to 85° C

11/1/01; V.0.9.8

Alliance Semiconductor

P. 11 of 11

© Copyright Alliance Semiconductor Corporation. All rights reserved. Our three-point logo, our name and Intelliwatt are trademarks or registered trademarks of Alliance. All other brand and product names may be the trademarks of their respective companies. Alliance reserves the right to make changes to this document and its products at any time without notice. Alliance assumes no responsibility for any errors that may appear in this document. The data contained herein represents Alliance's best data and/or estimates at the time of issuance. Alliance reserves the right to change or correct this data at may time, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warrantee to any user or customer. Alliance does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of Alliance products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as express agreed to in Alliance's Terms and Conditions of Sale (which are available from Alliance). All sales of Alliance products are made exclusively according to Alliance does not authorize its products from Alliance does not convey a license under any pattert rights, copyrights, mask works rights, trademarks, on yother intellectual property rights of Alliance or third parties. Alliance does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of Alliance products in such life-supporting systems implies that the manufacturer a