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Fairchild Semiconductor
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FAIRCHILD SEMICONDUCTOR™

Using the Fairchild FST Bus Switch as a 5V to 3V Translator

Introduction

Fairchild FST Bus Switches can be used for bi-directional translators. They can interface 5V components to 3V components with negligible propagation delay ($t_{PD} \leq 250ps$) and minimal power dissipation ($I_{CC} \leq 10\mu A$).

As the number of systems that interface between 5V and 3.3V levels increase, the use of switches for voltage level interfacing has become more widespread.

FST Devices

FST devices produce an output voltage that is a maximum of 1V below V_{CC}. This is due to the inherent design characteristics of the NMOS device used in FST switch products. When the V_{GS} voltage reaches V_{TN}, which is approximately 1V, the NMOS channel closes off. With the channel closed, R_{ON} is increased dramatically and current flow through the device is cut off. The drain, starved of current, cannot exceed a voltage of V_{CC} –1V. Therefore, due to the electrical properties of the device, a 5V switch becomes a 5V-to-4V translator.

With many systems now incorporating both 5V and 3.3V level sections and components, the switch can be configured to translate between these two levels. By dropping the V_{GATE} of the NMOS by 700mV, the Bus Switch output will be reduced to 3.3V maximum. (See Figure 1) This is accomplished with the addition of a diode and resistor stack on the V_{CC} input (see Figure 2)

To preserve the low power design of the switch and to provide optimal operation, select a low current turn on diode with a forward turn on voltage (V*f*) of at least 0.7V. A resistor (R) is added from the V_{CC} pin to GND to provide forward turn on current (I**f**) for the diode. This is necessary to help the diode maintain a constant voltage drop. The value of R is dependent on the diode characteristics.

By dropping 0.7V down from the 5V power supply, ≈4.3V will be supplied to the V_{CC} pin of the switch (5V – 0.7V = 4.3V). The gate of the switch will therefore be at 4.3V. Coupled with the gate-to-source voltage drop of 1V limits the V_{OUT} to ≈3.3V. This provides an efficient and simple 5V-to-3.3V translator.

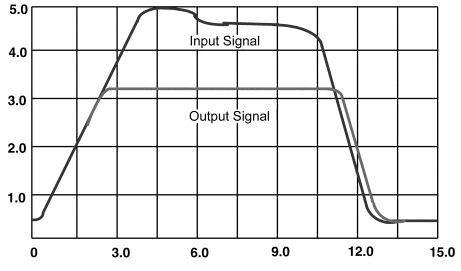

FIGURE 1. Typical NMOS Bus Switch Waveform

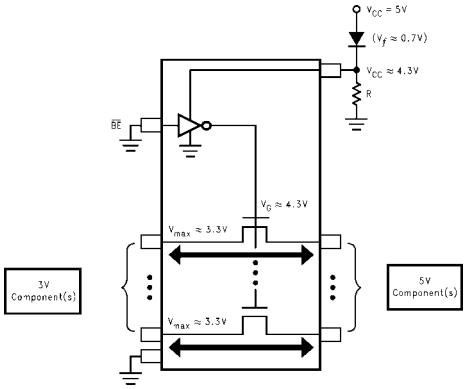

FIGURE 2. Typical 5V to 3V Translation Circuit

FSTD Devices

With the increase in the number of systems that interface between 5V and 3.3V levels, the use of switches for voltage level interfacing is becoming more widespread. Fairchild Semiconductor has recognized this, and has incorporated this feature directly into a sub-family of FST devices named FSTD. (See Figure 3)

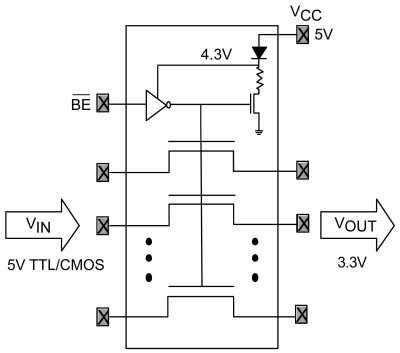

FIGURE 3. Fairchild Semiconductor's FSTD device incorporating the diode translation function and a switch to eliminate current flow during High Impedance mode.

The advantages of a FSTD device over the more traditional design are lower device count, and lower power consumption. FSTD devices incorporate the V_{CC} diode and resistor needed for level shifting internally. In addition, there is a switch network that shuts off the V_{CC} to ground current path created by the diode and resistor when the device is in high impedance mode. This lowers system power consumption, an especially useful feature in battery operated systems.

Special Considerations

Translation from 5V to 3V using Bus Switches is a straightforward process. However there are some special considerations when driving signals from a 3V node through a translating switch to a 5V node.

A Bus Switch configured for translation will give a maximum output voltage level of 3.3V (V_{CC} is still 5V and no clipping occurs at 3.3V)

Due to their behavior, translating Bus Switches are optimal for translating from 3.3V devices to 5V TTL compatible level inputs.

If 5V CMOS level signals are required, the switching threshold margin will be limited by the maximum 3.3V level from the switch output. 5V CMOS thresholds are typically $V_{CC}/2$, giving a threshold margin of 0.8V maximum (3.3V – 2.5V = 0.8V).

In some cases, using a pull up resistor to the 5V rail may help achieve a higher margin; for example, a high impedance short point to point 5V node, and a 3V driver with a high output On Resistance (see Figure 4). However, this layout can create a low impedance current path from the 5V rail through the pull up resistor to the 3.3V ground. This path is created when the 3.3V device is on and driving low, as shown in Figure 4.

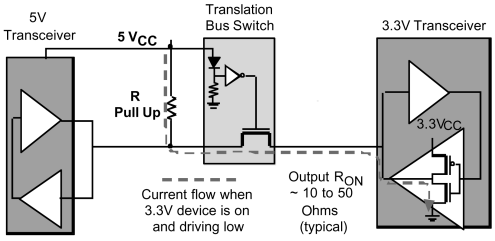

FIGURE 4. CMOS 5V to 3.3V translation using a pull up resistor, showing the current paths through the 3.3V device ground rail this design creates.

Excessive current flow can cause circuit damage. Therefore, the resistance values of all components in this path must be taken into consideration to insure that current flow is not above levels that will damage the system.

Another possible option is the use of a Schottky diode on the Bus Switch V_{CC}, in place of the more standard 0.7V diode. this will give a switch output level to ≈3.6V, and increases the threshold margin to 1.1V. In this case, devices on the 3V node would need Over Voltage Tolerance or at least be specified for 3.6V on inputs and outputs.As can be seen, using Bus Switches as 3V to 5V CMOS translation requires careful consideration.

Summary

Fairchild FST Bus Switches can be used as bi-directional translators. They can interface 5V components to 3V components with negligible propagation delay and minimal power dissipation.

This is accomplished with the addition of a diode and resistor stack on the V_{CC} input or the use of a Fairchild Semiconductor FSTD device. FSTD devices reduce system device count and lower power consumption. Translation is optimized for 5V to 3.3V, and 3.3V to 5V-TTL levels.