VIPER25

Off-line high voltage converters

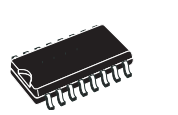
Preliminary data

Features

- 800 V avalanche rugged power section
- Quasi-resonant (QR) control for valley switching operation
- Standby power < 50 mW at 265 Vac
- Limiting current with adjustable set point
- Adjustable and accurate overvoltage protection
- On-board soft-start
- Safe auto-restart after a fault condition
- Hysteretic thermal shutdown

Applications

- Adapters for PDA, camcorders, shavers, cellular phones, cordless phones, videogames
- Auxiliary power supply for LCD/PDP TV, monitors, audio systems, computer, industrial systems, LED driver, No el-cap LED driver, utility power meter
- SMPS for set-top boxes, DVD players and recorders, white goods



SO16 narrow

DIP-7

Description

The device is an off-line converter with an 800 V rugged power section, a PWM control, double levels of overcurrent protection, overvoltage and overload protections, hysteretic thermal protection, soft-start and safe auto-restart after any fault condition removal. Burst mode operation and device very low consumption helps to meet the standby energy saving regulations. The quasi-resonant feature reduces EMI filter cost. Brown-out and brown-in function protects the switch mode power supply when the rectified input voltage level is below the normal minimum level specified for the system. The high voltage start-up circuit is embedded in the device.

Figure 1. Typical topology

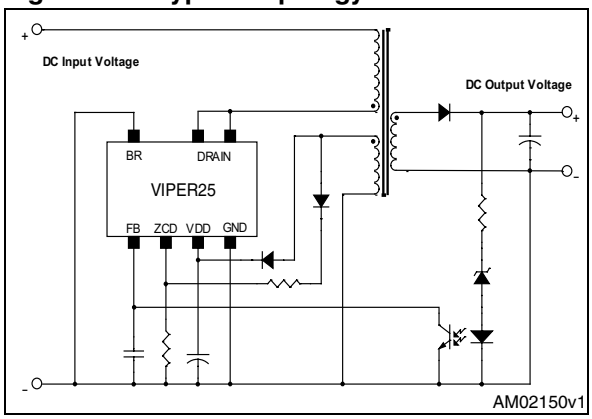


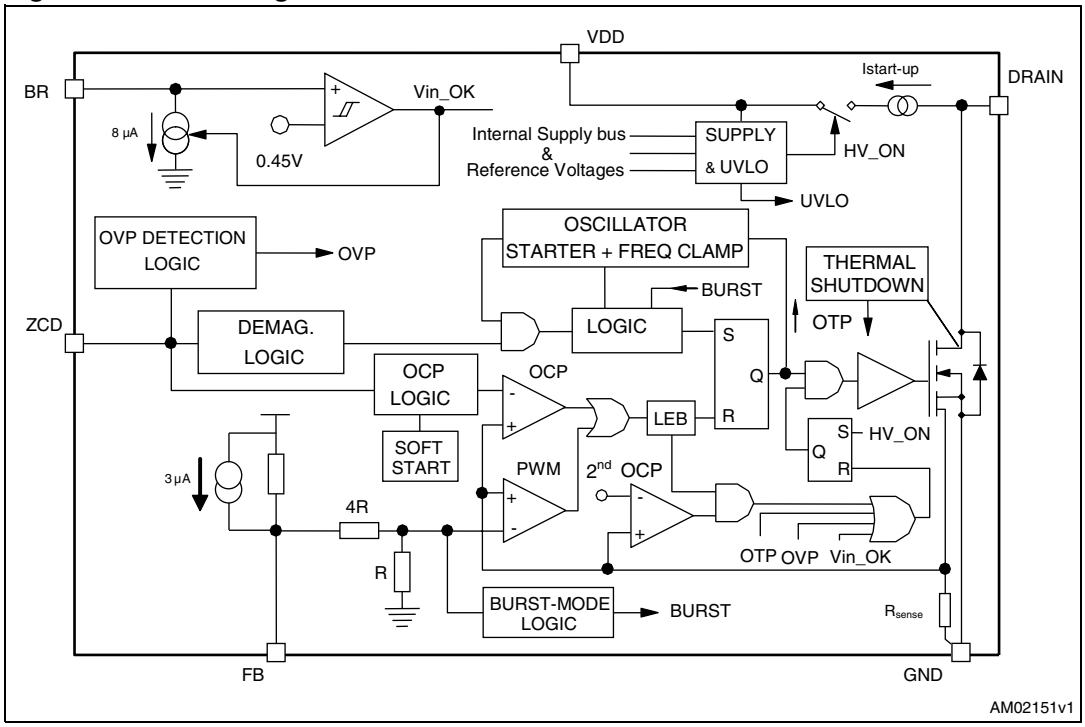
Table 1. Device summary

Order codes	Package	Packaging
VIPER25LN / VIPER25HN	DIP-7	Tube
VIPER25HD / VIPER25LD	SO16 narrow	Tube
VIPER25HDTR / VIPER25LDTR		Tape and reel

Contents

1 Block diagram

Figure 2. Block diagram



2 Typical power

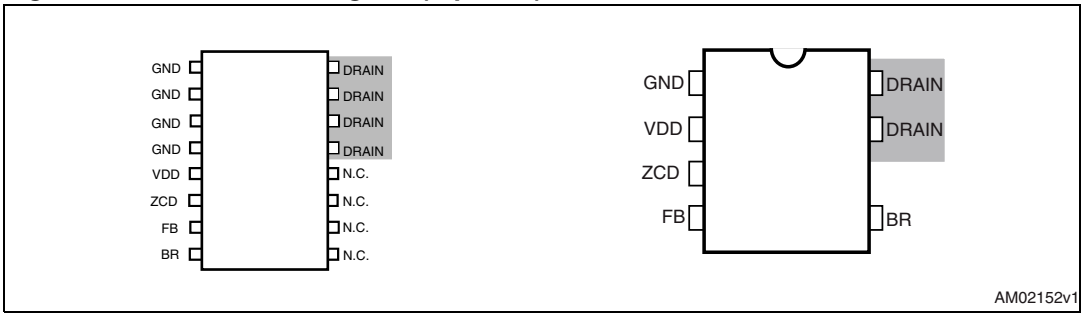
Table 2. Typical power

Part number	230 V_{AC}		85-265 V_{AC}	
	Adapter(1)	Open frame(2)	Adapter(1)	Open frame(2)
VIPER25	18 W	24 W	10 W	13 W

1. Typical continuous power in non ventilated enclosed adapter measured at 50 °C ambient.
2. Maximum practical continuous power in an open frame design at 50 °C ambient, with adequate heat sinking.

3 Pin settings

Figure 3. Connection diagram (top view)



Note: The copper area for heat dissipation has to be designed under the DRAIN pins.

Table 3. Pin description

Pin n.		Name	Function
DIP-7	SO16		
1	1...4	GND	This pin represents the device ground and the source of the power section.
2	5	VDD	Supply voltage of the control section. This pin also provides the charging current of the external capacitor during start-up time.
3	6	ZCD	This is a multifunction pin. 1. Input for the zero current detection circuit for transformer demagnetization sensing. (i.e. R_{LIM}, R_{FF}, R_{OVP} and D_{OVP}, *Figure 31*) 2. User defined drain current limit set-point and voltage feed forward.The resistor, R_{LIM}, connected between ZCD pin and GND causes the current I_{ZCD} and then it limits the static maximum drain current. 3. The resistor R_{FF}, between ZCD pin and the auxiliary winding, performs the feed-forward operation and then the drain current limitation changes according to the converter input voltage. 4. Output overvoltage protection. A voltage exceeding V_{OVP} threshold (typ 4.2 V, see *Table 8 on page 8*), shuts the IC down reducing the device consumption. This function is strobed and digitally filtered for high noise immunity.
4	7	FB	Control input for duty cycle control. Internal current generator provides bias current for loop regulation. A voltage below 0.5 V (V_{FBbm} + $V_{FBbmhys}$, see *Table 8 on page 8* and *Figure 35*) activates the burst-mode operation. A level close to 3.3 V means that we are approaching the cycle-by-cycle over-current set point.
5	8	BR	Brownout protection input with hysteresis. A voltage below 0.45 V shuts down (not latch) the device and lowers the power consumption. Device operation restarts as the voltage exceeds V_{BRth} plus hysteresis voltage. It can be connected to ground when not used.
7,8	13...16	DRAIN	High voltage drain pin. The built-in high voltage switched start-up bias current is drawn from this pin too. Pins connected to the metal frame to facilitate heat dissipation.

4 Electrical data

4.1 Maximum ratings

Table 4. Absolute maximum ratings

Symbol	Pin (DIP7)	Parameter	Value		Unit
			Min.	Max.	
V_{DRAIN}	7, 8	Drain-to-source (ground) voltage		800	V
E_{AV}	7, 8	Repetitive avalanche energy (limited by T_J = 150 °C)		5	mJ
I_{AR}	7, 8	Repetitive avalanche current (limited by T_J = 150 °C)		1.5	A
I_{DRAIN}	7, 8	Pulse drain current		3	A
V_{ZCD}	3	Control input pin voltage (with I_{ZCD} = 1 mA)	-0.3	Self limited	V
V_{FB}	4	Feedback voltage	-0.3	5.5	V
V_{BR}	5	Brown-out input pin voltage (with I_{BR} = 0.5 mA)	-0.3	Self limited	V
V_{DD}	2	Supply voltage (I_{DD} = 25 mA)	-0.3	Self limited	V
I_{DD}	2	Input current		25	mA
P_{TOT}		Power dissipation at T_A < 40 °C (DIP-7)		1	W
		Power dissipation at T_A < 60 °C (SO16N)		1	W
T_J		Operating junction temperature range	-40	150	°C
T_{STG}		Storage temperature	-55	150	°C

4.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Max. value SO16N	Max. value DIP7	Unit
R_{thJP}	Thermal resistance junction pin (Dissipated power = 2 W)	20	40	°C/W
R_{thJA}	Thermal resistance junction ambient (Dissipated power = 2 W)	50	100	°C/W
R_{thJA}	Thermal resistance junction ambient (1) (Dissipated power = 2 W)	40	80	°C/W

1. When mounted on a standard single side FR4 board with 100 mm^2 (0.155 sq in) of Cu (35 µm thick)

4.3 Electrical characteristics

(T_J = -25 to 125 °C, V_{DD} = 14 V; unless otherwise specified)

Table 6. Power section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{BVDSS}	Break-down voltage	I_{DRAIN} = 1 mA, V_{FB} = GND T_J = 25 °C	800			V
I_{OFF}	OFF state drain current	V_{DRAIN} = max rating, V_{FB} = GND			60	µA
$R_{DS(on)}$	Drain-source on state resistance	I_{DRAIN} = 0.2 A, V_{FB} = 3 V, V_{BR} = GND, T_J = 25 °C			7	Ω
		I_{DRAIN}=0.2 A, V_{FB}=3 V, V_{BR} = GND, T_J = 125 °C			14	Ω
C_{OSS}	Effective (energy related) output capacitance	V_{DRAIN} = 0 to 640 V		40		pF

Table 7. Supply section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Voltage						
V_{DRAIN_START}	Drain-source start voltage		60	80	100	V
I_{DDch}	Start-up charging current	V_{DRAIN} = 120 V, V_{BR} = GND, V_{FB} = GND, V_{DD} = 4 V	-2	-3	-4	mA
		V_{DRAIN} = 120 V, V_{BR} = GND, V_{FB} = GND, V_{DD} = 4 V after fault.	-0.4	-0.6	-0.8	mA
V_{DD}	Operating voltage range	After turn-on	8.5		23.5	V
$V_{DDclamp}$	V_{DD} clamp voltage	I_{DD} = 20 mA	23.5			V
V_{DDon}	V_{DD} start-up threshold	V_{DRAIN} = 120 V, V_{BR} = GND, V_{FB} = GND	13	14	15	V
V_{DDoff}	V_{DD} under voltage shutdown threshold		7.5	8	8.5	V
$V_{DD(RESTART)}$	V_{DD} restart voltage threshold	V_{DRAIN} = 120 V, V_{BR} = GND, V_{FB} = GND	4	4.5	5	V
Current						
I_{DD0}	Operating supply current, not switching	V_{FB}=GND, F_{SW}=0 kHz, V_{BR} = GND, V_{DD} = 10 V			0.9	mA
I_{DD1}	Operating supply current, switching	V_{DRAIN} = 120 V,			3.5	mA
I_{DD_FAULT}	Operating supply current, with protection tripping				400	µA
I_{DD_OFF}	Operating supply current with V_{DD} < VDD_off	V_{DD} = 7 V			270	µA

(T_J = -25 to 125 °C, V_{DD} = 14 V; unless otherwise specified)

Table 8. Controller section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Feedback pin						
V_{FBolp}	Over load shutdown threshold		4.5	4.8	5.2	V
V_{FBlin}	Linear dynamics upper limit		3.2	3.3	3.4	V
V_{FBbm}	Burst mode threshold	Voltage falling	0.4	0.45	0.6	V
$V_{FBbmhys}$	Burst mode hysteresis	Voltage rising		50		mV
I_{FB}	Feedback sourced current	V_{FB} = 0.3 V	-150	-200	-280	uA
		3.3 V < V_{FB} < 4.8 V		-3		uA
$R_{FB(DYN)}$	Dynamic resistance	V_{FB} < 3.3 V	14		19	kΩ
H_{FB}	ΔV_{FB} / ΔI_D		2		6	V/A
ZCD pin						
V_{ZCDCL_h}	Upper clamp voltage	I_{ZCD} = 1 mA	5	5.5	6	V
V_{ZCDA_th}	Arming voltage threshold	Positive-going edge		0.8		V
V_{ZCDT_th}	Triggering voltage threshold	Negative-going edge		0.6		V
I_{ZCD}	Internal pull-up			-2		µA
T_{BLANK}	Turn-on inhibit time after MOSFET's turn-off	V_{ZCD} < 1 V		6.3		µs
		V_{ZCD} >1 V		2.5		µs
Current limitation						
I_{Dlim}	Max drain current limitation	V_{FB} = 4 V, I_{ZCD} = -10 µA T_J = 25 °C	0.66	0.7	0.74	A
t_{SS}	Soft-start time				3.5	ms
t_{SU}	Start-up time		10			
T_{ON_MIN}	Minimum turn ON time		220	400	480	ns
td	Propagation delay			100		ns
t_{LEB}	Leading edge blanking			300		ns
I_{D_BM}	Peak drain current during burst mode	V_{FB} = 0.6 V		160		mA
Oscillator section						
F_{OSClim}	Internal frequency limit	VIPER25L	122	136	150	kHz
	Internal frequency limit	VIPER25H	200	225	250	kHz
$F_{STARTER}$	Starter frequency	VFB = 1 V, V_{ZCD} < V_{ZCDT_th}		1/4 F_{OSClim}		kHz
F_{OSCmin}		VFB = 1 V, V_{ZCD} > V_{ZCDA_th}		1/64 F_{OSClim}		kHz

(T_J = -25 to 125 °C, V_{DD} = 14 V; unless otherwise specified)

Table 8. Controller section (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Overcurrent protection (2nd OCP)						
I_{DMAX}	Second overcurrent threshold			1.2		A
Overvoltage protection						
V_{OVP}	Overvoltage protection threshold		3.8	4.2	4.6	V
T_{STROBE}	Overvoltage protection strobe time			2.2		µs
Brown-out protection						
V_{BRth}	Brown-out threshold	Voltage falling	0.41	0.45	0.49	V
V_{BRhyst}	Voltage hysteresis above V_{BRth}			50		mV
I_{BRhyst}	Current hysteresis		7		10	µA
$V_{BRclamp}$	Clamp voltage	I_{BR} = 250 µA		3		V
V_{EN}	Brown-out enable voltage		150			mV
V_{DIS}	Brown-out disable voltage				50	mV
Thermal shutdown						
T_{SD}	Thermal shutdown temperature		150	160		°C
T_{HYST}	Thermal shutdown hysteresis			30		°C

Figure 4. Minimum turn-on time test circuit

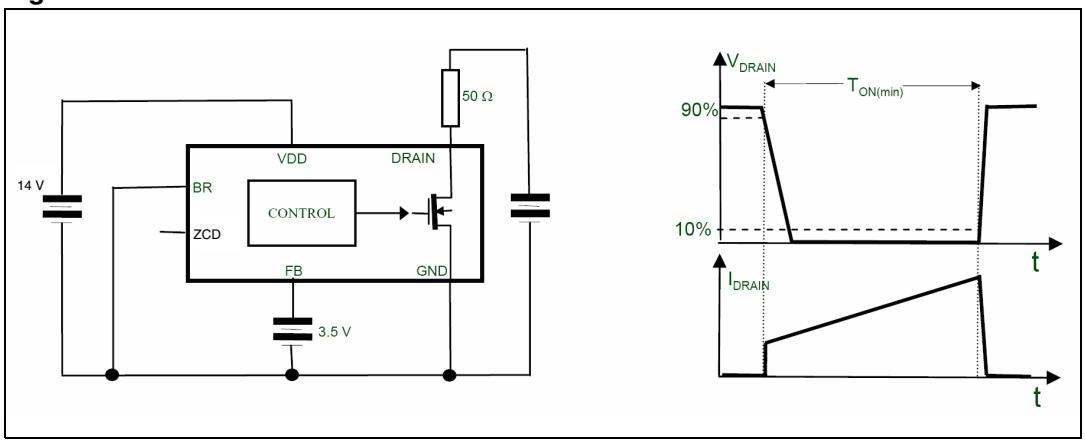


Figure 5. Brown-out threshold test circuits

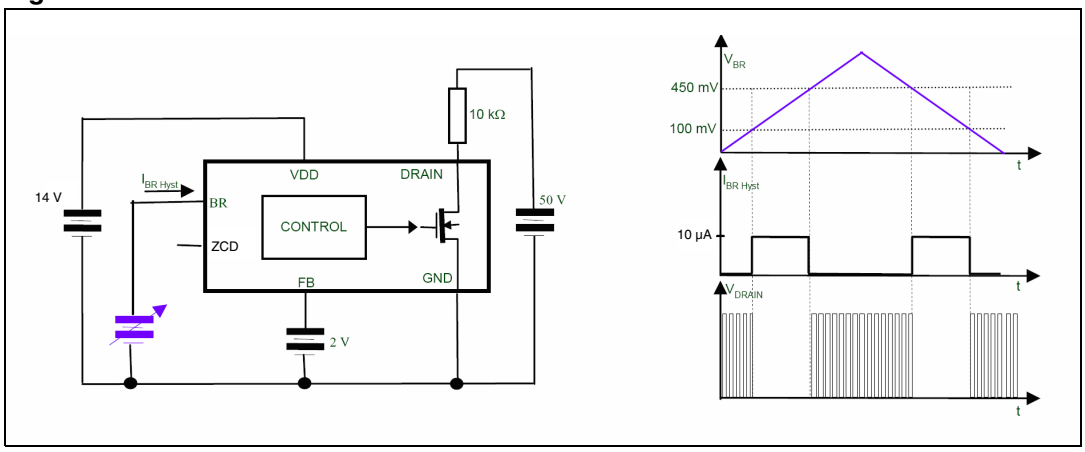
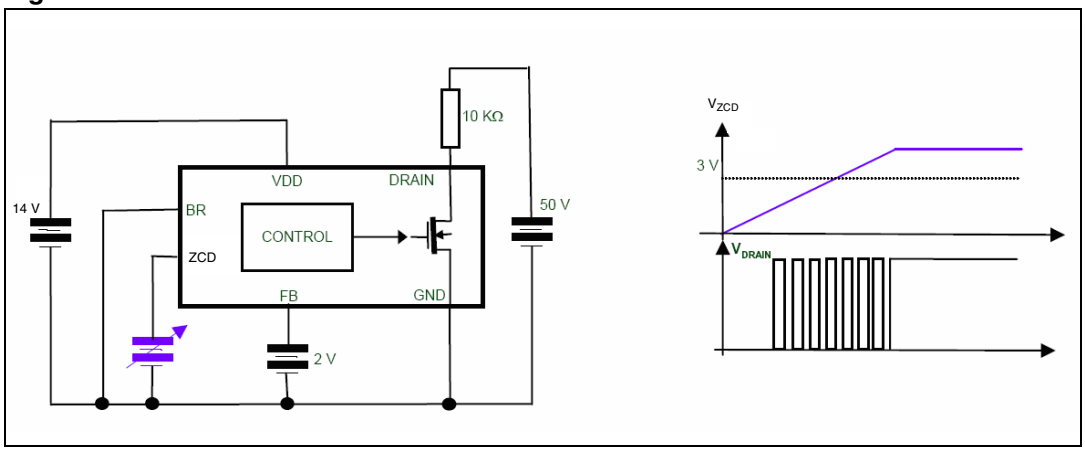


Figure 6. OVP threshold test circuits



5 Typical electrical characteristics

Figure 7. Current limit vs T_J

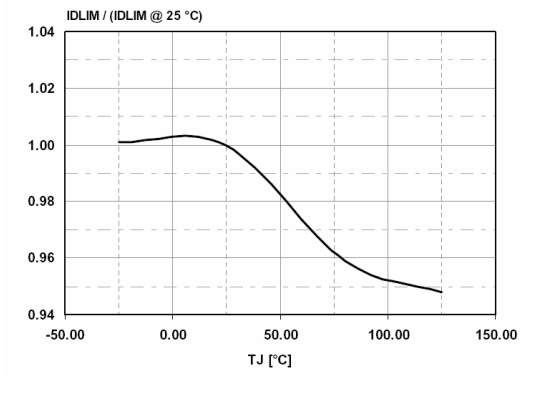


Figure 8. Drain start voltage vs T_J

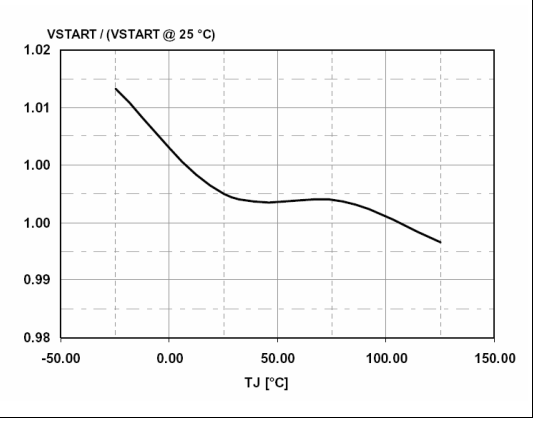


Figure 9. HFB vs T_J

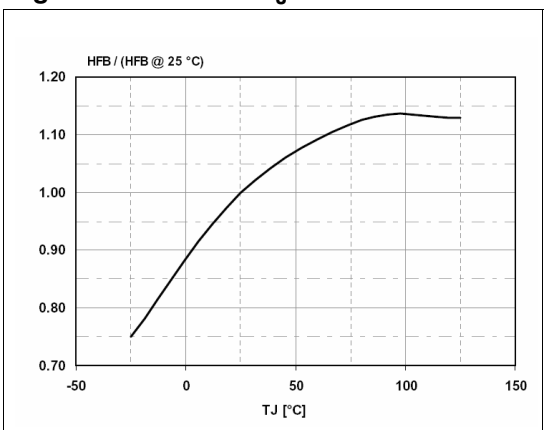


Figure 10. Brown-out threshold vs T_J

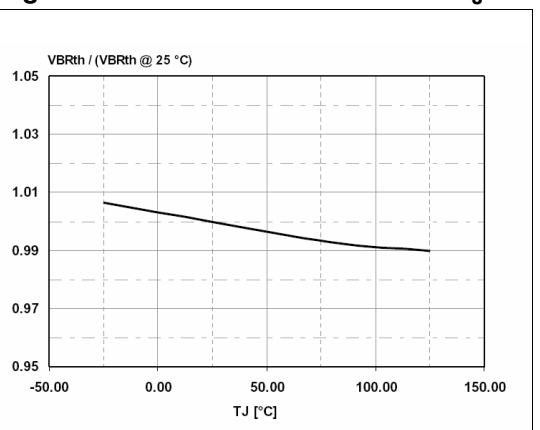


Figure 11. Brown-out hysteresis vs T_J

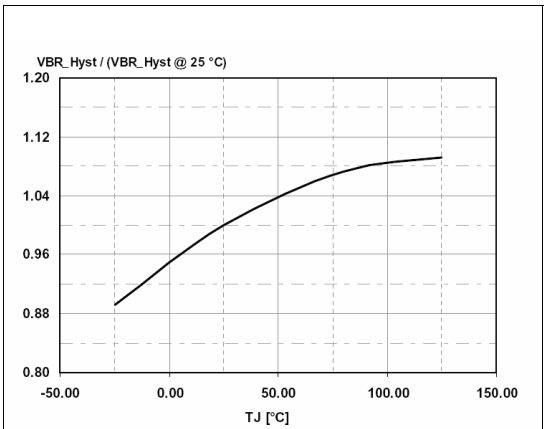


Figure 12. Brown-out hysteresis current vs T_J

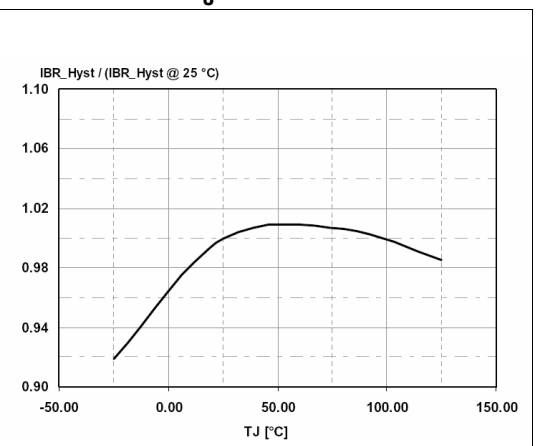


Figure 13. Operating supply current (no switching) vs T_J

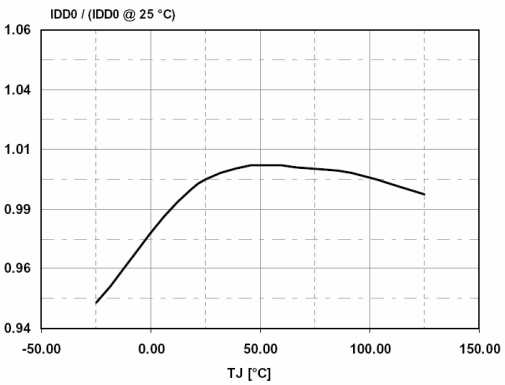


Figure 14. Operating supply current (switching) vs T_J

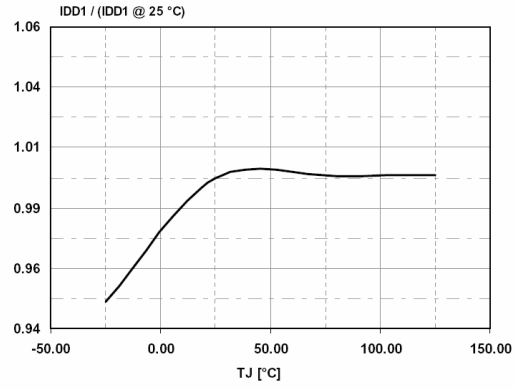


Figure 15. V_{ZCD} vs I_{ZCD}

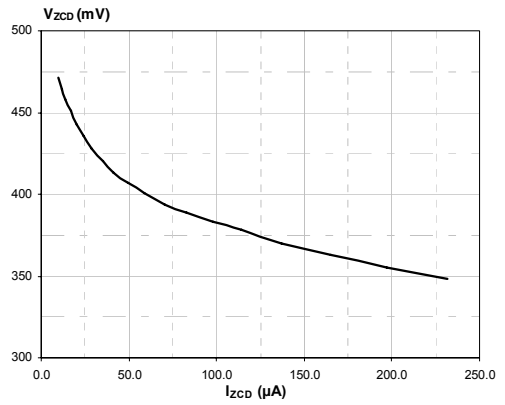


Figure 16. Current limit vs I_{ZCD}

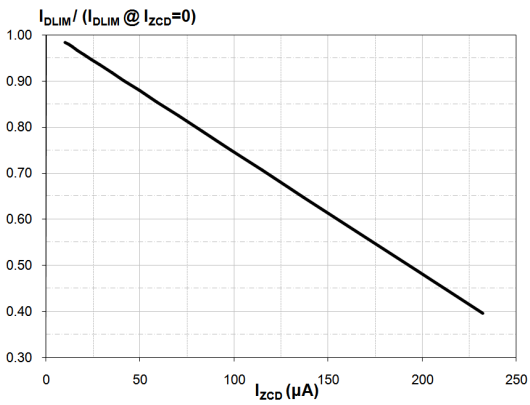


Figure 17. Power MOSFET on-resistance vs T_J

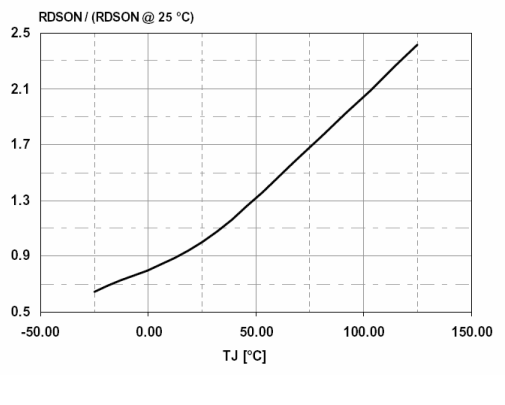


Figure 18. Power MOSFET break down voltage vs T_J

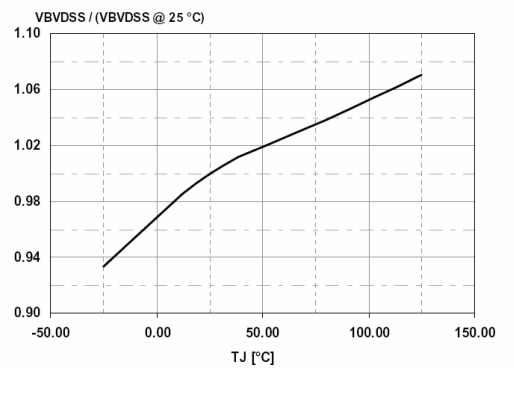
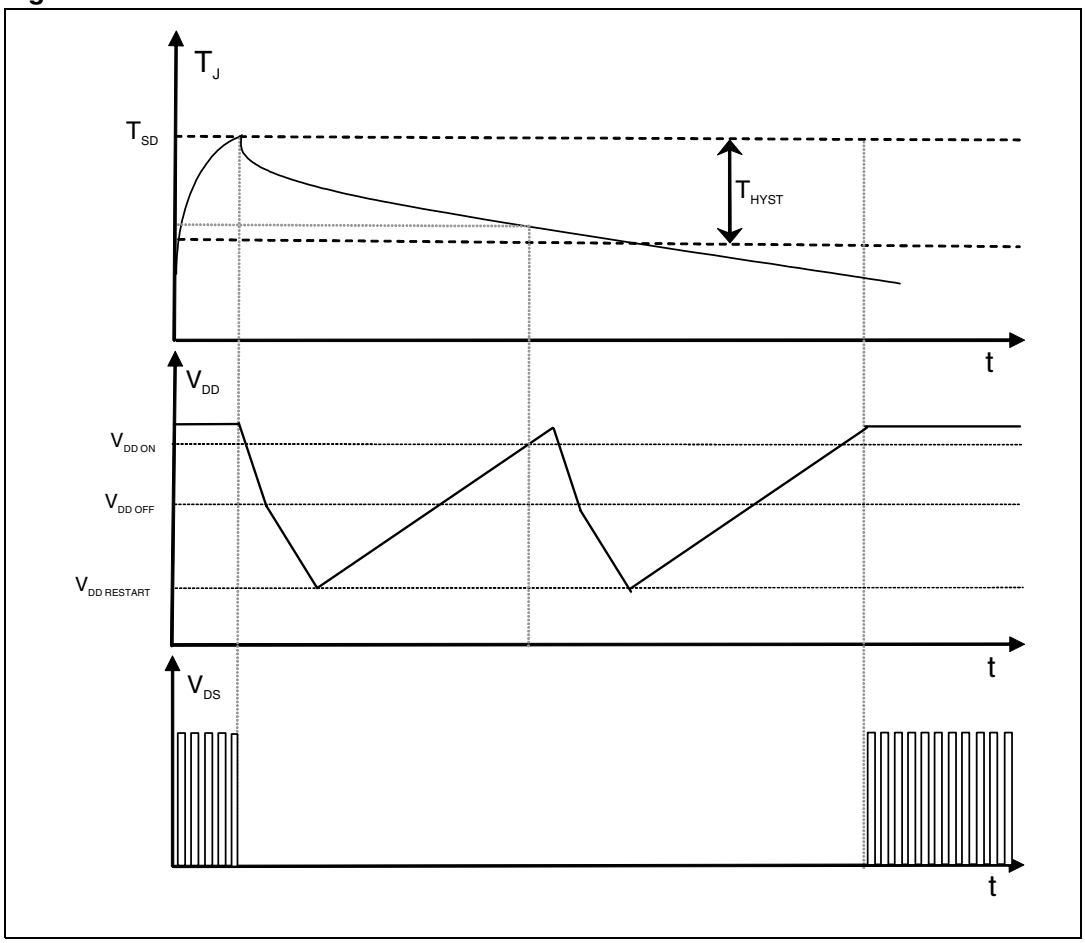


Figure 19. Thermal shutdown



6 Typical circuit

Figure 20. Min-features QR flyback application

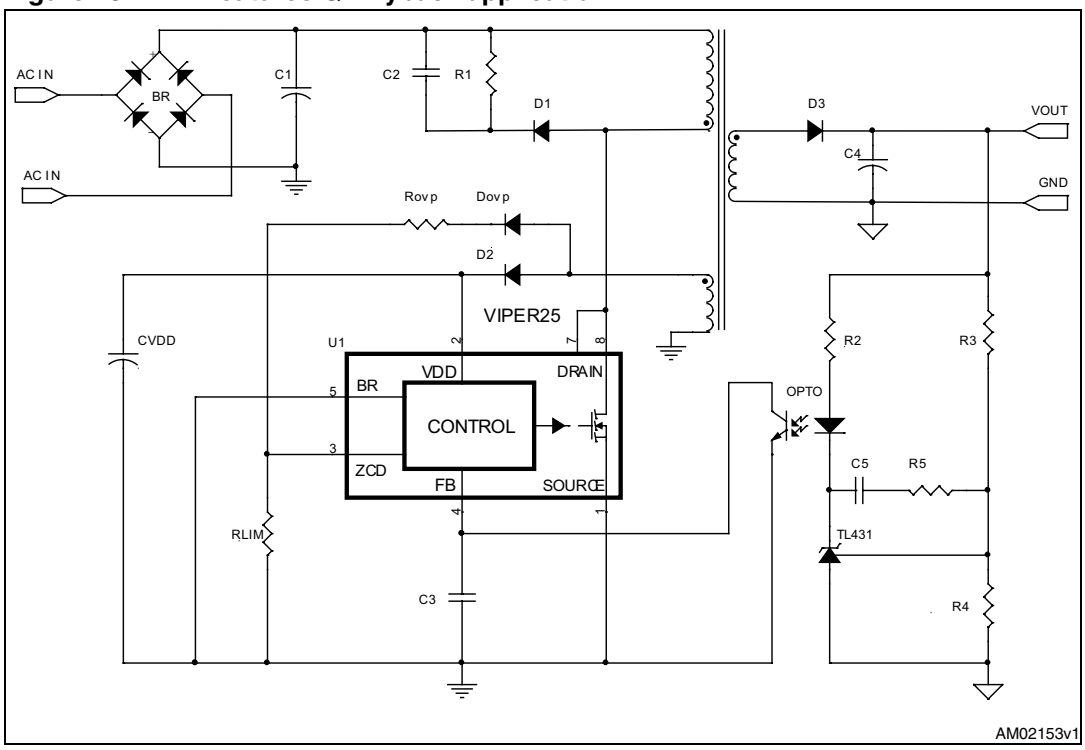
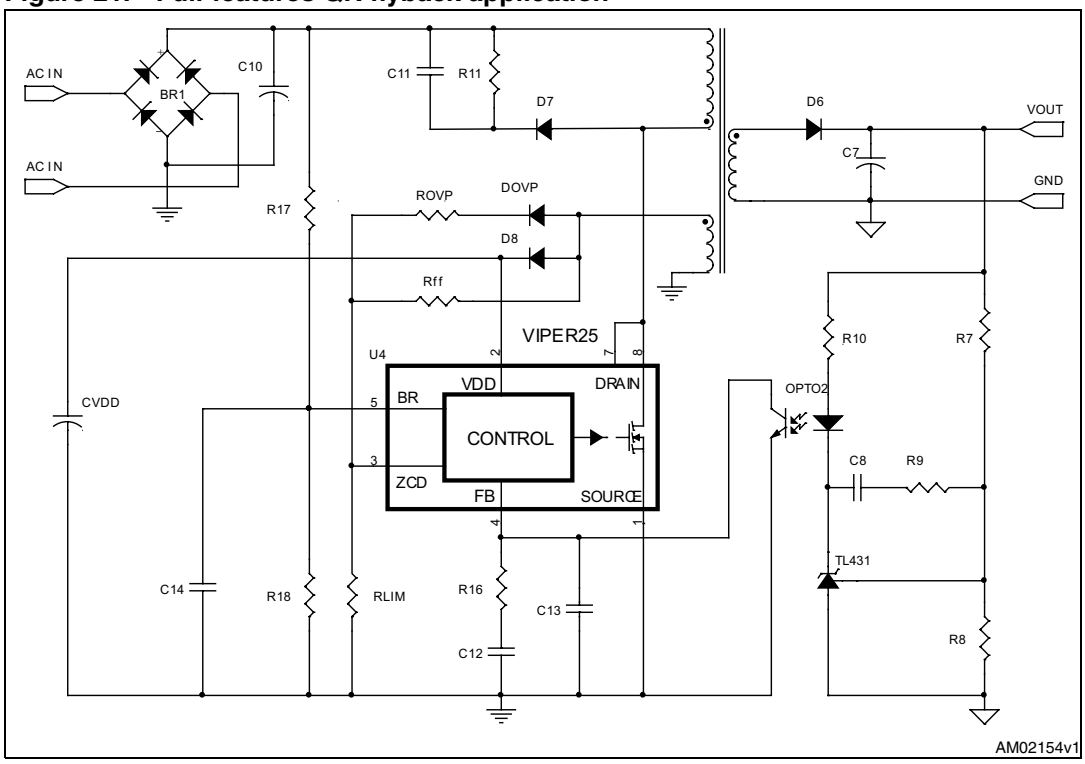


Figure 21. Full-features QR flyback application



7 Operation description

VIPER25 is a high-performance low-voltage PWM controller IC with an 800 V, avalanche rugged power section.

The controller includes the current-mode PWM logic and the ZCD (zero current detect) circuit for QR operation, the start-up circuitry with soft-start feature, an oscillator for frequency foldback function, the current limit circuit with adjustable set point, the second overcurrent circuit, the burst mode management circuit, the brown-out circuit, the UVLO circuit, the auto-restart circuit and the thermal shutdown circuit.

The current limit set-point is set by the ZCD pin. The burst mode operation guaranties high performance in the stand-by mode and helps in the energy saving norm accomplishment

All the fault protections are built in auto-restart mode with very low repetition rate to prevent IC's over heating.

7.1 Power section and gate driver

The power section is implemented with an avalanche ruggedness N-channel MOSFET, which guarantees safe operation within the specified energy rating as well as high dv/dt capability. The power section has a BV_{DSS} of 800 V min. and a typical $R_{DS(on)}$ of 20 Ω at 25 °C.

The integrated SenseFET structure allows a virtually loss-less current sensing.

The gate driver is designed to supply a controlled gate current during both turn-on and turn-off in order to minimize common mode EMI. Under UVLO conditions an internal pull-down circuit holds the gate low in order to ensure that the Power section cannot be turned on accidentally.

7.2 High voltage startup generator

The HV current generator is supplied through the DRAIN pin and it is enabled only if the input bulk capacitor voltage is higher than V_{DRAIN_START} threshold, 80 V_{DC} typically. When the HV current generator is ON, the IDD_ch current (3 mA typical value) is delivered to the capacitor on the V_{DD} pin. In case of Auto-restart mode after a fault event, the IDD_ch current is reduced to 0.6 mA, typ. in order to have a slow duty cycle during the restart phase.

7.3 Power-up and soft start-up

If the input voltage rises up till the device start level (V_{DRAIN_START}), the V_{DD} voltage begins to grow due to the I_{DD_ch} current (see *Table 7 on page 7*) coming from the internal high voltage start-up circuit. If the V_{DD} voltage reaches V_{DDon} threshold (~14 V) the power MOSFET starts switching and the HV current generator is turned OFF. See *Figure 23 on page 17*.

The IC is powered by the energy stored in the capacitor on the VDD pin, C_{VDD}, until when the self-supply circuit (typically an auxiliary winding of the transformer and a steering diode) develops a voltage high enough to sustain the operation.

C_{VDD} capacitor must be sized enough to avoid fast discharge and keep the needed voltage value higher than V_{DDoff} threshold. In fact, a too low capacitance value could terminate the switching operation before the controller receives any energy from the auxiliary winding.

The following formula can be used for the V_{DD} capacitor calculation:

Equation 1

$$C_{VDD} = \frac{I_{DDch} \cdot t_{SSaux}}{V_{DDon} - V_{DDoff}}$$

The t_{SSaux} is the time needed for the steady state of the auxiliary voltage. This time is estimated by applicator according to the output stage configurations (transformer, output capacitances, etc.).

The VIPER25 internal power MOSFET is switched on or according the voltage signal sensed on the ZCD pin, or by the internal oscillator. When the converter is just powered and VIPER25 starts switching the output voltage is zero and then the voltage on ZCD pin is not high enough to correct arming the ZCD circuit. In this condition the power MOSFET is switched on by the internal oscillator. According to the VIPER25 version (L or H) the internal oscillator frequency is 136 kHz or 225 kHz. If no signal comes from ZCD circuit, the power MOSFET is switched on each 4/fosc seconds. So the firsts switching cycles are at $f_{OSC}/4$ switching frequency.

When the voltage on ZCD pin is high enough to arm and trigger the ZCD circuit (see relevant section) properly, the switching frequency is no more related (except for the frequency foldback function) to the internal oscillator but it depends by the load and the input voltage.

Two parameters are defined, the soft start-up time (T_{SS}) and the start-up length (T_{SU}).

The T_{SS} is the soft start-up time during which the drain current is increased cycle by cycle up to the drain current limitation while T_{SU} is the time during which the device is working at its drain current limitation keeping the feedback voltage at V_{FB_lin}, not allowing to ramp up towards the V_{FB_OLP} threshold (See *Figure 24*).

These two parameters are obtained as a number of oscillator cycles. Because each MOSFET turn-on the internal oscillator is reset T_{SS} and T_{SU} are not exactly defined in terms of ms. Considering the worst case the T_{SS_MAX} and T_{SU_MIN}. are reported in the electrical characteristic.

Figure 22. Start-up I_{DD} current

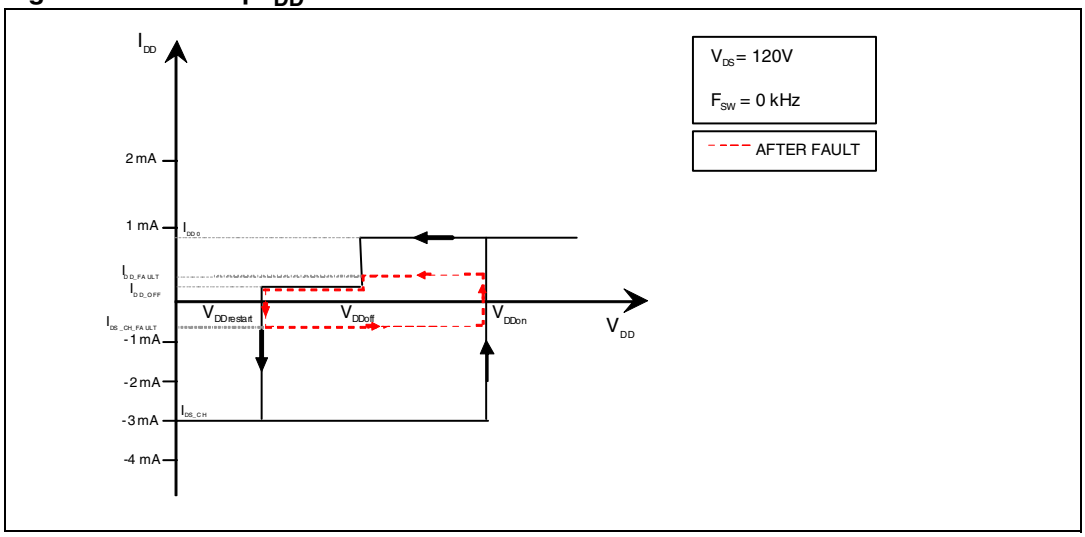


Figure 23. Timing diagram: normal power-up and power-down sequences

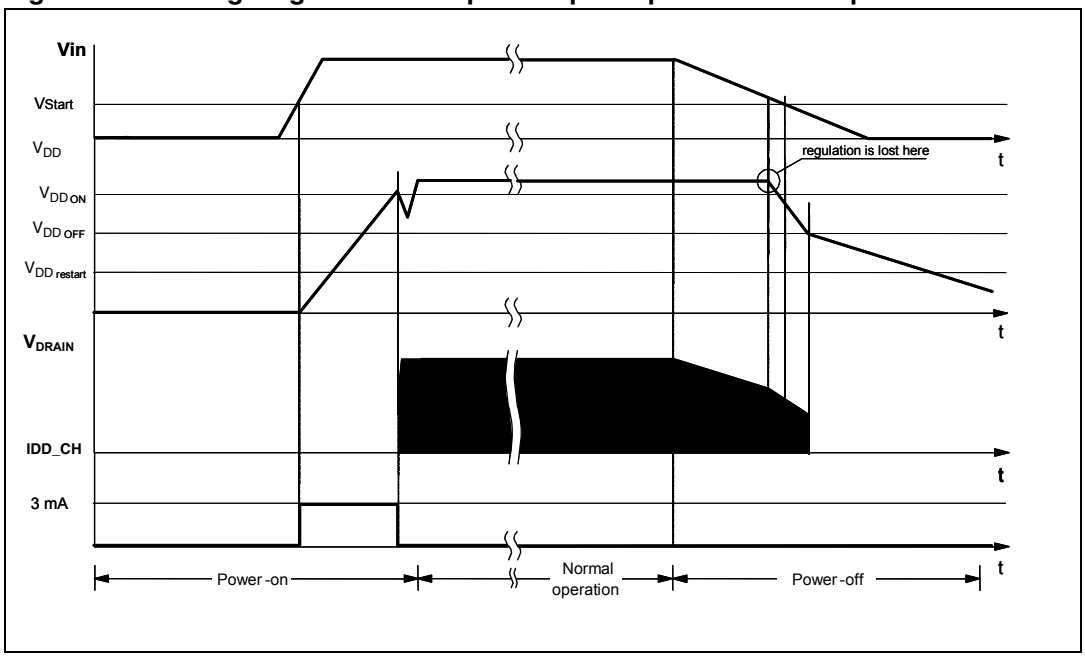
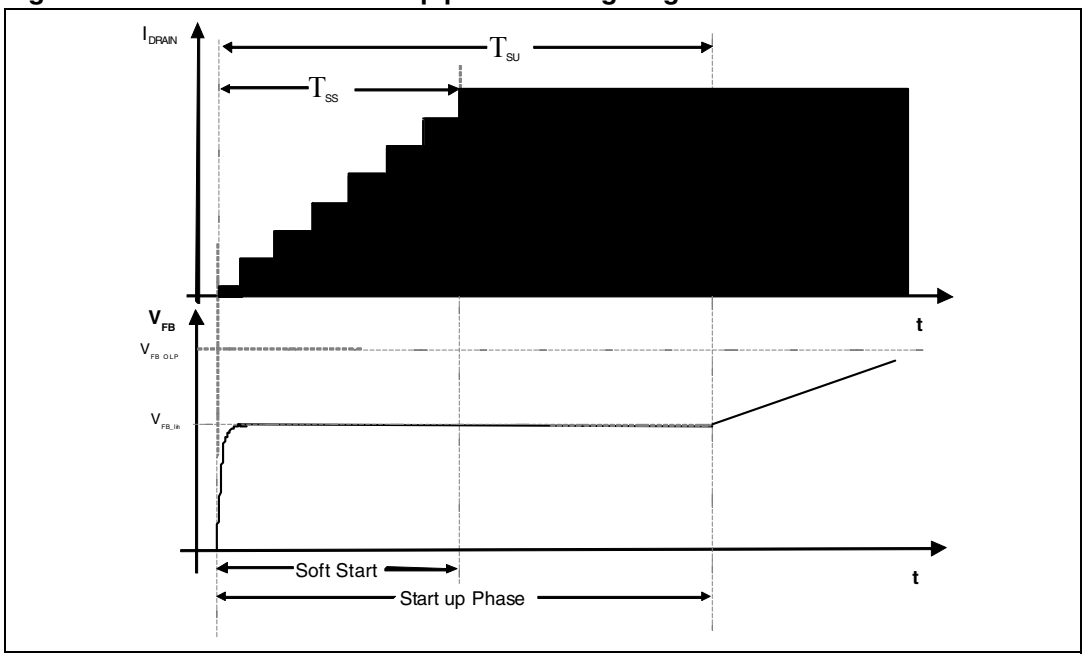


Figure 24. Soft-start and start-up phase: timing diagram



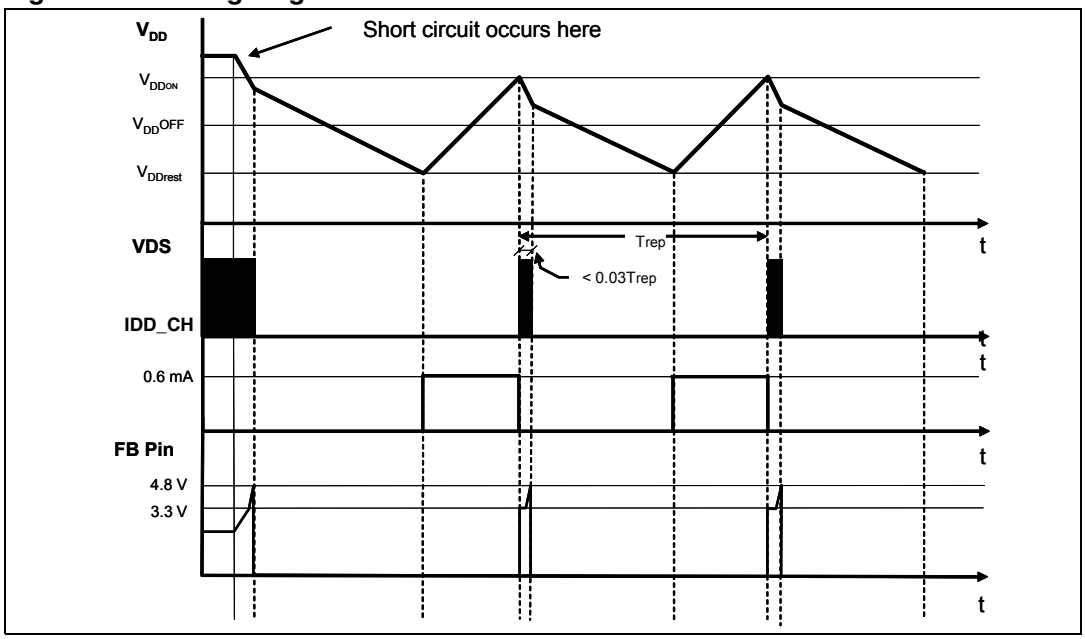
7.4 Power-down operation

At converter power-down, the system loses regulation as soon as the input voltage is so low that the peak current limitation is reached. The V_{DD} voltage drops and when it falls below the V_{DDoff} threshold (8 V typical) the power MOSFET is switched OFF, the energy transfers to the IC interrupted and consequently the V_{DD} voltages decreases, *Figure 23 on page 17*. Later, if the V_{IN} is lower than V_{DRAIN_START} (80 V typical), the start-up sequence is inhibited and the power-down completed. This feature is useful to prevent converter's restart attempts and ensures monotonic output voltage decay during the system power-down.

7.5 Auto-restart operation

If after a converter power-down, the V_{IN} is higher than $V_{DRAIN\_START,}$ the start-up sequence is not inhibited and will be activated only when the V_{DD} voltage drops down the $V_{DDrestart}$ threshold (4.5 V typical). This means that the HV start-up current generator restarts the V_{DD} capacitor charging only when the V_{DD} voltage drops below $V_{DDrestart}$. The scenario above described is for instance a power-down because of a fault condition. After a fault condition, the charging current is 0.6 mA (typ.) instead of the 3 mA (typ.) of a normal start-up converter phase. This feature together with the low $V_{DDrestart}$ threshold (4.5 V) ensures that, after a fault, the restart attempts of the IC has a very long repetition rate and the converter works safely with extremely low power throughput. The *Figure 25* shows the IC behavioral after a short circuit event.

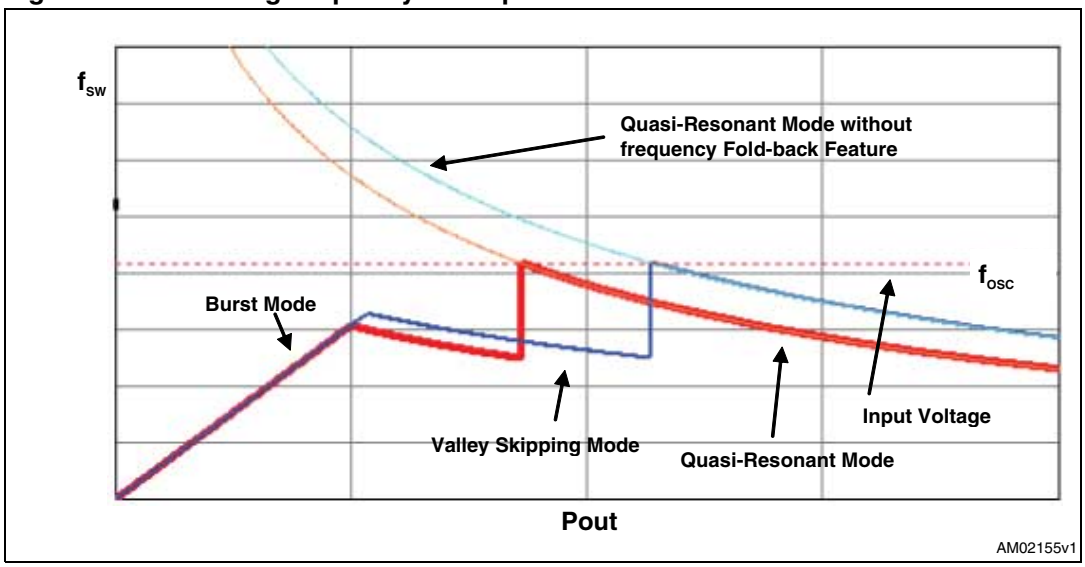
Figure 25. Timing diagram: behavior after short circuit



7.6 Quasi-resonant operation

The control core of the VIPER25 is a current-mode PWM controller with a zero current detection circuit designed for quasi-resonant (QR) operation, a technique that provides the benefits of minimum turn-on losses, low EMI emission and safe behavior in case of short circuit. At heavy load the converter operates in quasi-resonant mode; operation lies in synchronizing MOSFET's turn-on to the transformer's demagnetization by detecting the resulting negative-going edge of the voltage across any winding of the transformer. The system works close to the boundary between discontinuous (DCM) and continuous conduction (CCM) of the transformer and as a result, the switching frequency will be different for different line/load conditions (see the hyperbolic-like portion of the curves in *Figure 26*).

Figure 26. Switching frequency vs output load



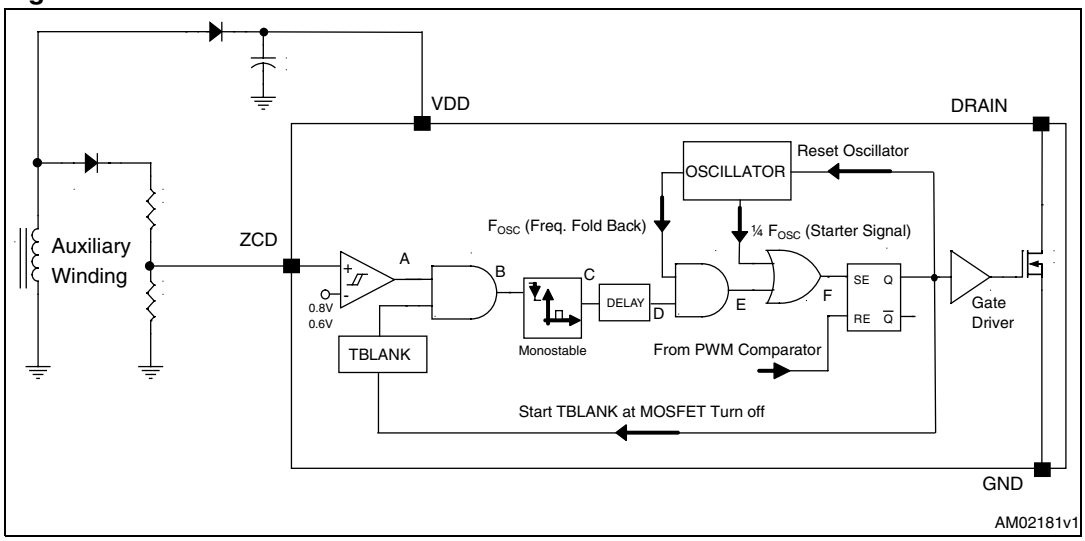
At medium/ light load, depending also from the converter input voltage the device enters in Valley-skipping mode. An internal oscillator, synchronized to MOSFET's turn-on, defines the maximum operating frequency of the converter. This frequency is set below 150 kHz (136 kHz Typ.) for applications where EMI filtering needs minimizing; a device option is available where the oscillator is set at 220 kHz for applications where an extended QR operation range is a plus. As the load is reduced, and the switching frequency tends to exceed that of the oscillator, MOSFET's turn-on will not any more occur on the first valley but on the second one, the third one and so on. In this way a "frequency clamp" effect is achieved (piecewise linear portion in *Figure 26*).

When the load is extremely light or disconnected, the converter enters in burst mode operation. Decreasing the load will then result in frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations or recommendations. Being the peak current low enough, no issue of audible noise.

The above mentioned way of operation is based on the ZCD pin. This pin is the input of the ZCD circuit which allows the power section to turn-on at the end of the transformer demagnetization. The input signal for the ZCD is obtained as a partition of the auxiliary voltage used to supply the device. (See *Figure 26*).

When the triggering circuit senses a negative-going edge of the signal applied to the ZCD pin going below the V_{ZCDTth} threshold (typ, 0.6 V), after an internal delay that helps to achieve minimum Drain Source voltage switch-on ("valley switching"), the power section is turned on. However, to enable Power Section turn-on, the triggering circuit has to be previously armed by a positive-going edge exceeding the V_{ZCDAth} threshold (typ, 0.8 V) on the same ZCD pin.

Figure 27. Zero current detection circuit and oscillator circuit



After the MOSFET turn-OFF, the blanking time, T_{BLANK}, is generated in order to avoid an erroneous arming and consequently triggering due to the noise, generated by the transformer's leakage inductance resonance ringing and coupled to the ZCD pin.

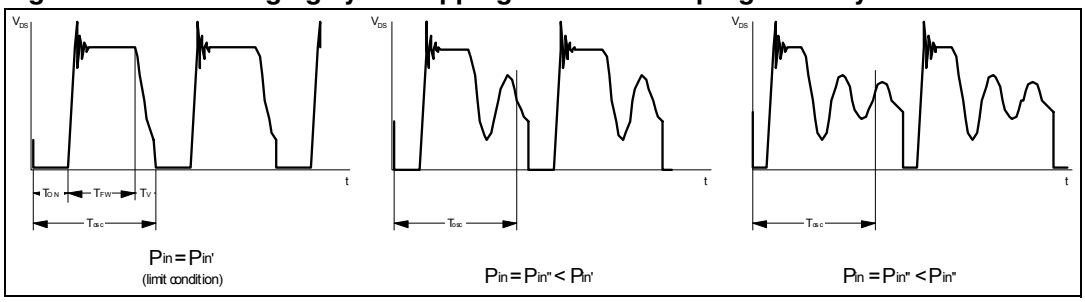
7.7 Frequency foldback function and valley skipping mode

In quasi-resonant mode, the switching frequency is not fixed and depends on both the load and the converter's input voltage. The switching frequency increases when the load decreases, or when the input voltage mains increases, and vice versa. In principle it could reach an infinite value. To avoid that, the VIPER25 taps the maximum switching frequency of the application thanks to its control logic.

Application frequency limitation is realized with an internal oscillator switching at 136 kHz (typical value) for VIPER25L or at 225 kHz (typical value) for the VIPER25H.This oscillator is synchronized with power MOSFET turn-on every switching cycle. When the power MOSFET is off, if the first negative-going edge voltage of the ZCD pin, resulting from transformer's demagnetization, appears after at least one internal oscillator cycle has been completed, the MOSFET is turned ON and the oscillator re-synchronized.

Otherwise, if the first negative-going edge voltage appears before completing one oscillator cycle, the signal is ignored. Due to the ringing of the drain voltage, the ZCD pin will experience another positive-going edge voltage that arms the circuit and a subsequent negative-going edge voltage. Again, if this appears before the internal oscillator cycle is complete, it is ignored, otherwise the MOSFET is turned ON and the oscillator re-synchronized. In this way, one or more drain ringing cycles will be skipped ("valley-skipping mode", see *Figure 28*) and the switching frequency will be prevented from exceeding F_{OSC}.

Figure 28. Drain ringing cycle skipping as the load is progressively reduced



When the system operates in valley skipping-mode, uneven switching cycles may be observed under some line/load conditions, due to the fact that the OFF-time of the power MOSFET is allowed to change with discrete steps of one ringing cycle, while the OFF-time needed for cycle-by-cycle energy balance could fall in between. Thus one or more longer switching cycles will be compensated by one or more shorter cycles and vice versa. This mechanism is natural and there is no appreciable effect on the converter's performances and on its output voltage.

The operation described so far does not consider the blanking time T_{BLANK} after power MOSFET's turn OFF. Actually T_{BLANK} does not come into play as long as the following condition is met:

Equation 2

$$D \leq 1 - \frac{T_{BLANK}}{T_{OSC}} = 1 - T_{BLANK} \bullet f_{SW}$$

Where D is the MOSFET duty cycle. If this condition is not met, the time during which MOSFET's turn-ON is inhibited is extended beyond T_{OSC} by a fraction of T_{BLANK}. As a consequence, the maximum switching frequency will be a little lower than the internal limit set by the oscillator and valley-skipping mode will take place slightly earlier than expected.

7.8 Double blanking time

The just said blanking time (T_{BLANK}) has two values (see *Table 8 on page 8*). Which value is used is decided cycle by cycle according to the value of the ZCD pin voltage, during demagnetization of the transformer in the previous cycle. If V_{ZCD}>1V the T_{BLANK} has the lower value (2.5 µs) if V_{ZCD} < 1 V T_{BLANK} has the higher value (6.3 µs). Actually the voltage on ZCD pin is monitored during the T_{SROBE} of the OVP (overvoltage protection) function (see relevant *Section 7.6 on page 19*).This feature is introduced in order to avoid that, during start-up phase or in output short circuit condition, when the ZCD voltage can be below 1 V, the ZCD circuit is erroneously trigged leading the system to work at higher frequency and in continuous mode.

In both the above mentioned conditions, the output voltage of the power supply is quite lower than its nominal value and the ZCD pin voltage, during transformer demagnetization, has a value close to the arming and triggering thresholds (<1 V).

Normally this feature doesn't have impact on converter design; during steady state operations normally the used T_{BLANK} is the lower one.

Figure 29. Double T_{BLANK} timing diagram

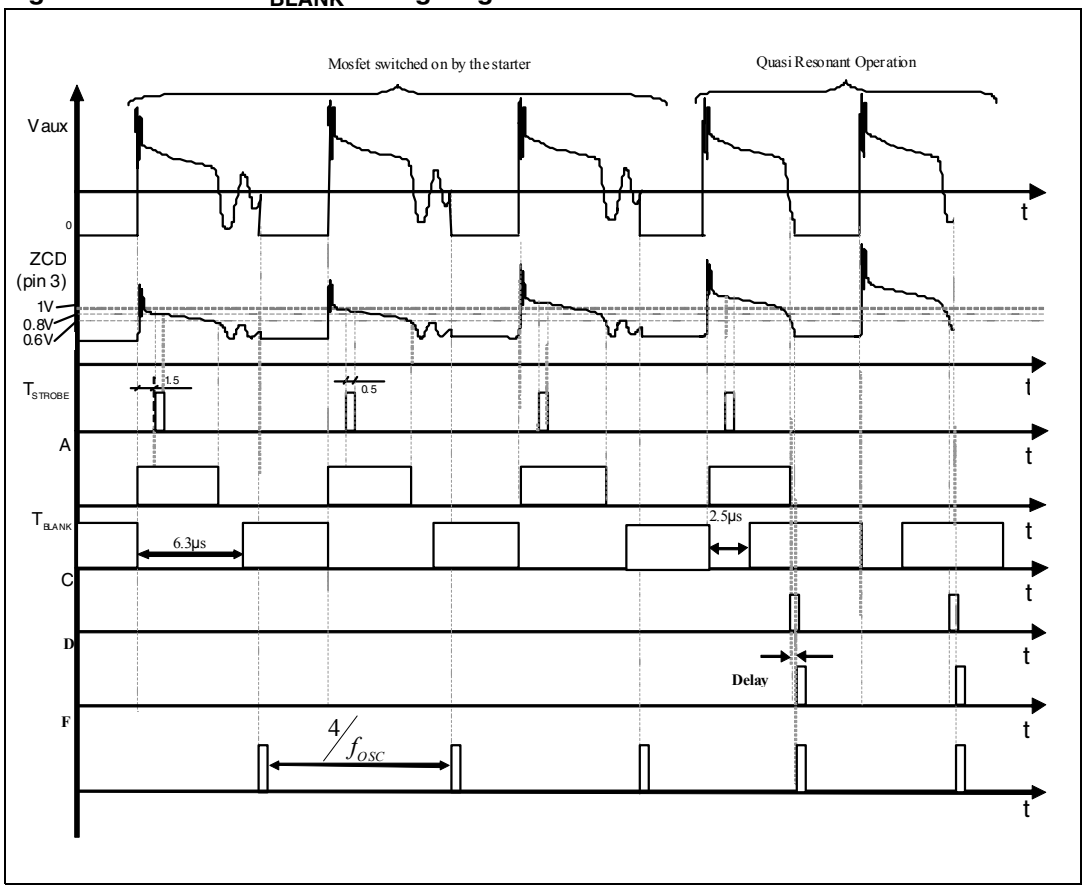


Figure 29 shows the typical situation at the converter start-up, when the output voltage is still low and the ZCD voltage can lead to false trigger to the ZCD circuit and not correct MOSFET switch-on.

7.9 Starter

If the amplitude of the voltage on ZCD pin at the end of one oscillator cycle is smaller than the V_{ZCDAth} arming threshold, in which case MOSFET's turn-ON could not be triggered, the system would stop.

This is what normally happens during converter's start-up or under overload/short circuit conditions.

During the converter's startup phase, the voltage on ZCD pin is not high enough to arm the triggering circuit. Thus, the converter operates at a fixed frequency, $F_{STARTER}$, (see *Table 8 on page 8*). As the voltage developed across the auxiliary winding becomes high enough to arm the ZCD circuit, MOSFET's turn-ON is locked to transformer demagnetization, hence setting up quasi-resonant operation.

As protection, in case the ZCD voltage is permanently above the threshold V_{ZCDAth}, the switching frequency is reduced to the minimum value, F_{OSCmin}, (see *Table 8 on page 8*).

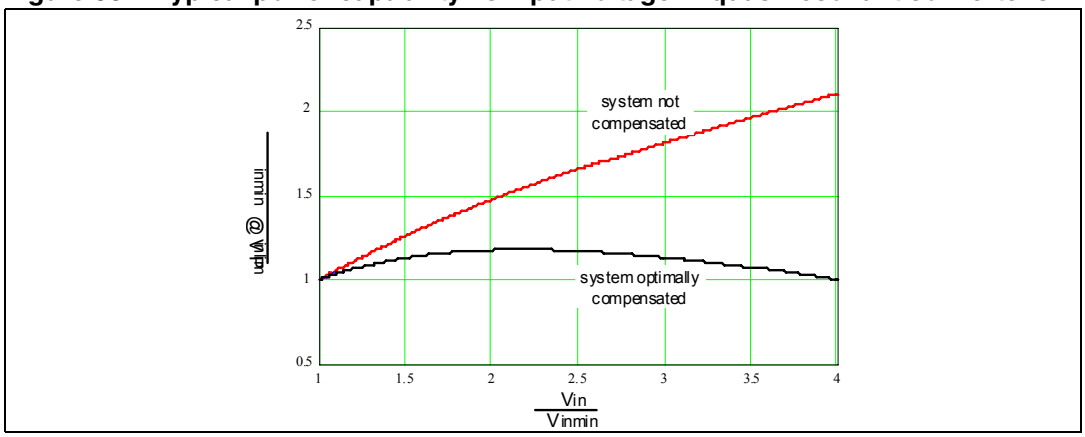
7.10 Current limit set point and feed-forward option

The VIPER25 is a current mode converter and the drain current is limited cycle by cycle according to the FB pin voltage value that is related with the feedback loop response and the load. When the drain current, sensed by the integrated Sense-FET, reaches the current limitation, after the internal propagation delay, the MOSFET is switched OFF. The current limitation cannot exceed a certain value (I_{DLIM}) that can be adjusted acting on the current sunk from the ZCD pin during MOSFET's ON-time.

Usually a resistor, R_{LIM}, connected from ZCD pin to ground is used to fix this sunk current and then the peak drain current set-point: the lower the resistor is, the lower I_{DLIM} will be.

For a QR flyback converter the power capability strongly depends on the input voltage. In wide-range applications at maximum line the power capability can be more than twice the value at minimum line, as shown by the upper curve in the diagram of *Figure 29*. To reduce this dependence, the I_{DLIM} can be reduced according to the input voltage increase (line feed-forward). This can be easily realized with a resistor, R_{FF} (see *Figure 30*), connected between the ZCD pin and the auxiliary winding. Since the voltage across the auxiliary winding during MOSFET's ON-time is proportional to the input voltage through the auxiliary-to-primary turns ratio N_{AUX}/N_P, a current proportional to the input voltage is sunk from the ZCD pin, thus lowering the overcurrent set point.

Figure 30. Typical power capability vs input voltage in quasi-resonant converter's



In order to proper select the value of the resistance R_{FF} (*Figure 31*), once are known the proper overcurrent set points at minimum and at the maximum converter input voltage, we can find from graph of *Figure 16* the needed current to sink from ZCD pin during MOSFET on time. Using the following approximated formula we can calculate the R_{FF}.

Equation 3

$$R_{FF} = \frac{V_{in\_Max} - V_{in\_min}}{n_{aux} \cdot (I_{ZCD1} - I_{ZCD2})}$$

Where:

- V_{in_Max} and V_{in_min} are the maximum and minimum converter rectified input voltage
- n_{aux} is the primary to auxiliary winding turn ratio
- I_{ZCD1}, and I_{ZCD2} are the currents needed to sink from the ZCD pin, in order to obtain the selected overcurrent set points, at maximum and minimum flyback input voltage (see *Figure 6*).

The R_{LIM} Value can be calculated from the following formula knowing the R_{FF} value:

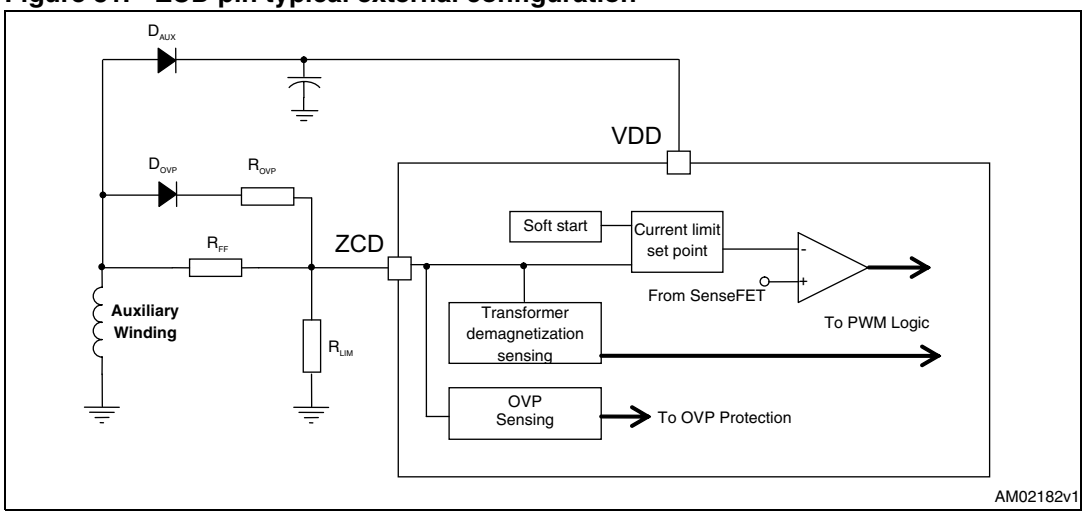
Equation 4

$$R_{LIM} = Max\left(\frac{V_{ZCD1}}{I_{ZCD1} - \frac{\frac{V_{in\_min}}{n_{aux}} + V_{ZCD1}}{R_{FF}}}, \frac{V_{ZCD2}}{I_{ZCD2} - \frac{\frac{V_{in\_max}}{n_{aux}} + V_{ZCD2}}{R_{FF}}}\right)$$

Where:

V_{ZCD1} and V_{ZCD2} are the ZCD pin voltages when the sunk current is I_{ZCD1} and I_{ZCD2} respectively (see *Figure 5*).

Figure 31. ZCD pin typical external configuration



7.11 Overvoltage protection (OVP)

If the voltage applied to the ZCD pin exceeds the internal voltage reference V_{OVP}(4.2 V typ. see *Table 8*), for four consecutive cycle in a row, the device interpreters this condition like a fault and stops operation. This feature is the output overvoltage protection. The auxiliary winding, during transformer demagnetization, tracks converter's output voltage through turn ratio See *Figure 31*. Proper selecting the resistor divider that connect ZCD pin to the auxiliary winding (R_{LIM} and R_{OVP} in *Figure 31)* it is possible to set the Overvoltage Protection limit.

The function is digital filtered and strobed to reduce noise sensitivity and prevent the protection to be erroneously activated. In fact, in order to trip the protection the ZCD has to sense the overvoltage for four consecutive switching cycles (digital filter). This special feature uses an internal counter that is reset at MOSFET switch on every time the OVP signal is not triggered. The internal OVP block senses the ZCD pin voltage for a time interval whose width is of 500ns and starts 2 µs (T_{STROBE} on *Table 8*) after MOSFET turn off.

Referring to the *Figure 31*, the resistors divider ratio k_{OVP} will be given by:

Equation 5

$$k_{OVP} = \frac{V_{OVP}}{\frac{N_{AUX}}{N_{SEC}} \cdot (V_{OUTOVP} + V_{DSEC}) - V_{DAUX}}$$

Equation 6

$$k_{OVP} = \frac{R_{LIM}}{R_{LIM} + R_{OVP}}$$

Where:

- V_{OVP} is the OVP threshold (see *Table 8 on page 9*)
- $V_{OUT\ OVP}$ is the converter output voltage value to activate the OVP (set by designer) designer
- N_{AUX} is the auxiliary winding turns
- N_{SEC} is the secondary winding turns
- V_{DSEC} is the secondary diode forward voltage
- V_{DAUX} is the auxiliary diode forward voltage
- R_{OVP} together R_{LIM} make the output voltage divider

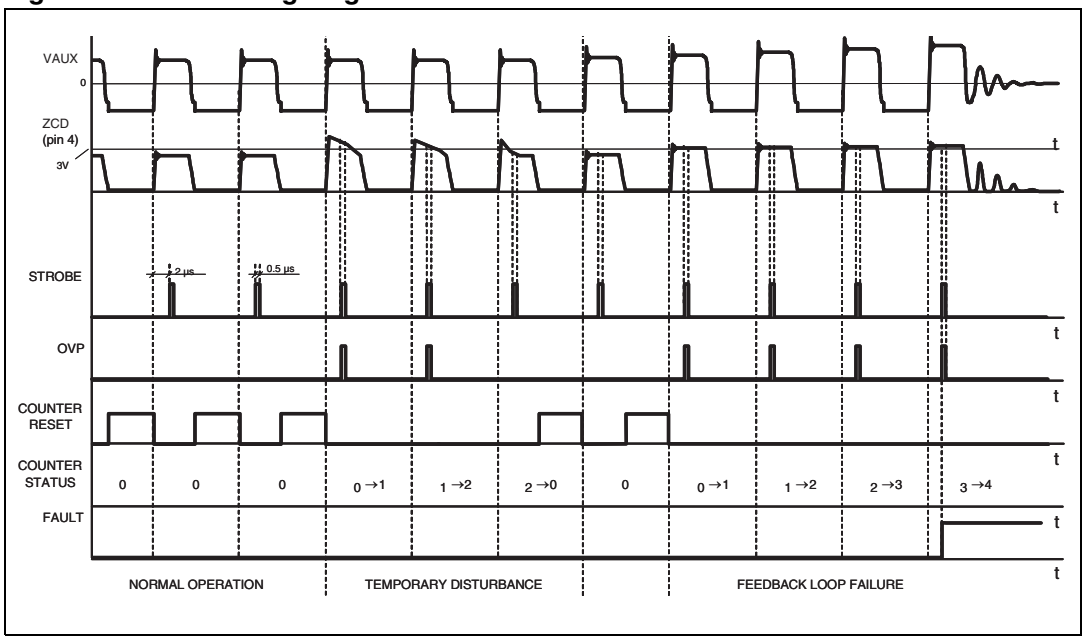
Than, fixed $R_{LIM,}$ according to the desired I_{DLIM}, the R_{OVP} can be calculating by:

Equation 7

$$R_{OVP} = R_{LIM} \times \frac{1 - k_{OVP}}{k_{OVP}}$$

The resistor values will be such that the current sourced and sunk by the ZCD pin be within the rated capability of the internal clamp.

Figure 32. OVP timing diagram



7.12 Summary on ZCD pin

Referring to the *Figure 30*, the circuitry connected to the ZCD pin enables to implement the following functions:

1. Current limit set point
2. Line feed-forward compensation
3. Output overvoltage protection (OVP)
4. Zero current detection for QR operation

Chosen R_{LIM}, R_{FF} and R_{OVP} as described in previous paragraphs this function are automatically defined.

Table 9 refers to the *Figure 31* and list the external resistance combinations needed to activate one or more functions associated to the ZCD pin.

Table 9. ZCD pin configurations

Function / component	R_{LIM}	R_{OVP}	R_{FF}	D_{OVP}
I_{DLIM} set point	See *Equation 4*	Required for ZCD	Not required	Yes
OVP	22 kΩ	See equation 7	Not required	Yes
Line feed-forward	22 kΩ	Required for ZCD	See *Equation 3*	Yes
I_{DLIM} set point and OVP	See *Equation 4* with RFF = ∞	See equation 7	Not required	Yes
OVP and line feed-forward	22 kΩ	See equation 7	See *Equation 3*	Yes
I_{DLIM} set point and line feed-forward	See *Equation 4*	Required for ZCD	See *Equation 3*	Yes
I_{DLIM} reduction+ OVP + Line feed-forward	See *Equation 4*	See equation 7	See *Equation 3*	Yes

7.13 Feedback and over load protection (OLP)

The VIPER25 is a current mode converter: the feedback pin controls the PWM operation, controls the burst mode and actives the overload protection of the device. *Figure 33 on page 29* and *Figure 34* show the internal current mode structure.

With the feedback pin voltage between V_{FBbm} and V_{FBlin}, (respectively 0.5 V and 3.3 V, typical values) the drain current is sensed and converted in voltage that is applied to the non inverting pin of the PWM comparator.

This voltage is compared with the one on the feedback pin through a voltage divider on cycle by cycle basis. When these two voltages are equal, the PWM logic orders the switch off of the power MOSFET. The drain current is always limited to I_{DLIM} value.

In case of overload the feedback pin increases in reaction to this event and when it goes higher than V_{FBlin} the drain current is limited to the default I_{DLIM} value or the one imposed through a resistor at the ZCD pin.

At the same time an internal current generator starts to charge the feedback capacitor (C_{FB}) and when the feedback voltage reaches the V_{FBolp} threshold, the converter is turned off and the restart phase is activated with reduced value of I_{DDch} current (0.6 mA typ, see *Table 7 on page 7*).

During the first start-up phase of the converter, after the soft-start-up time (typical value is 8.5 ms) the output voltage could force the feedback pin voltage to rise up to the V_{FBolp} threshold that switches off the converter itself.

To avoid this event, the appropriate feedback network has to be selected according to the output load. More the network feedback fixes the compensation loop stability. The *Figure 33 on page 29* and *Figure 34* show the two different feedback networks.

The time from the over load detection (VFB = V_{FBlin}) to the device shutdown (VFB = V_{FBolp}) can be calculating by C_{FB} value (see *Figure 33 on page 29* and *Figure 34*), using the formula:

Equation 8

$$T_{OLP-delay} = C_{FB} \times \frac{V_{FBolp} - V_{FBlin}}{3\mu A}$$

In the *Figure 33*, the capacitor connected to FB pin (C_{FB}) is used as part of the circuit to compensate the feedback loop but also as element to delay the OLP shut down owing to the time needed to charge the capacitor (see equation 8).

After the start-up time, 8.5 ms typ value, during which the feedback voltage is fixed at V_{FBlin}, the output capacitor could not be at its nominal value and the controller interpreter this situation as an over load condition. In this case, the OLP delay helps to avoid an incorrect device shut down during the start-up.

Owing to the above considerations, the OLP delay time must be long enough to by-pass the initial output voltage transient and check the over load condition only when the output voltage is in steady state. The output transient time depends from the value of the output capacitor and from the load.

When the value of the C_{FB} capacitor calculated for the loop stability is too low and cannot ensure enough OLP delay, an alternative compensation network can be used and it is showed in *Figure 34 on page 30*.

Using this alternative compensation network, two poles (f_{PFB}, f_{PFB1}) and one zero (f_{ZFB}) are introduced by the capacitors C_{FB} and C_{FB1} and the resistor R_{FB1}.

The capacitor C_{FB} introduces a pole (f_{PFB}) at higher frequency than f_{ZB} and f_{PFB1}. This pole is usually used to compensate the high frequency zero due to the ESR (Equivalent Series Resistor) of the output capacitance of the flyback converter.

The mathematical expressions of these poles and zero frequency, considering the scheme in *Figure 34* are reported by the equations below:

Equation 9

$$f_{ZFB} = \frac{1}{2 \cdot \pi \cdot C_{FB1} \cdot R_{FB1}}$$

Equation 10

$$f_{PFB} = \frac{R_{FB(DYN)} + R_{FB1}}{2 \cdot \pi \cdot C_{FB} \cdot \left(R_{FB(DYN)} \cdot R_{FB1}\right)}$$

Equation 11

$$f_{PFB1} = \frac{1}{2 \cdot \pi \cdot C_{FB1} \cdot \left(R_{FB1} + R_{FB(DYN)}\right)}$$

The $R_{FB(DYN)}$ is the dynamic resistance seen by the FB pin.

The C_{FB1} capacitor fixes the OLP delay and usually C_{FB1} results much higher than C_{FB}. The *Equation 8* can be still used to calculate the OLP delay time but C_{FB1} has to be considered instead of C_{FB}. Using the alternative compensation network, the designer can satisfy, in all case, the loop stability and the enough OLP delay time alike.

Figure 33. FB pin configuration

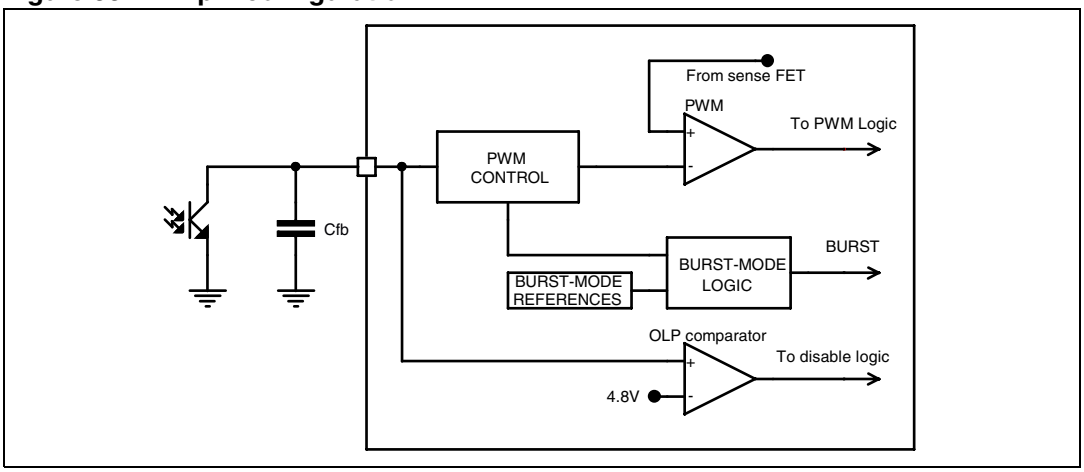
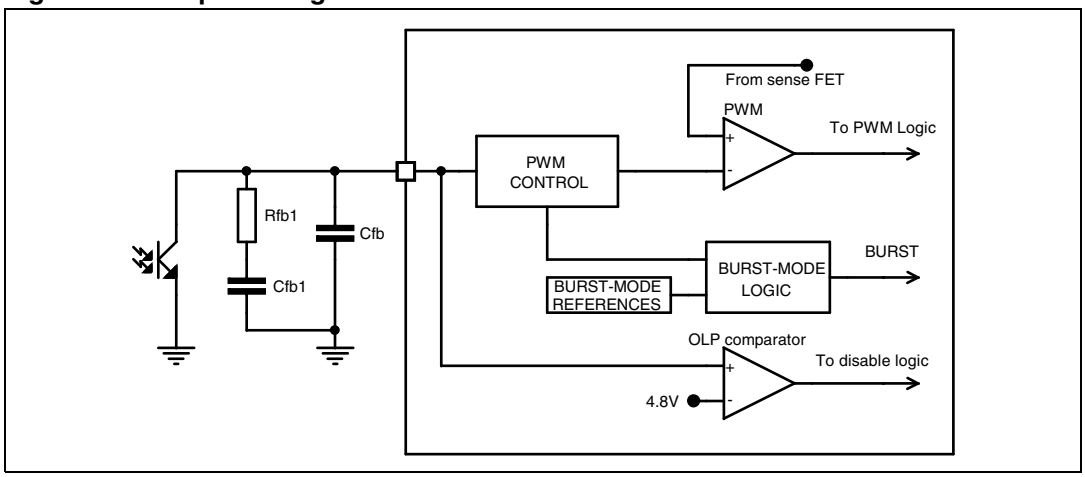


Figure 34. FB pin configuration

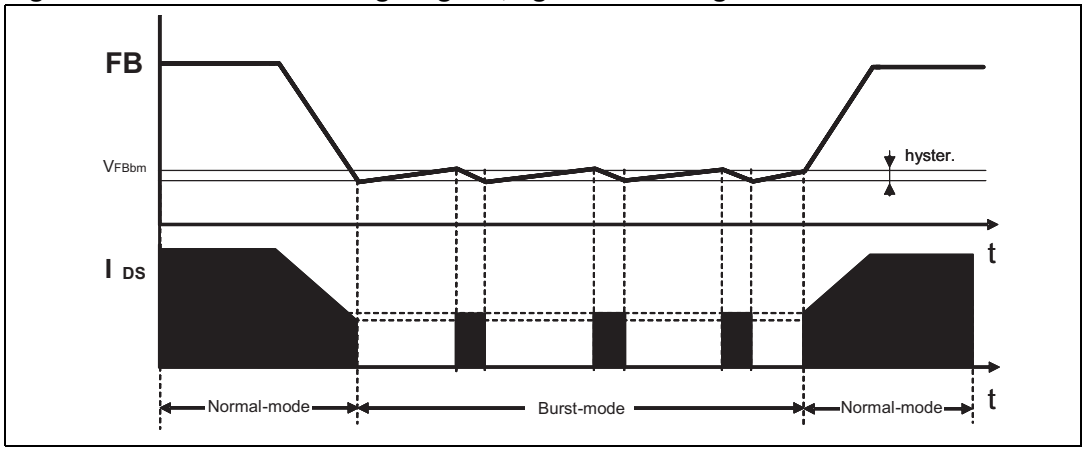


7.14 Burst-mode operation at no load or very light load

When the voltage on feedback pin falls down 50 mV below the burst mode threshold, V_{FBbm}, power MOSFET is not more allowed to be switched on. It can be switched on again if the voltage on feedback pin exceeds V_{FBbm}. The voltage on PWM comparator non inverting internal input, connected to feedback pin through a resistive voltage divider, is lower clamped to a certain value leading to a minimum value, of 160 mA (typ.) for the drain peak current.

When the load decrease the feedback loop reacts lowering the feedback pin voltage. As the voltage goes 50 mV below V_{FBbm} MOSFET stops switching. After the MOSFET stops, as a result of the feedback reaction to the energy delivery stop, the feedback pin voltage increases and exceeding V_{FBbm} threshold MOSFET the power device start switching again. *Figure 35* shows this behavior called burst mode. Systems alternates period of time where power MOSFET is switching to period of time where power MOSFET is not switching. The power delivered to output during switching periods exceeds the load power demands; the excess of power is balanced from not switching period where no power is processed. The advantage of burst mode operation is an average switching frequency much lower then the normal operation working frequency, up to some hundred of hertz, minimizing all frequency related losses.

Figure 35. Burst mode timing diagram, light load management



7.15 Brown-out protection

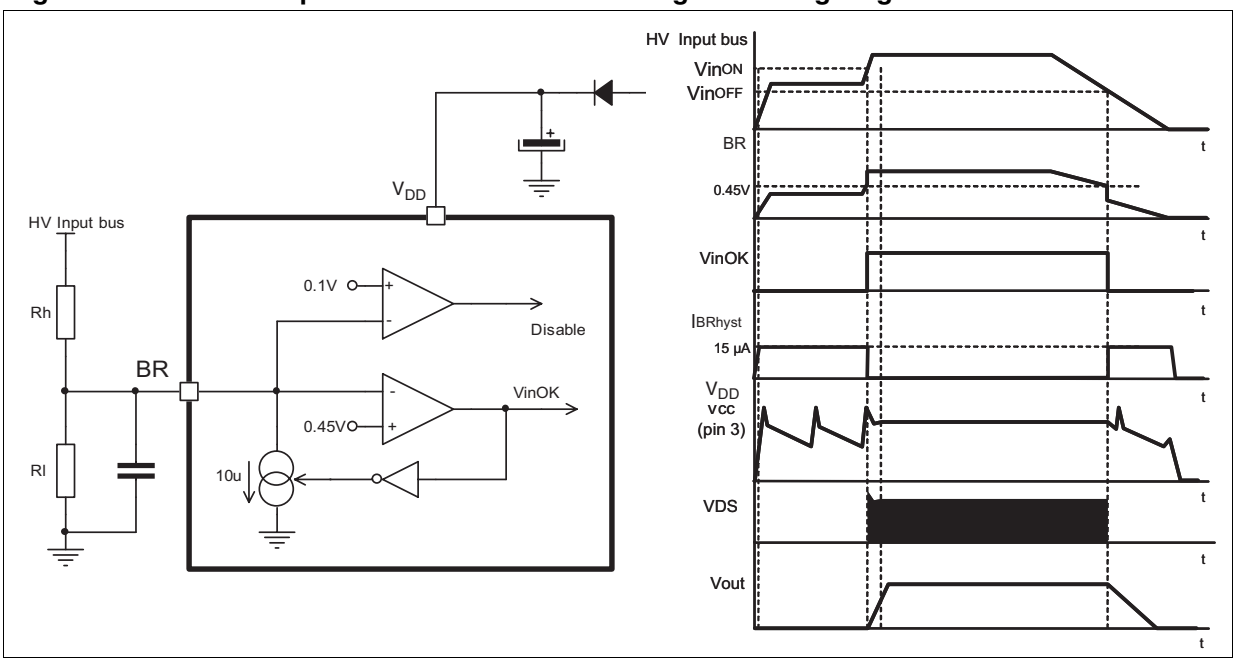
Brown-out protection is a not-latched shutdown function activated when a condition of mains under voltage is detected.

The Brown-out comparator is internally referenced to V_{BRth},0.45 V typ value, and disables the PWM if the voltage applied at the BR pin is below this internal reference. Under this condition the power MOSFET is turned off. Until the brown-out condition is present, the VDD voltage continuously oscillates between the V_{DDon} and the UVLO thresholds, as shown in the timing diagram of *Figure 36 on page 31*. A voltage hysteresis is present to improve the noise immunity.

The switching operation is restarted as the voltage on the pin is above the reference plus the before said voltage hysteresis. See *Figure 36*.

The brown-out comparator is provided also with a current hysteresis, I_{BRhyst}.With this approach is possible to set the V_{INon} threshold and V_{INoff} thresholds separately, by properly choosing the resistors of the divider connect to the BR pin.

Figure 36. Brown-out protection: BR external setting and timing diagram



Fixed the V_{INon} and the V_{INoff} levels, with reference to *Figure 36*, the following relationships can be established for the calculation of the resistors R_H and R_L:

Equation 12

$$R_L = -\frac{V_{BRhyst}}{I_{BRhyst}} + \frac{V_{INon} - V_{INoff} - V_{BRhyst}}{V_{INoff} - V_{BRth}} \times \frac{V_{BRth}}{I_{BRhyst}}$$

Equation 13

$$R_H = \frac{V_{INon} - V_{INoff} - V_{BRhyst}}{I_{BRhyst}} \times \frac{R_L}{R_L + \frac{V_{BRhyst}}{I_{BRhyst}}}$$

For a proper operation of this function, $V_{IN\ on}$ must be less than the peak voltage at minimum mains and $V_{IN\ off}$ less than the minimum voltage on the input bulk capacitor at minimum mains and maximum load.

The BR pin is a high impedance input connected to high value resistors, thus it is prone to pick up noise, which might alter the OFF threshold when the converter operates or gives origin to undesired switch-off of the device during ESD tests.

It is possible to bypass the pin to ground with a small film capacitor (e.g. 1-10 nF) to prevent any malfunctioning of this kind.

If the brown-out function is not used the BR pin has to be connected to GND, ensuring that the voltage is lower than V_{DIS} (see *Table 8*). In order to enable the brown-out function the BR pin voltage has to be higher than V_{EN} (see *Table 8*)

7.16 2nd level overcurrent protection and hiccup mode

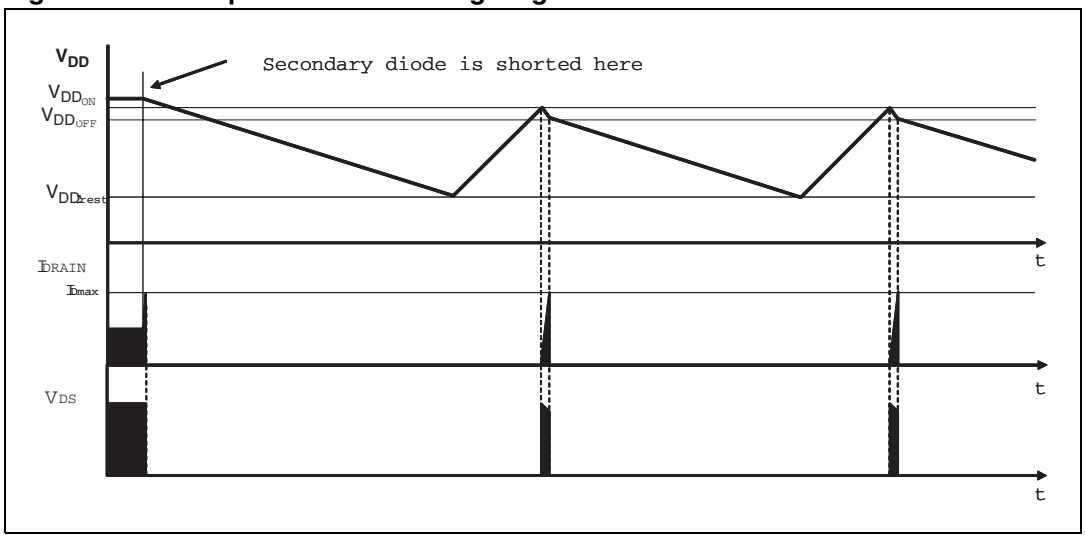
The VIPER25 is protected against short circuit of the secondary rectifier, short circuit on the secondary winding or a hard-saturation of flyback transformer. Such as anomalous condition is invoked when the drain current exceed 1.2 A typical.

To distinguish a real malfunction from a disturbance (e.g. induced during ESD tests) a “warning state” is entered after the first signal trip. If in the subsequent switching cycle the signal is not tripped, a temporary disturbance is assumed and the protection logic will be reset in its idle state; otherwise if the 2nd OCP threshold is exceeded for two consecutive switching cycles a real malfunction is assumed and the power MOSFET is turned OFF.

The shutdown condition is latched as long as the device is supplied. While it is disabled, no energy is transferred from the auxiliary winding; hence the voltage on the V_{DD} capacitor decays till the V_{DD} under voltage threshold (V_{DDoff}), which clears the latch.

The start-up HV current generator is still off, until V_{DD} voltage goes below its restart voltage, V_{DDrest}. After this condition the V_{DD} capacitor is charged again by 600 µA current, and the converter switching restart if the V_{DDon} occurs. If the fault condition is not removed the device enters in auto-restart mode. This behavioral, results in a low-frequency intermittent operation (Hiccup-mode operation), with very low stress on the power circuit. See the timing diagram of *Figure 37*.

Figure 37. Hiccup-mode OCP: timing diagram



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 10. DIP-7 mechanical data

Dim.	mm		
	Typ.	Min.	Max.
A			5.33
A1		0.38	
A2	3.30	2.92	4.95
b	0.46	0.36	0.56
b2	1.52	1.14	1.78
c	0.25	0.20	0.36
D	9.27	9.02	10.16
E	7.87	7.62	8.26
E1	6.35	6.10	7.11
e	2.54		
eA	7.62		
eB			10.92
L	3.30	2.92	3.81
M (1)(2)	2.508		
N	0.50	0.40	0.60
N1			0.60
O (2)(3)	0.548		

1. Creepage distance > 800 V
2. Creepage distance as shown in the 664-1 CEI / IEC standard
3. Creepage distance 250 V

Note: 1 The leads size is comprehensive of the thickness of the leads finishing material.

2 Dimensions do not include mold protrusion, not to exceed 0,25 mm in total (both side).

3 Package outline exclusive of metal burrs dimensions.

4 Datum plane “H” coincident with the bottom of lead, where lead exits body.

5 Ref. POA mother doc. 0037880

Figure 38. DIP-7 package dimensions

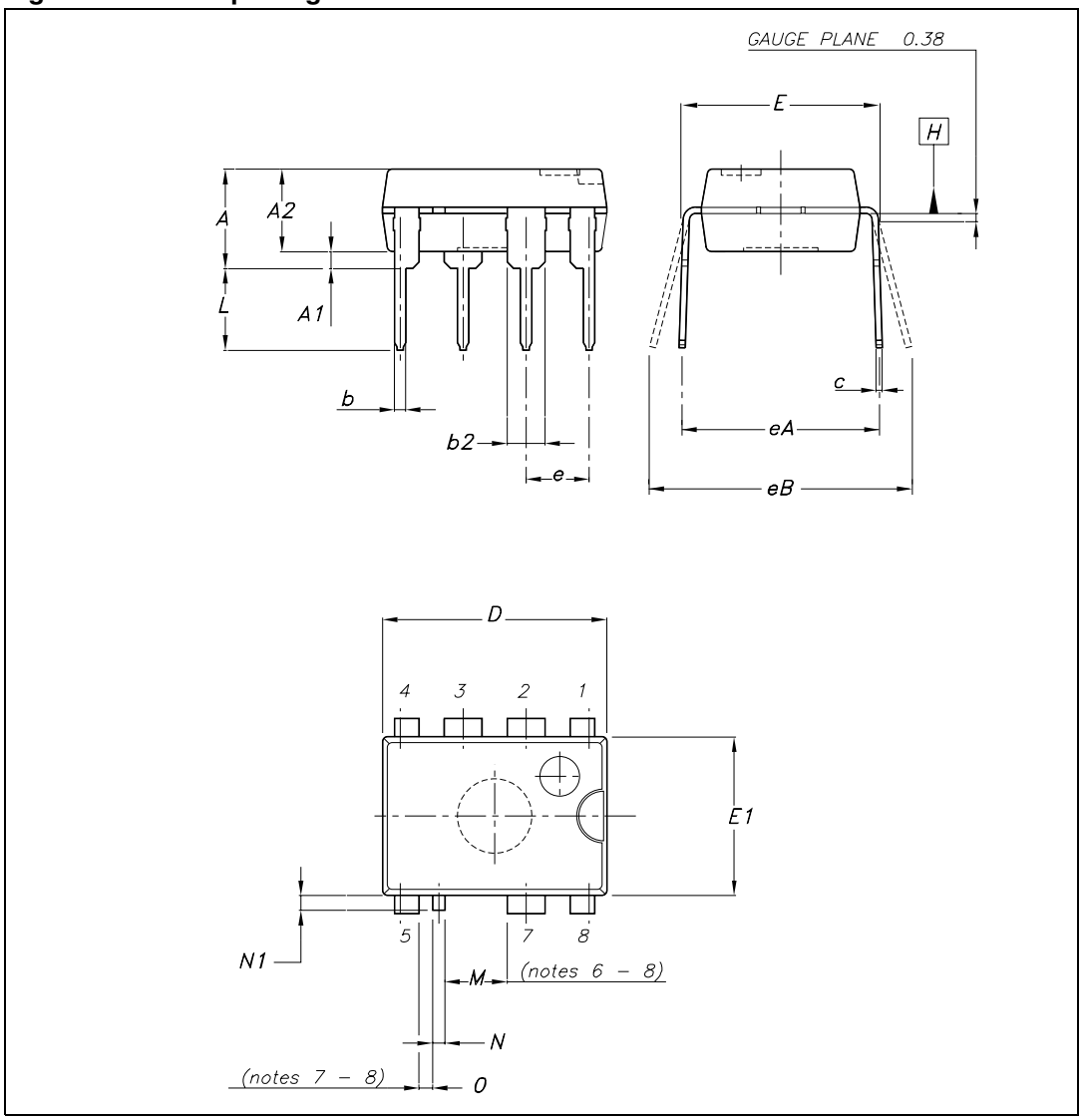
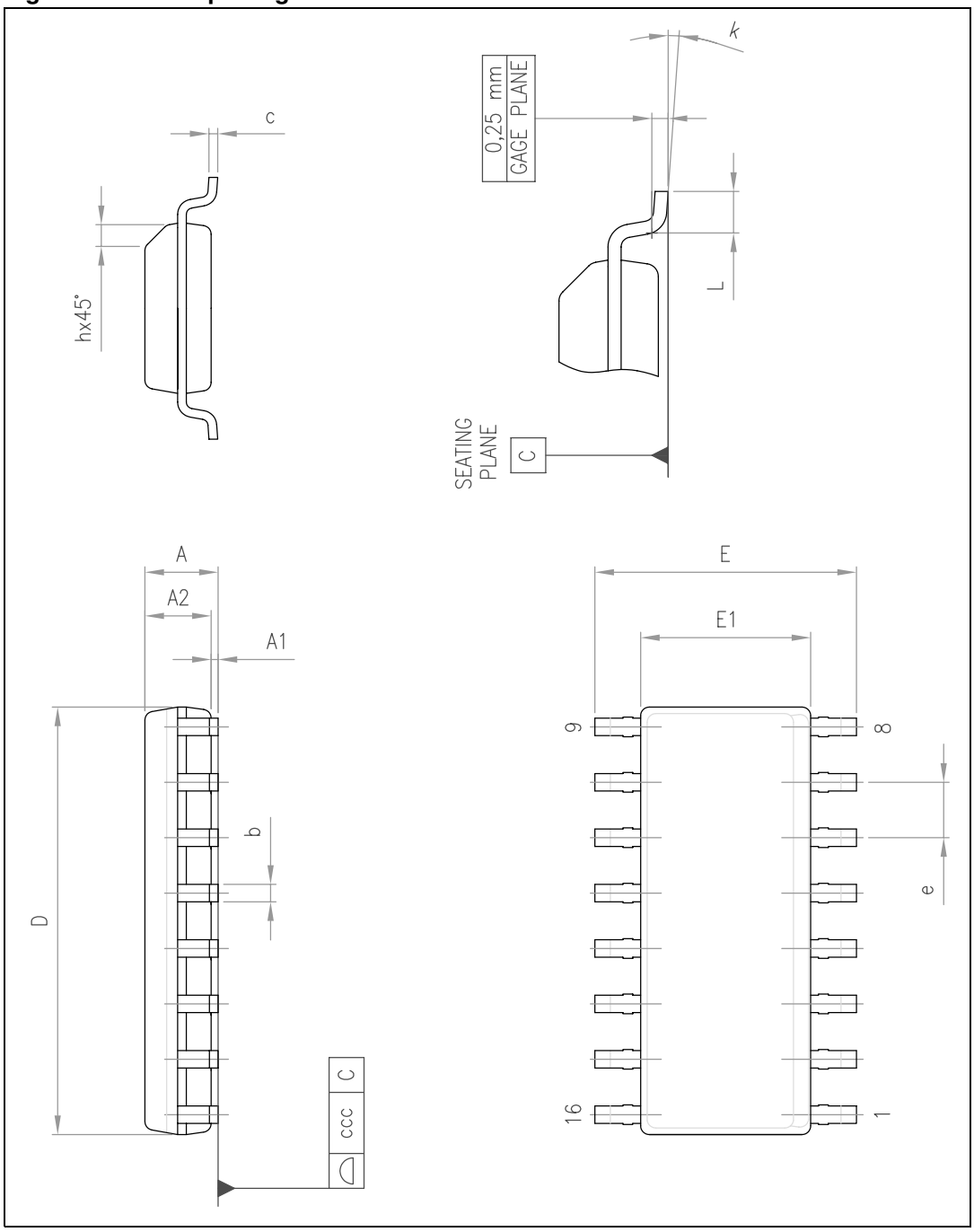


Table 11. SO16 narrow mechanical data

Dim.	Databook (mm.)		
	Min.	Typ.	Max.
A			1.75
A1	0.1		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.8	9.9	10
E	5.8	6	6.2
E1	3.8	3.9	4
e		1.27	
h	0.25		0.5
L	0.4		1.27
k	0		8
ccc			0.1

Figure 39. SO16 package dimensions



9 Revision history

Table 12. Document revision history

Date	Revision	Changes
17-Apr-2009	1	Initial release
09-Jun-2009	2	Updated application paragraph in coverpage and *Table 8 on page 8*

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com