



August 1993

54LVQ/74LVQ125

Low Voltage Quad Buffer with TRI-STATE® Outputs

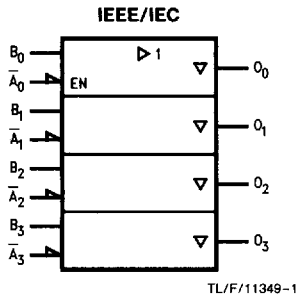
General Description

The 74LVQ125 contains four independent non-inverting buffers with TRI-STATE outputs.

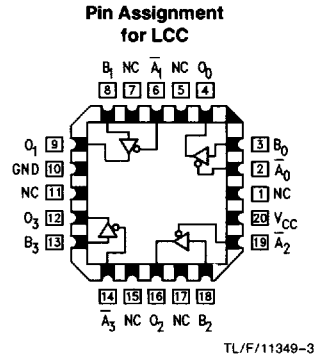
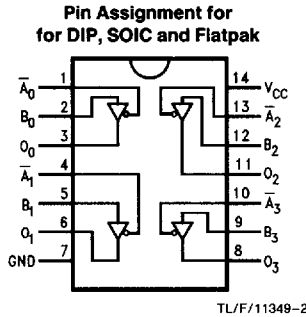
Features

- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Guaranteed incident wave switching into 75Ω

Logic Symbol



Connection Diagrams



Pin Names	Description
\bar{A}_n, B_n	Inputs
O_n	Outputs

Function Table

Inputs		Output
A_n	B_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 Z = HIGH Impedance
 X = Immaterial

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54LVQ/74LVQ125 Low Voltage Quad Buffer with TRI-STATE Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V _{CC})	-0.5V to +7.0V
DC Input Diode Current (I _{IK})	
V _I = -0.5V	-20 mA
V _I = V _{CC} + 0.5V	+20 mA
DC Input Voltage (V _I)	-0.5V to V _{CC} + 0.5V
DC Output Diode Current (I _{OK})	
V _O = -0.5V	-20 mA
V _O = V _{CC} + 0.5V	+20 mA
DC Output Voltage (V _O)	-0.5V to V _{CC} + 0.5V
DC Output Source or Sink Current (I _O)	±50 mA
DC V _{CC} or Ground Current per Output Pin (I _{CC} or I _{GND})	±50 mA
Storage Temperature (T _{STG})	-65°C to +150°C
DC Latch-Up Source or Sink Current	±100 mA
Junction Temperature (T _J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of 'LVQ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V _{CC})	'LVQ	3.0V to 3.6V
Input Voltage (V _I)		0V to V _{CC}
Output Voltage (V _O)		0V to V _{CC}
Operating Temperature (T _A)	74LVQ	-40°C to +85°C
	54LVQ	-55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt)	V _{IN} from 0.8V to 2.0V	
	V _{CC} @ 3.0V	125 mV/ns

DC Characteristics

Symbol	Parameter	V _{CC} (V)	74LVQ		54LVQ	74LVQ		Units	Conditions
			T _A = +25°C		T _A = -55°C to +125°C	T _A = -40°C to +85°C			
			Typ	Guaranteed Limits					
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	2.0	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	0.8	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I _{OUT} = -50 μA	
		3.0		2.56	2.4	2.46		*V _{IN} = V _{IL} or V _{IH} I _{OH} = -12 mA	
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I _{OUT} = 50 μA	
		3.0		0.36	0.50	0.44	V	*V _{IN} = V _{IL} or V _{IH} I _{OL} = 12 mA	
I _{IN}	Maximum Input Leakage Current	3.6		±0.1	±1.0	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum TRI-STATE Leakage Current	3.6		±0.5	±10.0	±5.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , V _{GND} V _O = V _{CC} , GND	

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V _{CC} (V)	74LVQ		54LVQ		74LVQ		Units	Conditions
			T _A = +25°C		T _A = -55°C to +125°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits						
I _{OLD}	†Minimum Dynamic Output Current	3.6					36		mA	V _{OLD} = 0.8V Max (Note 1)
I _{OHD}		3.6					-25		mA	V _{OHD} = 2.0V Min (Note 1)
I _{CC}	Maximum Quiescent Supply Current	3.6		5.0		100		50	μA	V _{IN} = V _{CC} or GND
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.6	1.0					V	(Notes 2 and 3)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.6	-1.0					V	(Notes 2 and 3)
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0					V	(Notes 2 and 4)
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.5	0.8					V	(Notes 2 and 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74LVQ			54LVQ		74LVQ		Units
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay Data to Output	3.3	1.0	6.5	9.0			1.0	10.0	ns
t _{PHL}	Propagation Delay Data to Output	3.3	1.0	6.5	9.0			1.0	10.0	ns
t _{PZH}	Output Enable Time	3.3	1.0	6.0	10.5			1.0	11.0	ns
t _{PZL}	Output Enable Time	3.3	1.0	7.5	10.0			1.0	11.0	ns
t _{PHZ}	Output Disable Time	3.3	1.0	7.5	10.0			1.0	10.5	ns
t _{PLZ}	Output Disable Time	3.3	1.0	7.5	10.5			1.0	11.5	ns
t _{OSHL} , t _{OSLH}	Output to Output Skew** Data to Output	3.3		1.0	1.5				1.5	ns

*Voltage range is 3.3V ± 0.3V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

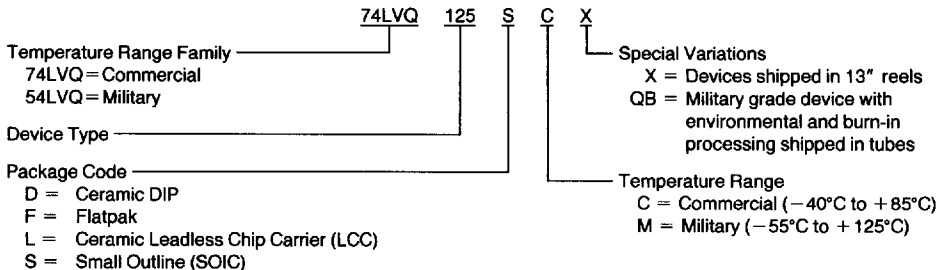
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 3.3V
C _{PD} (Note 1)	Power Dissipation Capacitance	34	pF	V _{CC} = 3.3V

Note 1: C_{PD} is measured at 10 MHz.

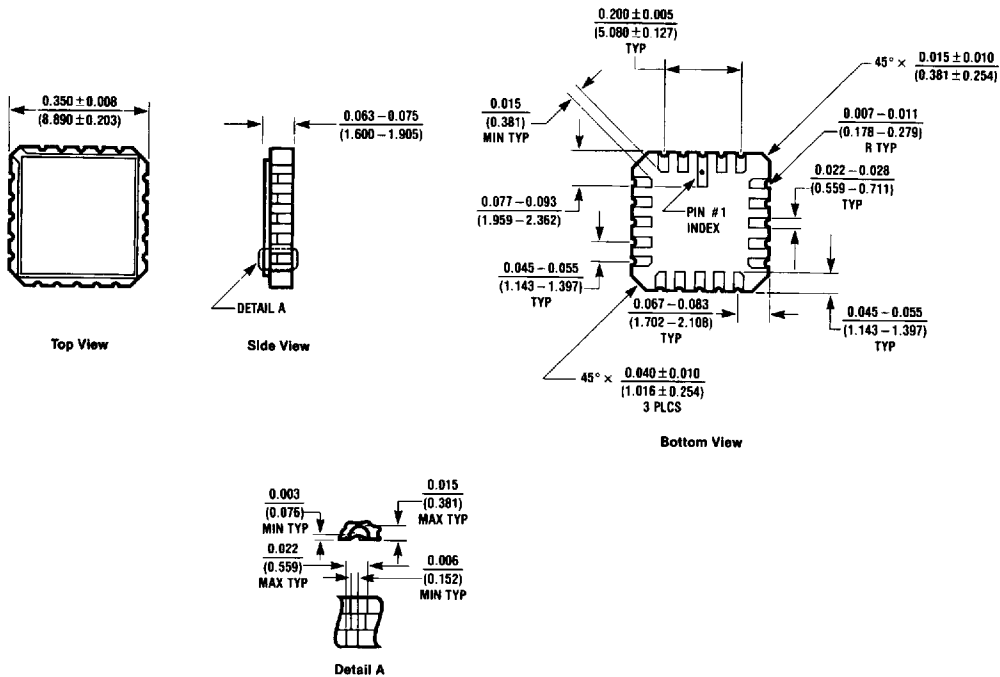
Ordering Information

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The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



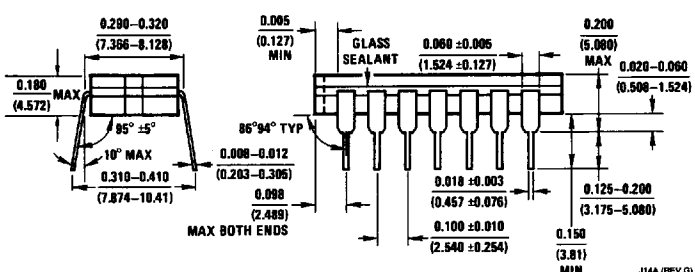
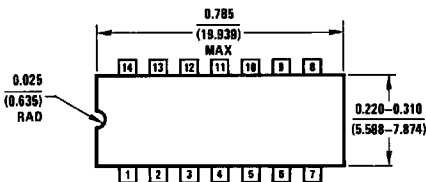
Physical Dimensions inches (millimeters)



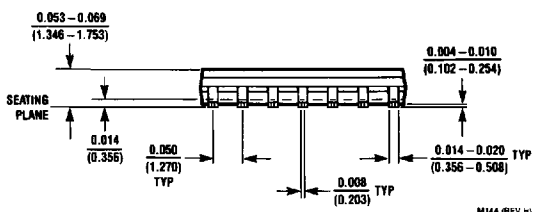
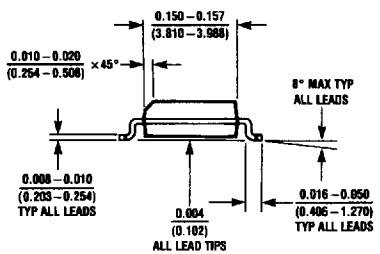
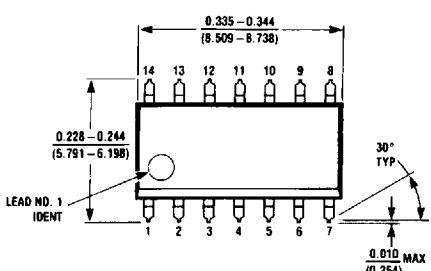
20 Terminal Ceramic Leadless Chip Carrier (L)
 NS Package Number E20A

E20A (REV D)

Physical Dimensions inches (millimeters) (Continued) **NATIONAL SEMICONDUCTOR LOGIC**



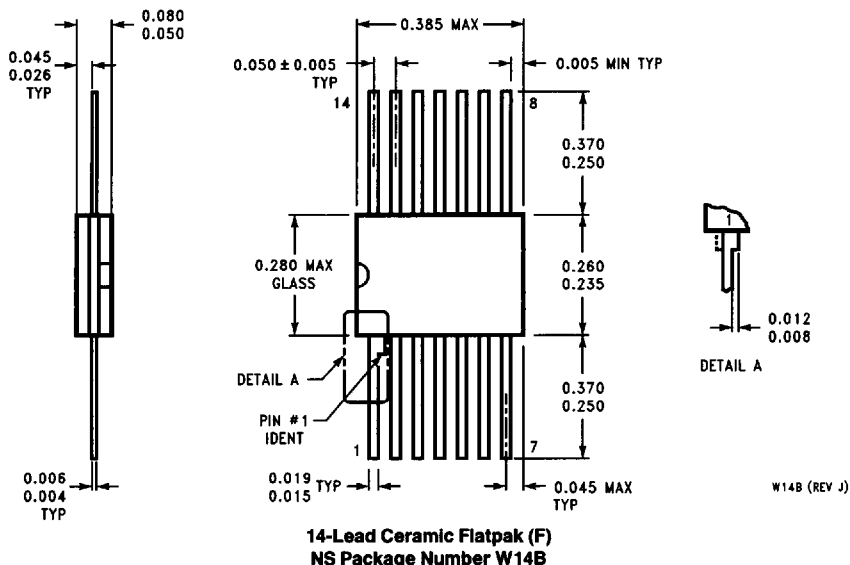
14-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J14A



14-Lead Small Outline Integrated Circuit (S)
NS Package Number M14A

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Physical Dimensions inches (millimeters) (Continued)



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