250 kSPS, 6-Channel,Simultaneous Sampling, Bipolar 12/14/16-Bit ADC

Preliminary Technical Data

AD7658/AD7657/AD7656*

FEATURES

6 Independent ADCs
True Bipolar Analog Inputs
Pin/Software Selectable Ranges:- ±10V, ±5V
Fast throughput rate: 250 kSPS
Specified for V_{CC} of 4.5 V to 5.5 V
Low power
160mW at 250 kSPS with 5 V supplies
Wide input bandwidth:
85 dB SNR at 50 kHz input frequency
On-chip Reference and Reference Buffers
Parallel and Serial Interface
High speed serial interface
SPI/QSPI/µWire/DSP compatible
Standby mode: 5 µA max
***i*CMOS™ Process Technology**
64 LQFP package

APPLICATIONS

Power Line Monitoring systems
Instrumentation and control systems
Multi-axis positioning systems

FUNCTIONAL BLOCK DIAGRAM

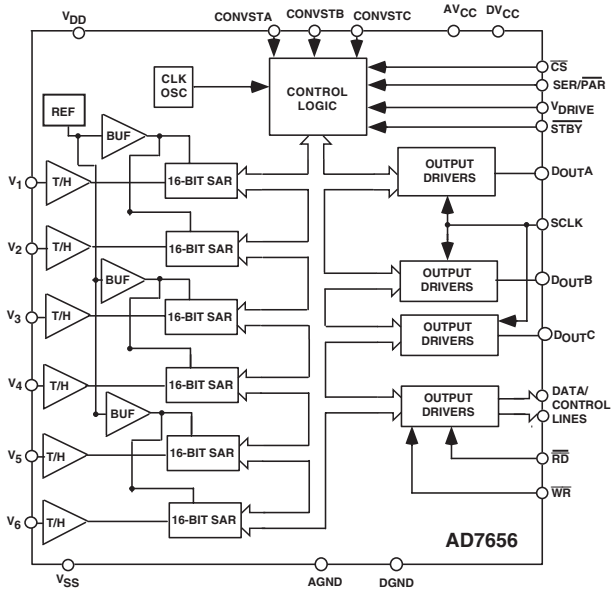

Figure 1.

GENERAL DESCRIPTION

The AD7658/AD7657/AD7656 contain six 12/14/16-bit, fast, low power, successive approximation ADCs all in the one package. The AD7658/AD7657/AD7656 core operates from a single 4.5 V to 5.5 V power supply and features throughput rates up to 250 kSPS. The parts contain low noise, wide bandwidth track-and-hold amplifiers that can handle input frequencies up to 8 MHz.

The conversion process and data acquisition are controlled using CONVST signals and an internal oscillator. Three CONVST pins allow independent simultaneous sampling of the three ADC pairs. The AD7658/AD7657/AD7656 have both a high speed parallel and serial interface allowing the devices to interface with microprocessors or DSPs. When in Serial interface mode these parts have a Daisy Chain feature allowing multiple ADCs to connect to a single serial interface. The AD7658/AD7657/AD7656 can accommodate true bipolar input signals in the ±10V range and ±5V range . They contain a 2.5V internal reference and can also accept an external reference. If a 3V external reference is applied to the VREF pin, the ADCs can accommodate a true bipolar ±12V analog input range. V_{DD} and V_{SS} supplies of ±12V are required for this ±12V input range.

PRODUCT HIGHLIGHTS

1. Six 12/14/16-bit 250 kSPS ADCs on board.
2. Six true bipolar high impedance analog inputs.
3. The AD7658/AD7657/AD7656 feature both a parallel and a high speed serial interface.

* Protected by U.S. Patent No. 6,731,232

*i*CMOS™ Process Technology
For analog systems designers within industrial/instrumentation equipment OEMs who need high performance ICs at higher-voltage levels, *i*CMOS is a technology platform that enables the development of analog ICs capable of 30V and operating at +/- 15V supplies while allowing dramatic reductions in power consumption and package size, and increased AC and DC performance.

Rev. PrI

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REVISION HISTORY

Revision PrI: Preliminary Version

AD7658 SPECIFICATIONS[1]

Table 1. AV_{CC} = 4.5 V to 5.5 V, V_{DD} = 9.5 V to 16.5 V, V_{SS} = -9.5 V to -16.5V, DV_{CC} = 4.5 V to 5.5 V, V_{DRIVE} = 2.7V to 5.25V, f_{SAMPLE} = 250 kSPS, VREF = 2.5V Internal/External, unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted

Parameter	B Versions[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 50 kHz sine wave
Signal-to-Noise + Distortion (SINAD)[2]	70	dB min	
	71	dB typ	
Total Harmonic Distortion (THD)[2]	−92	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[2]	−-TBD	dB typ	
Intermodulation Distortion (IMD)[2]			
Second-Order Terms	−94	dB typ	
Third-Order Terms	−100	dB typ	
Aperture Delay	20	ns max	
Aperature Delay Matching	2	ns max	
	100	ps typ	
Aperture Jitter	30	ps typ	
Full Power Bandwidth	8	MHz typ	@ −3 dB
	2.2	MHz typ	@ −0.1 dB
DC ACCURACY			
No Missing Codes	12	Bits min	
Integral Nonlinearity[2]	±1	LSB typ	
Positive Full Scale Error[2]	±0.4	% FS max	
Bipolar Zero Error[2]	±2.1	mV max	V_{DD} = 5.5 V
Negative Full Scale Error[2]	±0.4	% FS max	
ANALOG INPUT			
Input Voltage Ranges	±4xVREF	V	RNG bit/RANGE pin = 0
	±2xVREF	V	RNG bit/RANGE pin = 1
DC Leakage Current	±0.3	µA max	
Input Capacitance	30	pF typ	
REFERENCE INPUT/OUTPUT			
Reference output voltage	2.49/2.51	V min/max	
Reference input Voltage range	2.5/3	V min/max	
DC Leakage current	±0.5	µA max	V_{REF} Pin
Input capacitance	20	pF typ	
V_{REF} Output Impedance	1	kOhms typ	
Reference temperature Coefficient	25	ppm/°C max	
	10	ppm/°C typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 x V_{DRIVE}	V min	
Input Low Voltage, V_{INL}	03 x V_{DRIVE}	V max	
Input Current, I_{IN}	±0.3	µA max	Typically 10 nA, V_{IN} = 0 V or V_{CC}
Input Capacitance, C_{IN}[3]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} − 0.2	V min	I_{SOURCE} = 200 µA;
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±0.3	µA max	
Floating-State Output Capacitance[3]	10	pF max	
Output Coding	Two's Complement		
CONVERSION RATE			
Conversion Time	3	µs max	
Track-and-Hold Acquisition Time	400	ns max	
Throughput Rate	250	kSPS	
POWER REQUIREMENTS			
V_{DD}	+9.5V/+16.5V	V min/max	

Parameter	B Versions[1]	Unit	Test Conditions/Comments
V_{SS}	-9.5V/-16.5V	V min/max	
AV_{CC}	4.5/5.5	V min/V max	
I_{DD}			Digital I/P_S = 0 V or V_{CC}
Normal Mode (Static)	40	mA max	SCLK on or off. V_{CC} = 5.5 V
Normal Mode (Operational)	35	mA max	f_{SAMPLE} = 250 kSPS. V_{CC} = 5.5 V
Full Power-Down Mode	5	µA max	SCLK on or off. V_{CC} = 5.5 V
Power Dissipation			V_{CC} = 5.5 V
Normal Mode (Operational)	192.5	mW max	f_{SAMPLE} = 250 kSPS
Full Power-Down	16.5	µW max	

[1]Temperature range as follows: B Version: −40°C to +85°C.
[2] See terminology section.
[3] Sample tested during initial release to ensure compliance.

AD7657 SPECIFICATIONS[1]

Table 2. AV_{CC} = 4.5 V to 5.5 V, V_{DD} = 9.5 V to 16.5 V, V_{SS} = -9.5 V to -16.5V, DV_{CC} = 4.5 V to 5.5 V, V_{DRIVE} = 2.7V to 5.25V, f_{SAMPLE} = 250 kSPS, VREF = 2.5V Internal/External, unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted

Parameter	B Versions[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 50 kHz sine wave
Signal-to-Noise + Distortion (SINAD[2]	81	dB min	
Signal-to-Noise Ratio (SNR)[2]	82	dB min	
	83	dB typ	
Total Harmonic Distortion (THD)[2]	−97	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[2]	−95	dB typ	
Intermodulation Distortion (IMD)[2]			
Second-Order Terms	−94	dB typ	
Third-Order Terms	−100	dB typ	
Aperture Delay	20	ns max	
Aperature Delay Matching	2	ns max	
	100	ps typ	
Aperture Jitter	30	ps typ	
Full Power Bandwidth	8	MHz typ	@ −3 dB
	2.2	MHz typ	@ −0.1 dB
DC ACCURACY			
No Missing Codes	14	Bits min	
Integral Nonlinearity[2]	±1.5	LSB typ	
Positive Full Scale Error[2]	±0.4	% FS max	
Bipolar Zero Error[2]	±2.1	mV max	V_{DD} = 5.5 V
Negative Full Scale Error[2]	±0.4	% FS max	
ANALOG INPUT			
Input Voltage Ranges	±4xVREF	V	RNG bit/RANGE pin = 0
	±2xVREF	V	RNG bit/RANGE pin = 1
DC Leakage Current	±0.3	µA max	
Input Capacitance	30	pF typ	
REFERENCE INPUT/OUTPUT			
Reference output voltage	2.49/2.51	V min/max	
Reference input Voltage range	2.5/3	V min/max	
DC Leakage current	±0.5	µA max	V_{REF} Pin
Input capacitance	20	pF typ	
V_{REF} Output Impedance	1	kOhms typ	
Reference temperature Coefficient	25	ppm/°C max	
	10	ppm/°C typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 x V_{DRIVE}	V min	
Input Low Voltage, V_{INL}	0.3 x V_{DRIVE}	V max	
Input Current, I_{IN}	±0.3	µA max	Typically 10 nA, V_{IN} = 0 V or V_{CC}
Input Capacitance, C_{IN} [3]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} − 0.2	V min	I_{SOURCE} = 200 µA;
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±0.3	µA max	
Floating-State Output Capacitance [3]	10	pF max	
Output Coding	Two's Complement		
CONVERSION RATE			
Conversion Time	3	µs max	
Track-and-Hold Acquisition Time	500	ns max	
Throughput Rate	250	kSPS	
POWER REQUIREMENTS			

Parameter	B Versions[1]	Unit	Test Conditions/Comments
V_{DD}	+9.5V/+16.5V	V min/max	
V_{SS}	-9.5V/-16.5V	V min/max	
AV_{CC}	4.5/5.5	V min/V max	
I_{DD}			Digital I/P_S = 0 V or V_{CC}
Normal Mode (Static)	40	mA max	SCLK on or off. V_{CC} = 5.5 V
Normal Mode (Operational)	35	mA max	f_{SAMPLE} = 250 kSPS. V_{CC} = 5.5 V
Full Power-Down Mode	5	μA max	SCLK on or off. V_{CC} = 5.5 V
Power Dissipation			V_{CC} = 5.5 V
Normal Mode (Operational)	192.5	mW max	f_{SAMPLE} = 250 kSPS
Full Power-Down	16.5	μW max	

[1]Temperature range as follows: B Version: −40°C to +85°C.
[2] See Terminology Section.
[3] Sample tested during initial release to ensure compliance.

AD7656 SPECIFICATIONS[1]

Table 3. AV_{CC} = 4.5 V to 5.5 V, V_{DD} = 9.5 V to 16.5 V, V_{SS} = -9.5 V to –16.5V, DV_{CC} = 4.5 V to 5.5 V, V_{DRIVE} = 2.7V to 5.25V, f_{SAMPLE} = 250 kSPS, VREF = 2.5V Internal/External, unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted

Parameter	B Versions[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 50 kHz sine wave
Signal-to-Noise + Distortion (SINAD)[2]	82.5	dB min	
	85	dB typ	
Signal-to-Noise Ratio (SNR)[2]	83	dB min	
	86	dB typ	
Total Harmonic Distortion (THD)[2]	−97	dB max	
Peak Harmonic or Spurious Noise (SFDR)[2]	−95	dB typ	
Intermodulation Distortion (IMD)[2]			
Second-Order Terms	−94	dB typ	
Third-Order Terms	−100	dB typ	
Aperture Delay	20	ns max	
Aperature Delay Matching	2	ns max	
	100	ps typ	
Aperture Jitter	30	ps typ	
Full Power Bandwidth	8	MHz typ	@ −3 dB
	2.2	MHz typ	@ −0.1 dB
DC ACCURACY			
No Missing Codes	15	Bits min	
Integral Nonlinearity[2]	±2	LSB typ	
	±4	LSB max	
Positive Full Scale Error[2]	±0.4	% FS max	
Bipolar Zero Error[2]	±2.1	mV max	V_{DD} = 5.5 V
Negative Full Scale Error[2]	±0.4	% FS max	
ANALOG INPUT			
Input Voltage Ranges	±4xVREF	V	RNG bit/RANGE pin = 0
	±2xVREF	V	RNG bit/RANGE pin = 1
DC Leakage Current	±0.3	µA max	
Input Capacitance	30	pF typ	
REFERENCE INPUT/OUTPUT			
Reference output voltage	2.49/2.51	V min/max	
Reference input Voltage range	2.5/3	V min/max	
DC Leakage current	±0.5	µA max	V_{REF} Pin
Input capacitance	20	pF typ	
V_{REF} Output Impedance	1	kOhms typ	
Reference temperature Coefficient	25	ppm/°C max	
	10	ppm/°C typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 x V_{DRIVE}	V min	
Input Low Voltage, V_{INL}	0.3 x V_{DRIVE}	V max	
Input Current, I_{IN}	±0.3	µA max	Typically 10 nA, V_{IN} = 0 V or V_{CC}
Input Capacitance, C_{IN}[3]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} − 0.2	V min	I_{SOURCE} = 200 µA;
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±0.3	µA max	
Floating-State Output Capacitance[3]	10	pF max	
Output Coding	Two's Complement		
CONVERSION RATE			
Conversion Time	3	µs max	
Track-and-Hold Acquisition Time	1	µs max	
Throughput Rate	250	kSPS	

Parameter	B Versions[1]	Unit	Test Conditions/Comments
POWER REQUIREMENTS			
V_{DD}	+9.5V/+16.5V	V min/max	
V_{SS}	-9.5V/-16.5V	V min/max	
AV_{CC}	4.5/5.5	V min/V max	
I_{DD}			Digital I/P_S = 0 V or V_{CC}
Normal Mode (Static)	40	mA max	SCLK on or off. V_{CC} = 5.5 V
Normal Mode (Operational)	35	mA max	f_{SAMPLE} = 250 kSPS. V_{CC} = 5.5 V
Full Power-Down Mode	5	µA max	SCLK on or off. V_{CC} = 5.5 V
Power Dissipation[4]			V_{CC} = 5.5 V
Normal Mode (Operational)	192.5	mW max	f_{SAMPLE} = 250 kSPS
Full Power-Down	16.5	µW max	

[1]Temperature range as follows: B Version: −40°C to +85°C.
[2] See terminology section.
[3] Sample tested during initial release to ensure compliance.

TIMING SPECIFICATIONS[1]

Table 4. AV_{CC} = 4.5 V to 5.5 V, V_{DD} = 9.5 V to 16.5 V, V_{SS} = -9.5 V to -16.5V, V_{DRIVE} = 2.7V to 5.25V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted

	Limit at T_{MIN}, T_{MAX}		
Parameter	**5 V**	**Unit**	**Description**
Parallel Mode			
$t_{CONVERT}$	3	µs typ	Conversion Time, Internal Clock
t_{QUIET}	400	ns min	Minimum quiet time required between bus relinquish and start of next conversion
t_1	3	ns min	CONVST high to BUSY high
$T_{wake-up}$	TBD	ns typ	$\overline{STBY}$ rising edge to CONVST rising edge
Write Operation			
t_{13}	0	ns min	$\overline{CS}$ to $\overline{WR}$ setup time
t_{14}	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold time
t_{12}	20	ns min	$\overline{WR}$ Pulse width
t_{15}	5	ns min	Data setup time before $\overline{WR}$ rising edge
$t_{12/14/16}$	5	ns min	Data hold after $\overline{WR}$ rising edge
Read Operation			
t_2	0	ns min	BUSY to $\overline{RD}$ Delay
t_3	0	ns min	$\overline{CS}$ to $\overline{RD}$ setup time
t_4	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold time
t_5	30	ns min	$\overline{RD}$ Pulse width
t_6	30	ns max	Data access time after $\overline{RD}$ falling edge
t_7	15	ns min	Bus relinquish time after $\overline{RD}$ rising edge
	25	ns max	
t_9	20	ns min	Minimum time between reads
Serial Interface			
f_{SCLK}	20	MHz max	Frequency of Serial Read Clock
t_{17}	10	ns max	$\overline{CS}$ to SCLK setup time
t_{18}	15	ns max	Delay from $\overline{CS}$ until SDATA three-state disabled
t_{19}	20	ns max	Data access time after SCLK rising edge
t_{20}	0.4 t_{SCLK}	ns min	SCLK low pulse width
t_{21}	0.4 t_{SCLK}	ns min	SCLK high pulse width
t_{22}	5	ns min	SCLK to data valid hold time
t_{23}	30	ns max	$\overline{CS}$ rising edge to SDATA high impedance

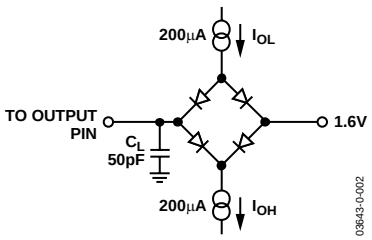


Figure 2. Load Circuit for Digital Output Timing Specification

[1] Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

ABSOLUTE MAXIMUM RATINGS

Table 5. T_A = 25°C, unless otherwise noted

Parameter	Rating
V_{DD} to AGND, DGND	-0.3 V to +16.5 V
V_{SS} to AGND, DGND	+0.3 V to –16.5 V
V_{CC} to AGND, DGND	-0.3V to +7V
V_{DRIVE} to V_{CC}	-0.3 V to V_{CC} + 0.3V
AGND to DGND	-0.3 V to +0.3 V
V_{DRIVE} to DV_{DD}	-0.3 V to DV_{DD} + 0.3V
Analog Input Voltage to AGND	V_{SS} – 0.5V to V_{DD} + 0.5V
Digital Input Voltage to DGND	-0.3 V to V_{DRIVE} +0.3 V
Digital Output Voltage to GND	-0.3 V to V_{DRIVE} +0.3V
REF_{IN} to AGND	-0.3 V to V_{CC} +0.3V
Input Current to Any Pin Except Supplies[2]	±10mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
64-LQFP Package, Power Dissipation	
θ_{JA} Thermal Impedance	TBD°C/W
θ_{JC} Thermal Impedance	TBD°C/W
Pb-free Temperature, Soldering	
Reflow	260(+0)°C
ESD	TBD kV

[1]Transient currents of up to 100 mA will not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTIONAL DESCRIPTIONS

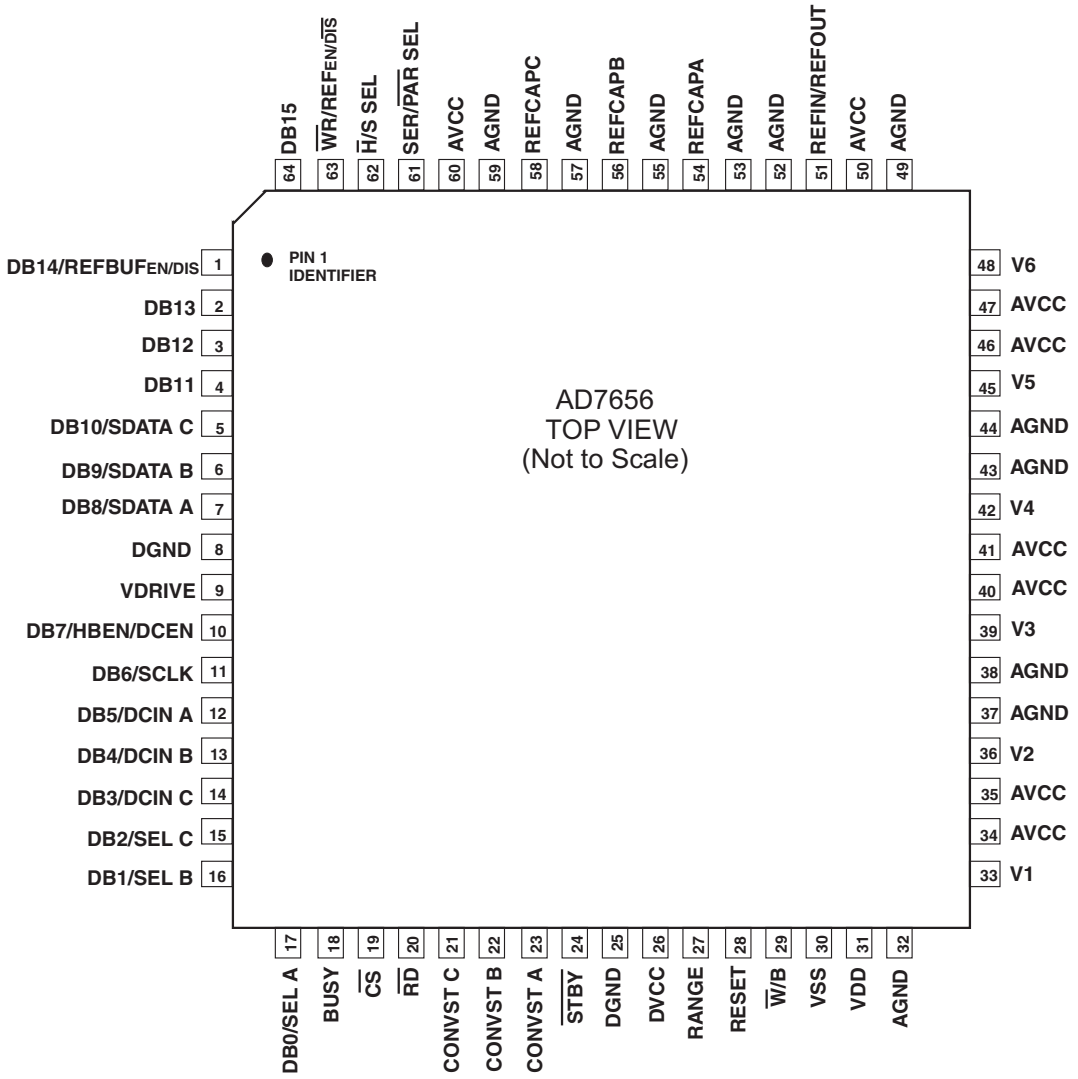


Table 6. AD7658/AD7657/AD7656 Pin Function Descriptions

Pin Mnemonic	Description
REFCAPA, REFCAPB, REFCAPC	Decoupling capacitors are connected to these pins to decouple the reference buffer for each ADC pair. Each REFCAP pin should be decoupled to AGND using 10 µF and 100 nF capacitors.
V1 – V6	Analog Input1-6. These are six single-ended Analog inputs. The Analog input range on these channels is ddetermined by the RANGE pin.
AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7658/AD7657/AD7656. All analog input signals and any external reference signal should be referred to this AGND voltage. All eleven of these AGND pins should be connected to the AGND plane of a system. The AGND and DGND voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
DVCC	Digital Power. Normally at 5V. The DVCC and AVCC voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis. This supply should be decoupled to DGND. 10 µF and 100 nF decoupling capacitors should be placed on the DVCC pin.
VDRIVE	Logic power supply input. The voltage supplied at this pin determines at what voltage the interface will operate. Nominally at the same supply as the supply of the host interface. This pin should be decoupled to DGND. 10 µF and 100 nF decoupling capacitors should be placed on the VDRIVE pin.

DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7658/AD7657/AD7656. Both DGND pins should connect to the DGND plane of a system. The DGND and AGND voltages ideally should be at the same potential and must not be more than 0.3 V apart even on a transient basis.
AVCC	Analog Supply Voltage, 4.5 V to 5.5 V. This is the only supply voltage for ADC cores. The AVCC and DVCC voltages ideally should be at the same potential and must not be more than 0.3 V apart even on a transient basis. This supply should be decoupled to AGND. 10 µF and 100 nF decoupling capacitors should be placed on the AVCC pins.
CONVSTA, B, C	Conversion Start Input A,B,C. Logic Inputs. These inputs are used to initiate conversions on the ADC pairs. CONVSTA is used to initiate simultaneous conversions on V1 and V2. CONVSTB is used to initiate simultaneous conversions on V3 and V4. CONVSTC is used to initiate simultaneous conversions on V5 and V6. When CONVSTX switches from low to high the track-and-hold switch on the selected ADC pairs switches from track to hold and the conversion is initiated.
$\overline{CS}$	Chip Select. Active low logic input. This input frames the data transfer. When both $\overline{CS}$ and $\overline{RD}$ are logic low in parallel mode the output bus is enabled and the conversion result is output on the Parallel Data Bus lines. When both $\overline{CS}$ and $\overline{WR}$ are logic low in parallel mode DB[15:8] are used to write data to the on-chip control register. In serial mode the $\overline{CS}$ is used to frame the serial read transfer.
$\overline{RD}$	Read Data. When both $\overline{CS}$ and $\overline{RD}$ are logic low in parallel mode the output bus is enabled. In serial Mode the $\overline{RD}$ line should be held low.
$\overline{WR}$/ REF EN/$\overline{DISABLE}$	Write Data/ reference Enable/Disable. When H/S SEL pin is high both $\overline{CS}$ and $\overline{WR}$ are logic low DB[15:8] are used to write data to the internal Control Register. When H/S SEL pin is low this pin is used to enable or disable the internal Reference. When H/S SEL =0 and REF EN/$\overline{DISABLE}$ = 0 the internal reference is disabled and an external reference should be applied to this pin. When H/S SEL = 0 and REF EN/$\overline{DISABLE}$ = 1 the internal reference is enabled.
BUSY	BUSY Output. Transitions high when a conversion is started and remains high until the conversion is complete and the conversion data is latched into the Output Data registers.
REFIN/REFOUT	Reference Input/Output. The on-chip reference is available on this pin for use external to the AD7658/AD7657/AD7656. Alternatively, the internal reference can be disabled and an external reference applied to this input. See Reference Section.
SER/$\overline{PAR}$	Serial/parallel selection Input. When low, the parallel port is selected. When high the serial interface mode is selected. In serial mode DB[10:8] take on their SDATA [C:A] function, DB[0:2] take on their DOUT select function, DB[7] takes on its DCEN function. In serial mode DB15 and DB[13:11] should be tied to DGND.
DB[0]/SEL A	Data Bit [0]/Select DOUT A. When SER/$\overline{PAR}$ = 0, this pin acts as a three-state Parallel Digital Output pin. When SER/$\overline{PAR}$ is =1, this pin takes on its SEL A function, it is used to configure the serial interface. If this pin is 1, the serial interface will operate with one/two/three DOUT ouput pins and enables DOUT A as a serial output. When operating in serial mode this pin should always be = 1.
DB[1]/SEL B	Data Bit [1]/Select DOUT B. When SER/$\overline{PAR}$ = 0, this pin acts as a three-state Parallel Digital Output pin. When SER/$\overline{PAR}$ is =1, this pin takes on its SEL B function, it is used to configure the serial interface. If this pin is 1, the serial interface will operate with two/three DOUT ouput pins and enables DOUT B as a serial output. If this pin is 0 the DOUT B is not enabled to operate as a serial Data Output pin and only one DOUT output pin is used.
DB[2]/SEL C	Data Bit [2]/Select DOUT C. When SER/$\overline{PAR}$ = 0, this pin acts as a three-state Parallel Digital Output pin. When SER/$\overline{PAR}$ is =1, this pin takes on its SEL C function, it is used to configure the serial interface. If this pin is 1, the serial interface will operate with three DOUT ouput pins and enables DOUT C as a serial output. If this pin is 0 the DOUT C is not enabled to operate as a serial Data Output pin.
DB[3]/DCIN C	Data Bit [3]/Daisy Chain in C. When SER/$\overline{PAR}$ =0, this pin acts as a three-state Parallel Digital Output pin. When SER/$\overline{PAR}$ is =1 and DCEN = 1, this pin acts as Daisy Chain Input C.
DB[4]/DCIN B	Data Bit [4]/Daisy Chain in B. When SER/$\overline{PAR}$ =0, this pin acts as a three-state Parallel Digital Output pin. When SER/$\overline{PAR}$ is =1 and DCEN = 1, this pin acts as Daisy Chain Input B.
DB[5]/DCIN A	Data Bit [5]/Daisy Chain in A. When SER/$\overline{PAR}$ is low, this pin acts as a three-state Parallel Digital Output pin. When SER/$\overline{PAR}$ is =1 and DCEN = 1, this pin acts as Daisy Chain Input A.
DB[6]/SCLK	Data Bit [6[/Serial Clock. When SER/$\overline{PAR}$ =0, this pin acts as three-state Parallel Digital Output

	pin. When SER/$\overline{PAR}$ =1 this pin takes on its SCLK input function, obtaining the read serial clock for the serial transfer.
DB[7]/HBEN/DCEN	Data bit 7/ High Byte Enable/ Daisy Chain Enable. When operating in Parallel Word mode (SER/$\overline{PAR}$ = 0 and W/$\overline{B}$ = 1) this pin takes on its Data bit 7 function. When operating in Parallel Byte mode (SER/$\overline{PAR}$ = 0 and W/$\overline{B}$ = 0), this pin takes on its HBEN function. When in this mode and the HBEN pin is a logic high, the data will be output MSB byte first on DB[15:8]. When the HBEN pin is a logic low the data will be output LSB byte first on DB[15:8]. When operating in Serial mode (SER/$\overline{PAR}$ = 1) this pin takes on its DCEN function. When DCEN pin is a logic high the part will operate in Daisy Chain mode with DB[5:3] taking on their DCIN[A:C] function.
DB[8]/DOUT A	Data Bit [8]/Serial Data Output A. When SER/$\overline{PAR}$ =0, this pin acts as a three-state Parallel Digital Output pin. When SER/$\overline{PAR}$ =1 and SEL A = 1, this pin takes on its DOUT A function.
DB[9]/DOUT B	Data Bit [9]/Serial Data Output B. When SER/$\overline{PAR}$ =0, this pin acts as a three-state Parallel Digital Output pin. When SER/$\overline{PAR}$ =1 and SEL B = 1, this pin takes on its DOUT B function. This configures the serial interface to have two SDATA output lines.
DB[10]/DOUT C	Data Bit [10]/Serial Data Output C. When SER/$\overline{PAR}$ =0, this pin acts as a three-state Parallel Digital Output pin. When SER/$\overline{PAR}$ =1 and SEL C = 1, this pin takes on its DOUT C function. This configures the serial interface to have three SDATA output lines.
DB[11]/DGND	Data Bit [11]/Digital Ground. When SER/$\overline{PAR}$ =0, this pin acts as a three-state Parallel Digital Output pin. When SER/$\overline{PAR}$ =1, this pin should be tied to DGND.
DB[12:13], DB[15]	Data Bit [12:15]. SER/$\overline{PAR}$ =0 these pins act as a three-state parallel Digital Input/Output pins. When $\overline{CS}$ and $\overline{RD}$ are low these pins are used to output the conversion result. When $\overline{CS}$ and $\overline{WR}$ are low these pins are used to write to the Control Register. When SER/$\overline{PAR}$ =1 these pins should be tied to DGND.
DB[14]/REFBUF EN/$\overline{DIS}$	Data Bit [14]/ REFBUF ENABLE/$\overline{DISABLE}$. When SER/$\overline{PAR}$ =0, this pin acts as a three-state Digital Input/output pin. When SER/$\overline{PAR}$ =1, this pin can be used to enable or disable the internal reference buffers.
RESET	Reset Input. When set to a logic high, reset the AD7658/AD7657/AD7656. The Current conversion if any is aborted. Internal register is set to all 0's. If not in use, this pin could be tied low. In Hardware mode the AD7658/AD7657/AD7656 will be configured depending on the logic levels on the hardware select pins. When operating in software mode a reset pulse is required afterpower up to select the default settings in the Internal register. (See Register section)
RANGE	Analog Input Range Selection. Logic input. The polarity on this pin will determine what input range the analog input channels will have. When this pin is a logic 1 at the falling edge of BUSY then range for the next conversion is ± 2 x VREF. When this pin is a logic 0 at the falling edge of BUSY then range for the next conversion is ± 4 x VREF.
VDD	Positive power supply voltage. This is the positive supply voltage for the Analog Input section. 10 µF and 100 nF decoupling capacitors should be placed on the VDD pin.
VSS	Negative power supply voltage. This is the negavtive supply voltage for the Analog Input section. 10 µF and 100 nF decoupling capacitors should be placed on the VSS pin.
$\overline{STBY}$	Standby mode Input. This pin is used to put all six on-chip ADCs into standby mode. The $\overline{STBY}$ pin is high for normal operation and low for standby operation.
$\overline{H}$/S SEL	Hardware/Software Select Input. Logic Input. When SER/$\overline{PAR}$ =0 and this pin is a logic low the AD7658/AD7657/AD7656 operates in Hardware select mode. The ADC pairs to be simultaneously sampled are selected by the $\overline{CONVST}$ pins. When SER/$\overline{PAR}$ =0 this pin is a logic high the ADC pairs to be simultaneously sampled are selected by writing to the control register.
$\overline{W}$/B	Word/Byte Input. When this pin is a logic low data can be transfered to and from the AD7658/AD7657/AD7656 using the parallel data lines DB[15:0]. When this pin is a logic high Byte mode is enabled. In this mode data is transferred using data lines DB[15:8], DB[7] takes on its HBEN function. To obtain the 12/14/16-bit conversion result two byte reads are required.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Bipolar Zero Code Error
It is the deviation of the midscale transition (all 1s to all 0s) from the ideal V_{IN} voltage, i.e., AGND - 1 LSB.

Positive Full Scale Error
It is the deviation of the last code transition (011…110) to (011…111) from the ideal (+4 x V_{REF} - 1 LSB, + 2 x V_{REF} – 1 LSB) after the bipolar Zero Code Error has been adjusted out.

Negative Full Scale Error
This is the deviation of the first code transition (10…000) to (10…001) from the ideal (i.e., - 4 x V_{REF} + 1 LSB, - 2 x V_{REF} + 1 LSB) after the Bipolar Zero Code Error has been adjusted out.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode at the end of conversion. The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1 LSB, after the end of the conversion. See the Track-and-Hold Section for more details.

Signal-to-(Noise + Distortion) Ratio
This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency (f_S/2, excluding dc). The ratio depends on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02\ N + 1.76)\ dB$$

Thus, for a 12-bit converter, this is 74 dB, for a 14-bit converter, this is 86 dB and for a 16-bit converter, this is 98 dB.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7658/AD7657/AD7656, it is defined as

$$THD(dB) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to f_S/2, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second-order terms include (fa + fb) and (fa – fb), while the third-order terms include (2fa + fb), (2fa – fb), (fa + 2fb), and (fa –2fb).

The AD7658/AD7657/AD7656 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

CONVERTER DETAILS

The AD7658/AD7657/AD7656 are high-speed, low power converters that allow the simultaneous sampling of their six on-chip ADCs. The Analog Inputs on the AD7658/AD7657/AD7656 can accept True bipolar Input signals, the RANGE pin/RNG bits are used to select between ±4 x VREF or ±2 x VREF as the Input Range for the next conversion.

The AD7658/AD7657/AD7656 contain six SAR ADCs, six track-and-hold amplifiers, on-chip 2.5V reference, reference buffers, high speed parallel and serial interfaces. The AD7658/AD7657/AD7656 allow the simultaneous sampling of all six ADCs when all three CONVST signals are tied together. Alternatively the six ADCs can be grouped into three pairs. Each pair has an associated CONVST signal used to initiate simultaneous sampling on each ADC pair, on four ADCs or all six ADCs. CONVSTA is used to initiate simultaneous sampling on V1 and V2, CONVSTB is used to initiate simultaneous sampling on V3 and V4, and CONVSTC is used to initiate simultaneous sampling on V5 and V6.

A conversion is initiated on the AD7658/AD7657/AD7656 by pulsing the CONVSTX input. On the rising edge of CONVSTX the track-and-hold on the selected ADCs will be placed into hold mode and the conversions are started. After the rising edge of CONVSTX the BUSY signal will go high to indicate the conversion is taking place. The conversion clock for the part is internally generated and the conversion time for the AD7658/AD7657/AD7656 is 3 µs from the rising edge of CONVSTX. The BUSY signal will return low to indicate the end of conversion. On the falling edge of BUSY the track-and-hold will return to track mode. Data can be read from the output register via the parallel or serial interface.

Track-and-Hold Section

The track-and-Hold amplifiers on the AD7658/AD7657/AD7656 allow the ADCs to accurately convert an input sine wave of full-scale amplitude to 12/14/16-bit resolution. The input bandwidth of the track-and-hold amplifiers is greater that the Nyquist rate of the ADC even when the AD7658/AD7657/AD7656 is operating at its maximum throughput rate. The AD7658/AD7657/AD7656 can handle input frequencies up to 8 MHz.

The track-and-hold amplifiers sample their respective inputs simultaneously on the rising edge of CONVSTX. The aperture time for the track-and-hold, (i.e. the delay time between the external CONVSTX signal actually going into hold), is typically 20ns. This is well matched across all six track-and-holds on the one device and also from device to device. This allows more than six ADCs to be simultaneously sampled. The end of the conversion is signaled by the falling edge of BUSY and its at this point the track-and-holds return to track mode and the acquisition time begins.

Analog Input Section

The AD7658/AD7657/AD7656 can handle True bipolar input voltages. The logic level on the RANGE pin or the value written to the RNGX bits in the Control register will determine the Analog input Range on the AD7658/AD7657/AD7656 for the next conversion. When the RANGE pin/ RNGX bit is 1 the Analog input range for the next conversion is ±2 x VREF, when the RANGE pin/ RNG bit is 0 the Analog Input range for the next conversion is ±4 x VREF.

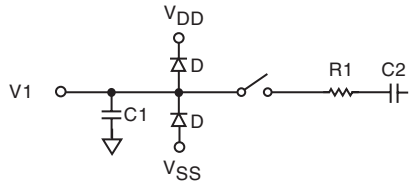


Figure 3. Equivalent Analog Input Structure

Figure 3 shows an equivalent circuit of the analog input structure of the AD7658/AD7657/AD7656. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the V_{DD} and V_{SS} supply rails by more than TBD mV. This will cause these diodes to become forward-biased and to start conducting current into the substrate. The maximum current these diodes can conduct without causing irreversible damage to the part is 10 mA. Capacitor C1 in Figure 3 is typically about 5 pF and can be attributed primarily to pin capacitance. Resistor R1 is a lumped component made up of the on resistance of a switch (track-and-hold switch). This resistor is typically about 25 Ω. Capacitor C2 is the ADC sampling capacitor and has a capacitance of 25 pF typically.

ADC TRANSFER FUNCTION

The output coding of the AD7658/AD7657/AD7656 is two's Complement. The designed code transitions occur midway between successive integer LSB values, i.e., 1/2 LSB, 3/2 LSBs. The LSB size is FSR/4096 for the AD7658, FSR/16384 for the AD7657 and FSR/65536 for the AD7656. The ideal transfer characteristic for the AD7658/AD7657/AD7656 is shown in Figure 4.

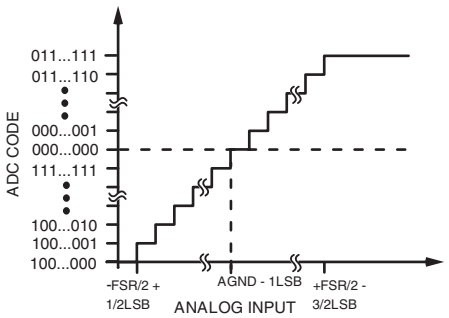


Figure 4. AD7658/AD7657/AD7656 Transfer Characteristic

The LSB size is dependant on the Analog Input Range selected. See Table 7.

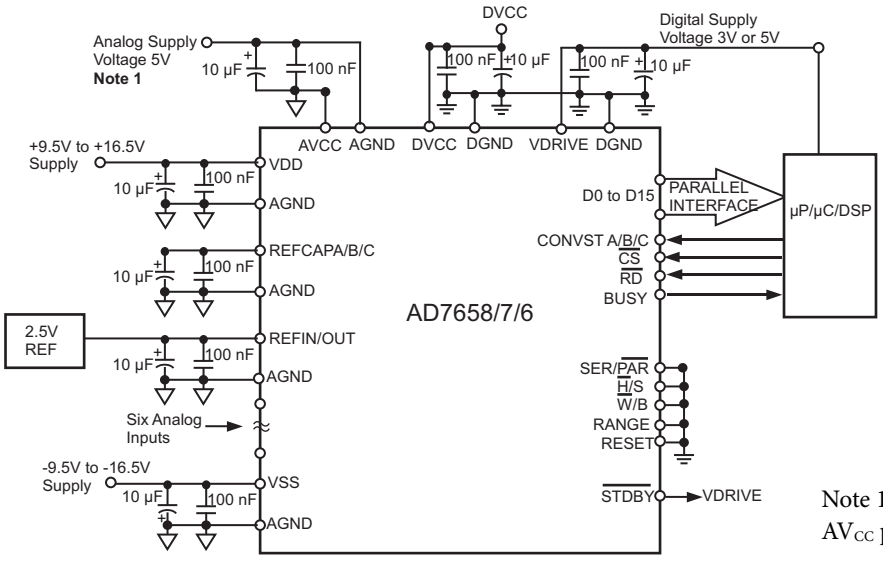
Reference Section

The VREF pin either provides access to the AD7658/AD7657/AD7656's own 2.5V reference or allows for an external reference to be connected providing the reference source for the AD7658/AD7657/AD7656 conversions. The AD7658/AD7657/AD7656 can accommodate a 2.5V to 3V external reference range. When using an external reference the internal reference needs to be disabled. After a RESET the AD7658/AD7657/AD7656 defaults to operating in external Reference mode. The internal reference can be enabled in either hardware or software mode. To enable the internal reference in hardware mode, $\overline{H}$/S SEL pin =0 and the REF EN/$\overline{DISABLE}$ = 1. To enable the internal reference in software mode $\overline{H}$/S SEL pin =1, a write to the control register is necessary to make DB1 of the register = 1. The REFIN/OUT pin should be decoupled using 10 µF and 100 nF capacitors.

The AD7656 contains three on-chip reference buffers. Each of the three ADC pairs has an associated reference buffer. These reference buffers require external decoupling caps on $REF_{CAP}A$, $REF_{CAP}B$, and $REF_{CAP}C$ pins. 10 µF and 100 nF decoupling capacitor should be placed on these REF_{CAP} pins.

Table 7. LSB sizes for each Analog Input Range

	AD7656		AD7657		AD7658	
Input Range	**±10V**	**±5V**	**±10V**	**±5V**	**±10V**	**±5V**
FS Range	20V/65536	10V/65536	20V/16384	10V/16384	20V/4096	10V/4096
LSB Size	0.305 mV	0.152 mV	1.22 mV	0.61 mV	4.88 mV	2.44 mV



Note 1: Decoupling shown on the AV_{CC} pin applies to each AV_{CC} pin.

Figure 5. AD7658/AD7657/AD7656 Typical connection diagram.

INTERFACE SECTION

The AD7658/AD7657/AD7656 provides two interface options, a parallel interface and a high speed serial interface. The required interface mode is selected via the SER/$\overline{PAR}$ pin. The parallel interface can operate in word (W/$\overline{B}$ = 1) or byte (W/$\overline{B}$ = 0) mode. The interface modes are discussed in the following sections.

Parallel Interface (SER/$\overline{PAR}$ = 0)

The AD7658/AD7657/AD7656 consist of six 12/14/16-bit ADCs. A simultaneous sample of all six ADCs can be performed by connecting all three CONVST pins together, CONVSTA, CONVSTB, CONVSTC. The rising edge of CONVSTX initiates simultaneous conversions on the selected ADCs. The AD7658/AD7657/AD7656 contains an on-chip oscillator that is used to perform the conversions. The conversion time, t_{CONV}, is 3 µs. The BUSY signal goes low to indicate the End of Conversion. The falling edge of the BUSY signal is used to place the track-and-hold into track mode. The AD7658/AD7657/AD7656 also allow the six ADCs to be simultaneously converted in pairs by pulsing the three CONVST pins independently. CONVSTA is used to initiate simultaneous conversions on V1 and V2, CONVSTB is used to initiate simultaneous conversions on V3 and V4, and CONVSTC is used to initiate simultaneous conversions on V5 and V6. The conversion results from the simultaneously sampled ADCs are stored in the output data registers.

Data can be read from the AD7658/AD7657/AD7656 via the parallel data bus with standard $\overline{CS}$ and $\overline{RD}$ signals ($\overline{W}$/B = 0). To read the data over the parallel bus SER/$\overline{PAR}$ should be tied low. The $\overline{CS}$ and $\overline{RD}$ input signals are internally gated to enable the conversion result onto the data bus. The data lines DB0 to DB15 leave their high impedance state when both $\overline{CS}$ and $\overline{RD}$ are logic low. The $\overline{CS}$ signal can be permanently tied low and the $\overline{RD}$ signal can be used to access the conversion results. A read operation can take place after the BUSY signal goes low.

The number of read operations required will depend on the number of ADCs that were simultaneously sampled, see Figure 5. If CONVSTA and CONVSTB were brought low simultaneously, four read operations are required to obtain the conversion results from V1, V2, V3 and V4. The conversion results will be output in ascending order. For the AD7657 DB15 and DB14 will contain two leading zeros and DB[13:0] will output the 14-bit conversion result. For the AD7658 DB[15:12] will contain four leading zeros and DB[11:0] will output the 12-bit conversion result.

If there is only an 8-bit bus available the AD7658/AD7657/AD7656 interface can be configured to operate in BYTE mode ($\overline{W}$/B= 1). In this configuration the DB7/HBEN/DCEN pin takes on its HBEN function. The conversion results from the AD7658/AD7657/AD7656 can be accessed in two read operations with 8-bits of data provided on DB15 to DB8 for each of the read operations, See Figure 6. The HBEN pin determines whether the read operation accesses the high byte or the low byte of the 12/14/16-bit conversion result first. To always access the low byte first on DB15 to DB8, the HBEN pin should be tied low. To always access the high byte first on DB15 to DB8 then the HBEN pin should be tied high. In BYTE mode when all three CONVST pins are pulsed together to initiate simultaneous conversions on all six ADCs, twelve read operations are necessary to read back the six 12/14/16-bit conversion results when operating in BYTE mode. DB[6:0] should be left unconnected in byte mode.

The AD7658/AD7657/AD7656 allow the option of reading during a conversion. If for example, a simultaneous conversion had occurred on V1 and V2 by pulsing the CONVSTA pin. The processor will next read the conversion results from the AD7658/AD7657/AD7656. During the read operation after the BUSY signal has gone low further simultaneous conversions can be initiated by pulsing the CONVST pins. However to achieve the specified performance from the AD7658/AD7657/AD7656 reading after the conversion is recommended.

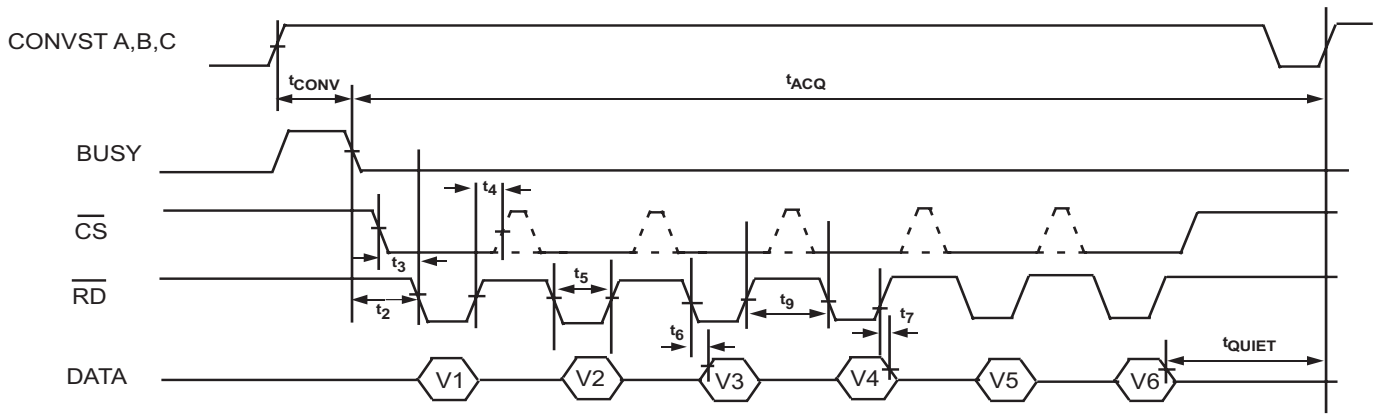


Figure 6. AD7658/AD7657/AD7656 Parallel Interface Timing Diagram ($\overline{W}$/B= 0)

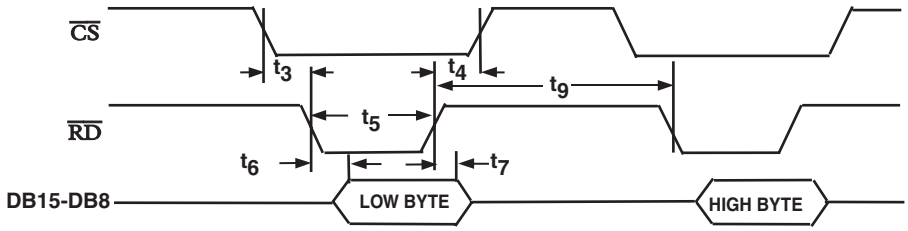


Figure 7. Parallel Interface – Read cycle for Byte mode of operation. ($\overline{W}$/B= 1, HBEN = 0)

Software Selection of ADCs

The $\overline{H}$/S SEL pin determines the source of the combination of ADCs that are to be simultaneously sampled. When the $\overline{H}$/S SEL pin is a logic low the combination of channels to be simultaneously sampled is determined by the CONVSTA, CONVSTB, and CONVSTC pins. When the $\overline{H}$/S SEL pin is a logic high the combination of channels selected for simultaneous sampling is determined by the contents of the Control register DB15 to DB8. In this mode a write to the Control register is necessary.

The Control register is an 8-bit write only register. Data is written to this register using the $\overline{CS}$ and $\overline{WR}$ pins and DB[15:8] data pins, see Figure 8. The Control register is shown in Table 8. To select an ADC pair to be simultaneously sampled, set the corresponding data line high during the write operation.

The AD7658/AD7657/AD7656 control register allows individual ranges to be programmed on each ADC pair. DB12 to DB10 in the Control register are used to program the range on each ADC pair. The AD7658/AD7657/AD7656 allows the user to select either ± 4 x VREF or ± 2 x VREF as the analog input range. RNGA is used to select the range for the next conversion on V1 and V2, RNGB is used to select the Range for the next conversion on V3 and V4 and RNGC is used to select the range for V5 and V6. When the RNGX is 1 the range on the corresponding Analog input pair is ± 2 x VREF. When the RNGX bit is 0 the range on the corresponding Analog Input pair is ± 4 x VREF.

The REFEN pin is used to disable the internal reference, allowing the user to supply an external reference to the AD7658/AD7657/AD7656. When a 0 is written to this bit the on-chip reference is disabled. When a 1 is written to this bit the on-chip reference is enabled.

The REF BUF bit is used to disable the internal reference buffers. When this bit is 1 the internal reference buffers are disabled.

After a RESET occurs on the AD7658/AD7657/AD7656 the Control register will contain all zeros.

Table 8.Control Register

D15	D14	D13	D12	D11	D10	D9	D8
VC	VB	VA	RNGC	RNGB	RNGA	REFEN	REFBUF

The CONVSTA signal is used to initiate a simultaneous conversion on the combination of channels selected via the Control register. The CONVSTB and CONVSTC signals can be tied low when operating in software mode, $\overline{H}$/S SEL = 1. The number of read pulses required will depend on the number of ADCs selected in the Control register and also whether operating in word or BYTE mode. The conversion results will be output in ascending order.

During the write operation the Data Bus bits DB15 to DB8 are bidirectional and become inputs to the Control register when $\overline{RD}$ is a logic high, $\overline{CS}$ and $\overline{WR}$ are logic low. The logic state on DB15 through DB8 is latched into the Control register when $\overline{WR}$ goes logic high.

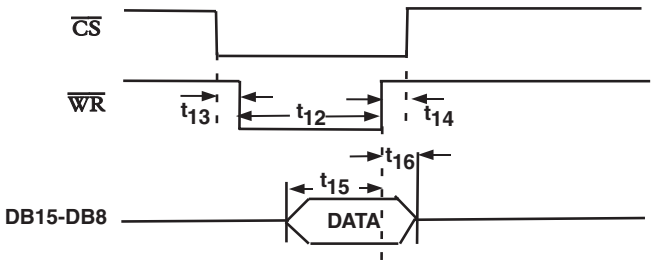


Figure 8. Parallel Interface – Write cycle for Word Mode . ($\overline{W}$/B= 0)

Changing the Analog Input Range($\overline{H}$/S SEL=0)

The AD7658/AD7657/AD7656 RANGE pin allows the user to select either ± 2 x VREF or ± 4 x VREF as the analog input range for the six Analog Inputs. When the $\overline{H}$/S SEL pin is low the logic state of the RANGE pin is sampled on the falling edge of the BUSY signal to determine the range for the next simultaneous conversion. When the RANGE pin is a logic high at the falling edge of the BUSY signal the range for the next

conversion is ± 2 x VREF. When the RANGE pin is a logic low at the falling edge of the BUSY signal the range for the next conversion is ± 4 x VREF.

Changing the Analog Input Range($\overline{H}$/S SEL=1)

When the $\overline{H}$/S SEL pin is high the range can be changed by writing to the Control Register. DB12:10 in the Control Register are used to select the Analog input Ranges for the next conversion. Each Analog input pair has an associated range bit, allowing independent ranges to be programmed on each ADC pair. When the RNGX bit is 1 the Range for the next conversion is ±2 x VREF. When the RNGX bit is 0 the range for the next conversion is ±4 x VREF.

SERIAL INTERFACE (SER/$\overline{PAR}$ = 1)

By pulsing one, two or all three CONVSTX signals the AD7658/AD7657/AD7656 will simultaneously convert the selected channel pairs on the rising edge of CONVSTX. The simultaneous conversions on the selected ADCs are performed using the on-chip trimmed oscillator. After the rising edge of CONVSTX the BUSY signal goes high to indicate the conversion has started. It returns low when the conversion is complete 3 µs later. The output register will be loaded with the new conversion results and data can be read from the AD7658/AD7657/AD7656. To read the data back from the AD7658/AD7657/AD7656 over the serial interface SER/$\overline{PAR}$ should be tied high. The $\overline{CS}$ and SCLK signal are used to transfer data from the AD7658/AD7657/AD7656. The AD7658/AD7657/AD7656 has three DOUT pins, DOUTA, DOUTB, DOUTC. Data can be read back from the AD7658/AD7657/AD7656 using one, two or all three DOUT lines. Figure 9 shows six simultaneous conversions and the read sequence using three DOUT lines. In figure 8, 32 SCLK transfers are used to access data from the AD7658/AD7657/AD7656, two 16 SCLK transfers individually framed with the $\overline{CS}$ signal can also be used to access the data on the three DOUT lines. When operating the AD7658/AD7657/AD7656 in serial mode with conversion data being clocked out on all three DOUT line DB0-DB2 should be tied to V_{DRIVE}. These pins are used to enable the DOUTA – DOUTC lines respectively.

If it is required to clock conversion data out on two data out lines then DOUTA and DOUTB should be used. Again to enable DOUTA and DOUTB, DB0 and DB1 should be tied to V_{DRIVE} and DB2 should be tied low. When six simultaneous conversions are performed and only two DOUT lines are used, a 48 SCLK transfer can be used to access the data from the AD7658/AD7657/AD7656. The read sequence is shown in Figure 10 for a simultaneous conversion on all six ADCs using two DOUT lines. If a simultaneous conversion occurred on all six ADCs and only two DOUT lines are used to read the results from the AD7658/AD7657/AD7656, DOUTA will clock out the result from V1, V2 and V5, while DOUTB will clock out the results from V3,V4 and V6.

Data can also be clocked out using just one DOUT line, in this case DOUTA should be used to access the conversion data. To configure the AD7658/AD7657/AD7656 to operate in this mode then DB0 should be tied to V_{DRIVE}, DB1 and DB2 should be tied low. The penalty for using just one DOUT line is the throughput rate will be reduced. Data can be accessed from the AD7658/AD7657/AD7656 using one 96 SCLK transfer, three 32 SCLK individually framed transfers or six 16 SCLK individually framed transfers. In Serial mode the $\overline{RD}$ signal should be tied low.

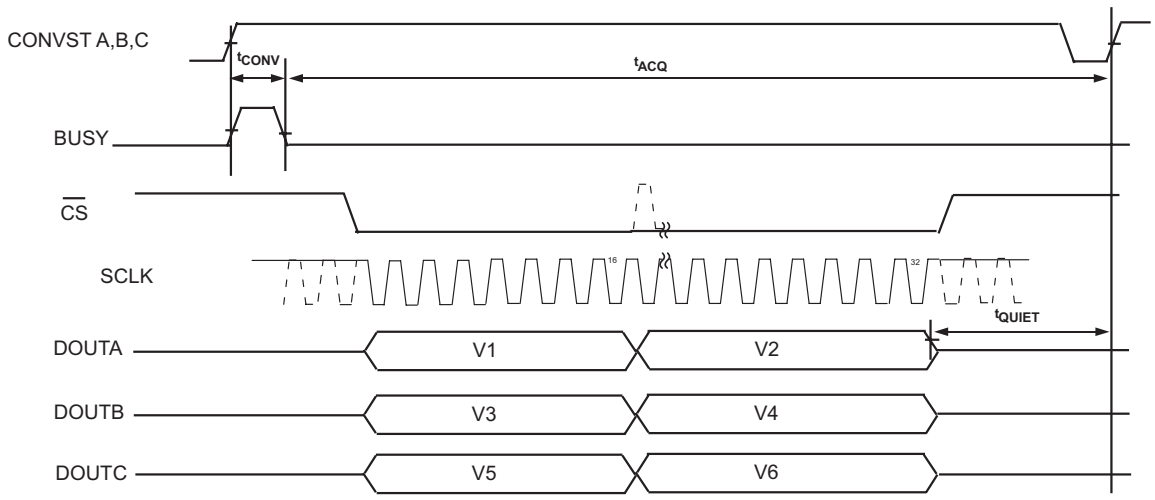


Figure 9. Serial Interface with three DOUT lines.

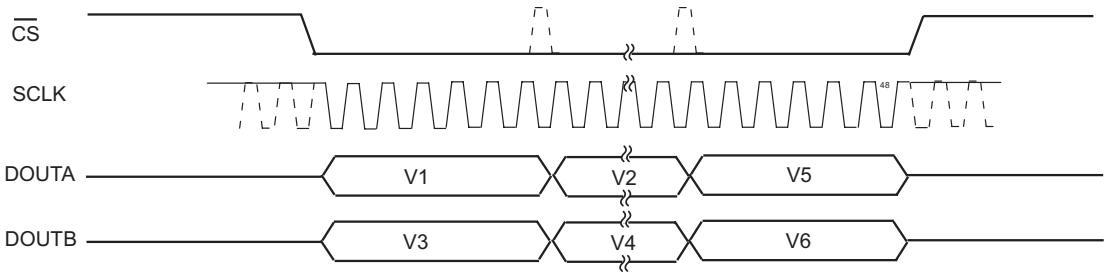


Figure 10. Serial Interface with two DOUT lines.

Serial Read Operation

Figure 11 shows the timing diagram for reading data from the AD7658/AD7657/AD7656 in serial mode. The SCLK input signal provides the clock source for the serial interface. The $\overline{CS}$ signal goes low to access data from the AD7658/AD7657/AD7656. The falling edge of $\overline{CS}$ takes the bus out of three-state and clocks out the MSB of the 12/14/16-bit conversion result. The ADCs output 16- bits for each conversion result. The data stream of the AD7658 consists of four leading zeros followed by 12 bits of conversion data provided MSB first; the data stream of the AD7657 consists of two leading zeros, followed by the 14-bits of conversion data provided MSB first; the data stream of the AD7656 consists of sixteen bits of conversion data provided MSB first. The first bit of the conversion result is valid on the first SCLK falling edge after the $\overline{CS}$ falling edge. The subsequent 15 data bits of the data are clocked out on rising edge of the SCLK signal. Data is valid on the SCLK falling edge. Sixteen clock pulses must be provided to the AD7658/AD7657/AD7656 to access each conversion result. Figure 11 shows how a 16 SCLK read is used to access the conversion results.

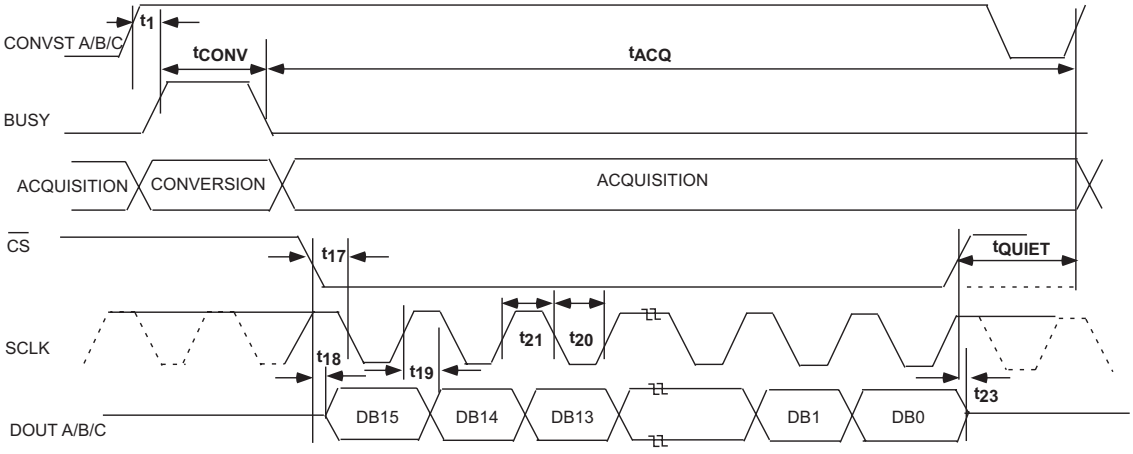


Figure 11. Serial Read Operation

Daisy-Chain Mode(DCEN = 1, SER/$\overline{PAR}$ = 1)

When reading conversion data back from the AD7658/AD7657/AD7656 using the three/two DOUT pins it is possible to Configure the AD7658/AD7657/AD7656 to operate in Daisy-Chain Mode, using the DCEN pin. This Daisy-Chain feature allows multiple AD7658/AD7657/AD7656 devices to be cascaded together. This feature is useful for reducing component count and wiring connections. An example connection of two devices is shown in Figure 12, this configuration shows two DOUT lines being used. Simultaneous sampling of the 12 Analog Inputs is possible by using a common CONVST signal. The DB5, DB4 and DB3 data pins are used as Data input pins, DCIN[A:C], for the Daisy-Chain Mode.

The rising edge of CONVST is used to initiate a conversion on the AD7658/AD7657/AD7656. After the BUSY signal has gone low to indicate the conversion is complete the user can begin to read the data from the two devices. Figure 13 shows the serial timing diagram when operating two AD7658/AD7657/AD7656

devices in Daisy Chain Mode.

The $\overline{CS}$ falling edge is used to frame the serial transfer from the AD7658/AD7657/AD7656 devices, take the bus out of three-state and clock out the MSB of the first conversion result. In the example shown all twelve ADC channels were simultaneously sampled. Two DOUT line are used to read the conversion results in this example. $\overline{CS}$ frames a 96 SCLK transfer. During the first 48 SCLK the conversion data is transferred from Device #2 to Device #1. DOUT A on device #2 transfers conversion data from V1, V2 and V5 into DCINA in device #1. DOUT B on device #2 transfers conversion results from V3, V4 and V6 to DCIN B in device #1. During the first 48 SCLK device #1 transfers data into the digital host, DOUTA on device #1 transfers conversion data from V1, V2 and V5. DOUTB on device #1 transfers conversion data from V3, V4 and V6.

During the last 48 SCLKs device #2 will clock out zeros, device #1 will shift the data it clocked in from device #2 during the first 48 SCLKs into the digital host. This example could also have been implemented using 3 x 32 SCLK individually framed SCLK transfers or 6 x 16 SCLK individually framed SCLK transfers provided DCEN remained high during the transfers. Figure 14 shows the timing if two AD7656 were configured in Daisy chain mode but operating with three DOUT lines. Again assuming a simultaneous sampling of all 12 inputs occurred. During the read operation the $\overline{CS}$ frames a 64 SCLK transfer. During the first 32 SCLKs of this transfer the conversion results from Device #1 are clocked into the digital host and the conversion results from device #2 are clocked into device #1. During the last 32 SCLKs of the transfer the conversion results from device #2 are clocked out of device #1 and into the digital host. Device #2 will clock out zeros.

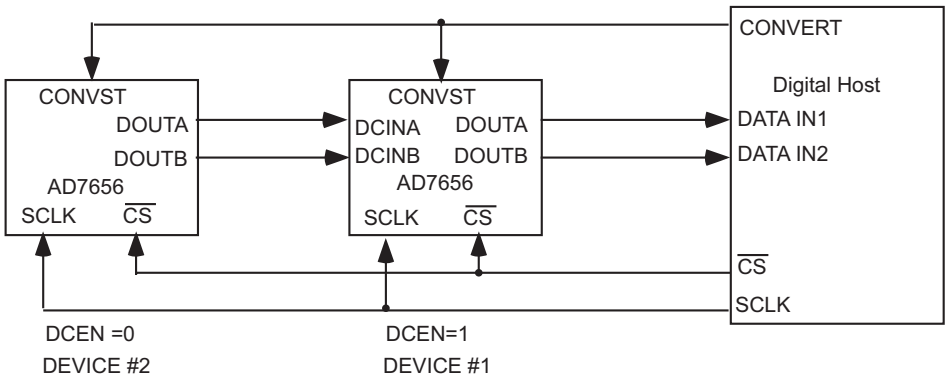


Figure 12. Daisy-Chain Configuration

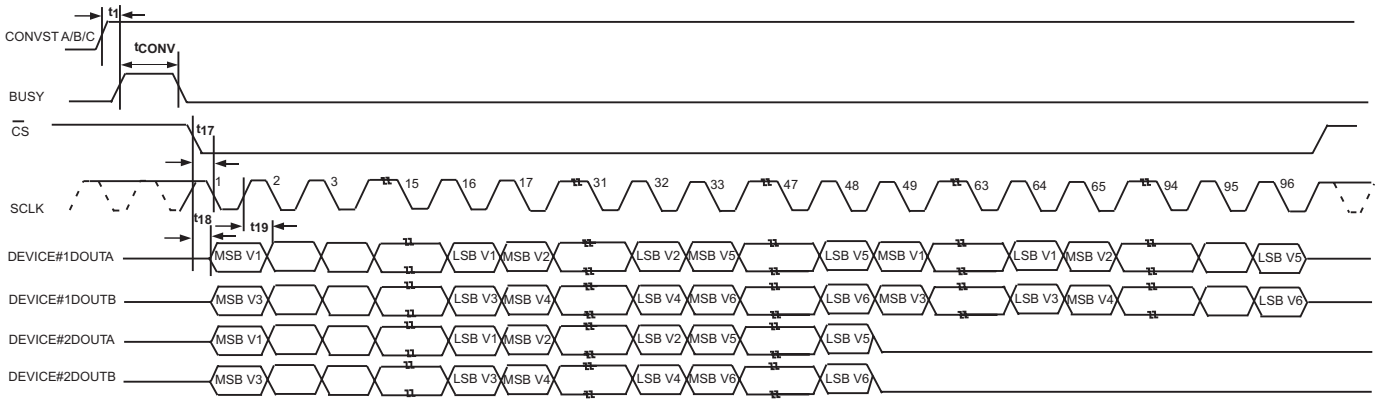


Figure 13. Daisy-Chain Serial Interface Timing with 2 DOUT lines

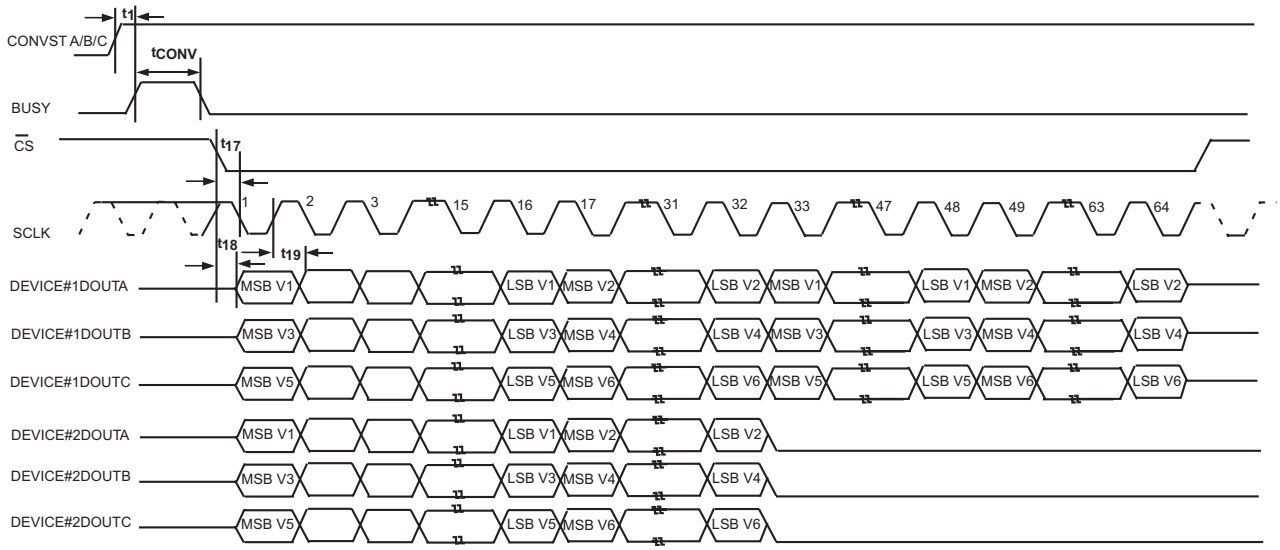


Figure 14. Daisy-Chain Serial Interface Timing with 3 DOUT lines

Standby/Partial Power Down Modes of Operation

Each ADC pair can be individually placed into partial power down by bringing the CONVSTX signal low before the falling edge of BUSY. To power the ADC pair back up again then the CONVSTX signal should be brought high to tell the ADC pair to power up and place the track-and-hold into track mode. In partial power down mode the reference buffers will remain powered up. While an ADC pair is in partial power down, conversions can still occur on the other ADCs.

The AD7658/AD7657/AD7656 has a standby mode whereby the device can be placed into a low current consumption mode (0.5 μA max). The AD7658/AD7657/AD7656 is placed into standby mode by bringing the logic input $\overline{\text{STBY}}$ low. The AD7658/AD7657/AD7656 can be powered up again for normal operation by bringing $\overline{\text{STBY}}$ logic high. The output data buffers are still operational when the AD7658/AD7657/AD7656 is in standby. This means the user can still continue to access the conversion results when the AD7658/AD7657/AD7656 is in standby. This standby feature can be used to reduce the average power consumed by the AD7658/AD7657/AD7656 when operating at lower throughput rates. The AD7658/AD7657/AD7656 could be placed into standby at the end of each conversion when BUSY goes low and taken out of standby again prior to the next conversion. The time it takes for the AD7658/AD7657/AD7656 to come out of standby is called the "wake-up" time. This wake-up time will limit the maximum throughput rate at which the AD7658/AD7657/AD7656 can operate when powering down between conversions.

APPLICATION HINTS

Layout

The printed circuit board that houses the AD7656 should be designed so the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. Digital and analog ground planes should be joined in only one place, preferably underneath the AD7656, or, at least, as close as possible to the AD7656. If the AD7656 is in a system where multiple devices require analog to digital ground connections, the connection should still be made at one point only, a star ground point, which should be established as close as possible to the AD7656.

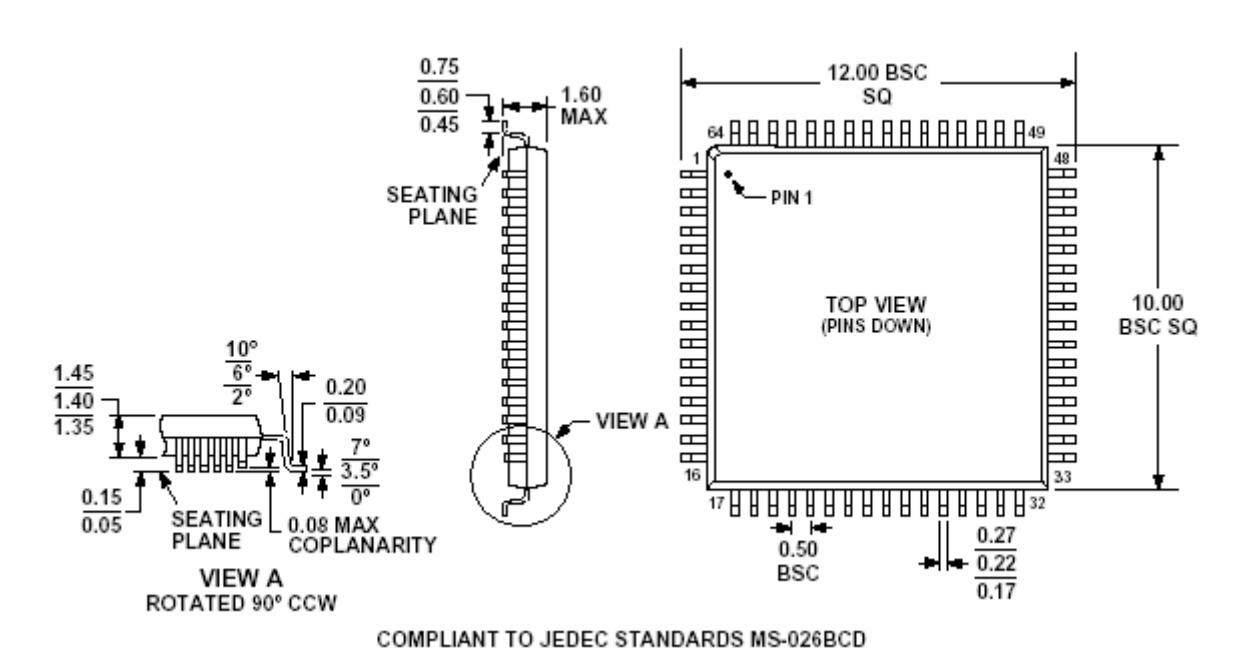
It is recommended to avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7656 to avoid noise coupling. Fast switching signals like CONVST or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board and should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on different but close layers of the board should run at right angles to each other. This will reduce the effect of feedthrough through the board.

The power supply lines to the AD7656 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good decoupling is also important to lower the supplies impedance presented to the AD7656 and to reduce the magnitude of the supply spikes. Decoupling ceramic capacitors, typically 100 nF, should be placed on all of the power supply pins, power supplies pins V_{DD}, V_{SS}, AV_{CC}, DV_{CC}, and V_{DRIVE}. The decoupling capacitors should be placed close to, and ideally right up against, these pins and their corresponding ground pins. Additionally, low ESR 10 µF capacitors should be located in the vicinity of the ADC to further reduce low frequency ripple.

The decoupling capacitors should be close to the ADC and connected with short and large traces to minimize parasitic inductances.

OUTLINE DIMENSIONS

64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64)
Dimensions shown in millimeters



ORDERING GUIDE

AD7658/AD7657/AD7656 Products	Temperature Package	Package Description	Package Outline
AD7658BSTZ[1]	–40°C to +85°C	LQFP	ST-64
AD7658BSTZ-REEL[1]	–40°C to +85°C	LQFP	ST-64
AD7657BSTZ[1]	–40°C to +85°C	LQFP	ST-64
AD7657BSTZ-REEL[1]	–40°C to +85°C	LQFP	ST-64
AD7656BSTZ[1]	–40°C to +85°C	LQFP	ST-64
AD7656BSTZ-REEL[1]	–40°C to +85°C	LQFP	ST-64
EVAL- AD7656CB[2]		Evaluation Board	
EVAL-CONTROL BRD2[3]		Controller Board	

NOTES
1 Z = Pb-free part.
2 This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL Board for evaluation/demonstration purposes.
3 This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators. To order a complete evaluation kit, the particular ADC evaluation board, e.g., EVAL-AD7658/AD7657/AD7656CB, the EVAL-CONTROL BRD2, and a 12V transformer must be ordered. See relevant Evaluation Board Technical note for more information.