Synchronous Buck PWM DC-DC Controller

Description

The FP6321 is designed to drive two N-channel MOSFETs in a synchronous rectified buck topology. It provides the output adjustment, internal soft-start, frequency compensation networks, monitoring and protection functions into a single package.

The IC operating at fixed 300kHz frequency provides simple, single feedback loop, voltage mode control with fast transient response. The resulting PWM duty ratio ranges from 0-100%.

The FP6321 features over current protection. The output current is monitored by sensing the voltage drop across the R_{DS-ON} of the low side MOSFET which eliminates the need for a current sensing resistor.

This device is available in SOP-8 package.

Features

- Operates from +5V or +12V
- Drives Two Low Cost N-Channel MOSFETs
- Fast Transient Response
- Simple Single-Loop Control Design (Voltage-Mode PWM Control)
- Internal Soft-Start
- Over-Current Fault Monitor
- SOP-8 Package
- RoHS Compliant

Applications

- Motherboard
- Graphic Card
- Telecomm Equipments
- High Power DC-DC Regulators
- Servers

Pin Assignment

SO Package (SOP-8)

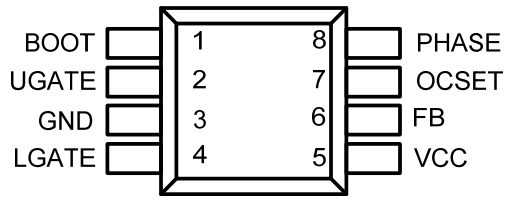
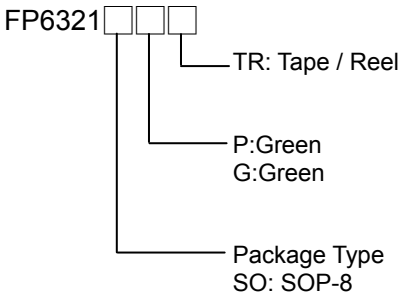


Figure 1. Pin Assignment of FP6321

Ordering Information



Typical Application Circuit

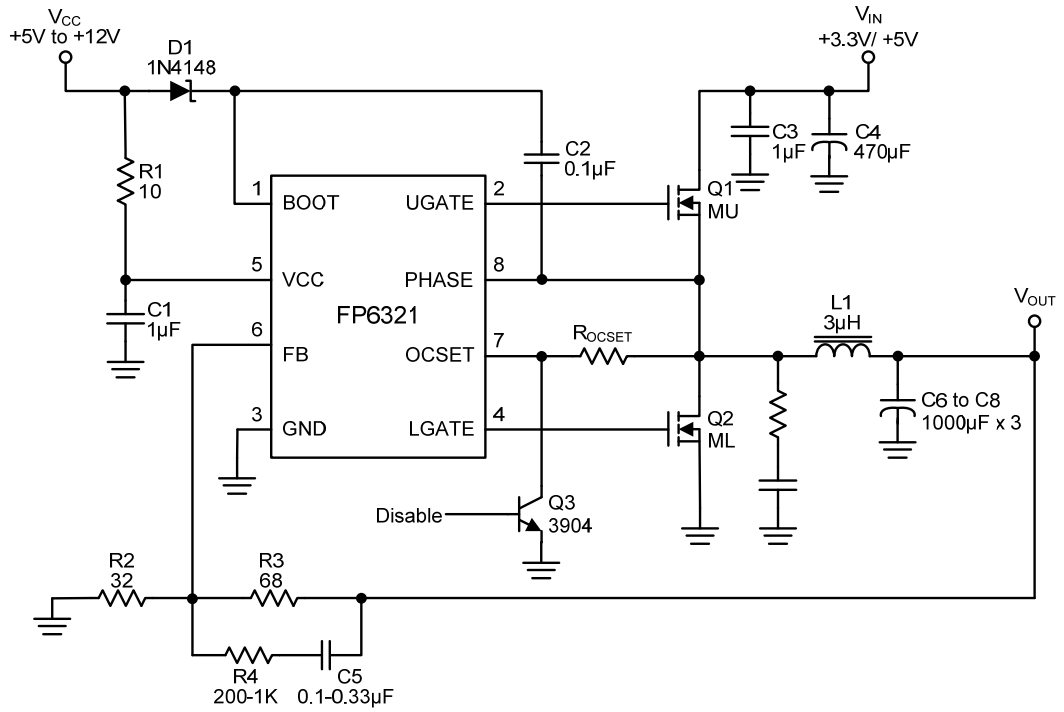


Figure 2. Typical Application Circuit of FP6321

Note: It is not recommended to apply FP6321 on V_{CC}=12V/ V_{IN} =12V condition

Functional Pin Description

Pin Name	Pin Function
BOOT	This pin provides bias voltage to the high side MOSFET Driver. A bootstrap circuit may be to create a BOOT voltage suitable to drive a standard N-Channel MOSFET.
UGATE	Connect UGATE to the high side MOSFET gate. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the high side MOSFET has turned off.
GND	Ground.
LGATE	Connect LGATE to the low side MOSFET gate. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the high side MOSFET has turned off.
VCC	Power Pin.
FB	Feedback Pin. The typical reference voltage is 0.8V.
OCSET	Shutdown Control and connect a resistance (R_{OCSET}) for over current setting.
PHASE	Connect the PHASE pin to the high side MOSFET source, and sensing converter's input power.

Block Diagram

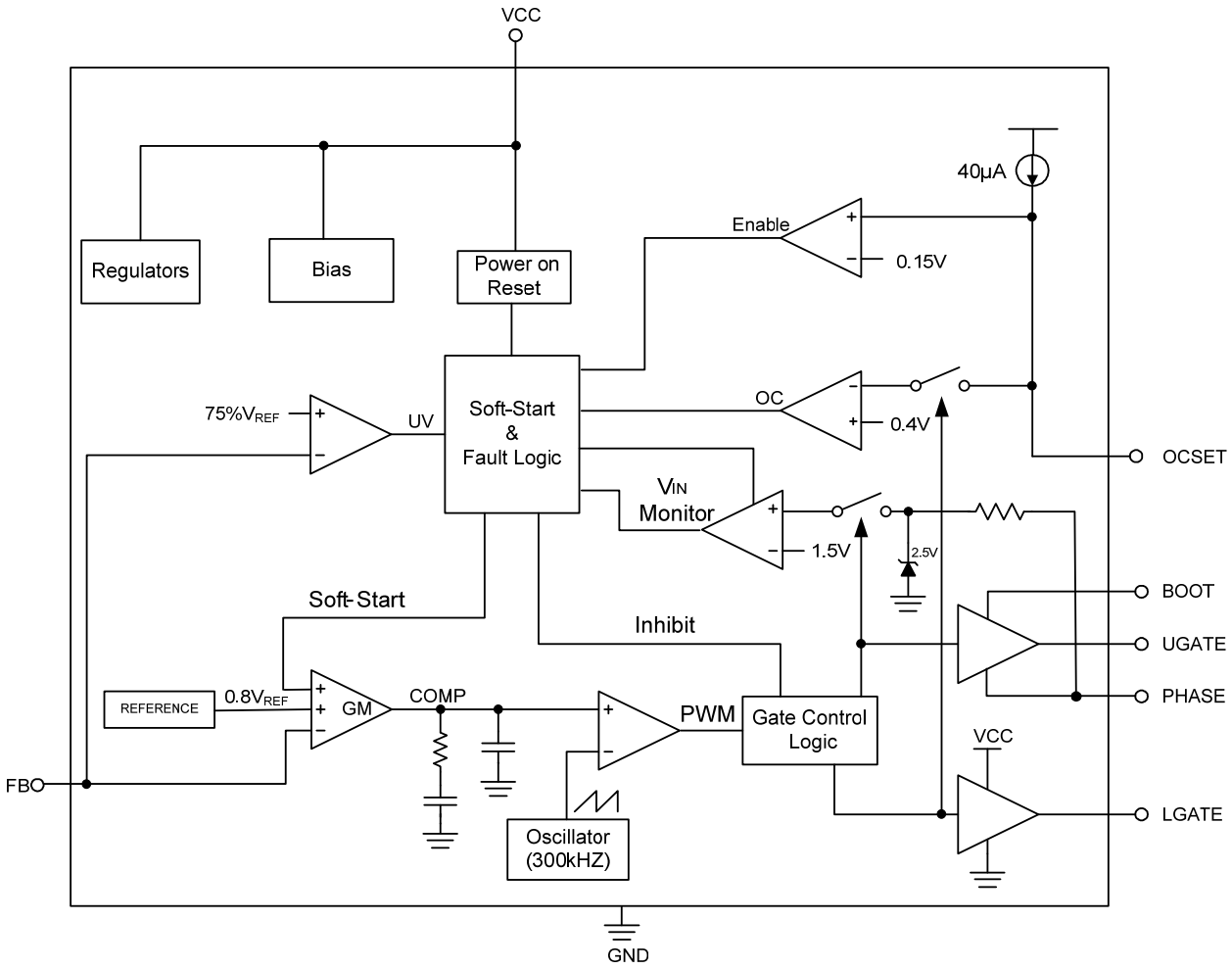


Figure 3. Block Diagram of FP6321

Absolute Maximum Ratings

- VCC to GND ---------- - 0.3V to +16V
- BOOT, V_{BOOT}-V_{PHASE} ---------- - 0.3V to +16V
- PHASE ---------- - 5V to +16V
- UGATE ---------- V_{PHASE} - 0.3V to V_{BOOT} +0.3V
- LGATE ---------- - 0.3V to V_{CC}+0.3V
- FB,OCSET to GND ---------- - 0.3V to +6V
- Power Dissipation @ T_A=25℃, SOP-8 (P_D)---------- 630mW
- Package Thermal Resistance, SOP-8 (θ_{JA})---------- 160°C/W
- Junction Temperature ---------- +150°C
- Operation Temperature Range ---------- - 40°C to +85°C
- Storage Temperature Range---------- - 65°C to +150°C
- Lead Temperature (Soldering, 10sec.) ---------- +260°C
- ESD Susceptibility

  HBM(Human Body Mode)---------- 2KV

  MM(Machine Mode)---------- 200V

Note1：Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage, V_{CC} ---------- 5V ± 5%, 12V ± 10%
- Operating Temperature Range ---------- -40°C to +85°C

Electrical Characteristics

(V_{CC}=5V/12V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT						
VCC Under Voltage Lockout	V_{RISING}	VCC rising	3.7	4.1	4.5	V
	$V_{FALLING}$	VCC falling		0.25		V
Quiescent Current	I_{CC}	U_{GATE} and L_{GATE} open		2	6	mA
ERROR AMPLIFIER						
Feedback Voltage	V_{FB}		0.784	0.8	0.816	V
FB Input Bias Current	I_{FB}	V_{FB}=1V		0.1		uA
Open Loop DC gain (Note2)	A_O			85		dB
OSCILLATOR						
Frequency	F_{OSC}	V_{CC}=12V	250	300	350	kHz
Ramp Amplitude (Note2)	$\triangle V_{OSC}$	V_{CC}=12V		1.5		Vp-p
GATE DRIVERS						
Upper Gate Source	I_{UGATE}	V_{BOOT}-V_{PHASE}=12V, V_{UGATE}-V_{PHASE}=6V	300	500		mA
Upper Gate Sink	R_{UGATE}	V_{BOOT}-V_{PHASE}=12V, V_{UGATE}-V_{PHASE}=1V		4	8	Ω
Lower Gate Source	I_{LGATE}	V_{CC}=12V, V_{LGATE} =6V	300	500		mA
Lower Gate Sink	R_{LGATE}	V_{CC}=12V, V_{LGATE} =1V		3	5	Ω
Dead Time (Note2)	T_{DT}				100	ns
PROTECTION						
FB Under-Voltage Trip		FB Falling	70	75	80	%
OC Current Source	I_{OCSET}	V_{PHASE}=0V	35	40	45	uA
Soft-Start Interval (Note2)	Tss		2	3.5		ms

Note2：Guarantee by design.

Typical Performance Curves

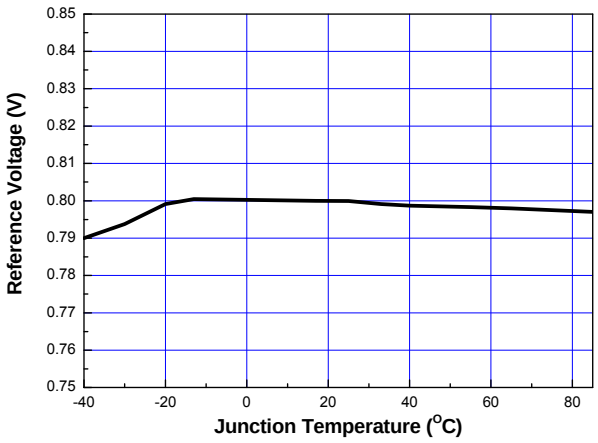


Figure 4. Reference Voltage vs. Junction Temperature

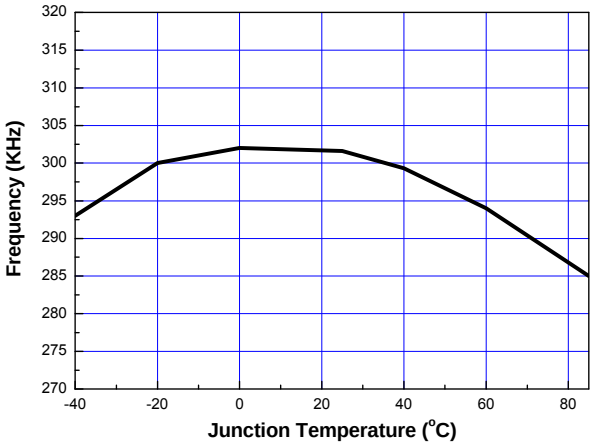


Figure 5. Frequency vs. Junction Temperature

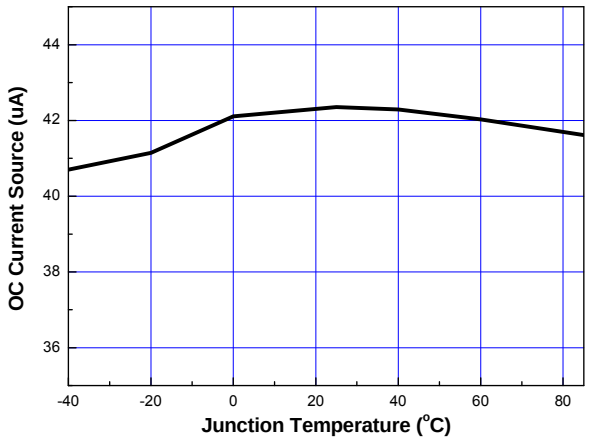


Figure 6. OC Current Source vs. Junction Temperature

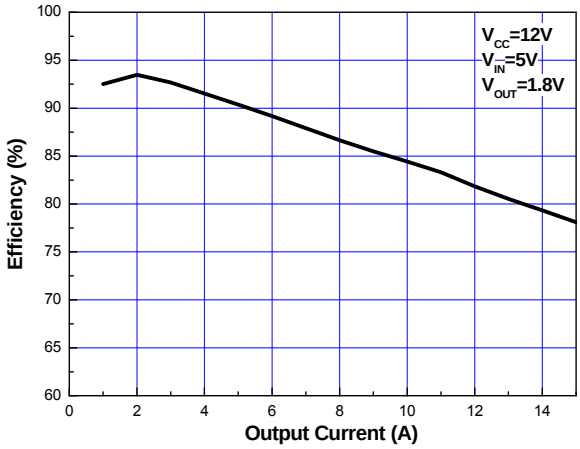


Figure 7. Efficiency

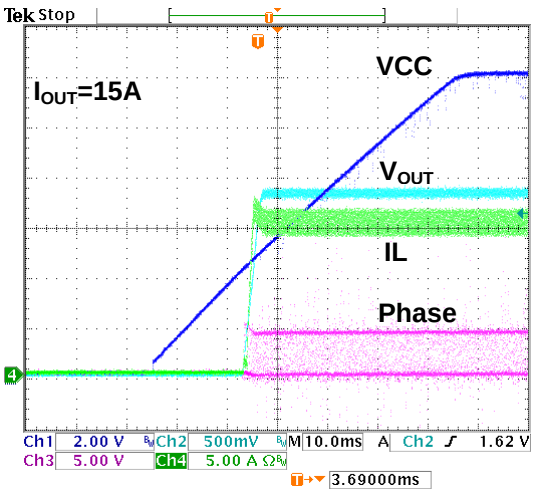


Figure 8. Power On

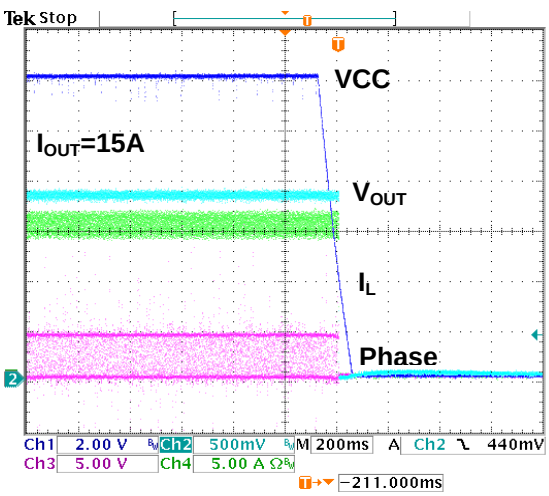


Figure 9. Power OFF

Typical Performance Curves (Continued)

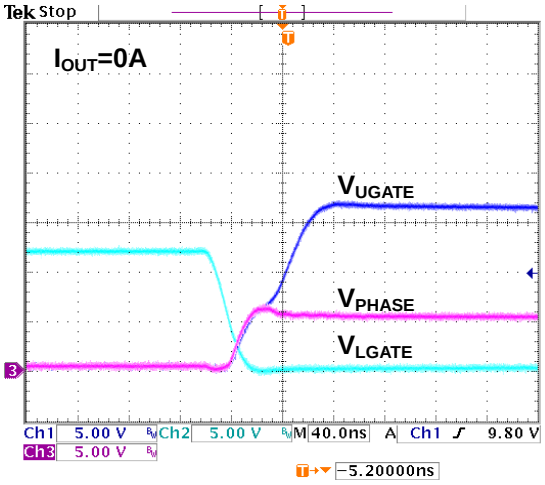


Figure 10. Switching waveform (UGATE rising)

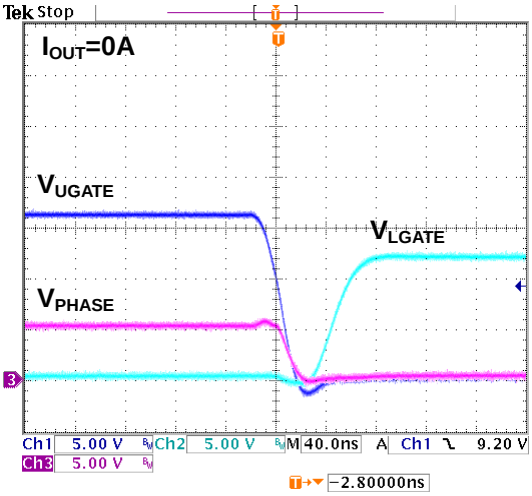


Figure 11. Switching waveform (UGATE falling)

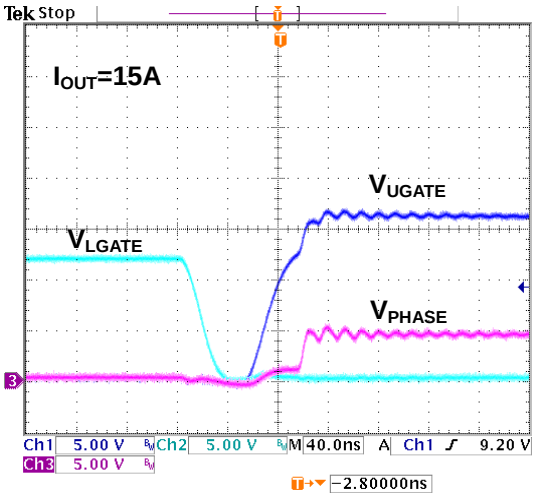


Figure 12. Switching waveform (UGATE rising)

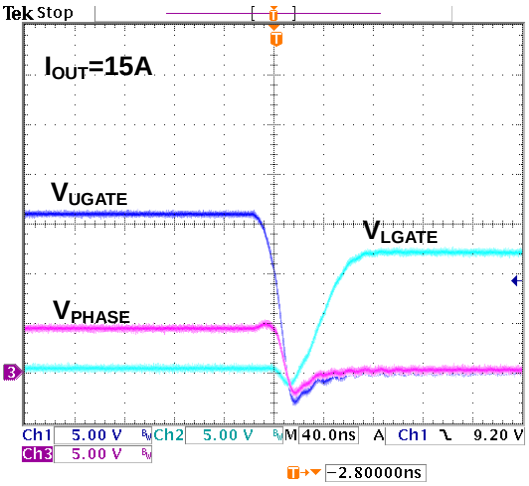


Figure 13. Switching waveform (UGATE falling)

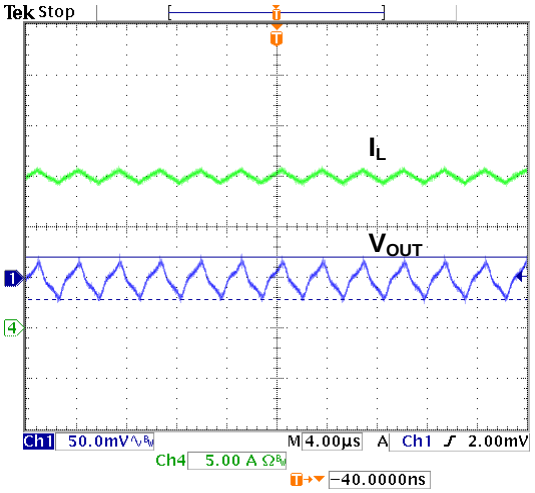


Figure 14. Output Ripple

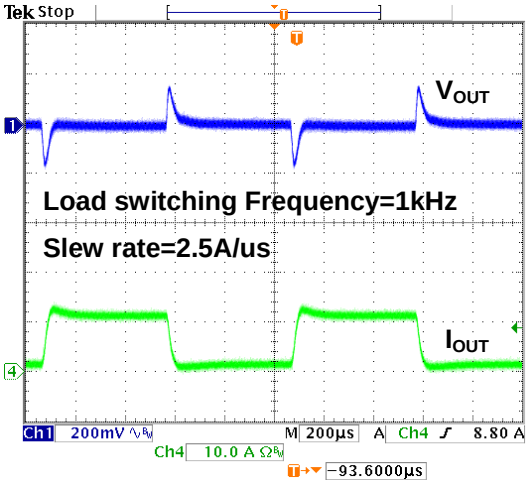


Figure 15. Load Transient Response

Typical Performance Curves (Continued)

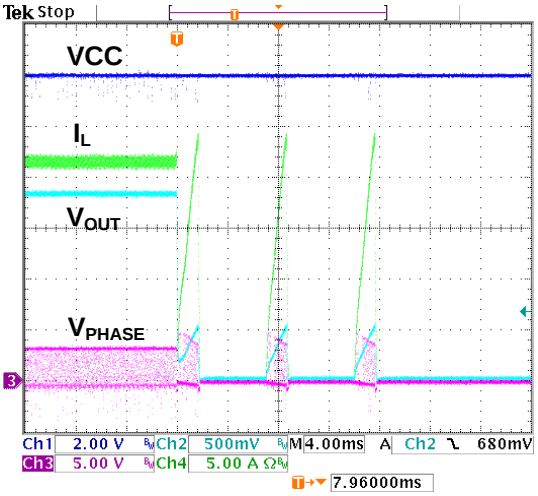


Figure 16. OCP using DC loading

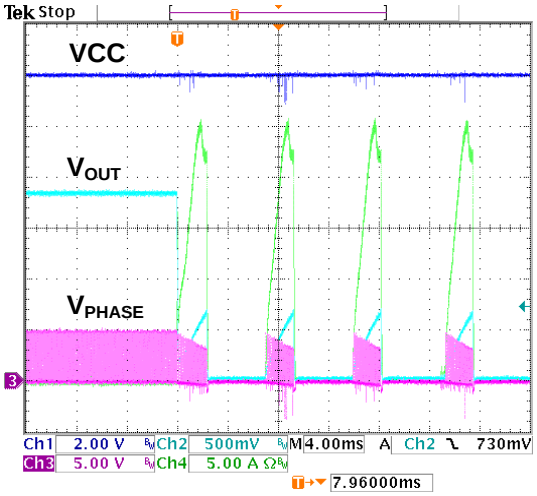


Figure 17. OCP using Dynamic loading

Functional Description

Initialization

The Power-On Reset (POR) function continually monitors the input supply voltage and the enable function. The POR monitors the bias voltage at the VCC pin and the input voltage (VIN) on the phase pin. After VCC power is ready, turning on the high side MOS by pulse cycle. After high side MOS turns on, the phase pin voltage is very close to VIN. The VIN power is ready by sensing the phase pin voltage reaches 1.5V four times.

Soft-Start

The FP6321 features soft-start to limit inrush current and control the output voltage rise at start-up. The soft-start is accomplished by ramping the internal reference input from 0V to 0.8V. The soft-start interval is 3.5ms typical.

Over-Current Protection

The over-current function protects the converter a shorted output by using the low side MOSFET on-resistance R_{DS-ON} to monitor the current. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor.

The over-current function cycles the soft-start function in a hiccup mode to provide fault protection. After four times are counted, the high side and low side MOSFET will turn off and the output is latched off.

A resistor (R_{OCSET}), connected from OCSET pin to the source of high side MOSFET and the drain of low side MOSFET to set the over-current triple level. An internal 40uA (typical) current source develops the voltage across the ROCSET. The over-current setting equation is shown as below:

$$I_{OCSET} = \frac{40uA \times R_{OCSET} - 0.4V}{R_{DS-ON}}$$

Shutdown

Connecting a small transistor to OCSET pin and pulling the OCSET voltage less than 0.15V can shutdown the FP6321. At this condition, the FP6321 is shutdown and high side and low side MOSFETS are turned off. The output is floating.

Under-Voltage Protection

The under-voltage function monitors the FB voltage to protection the converter against the output short-circuit condition. The under- voltage threshold is 75% V_{REF}. The UV has 20us triggered delay. The FP6321 will always trigger Vin power sensing after 4 times UV. The under- voltage protection is disable during the soft-start interval.

Application Information

Introduction

The FP6321 integrated circuit is a synchronous PWM controller, it operates over a wide input voltage range. Being low cost, it is a very popular choice of PWM controller. This section will describe the FP6321's application suggestion. The operation and the design of this application will also be discussed in detail.

Design Procedures

This section will describe the steps to design synchronous buck system, and explains how to construct basic power conversion circuits including the design of the control chip functions and the basic loop.

(1) Synchronous buck converter

Since this is a buck output system, the first quantity to be determined is the duty cycle value. The formula calculated the PWM duty ratio, apply to the system which we propose to design:

$$Duty\ ratio\ D = \frac{V_O + V_{DS(sat),\ Lowside\ N}}{V_{IN} - V_{DS(sat),\ Highside\ N} + V_{DS(sat),\ Lowside\ N}} = \frac{T_{ON}}{T_S}$$

(2) Inductor Selection

To find the inductor value it is necessary to consider the inductor ripple current. Choose an inductor which operated in continuous mode down to 10 percent of the rated output load:

$\Delta I_L = 2 \times 10\% \times I_O$

The inductor "L" value for this system is connected to be:

$$L \geq \frac{(V_{IN} - V_{DS(sat)} - V_O) \times D_{MIN}}{\Delta I_L \times f_S}$$

If the core loss is a problem, increasing the inductance of L will be helpful.

(3) Output Capacitor Selection

a. The output capacitor is required to filter the output noise and provide regulator loop stability. When selecting an output capacitor, the important capacitor parameters are; the 100kHz Equivalent Series Resistance (ESR), the RMS ripples current rating, the voltage rating, and capacitance value. For the output capacitor, the ESR value is the most important parameter.

The ESR can be calculated from the following formula.

$$ESR = \frac{V_{RIPPLE}}{\Delta I_L}$$

An aluminum electrolytic capacitor's ESR value is related to the capacitance and its voltage rating. In most case, higher voltage electrolytic capacitors have lower ESR values. Most of the time, capacitors with much higher voltage ratings may be needed to provide the low ESR values required for low output ripple voltage.

b. The capacitor voltage rating should be at least 1.5 times greater than the output voltage, and often much higher voltage ratings are needed to satisfy the low ESR requirements needed for low output ripple voltage.

(3) Output N-channel MOSFETs Selection

a. The current ability of the output N-channel MOSFETs must be at least more than the peak switching current I_{PK}. The voltage rating V_{DS} of the N-channel MOSFETs should be at least 1.25 times the maximum input voltage. Choose the low R_{DS-ON} MOSFETs for reducing the conduction power loss. Choose the low C_{ISS} MOSFETs for reducing the switching loss. But most of time, the two factors are trade-off. Consider the system requirement and define the MOSFETs rating.

b. The MOSFETs must be fast (switch time) and must be located close to the FP6321 using short leads and short printed circuit traces. In case of a large output current, we must layout a copper to reduce the temperature of these two MOSFETs.

(4) Input Capacitor Selection

a. The RMS current rating of the input capacitor can be calculated from the next page formula table.

b. This capacitor should be located close to the IC using short leads and the volt age rating should be approximately 1.5 times the maximum input voltage.

Application Information (Continued)

Calculation Formula	
$V_{OUT}=V_{FB} \times ((R3/R2) + 1)$	
$L \geq \frac{[V_{IN(min)} - V_{DS(SAT)} - V_{OUT}] \times T_{ON(max)}}{\Delta I_L}$ $I_{RIPPPLE} = I_{LOAD(max)} - I_{LOAD(min)}$	
C_{OUT}	$ESR = [\frac{V_{RIPPLE}}{\Delta I_L}]$ $V_{DC-Rating} \geq 1.5 \times V_{OUT}$
C_{IN}	$I_{IN(rms)} = I_{OUT} \times \sqrt{D(1-D)}$ $V_{DC-rating} \geq 1.5 \times V_{IN(max)}$

Calculation	Step-down (buck) regulator
D	$T_{ON} /(T_{ON} + T_{OFF})$
	V_{OUT}/V_{IN}
ΔI_L	2 x 10% x I_O
$I_{IN(rms)}$	$I_{OUT} \times \sqrt{D(1-D)}$

Board Layout

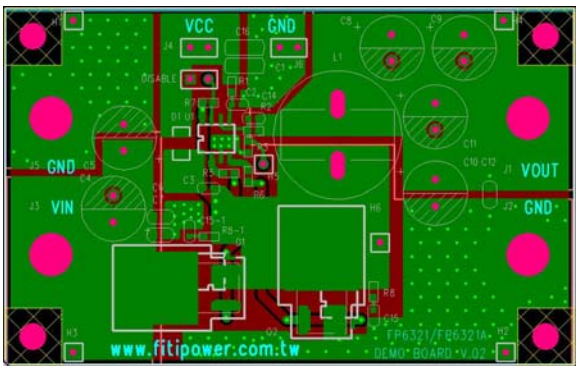


Figure 18. Top Layer

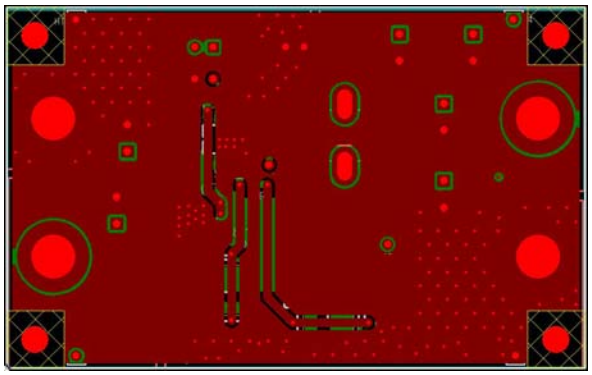


Figure 19. Bottom Layer

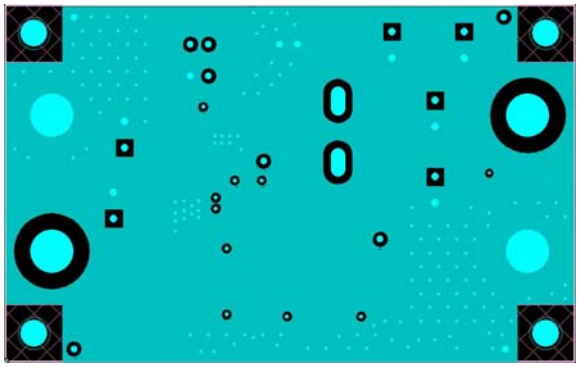


Figure 20. Inner Layer 2

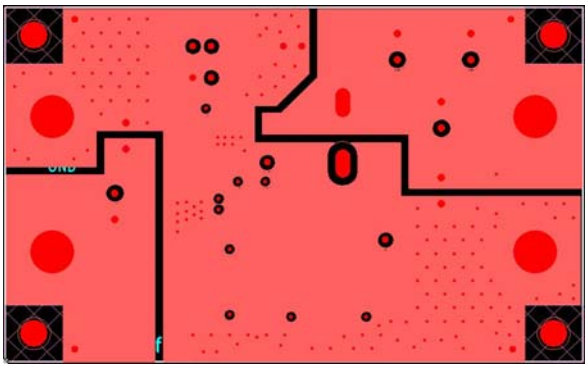


Figure 21. Inner layer 3

Application Information (Continued)

Layout Notice

When designing a high frequency switching regulated power supply, layout is very important. Using a good layout can solve many problems associated with these types of supplies. The problems due to a bad layout are often seen at high current levels and are usually more obvious at large input to output voltage differentials. Some of the main problems are loss of regulation at high output current and/or large input to output voltage differentials, excessive noise on the output and switch waveforms, and instability. Using the simple guidelines that follow will help minimize these problems.

(1) Inductor

Always try to use a low EMI inductor with a ferrite type closed core. Open core can be used if they have low EMI characteristics and are located a bit more away from the low power traces and components.

(2) Feedback

Try to put the feedback trace as far from the inductor and noisy power traces as possible. You would also like the feedback trace to be as direct as possible and somewhat thick. These two sometimes involve a trade-off, but keeping it away from inductor EMI and other noise sources is the more critical of the two. It is often a good idea to run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two.

(3) Filter Capacitors

When using a low value ceramic input filter capacitor, it should be located as close to the VIN pin of the IC as possible. This will eliminate as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply. Sometimes using a small resistor between V_{CC} and IC VCC pin will more useful because the RC will be a low-pass filter. Some designs require the use of a feed-forward capacitor connected from the output to the feedback pin as well, usually for stability reasons.

(4) Compensation

If external compensation components are needed for stability, they should also be placed closed to the IC. Surface mount components are recommended here as well for the same reasons discussed for the filter capacitors.

(5) Traces and Ground Plane

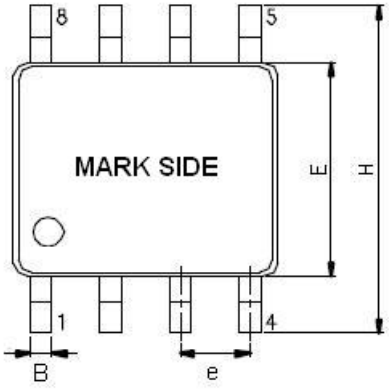
Make all of the power (high current) traces as short, direct, and thick as possible. It is a good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per Ampere. The inductor, output capacitors, and output diode (In synchronous case, means the low side switch) should be as close to each other possible. This will reduce lead inductance and resistance as well which in turn reduces noise spikes, ringing, and resistive losses which produce voltage errors. The grounds of the IC, input capacitors, output capacitors, and output diode (or switch, if applicable) should be connected close together directly to a ground plane. It would also be a good idea to have a ground plane on both sides of the PCB. For multi-layer boards with more than two layers, a ground plane can be used to separate the power plane (where the power traces and components are) and the signal plane (where the feedback and compensation and components are) for improved performance. It is good practice to use one standard via per 200mA of current if the trace will need to conduct a significant amount of current from one plane to the other. Due to the way switching regulators operate, there are power on and power off states. During each state there will be a current loop made by the power components that are currently conducting. Place the power components so that during each of the two states the current loop is conducting in the same direction.

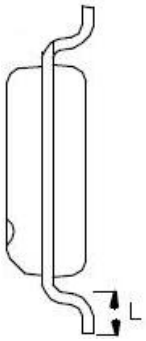
(6) Heat Sinking

When using a surface mount power IC or external power switches, the PCB can often be used as the heat-sink. This is done by simply using the copper area of the PCB to transfer heat from the device. Refer to the device datasheet for information on using the PCB as a heat-sink for that particular device. This can often eliminate the need for an externally attached heat-sink. These guidelines apply for any inductive switching power supply. These include Step-down (Buck), Step-up (Boost), Fly-back, inverting Buck/Boost, and SEPIC among others. The guidelines are also useful for linear regulators, which also use a feedback control scheme, that are used in conjunction with switching regulators or switched capacitor converters.

Outline Information

SOP- 8 Package (Unit: mm)





SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	1.35	1.75
A1	0.05	0.25
A2	1.30	1.50
B	0.31	0.51
D	4.80	5.00
E	3.80	4.00
e	1.20	1.34
H	5.80	6.20
L	0.40	1.27

Note：Followed From JEDEC MO-012-E