L7C174
8K x 8 Cache-Tag Static RAM

LOGIC DEVICES INCORPORATED

FEATURES

- 8K x 8 CMOS Static RAM with 8-bit Tag Comparison Logic
- High Speed Address-to-MATCH — 12 ns maximum
- High Speed Flash Clear
- High Speed Read Access Time — 12 ns maximum
- Low Power Operation
  Active: 300 mW typical at 35 ns
  Standby: 500 µW typical
- Data Retention at 2 V for Battery Backup Operation
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with IDT7174, IDT71B74, MK48H74
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Ceramic DIP
  - 28-pin Plastic SOJ
  - 32-pin Ceramic LCC

DESCRIPTION

The **L7C174** is a high-performance, low power CMOS static RAM optimized for use as the address tag comparator in high speed cache memory systems. One L7C174 can be used to map 8K cache lines into a 1 megabyte address space by comparing 20 address bits organized as 13-line address bits and 7-page address bits.

The storage circuitry is organized as 8192 words by 8 bits per word and includes an 8-bit data comparator with MATCH output. The 8-bit data is input/output on shared I/O pins and comparison is performed between 8-bit incoming data and accessed memory locations. Also provided is a high speed $\overline{\text{CLEAR}}$ control which clears all memory locations to zero when activated. This allows all address tag bits to be cleared when powering on or when flushing the cache.

This device is available in five speed grades with maximum address-to-MATCH times of 12 ns to 35 ns. Operation is from a single +5 V power supply with power consumption only being 300 mW (typical) at 35 ns. Dissipation drops to 500 µW (typical) when the memory is deselected (Enable is high).

The L7C174 consumes only 30 µW (typical) at 3 V allowing effective battery backup operation. For minimal power consumption, data may be retained in inactive storage with a supply voltage as low as 2 V.

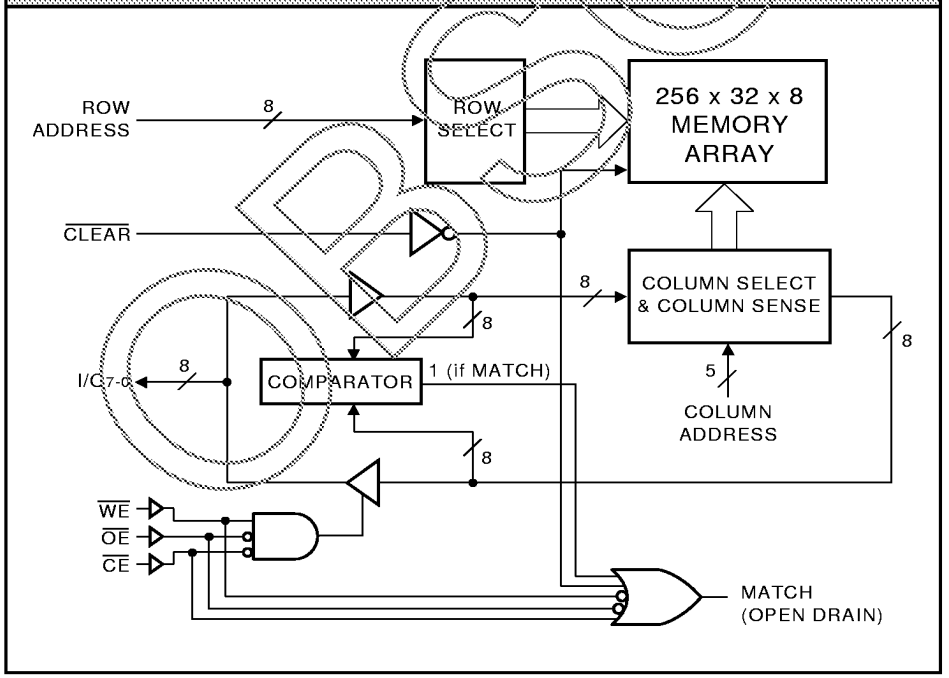
The L7C174 provides fully asynchronous (unclocked) operation with matching access and cycle times. An active low Chip Enable and Output Enable along with a three state I/O bus simplify the connection of several chips for increased storage capacity. Wide tag addresses are easily accommodated by paralleling devices and Wire-ORing the MATCH outputs. A low on the MATCH output indicates a data mismatch.

Memory locations are specified on address pins A_0 through A_{12} with functions defined in the Truth Table.

During $\overline{\text{CLEAR}}$, the state of the I/O pins remain completely defined by the $\overline{\text{WE}}$, $\overline{\text{CE}}$, and $\overline{\text{OE}}$ control inputs. Data In has the same polarity as Data Out.

Latchup and static discharge protection are provided on-chip. The L7C174 can withstand an injection current of up to 200 mA on any pin without damage.

L7C174 BLOCK DIAGRAM



Truth Table

$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{CLEAR}$	MATCH	I/O	FUNCTION
X	X	X	L	H	—	Reset all bits to low
X	H	X	H	H	High-Z	Deselect chip
H	L	H	H	L	D_{IN}	No MATCH
H	L	H	H	H	D_{IN}	MATCH
H	L	L	H	H	D_{OUT}	Read
L	L	X	H	H	D_{IN}	Write

X = Don't Care; L = V_{IL}; H = V_{IH}

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Industrial	–40°C to +85°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Industrial	–40°C to +85°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics

Over Operating Conditions (Note 5)

Symbol	Parameter	Test Condition	L7C174 Min	L7C174 Typ	L7C174 Max	Unit
V_{OH}	Output High Voltage (Note 11)	V_{CC} = 4.5 V, I_{OH} = –4.0 mA (all except MATCH pin)	2.4			V
V_{OL}	Output Low Voltage (Note 11)	I_{OL} = 8.0 mA (all except MATCH pin)			0.4	V
		I_{OL} = 18.0 mA (MATCH pin)			0.4	V
V_{IH}	Input High Voltage		2.2		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	V
I_{IX}	Input Leakage Current	Ground ≤ V_{IN} ≤ V_{CC}	–10		+10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}, $\overline{OE}$ = V_{CC} (except MATCH pin)	–10		+10	µA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		100	500	µA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Notes 9, 10)		10	200	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

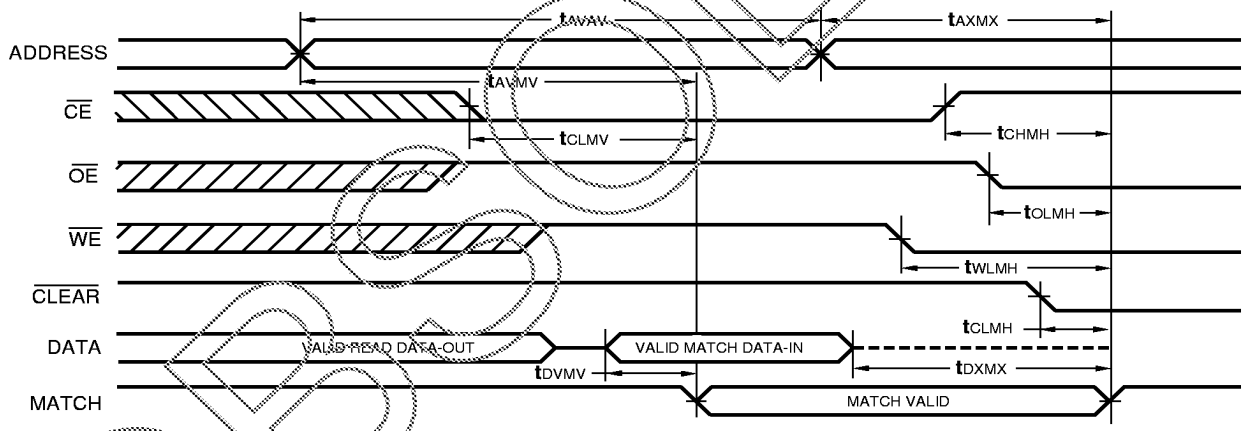
Symbol	Parameter	Test Condition	L7C174- 35	25	20	15	12	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	90	115	140	165	195	mA

SWITCHING CHARACTERISTICS *Over Operating Range*

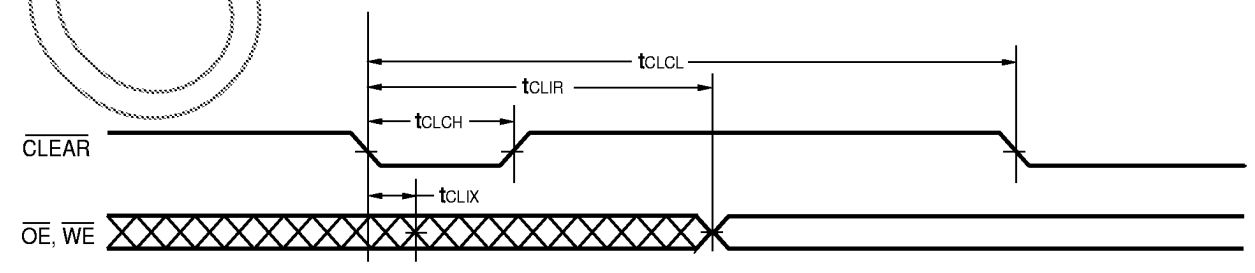
MATCH AND $\overline{\text{CLEAR}}$ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C174–									
		35		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	MATCH Cycle Time	35		25		20		15		12	
t_{AVMV}	Address Valid to MATCH Valid		30		22		20		15		12
t_{AXMX}	Address Change to MATCH Change	3		3		3		3		3	
t_{CLMV}	Chip Enable Low to MATCH Valid		20		15		10		10		8
t_{CHMH}	Chip Enable High to MATCH High	3		3		3		3		3	
t_{OLMH}	Output Enable Low to MATCH High	3		3		3		3		3	
t_{WLMH}	Write Enable Low to MATCH High	3		3		3		3		3	
t_{CLMH}	$\overline{\text{CLEAR}}$ Low to MATCH High	0	25	0	20	0	15	0	12	0	10
t_{DVMV}	Data Valid to MATCH Valid		20		15		15		13		10
t_{DXMX}	Data Change to MATCH Change	0		0		0		0		0	
t_{CLCL}	$\overline{\text{CLEAR}}$ Cycle Time	65		55		45		35		30	
t_{CLCH}	$\overline{\text{CLEAR}}$ Pulse Width	20		15		15		12		12	
t_{CLIX}	$\overline{\text{CLEAR}}$ Low to Inputs Don't Care	0		0		0		0		0	
t_{CLIR}	$\overline{\text{CLEAR}}$ Low to Inputs Recognized		70		60		50		50		45

MATCH CYCLE



CLEAR CYCLE

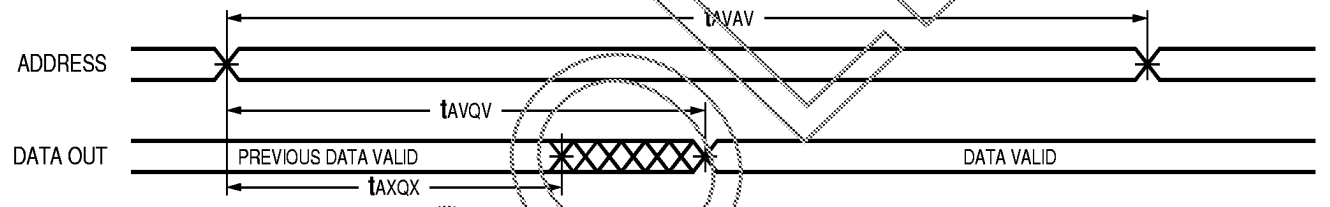


SWITCHING CHARACTERISTICS *Over Operating Range*

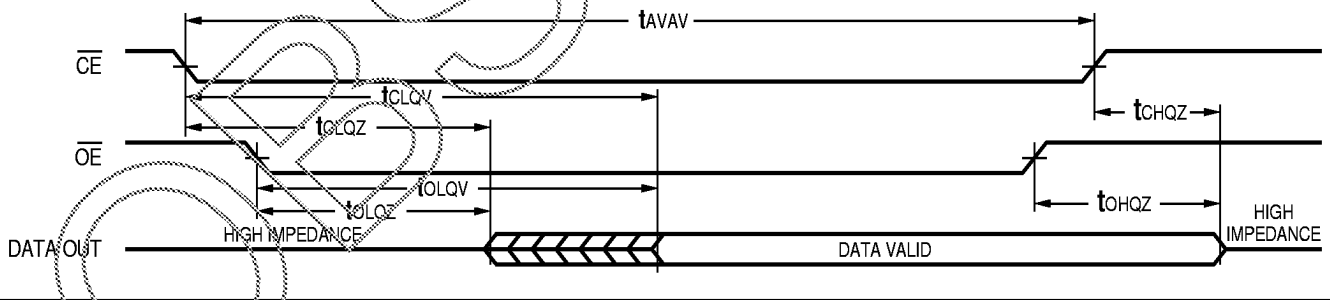
READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C174–									
		35		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Read Cycle Time	35		25		20		15		12	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		35		25		20		15		12
t_{AXQX}	Address Change to Output Change	3		3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		15		12		10		8		8
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		15		10		8		8		5
t_{OLQV}	Output Enable Low to Output Valid		15		12		10		8		6
t_{OLQZ}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (Notes 20, 21)		12		10		8		5		5
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0		0		0	

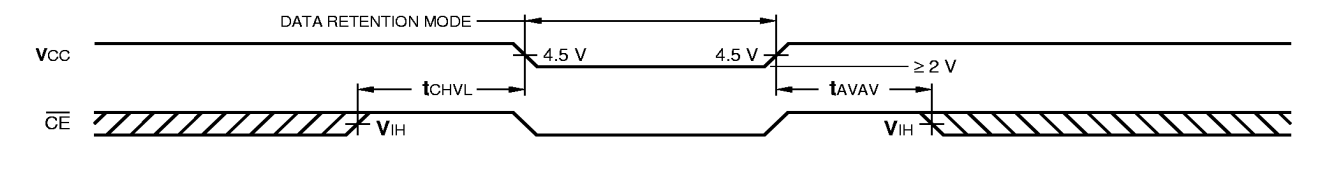
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}$/$\overline{OE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Notes 9, 10*

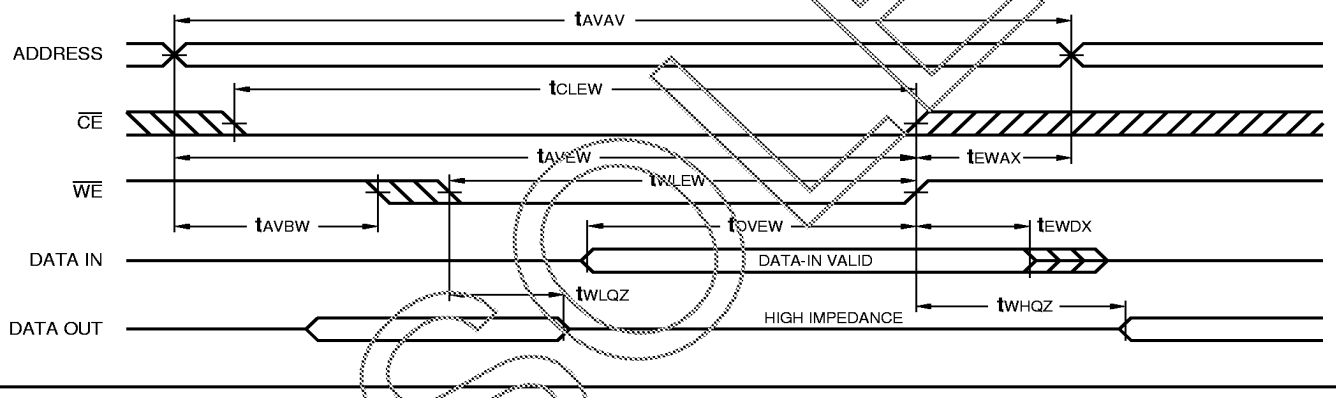


SWITCHING CHARACTERISTICS *Over Operating Range*

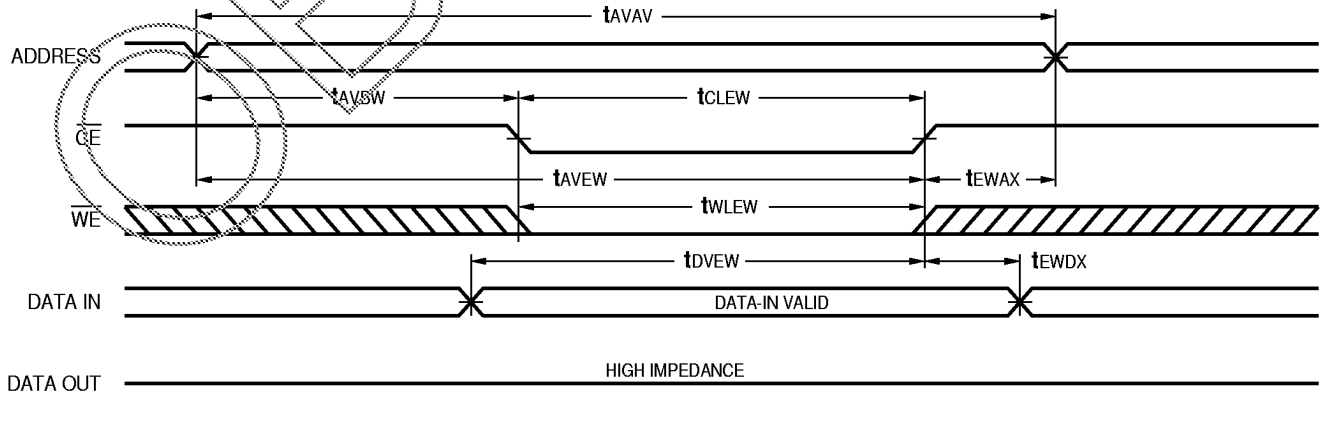
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C174–									
		35		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	25		20		20		15		12	
t_{CLEW}	Chip Enable Low to End of Write Cycle	25		15		15		12		10	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	25		15		15		12		10	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	20		15		15		12		10	
t_{DVEW}	Data Valid to End of Write Cycle	15		10		10		7		6	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		10		7		7		5		4

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE}$ must be $\ge V_{CC} - 0.2$ V. All other inputs must meet $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE}$ and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Figs. 1a and 1c), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior to or coincident-with the $\overline{CE}$ transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE}$ going active, the output remains in a high impedance state.

18. If $\overline{CE}$ goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

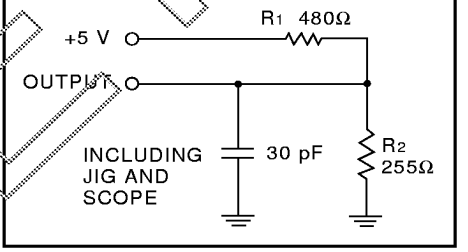


FIGURE 1b.

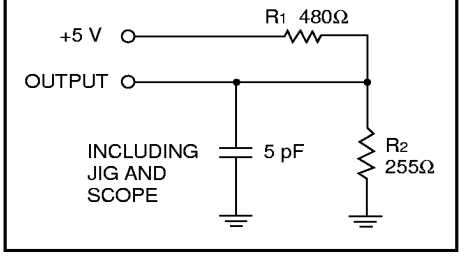


FIGURE 1c.

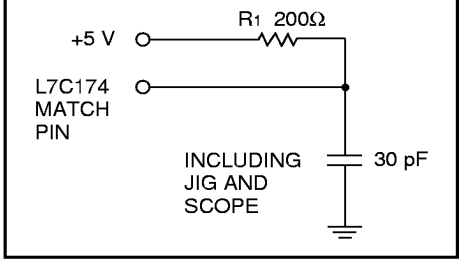
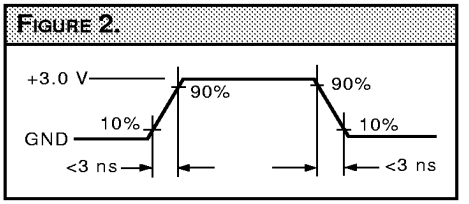
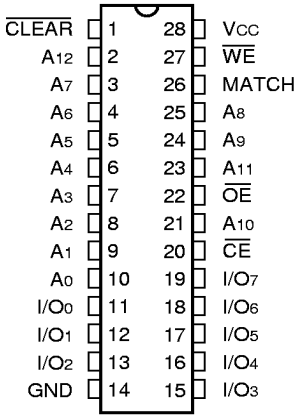


FIGURE 2.

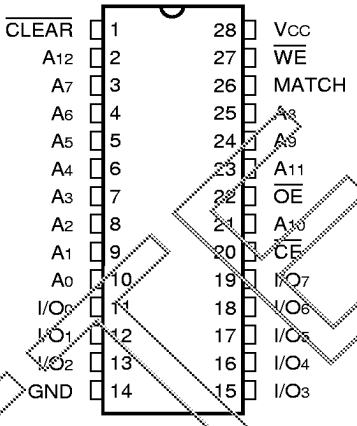


ORDERING INFORMATION

28-pin — 0.3" wide



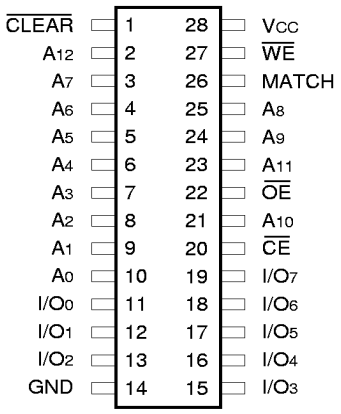
28-pin — 0.6" wide



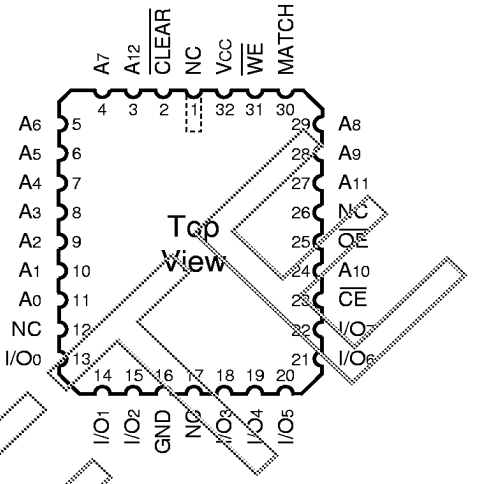
Speed	Plastic DIP (P10)	Ceramic DIP (C5)	Plastic DIP (P9)	Ceramic DIP (C6)
	0°C to +70°C — Commercial Screening			
25 ns	L7C174PC25	—	L7C174NC25	—
20 ns	L7C174PC20	L7C174CC20	L7C174NC20	L7C174IC20
15 ns	L7C174PC15	L7C174CC15	L7C174NC15	L7C174IC15
12 ns	L7C174PC12	L7C174CC12	L7C174NC12	L7C174IC12
	–40°C to +85°C — Commercial Screening			
25 ns	L7C174PI25		L7C174NI25	
20 ns	L7C174PI20		L7C174NI20	
15 ns	L7C174PI15		L7C174NI15	
12 ns	L7C174PI12		L7C174NI12	
	–55°C to +125°C — Commercial Screening			
25 ns		L7C174CM25		L7C174IM25
20 ns		L7C174CM20		L7C174IM20
15 ns		L7C174CM15		L7C174IM15
	–55°C to +125°C — MIL-STD-883 Compliant			
25 ns		L7C174CMB25		L7C174IMB25
20 ns		L7C174CMB20		L7C174IMB20
15 ns		L7C174CMB15		L7C174IMB15

ORDERING INFORMATION

28-pin — 0.3" wide



32-pin



Speed	Plastic SOJ (W2)	Ceramic Leadless Chip Carrier (K7)
	0°C to +70°C — Commercial Screening	
35 ns	L7C174WC35	—
25 ns	L7C174WC25	—
20 ns	L7C174WC20	L7C174KC20
15 ns	L7C174WC15	L7C174KC15
12 ns	L7C174WC12	L7C174KC12
	–40°C to +85°C — Commercial Screening	
35 ns	L7C174WI35	
25 ns	L7C174WI25	
20 ns	L7C174WI20	
15 ns	L7C174WI15	
12 ns	L7C174WI12	
	–55°C to +125°C — Commercial Screening	
25 ns		L7C174KM25
20 ns		L7C174KM20
15 ns		L7C174KM15
	–55°C to +125°C — MIL-STD-883 Compliant	
25 ns		L7C174KMB25
20 ns		L7C174KMB20
15 ns		L7C174KMB15