5V FLASH MODULE

*PRELIMINARY **

FEATURES

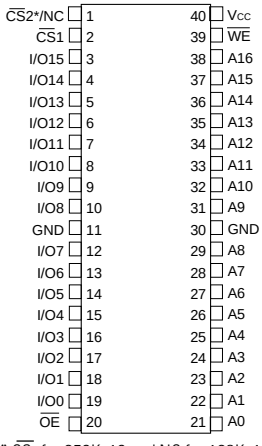
- Access Times of 50, 60, 70, 90, 120 and 150ns
- 40 pin Ceramic DIP (Package 303)
- Organized as 128Kx16 and 256Kx16
- Sector Architecture
  - 8 equal size sectors of 16KBytes each per chip
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- 100,000 Erase/Program Cycles Minimum (0°C to 70°C)
- Data Retention, 10 Years at 125°C
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming; 5V ±10% Supply
- Low Power CMOS
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Page Program Operation and Internal Program Control Time

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

Note: Programming information available upon request.

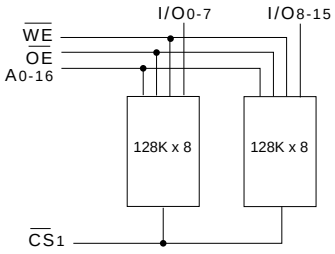
FIG. 1 PIN CONFIGURATION AND BLOCK DIAGRAM

TOP VIEW



* $\overline{CS}_2$ for 256Kx16 and NC for 128Kx16

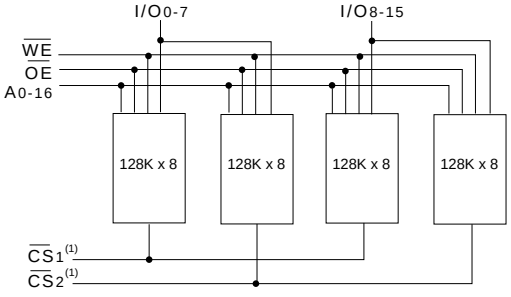
BLOCK DIAGRAM FOR WF128K16-XCX5



PIN DESCRIPTION

$A_{0\text{-}16}$	Address Inputs
$I/O_{0\text{-}15}$	Data Input/Output
$\overline{CS}_{1\text{-}2}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5.0V Power
GND	Ground

BLOCK DIAGRAM FOR WF256K16-XCX5



NOTE:

1. $\overline{CS}_1$ and $\overline{CS}_2$ are used to select the lower and upper 128Kx16 of the device. $\overline{CS}_1$ and $\overline{CS}_2$ must not be enabled at the same time.

ABSOLUTE MAXIMUM RATINGS (1)

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage Range (V_{CC})	-2.0 to +7.0	V
Signal voltage range (any pin except A9) (2)	-2.0 to +7.0	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Data Retention Mil Temp	10 years	
Endurance (write/erase cycles) Mil Temp	10,000 cycles min.	
A_9 Voltage for sector protect (V_{ID}) (3)	-2.0 to +14.0	V

NOTES:
1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot V_{SS} to -2.0 V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods of up to 20ns.
3. Minimum DC input voltage on A_9 pin is -0.5V. During voltage transitions, A_9 may overshoot Vss to -2V for periods of up to 20ns. Maximum DC input voltage on A_9 is +13.5V which may overshoot to 14.0 V for periods up to 20ns.

CAPACITANCE

(T_A = 25°C)

Test	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{CS}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	30	pF
I/O_{0-7} capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	30	pF
Address capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C
A_9 Voltage for Sector Protect	V_{ID}	11.5	12.5	V

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	128K x 16		256K x 16		Unit
			Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10	µA
Output Leakage Current	I_{LO}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10	µA
V_{CC} Active Current for Read (1)	I_{CC1}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}		70		80	mA
V_{CC} Active Current for Program or Erase (2)	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}		100		110	mA
V_{CC} Standby Current	I_{CC3}	V_{CC} = 5.5, $\overline{CS}$ = V_{IH}, f = 5MHz		6		8	mA
Output Low Voltage	V_{OL}	I_{OL} = 12.0 mA, V_{CC} = 4.5		0.45		0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.5 mA, V_{CC} = 4.5	0.85xVcc		0.85xVcc		V
Output High Voltage	V_{OH2}	I_{OH} = -100 µA, V_{CC} = 4.5	V_{CC} -0.4		V_{CC} -0.4		V
Low V_{CC} Lock Out Voltage	V_{LKO}		3.2		3.2		V

NOTES:
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

PRINCIPLES OF OPERATION

The following principles of operation of the WF128K16-XCX5 and WF256K16-XCX5 are applicable to each 128K x 8 memory chip inside the MCM. Programming of the device is accomplished by executing the program command sequence. The program algorithm, which is an internal algorithm, automatically times the program pulse widths and verifies proper cell margin. Sectors can be programmed and verified in less than 0.3 seconds. Erase is accomplished by executing the erase command sequence. The erase algorithm, which is internal, automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin. The entire memory is typically erased and verified in three seconds (including pre-programming).

BUS OPERATIONS

READ

The device has two control functions, both of which must be logically active, to obtain data at the outputs. Chip-Select ($\overline{CS}$) is the power control and should be used for device selection. Output-Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins. Figure 3 illustrates read timing waveforms.

OUTPUT DISABLE

With Output-Enable at a logic-high level (V_{IH}), output from the device is disabled. Output pins are placed in a high impedance state.

STANDBY MODE

The device has two standby modes, a CMOS standby mode ($\overline{CS}$ input held at V_{CC} + 0.5V), and a TTL standby mode ($\overline{CS}$ is held V_{IH}). In the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

WRITE

Device erasure and programming are accomplished via the command register. The contents of the register serve as input to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the commands, along with address and data information needed to execute the command. The command register is written by bringing Write-Enable to a logic-low level (V_{IL}), while Chip-Select is low and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of the Write-Enable while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used. Refer to AC Program characteristics, Figures 4 and 7.

TABLE 1 - BUS OPERATIONS

Operation	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_9	I/O
Read	L	L	H	A_0	A_1	A_9	D_{OUT}
Standby	H	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	HIGH Z
Write	L	H	L	A_0	A_1	A_9	D_{IN}
Enable Sector Protect	L	V_{ID}	L	X	X	V_{ID}	X
Verify Sector Protect	L	L	H	L	H	V_{ID}	Code

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{WE}$ CONTROLLED

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-50		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	50		60		70		90		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	25		30		35		45		50		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	25		30		30		45		50		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	40		45		45		45		50		50		ns
Chip Select Hold Time	t_{WHEH}	t_{CH}	0		0		0		0		0		0		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		20		20		20		ns
Duration of Byte Programming Operation (min)	t_{WHWH1}		14		14		14		14		14		14		µs
Chip and Sector Erase Time	t_{WHWH2}		2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	sec
Read Recovery Time Before Write	t_{GHWL}		0		0		0		0		0		0		ns
V_{CC} Setup Time		t_{VCS}	50		50		50		50		50		50		µs
Chip Programming Time				12.5		12.5		12.5		12.5		12.5		12.5	sec
Output Enable Setup Time		t_{OES}	0		0		0		0		0		0		ns
Output Enable Hold Time (1)		t_{OEH}	10		10		10		10		10		10		ns

1. For Toggle and $\overline{Data}$ Polling.

AC CHARACTERISTICS – READ ONLY OPERATIONS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-50		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	50		60		70		90		120		150		ns
Address Access Time	t_{AVQV}	t_{ACC}		50		60		70		90		120		150	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		50		60		70		90		120		150	ns
$\overline{OE}$ to Output Valid	t_{GLQV}	t_{OE}		25		30		35		40		50		55	ns
Chip Select to Output High Z (1)	t_{EHQZ}	t_{DF}		20		20		20		25		30		35	ns
$\overline{OE}$ High to Output High Z (1)	t_{GHQZ}	t_{DF}		20		20		20		25		30		35	ns
Output Hold from Address, $\overline{CS}$ or $\overline{OE}$ Change, whichever is first	t_{AXQX}	t_{OH}	0		0		0		0		0		0		ns

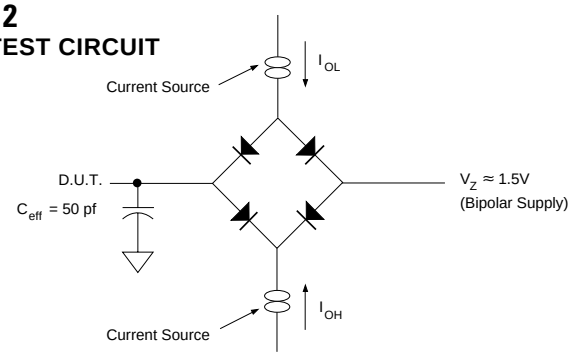
1. Guaranteed by design, not tested.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-50		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	50		60		70		90		120		150		ns
$\overline{WE}$ Setup Time	t_{WLEL}	t_{WS}	0		0		0		0		0		0		ns
$\overline{CS}$ Pulse Width	t_{ELEH}	t_{CP}	25		30		35		45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	25		30		30		45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	40		45		45		45		50		50		ns
$\overline{WE}$ Hold from $\overline{WE}$ High	t_{EHWH}	t_{WH}	0		0		0		0		0		0		ns
$\overline{CS}$ Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		20		20		20		ns
Duration of Programming Operation	t_{WHWH1}		14		14		14		14		14		14		µs
Duration of Erase Operation	t_{WHWH2}		2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	sec
Read Recovery before Write	t_{GHEL}		0		0		0		0		0		0		ns
Chip Programming Time				12.5		12.5		12.5		12.5		12.5		12.5	sec

FIG. 2
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 3
AC WAVEFORMS FOR READ OPERATIONS

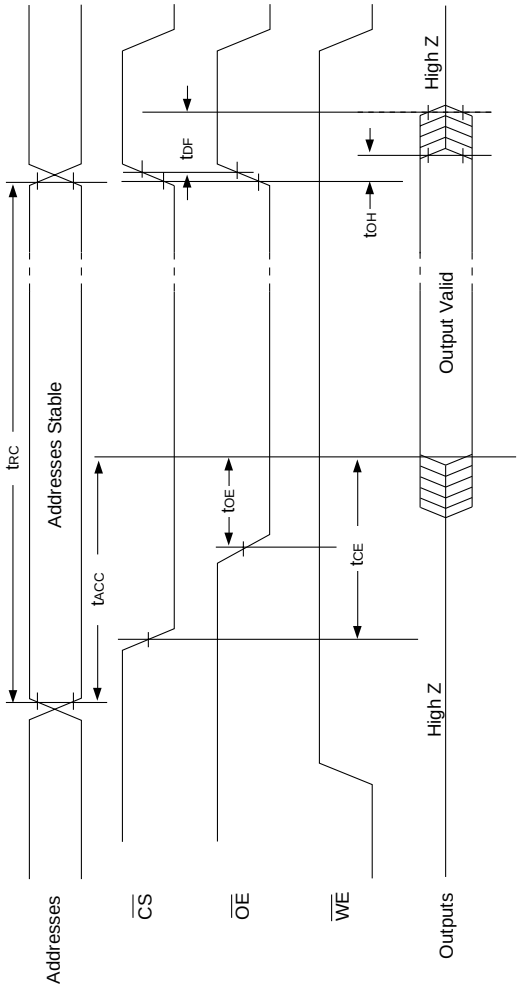
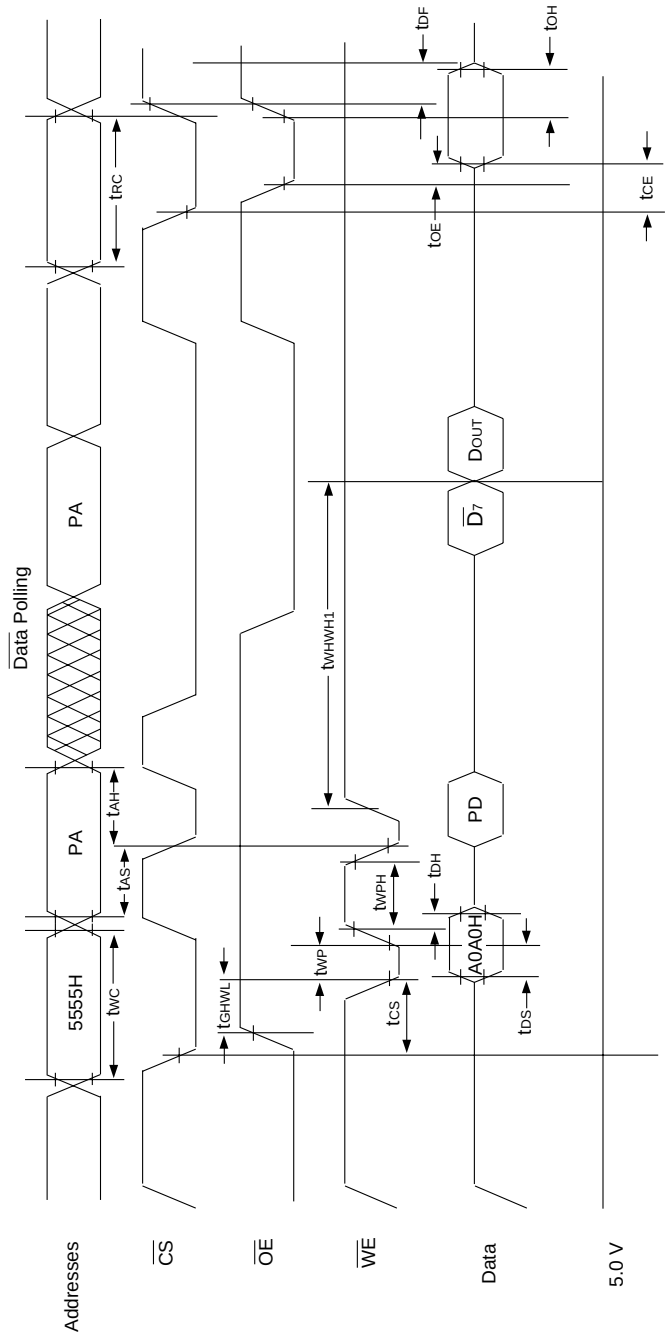
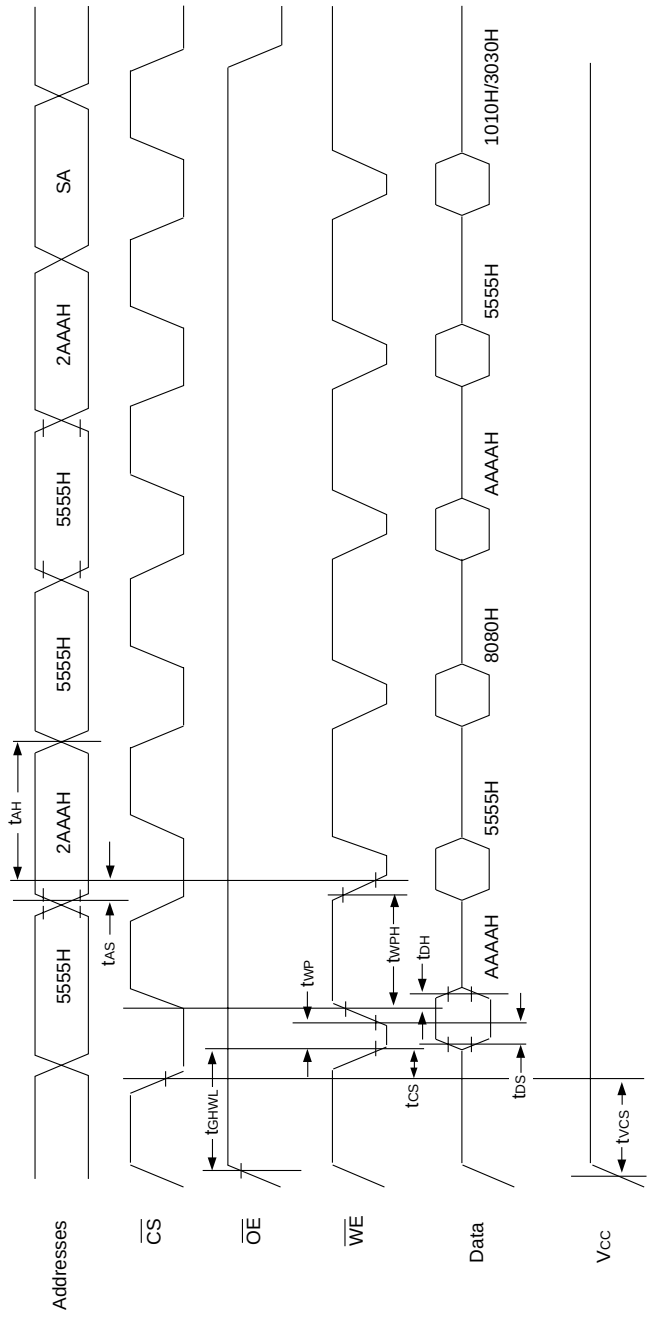


FIG. 4
AC WAVEFORMS FOR WRITE/ERASE/PROGRAM OPERATIONS, $\overline{WE}$ CONTROLLED



NOTES:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed.
3. $\overline{D7}$ is the output of the complement of the data written (for each chip).
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

FIG. 5
AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



NOTES:
1. SA is the sector address for Sector Erase.

FIG. 6
AC WAVEFORMS FOR $\overline{\text{DATA}}$ POLLING DURING EMBEDDED ALGORITHM OPERATIONS

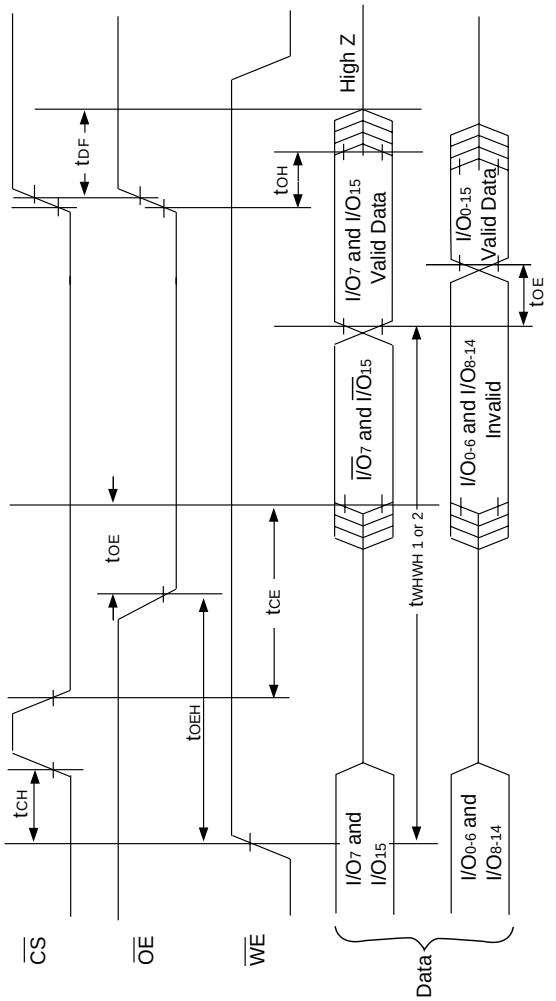
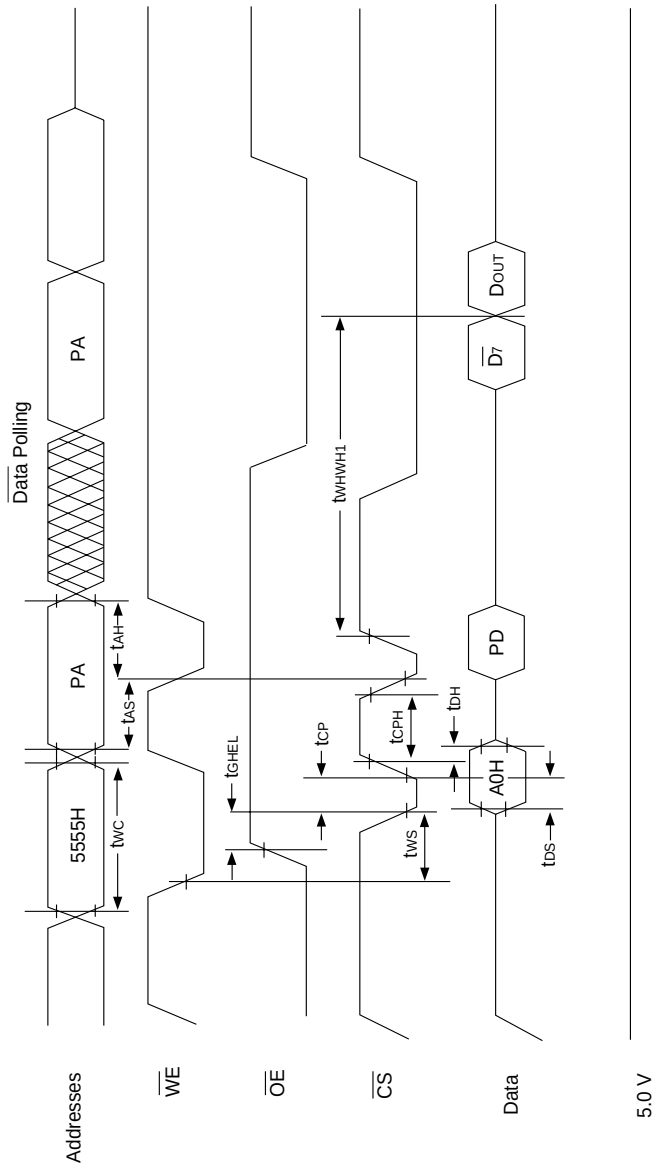
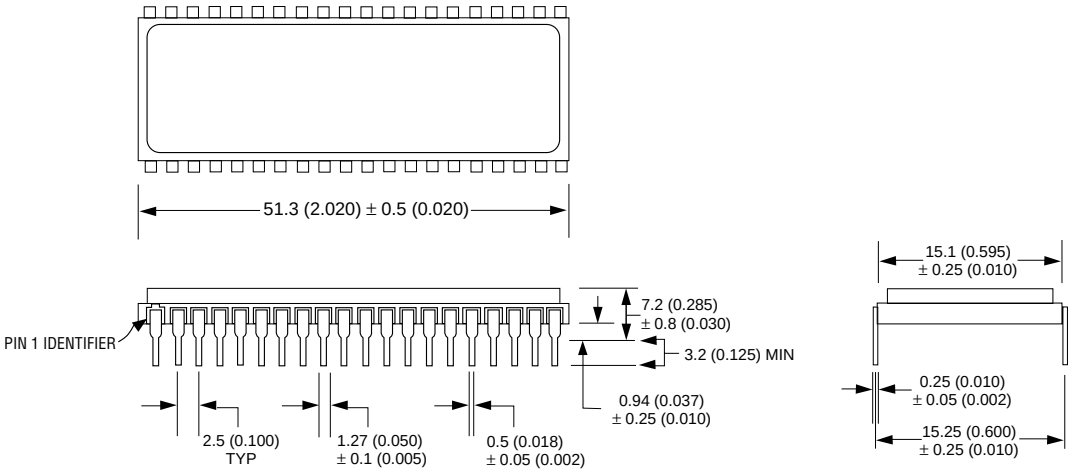


FIG. 7
AC WAVEFORMS FOR WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED



NOTES:
1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to the device (for each chip).
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

PACKAGE 303: 40 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W F XXXK16 - XXX C X 5 X

LEAD FINISH:
- Blank = Gold plated leads
- A = Solder dip leads

V_{PP} PROGRAMMING VOLTAGE
- 5 = 5V

DEVICE GRADE:
- Q = Compliant
- M = Military Screened -55°C to 125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0 to +70°C

PACKAGE TYPE:
- C = 40 Pin Ceramic 0.600" DIP (Package 303)

ACCESS TIME (ns)

ORGANIZATION, 128K x 16 or 256K x 16

Flash PROM

WHITE MICROELECTRONICS