MC100EL38

5V ECL ÷2, ÷4/6 Clock Generation Chip

The MC100EL38 is a low skew ÷2, ÷4/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

The Phase_Out output will go HIGH for one clock cycle whenever the ÷2 and the ÷4/6 outputs are both transitioning from a LOW to a HIGH. This output allows for clock synchronization within the system.

Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple EL38s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one EL38, the MR pin need not be exercised as the internal divider design ensures synchronization between the ÷2 and the ÷4/6 outputs of a single device.

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- ESD Protection: > 2 KV HBM, > 100 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = –4.2 V to –5.7 V
- Internal Input Pulldown Resistors on CLK, $\overline{EN}$, MR, and DIVSEL
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 code V–0 @ 1/8″,
  Oxygen Index 28 to 34
- Transistor Count = 388 devices

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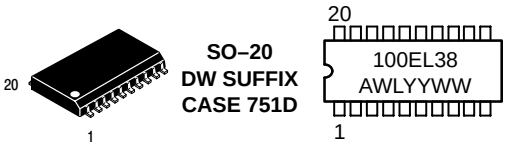
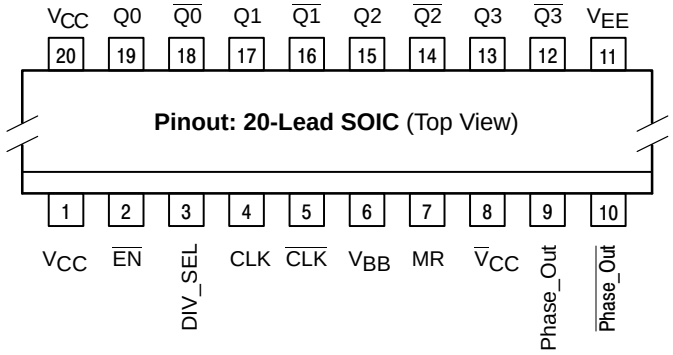
MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100EL38DW	SO–20	38 Units/Rail
MC100EL38DWR2	SO–20	1000 Units/Reel



* All V_{CC} pins are tied together on the die.

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Pinout Assignment

FUNCTION TABLE

CLK*	$\overline{EN}$*	MR*	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold $Q_{0–3}$
X	X	H	Reset $Q_{0–3}$

Z = Low-to-High Transition
ZZ = High-to-Low Transition
* Pin will default low when left open.

DIVSEL*	Q_2, Q_3 OUTPUTS
0	Divide by 4
1	Divide by 6

* Pin will default low when left open.

PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Diff Clock Inputs
$\overline{EN}$	ECL Sync Enable
MR	ECL Master Reset
Q0, $\overline{Q0}$; Q1,$\overline{Q1}$	ECL Diff ÷2 Outputs
Q2,$\overline{Q2}$; Q3, $\overline{Q3}$	ECL Diff ÷4/6 Outputs
DIV_SEL	ECL Frequency Select Input
Phase_Out, $\overline{Phase\_Out}$	ECL Phase Sync Signal
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

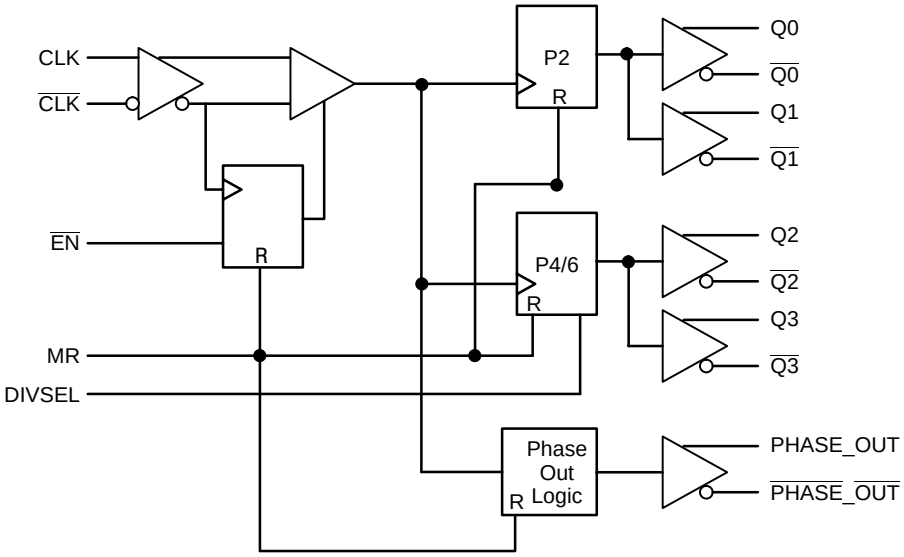


Figure 2. Logic Diagram

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

100EL SERIES PECL DC CHARACTERISTICS V_{CC} = 5.0 V; V_{EE} = 0.0 V (Note 2)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		50	60		50	60		54	65	mA
V_{OH}	Output HIGH Voltage (Note 3)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 3)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single–Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single–Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 4)	1.65		4.45	1.65		4.45	1.65		4.45	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
3. Outputs are terminated through a 50 Ω resistor to V_{CC} – 2.0 V.
4. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC} = 0.0 V; V_{EE} = –5.0 V (Note 5)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		50	60		50	60		54	65	mA
V_{OH}	Output HIGH Voltage (Note 6)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 6)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single–Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single–Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 7)	–3.35		–0.55	–3.35		–0.55	–3.35		–0.55	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
6. Outputs are terminated through a 50 Ω resistor to V_{CC} – 2.0 V.
7. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC} = 5.0 V; V_{EE} = 0.0 V or V_{CC} = 0.0 V; V_{EE} = –5.0 V (Note 8)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK → Q (Diff) to Output CLK → Q (S.E.) CLK → Phase_Out (Diff) CLK → Phase_Out (S.E.) MR → Q	760 710 800 750 510		960 1010 1000 1050 810	800 750 840 790 540		1000 1050 1040 1090 840	850 800 890 840 570		1050 1100 1090 1140 870	ps
t_{SKEW}	Within-Device Skew (Note 9) $Q_0 - Q_3$ All			50 75			50 75			50 75	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
	Part-to-Part $Q_0 - Q_3$ (Diff) All			200 240			200 240			200 240	
t_S	Setup Time $\overline{EN} \rightarrow \overline{CLK}$ DIVSEL → CLK		150			150			150		ps
t_H	Hold Time $\overline{CLK} \rightarrow \overline{EN}$ CLK → Div_Sel		150 200			150 200			150 200		ps
V_{PP}	Input Swing (Note 10)	150		1000	150		1000	150		1000	mV
t_{RR}	Reset Recovery Time			100			100			100	ps
t_{PW}	Minimum Pulse Width CLK MR	800 700			800 700			800 700			ps
t_r, t_f	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	ps

8. V_{EE} can vary +0.8 V / –0.5 V.
9. Skew is measured between outputs under identical transitions.
10. $V_{PP(}$min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

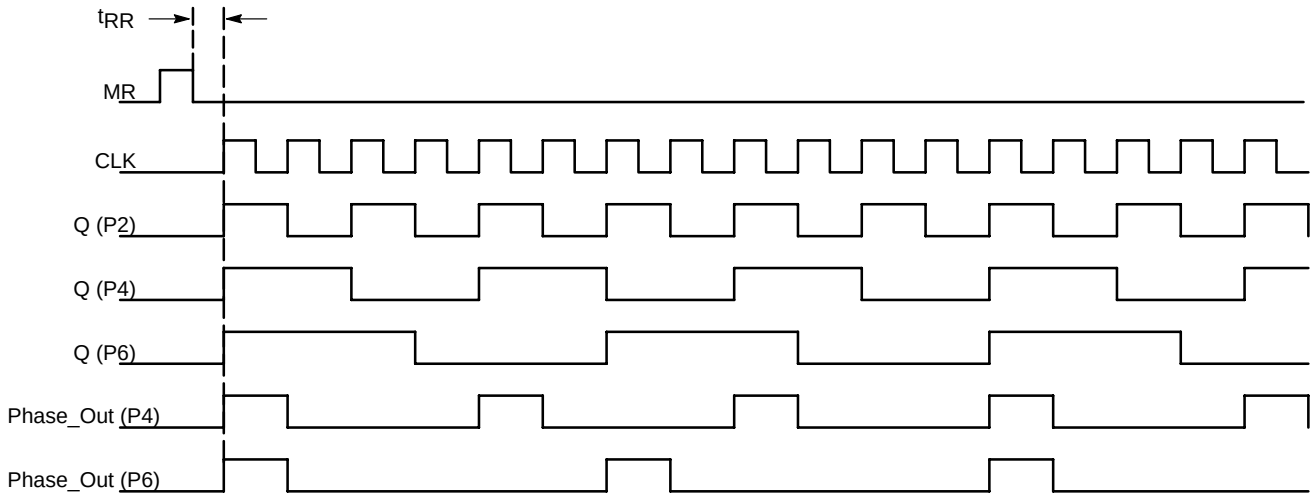
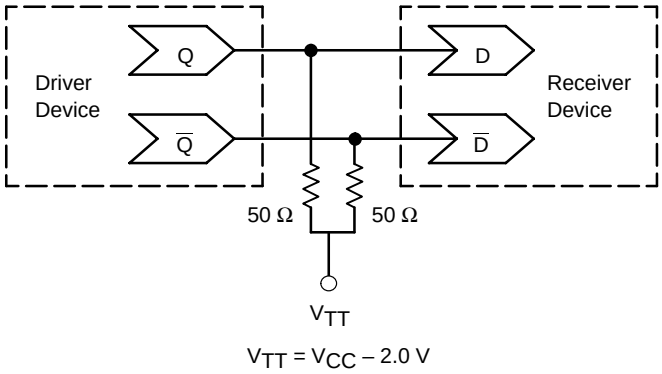


Figure 3. Timing Diagram



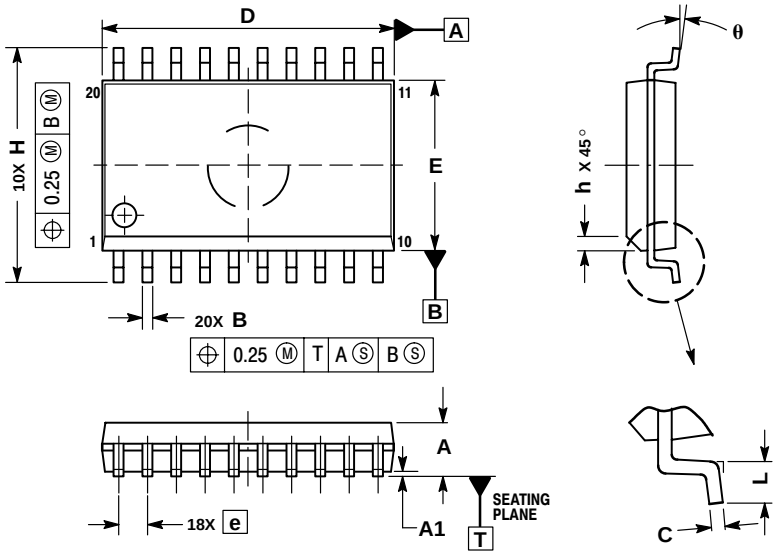
Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

PACKAGE DIMENSIONS

SO–20
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–05
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

Notes

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