# AKM
# AK4543

## AC'97™ Rev 2.1 Multimedia Audio CODEC

## Features

- **AC'97 Rev. 2.1 Compliant**
- **18bit Resolution A/D and D/A**
- **Exceeds a PC98/99 Performance Categories:**
    **A/D……………… 90dBA SNR**
    **D/A……………… 90dBA SNR**
    **D/A + Mixer …… 89dBA SNR**
    **A-A……………… 95BA SNR**
- **Analog Inputs:**
    **4 Stereo Inputs: LINE, CD, VIDEO, AUX**
    **Speakerphone and PC BEEP Inputs**
    **2 Independent MIC Inputs**
- **Direct PC_Beep Pass Through for lower system costs**
- **Analog Output:**
    **Stereo LINE Output with volume control**
    **True Line Level with volume control**
    **Mono Output with volume control**
- **3D Stereo Enhancement**
- **Multiple codec Capability**
    **The AK4543 can work as a Primary or Secondary.**
- **EAPD(External Amplifier Powerdown) Support**
- **Power Supplies:**
    **Analog 5.0V, Digital 3.3V or 5.0V**
- **Low Power Consumption**
    **200mW(Analog:5V/Digital:3.3V) at full operation**
- **48 Pin LQFP Package**

## General Description

The AK4543 is a 18bit high performance codec compliant with Audio Codec '97 Rev 2.1 requirements. The AC Link serial interface allows the AK4543 to be used with digital controllers as well as custom logic accelerators to meet full PC98 and PC99 requirements for a PCI audio solution.

The AK4543 provides two pairs of stereo outputs with independent volume controls along with a mono output, multiple stereo and mono inputs, are combined to create flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs.

The AK4543 can function as a Primary AC'97 or Secondary codec depending on the codec ID configuration(Multiple codec extension), making the AK4543 suitable for the docking station application and multiple codec applications such as 4 speaker output or 6 speaker output.
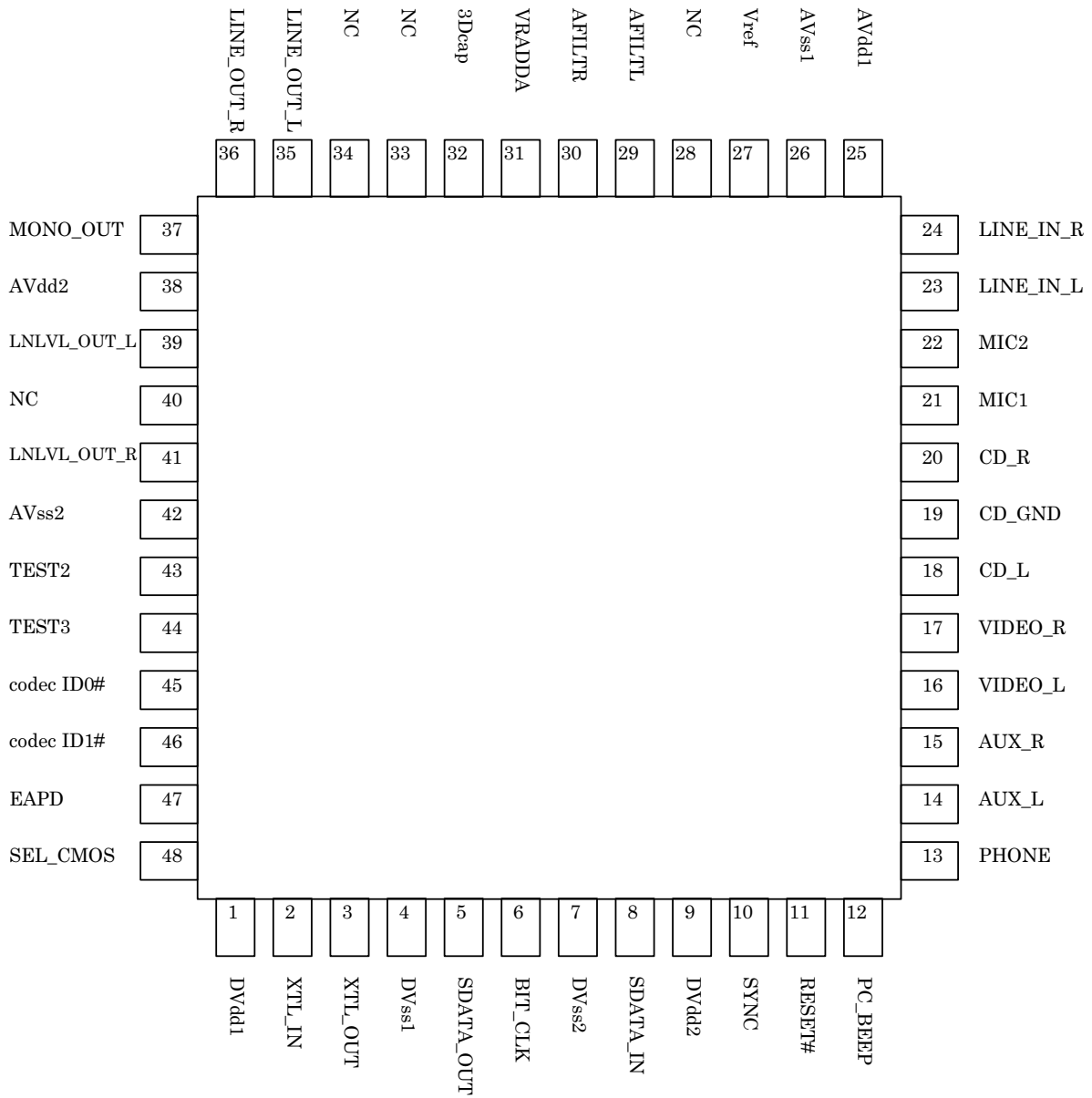
Sampling at 48kHz, the AK4543 provides excellent audio performance, meeting or exceeding all standard requirements. It offers low power consumption, and flexible power-down modes for use in laptops, desktop PCs, and aftermarket add-in boards.

Like the earlier pin-compatible AK4540 and AK4542, the AK4543 is available in a compact 48-lead LQFP package.

The AK4543 is a pin compatible upgrade for the AK4540 and AK4542, some software changes will be required to experience the extra functions ot the AK4543.
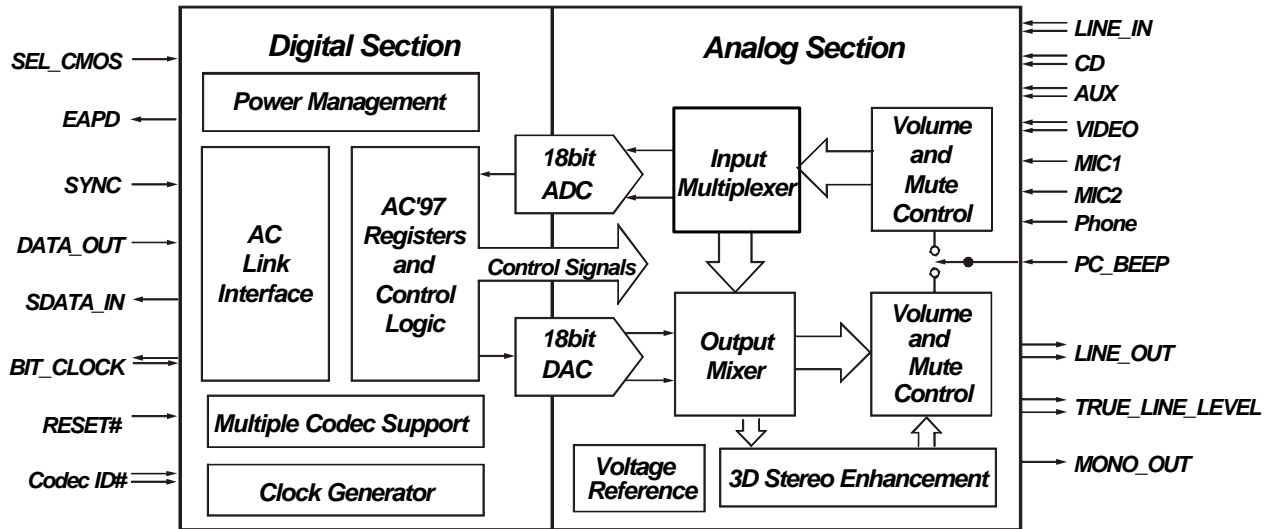


* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

| Pin | Signal |
|-----|--------|
| 36 | LINE_OUT_R |
| 35 | LINE_OUT_L |
| 34 | NC |
| 33 | NC |
| 32 | 3Dcap |
| 31 | VRADDA |
| 30 | AFILTR |
| 29 | AFILTL |
| 28 | NC |
| 27 | Vref |
| 26 | AVss1 |
| 25 | AVdd1 |

| Signal | Pin | | Pin | Signal |
|--------|-----|--|-----|--------|
| MONO_OUT | 37 | | 24 | LINE_IN_R |
| AVdd2 | 38 | | 23 | LINE_IN_L |
| LNLVL_OUT_L | 39 | | 22 | MIC2 |
| NC | 40 | | 21 | MIC1 |
| LNLVL_OUT_R | 41 | | 20 | CD_R |
| AVss2 | 42 | | 19 | CD_GND |
| TEST2 | 43 | | 18 | CD_L |
| TEST3 | 44 | | 17 | VIDEO_R |
| codec ID0# | 45 | | 16 | VIDEO_L |
| codec ID1# | 46 | | 15 | AUX_R |
| EAPD | 47 | | 14 | AUX_L |
| SEL_CMOS | 48 | | 13 | PHONE |

| Pin | Signal |
|-----|--------|
| 1 | DVdd1 |
| 2 | XTL_IN |
| 3 | XTL_OUT |
| 4 | DVss1 |
| 5 | SDATA_OUT |
| 6 | BIT_CLK |
| 7 | DVss2 |
| 8 | SDATA_IN |
| 9 | DVdd2 |
| 10 | SYNC |
| 11 | RESET# |
| 12 | PC_BEEP |

| No. | Signal Name | I/O | Description |
|---|---|---|---|
| | | | Pin/Function |
| 1 | DVdd1 | - | Digital power supply; 3.3V or 5.0V(DVdd1 = DVdd2)<br>0.1uF + 4.7uF capacitors should be connected to digital ground. |
| 2 | XTL_IN<br>(MCLKI) | I | 24.576MHz(512fs) crystal is normally connected.<br>If a crystal is not connected, an external clock can be used. |
| 3 | XTL_OUT(open) | O | 24.576MHz(512fs) crystal. If an external clock is used, this pin should be open. |
| 4 | DVss1 | - | Digital Ground; 0V<br>This pin should be directly connected to DVss2 on board. |
| 5 | SDATA_OUT | I | Serial 256-bit AC'97 data stream from digital controller |
| 6 | BIT_CLK | I/O | 12.288MHz(256fs) serial data clock<br>Output when Primary codec(codec ID=00).<br>Input when Secondary codec(codec ID=01, 10, 11). |
| 7 | DVss2 | - | Digital Ground; 0V<br>This pin should be directly connected to DVss1 on board. |
| 8 | SDATA_IN | O | Serial 256-bit AC'97 data stream to digital controller |
| 9 | DVdd2 | - | Digital power supply; 3.3V or 5.0V(DVdd1 = DVdd2)<br>0.1uF + 4.7uF capacitors should be connected to digital ground. |
| 10 | SYNC | I | AC'97 Sync Clock, 48kHz(1fs) fixed rate sampling rate |
| 11 | RESET# | I | AC'97 Master Hardware Reset |
| 12 | PC_BEEP | I | PC Speaker beep pass through |
| 13 | PHONE | I | From telephony subsystem speakerphone |
| 14 | AUX_L | I | Aux Left Channel |
| 15 | AUX_R | I | Aux Right Channel |
| 16 | VIDEO_L | I | Video Audio Left Channel |
| 17 | VIDEO_R | I | Video Audio Right Channel |
| 18 | CD_L | I | CD Audio Left Channel |
| 19 | CD_GND | I | CD Audio analog ground; 0V<br>CD_GND or analog ground should be connected. |
| 20 | CD_R | I | CD Audio Right Channel |
| 21 | MIC1 | I | Desktop Microphone Input |
| 22 | MIC2 | I | Second Microphone Input |
| 23 | LINE_IN_L | I | Line In Left Channel |
| 24 | LINE_IN_R | I | Line In Right Channel |
| 25 | AVdd1 | - | Analog power supply; 5.0V(AVdd1=AVdd2)<br>0.1uF + 4.7uF capacitors should be connected to AVss1(analog ground). |
| 26 | AVss1 | - | Analog Ground; 0V |
| 27 | Vref | O | Reference Voltage Output;<br>0.1μF +4.7μF capacitors should be connected to Avss1(analog ground). |
| 28 | NC | - | No Connection |
| 29 | AFILTL | O | Anti-Aliasing Filter Cap; Connected to analog ground with 1nF capacitor. |
| 30 | AFILTR | O | Anti-Aliasing Filter Cap; Connected to analog ground with 1nF capacitor. |
| 31 | VRADDA | O | Vref for ADC and DAC; 0.1μF capacitor should be connected to analog ground. |
| 32 | 3Dcap | O | 3D Enhancement Cap; 27nF capacitor should be connected to analog ground. |
| 33 | NC | - | No Connection |
| 34 | NC | - | No Connection |
| 35 | LINE_OUT_L | O | Line Out Left Channel |
| 36 | LINE_OUT_R | O | Line Out Right Channel |
| 37 | MONO_OUT | O | To telephony subsystem speakerphone |
| 38 | AVdd2 | - | Analog power supply; 5.0V(AVdd1=AVdd2)<br>0.1uF capacitor should be connected to AVss2(analog ground). |
| 39 | LNLVL_OUT_L | O | True Line Level Out Left Channel |
| 40 | NC | - | No Connection |
| 41 | LNLVL_OUT_R | O | True Line Level Out Right Channel |
| 42 | AVss2 | - | Analog Ground; 0V |
| 43 | TEST2 | I | Test pin (This pin should be open for normal operation) |
| 44 | TEST3 | I | Test pin (This pin should be open for normal operation) |
| 45 | Codec ID0# | I | Codec ID configuration(ID select input for multiple codec extension) See Page20. |
| 46 | Codec ID1# | I | Codec ID configuration(ID select input for multiple codec extension) See Page20. |
| 47 | EAPD | O | External amplifier powerdown                    See Page 20. |

| 48 | SEL_CMOS | I | CMOS/TTL selection for digital input levels<br>CMOS: Leave open for 3.3V supply.<br>TTL : Tie to GND for 5V supply. | See Page 28. |

### Absolute Maximum Rating

AVss1, AVss2, DVss1, DVss2 =0V   (Note 1)

| Parameter | Symbol | min | max | Units |
|---|---|---|---|---|
| Power Supplies<br>    Analog(AVdd1 & AVdd2)<br>    Digital(DVdd1 & DVdd2) | VA<br>VD | -0.3<br>-0.3 | 6.0<br>6.0 | V<br>V |
| Input Current (any pins except for supplies) | IIN | - | ±10 | mA |
| Analog Input Voltage | VINA | -0.3 | VA+0.3 | V |
| Digital Input Voltage | VIND | -0.3 | VD+0.3 | V |
| Ambient Temperature | Ta | -10 | 70 | °C |
| Storage Temperature | Ta | -65 | 150 | °C |

Note 1: All voltages with respect to ground.
    AGND(AVss1, AVss2) and DGND(DVss1, DVss2) must be the same voltage.


Warning: Operation at or beyond these limits may results in permanent damage to the device.
    Normal operation is not guaranteed at these extremes.


### Recommended Operating Condition

AGND, DGND=0V (Note 1)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| Power Supplies          AK4543 | | | | | |
|                                   Analog | VA | 4.75 | 5.0 | 5.25 | V |
|                                   Digital | VD | 3.135 | 3.3 or 5.0 | 5.25 | V |

Note 1 : All voltages with respect to ground.

| AK4543  Analog Characteristics |
|---|

Ta=25°C,AVdd=5.0V±5%, DVdd=3.3V±5% or 5V±5%, fs=48KHz, Signal Frequency =1kHz
All volume setting for ADC/DAC performance measurement is 0dB.

| Parameter | min | Typ | max | Units |
|---|---|---|---|---|
| Audio-ADC | | | | |
| Resolution | | | 18 | Bits |
| S/N (A weighted) | 85 | 90 | | dB |
| S/(N+D)                          (-1dB analog input) | 70 | 77 | | dBFS |
| Inter Channel Isolation | 70 | 77 | | dB |
| Inter Channel Gain Mismatch | | | 0.5 | dB |
| Full Scale Input Voltage | 0.88 | 1.0 | 1.12 | Vrms |
| Power Supply Rejection | | 50 | | dB |
| Audio DAC: measured at AOUTL/AOUTR via MIXER path | | | | |
| Resolution | | | 18 | Bits |
| S/N (A weighted)<br>: mixer+DAC measured at AOUT | 84 | 89 | | dB |
| S/(N+D)                          (-1dB digital input) | 75 | 83 | | dBFS |
| Inter Channel Isolation | 70 | 80 | | dB |
| Inter Channel Gain Mismatch | | | 1.0 | dB |
| Full Scale Output Voltage | 0.83 | 0.95 | 1.07 | Vrms |
| Total Out-of-Band Noise (28.8kHz - 100kHz) | | -70 | | dB |
| Power Supply Rejection | | 50 | | dB |
| MIC Amplifier / MUX | | | | |
| Gain : 20dB is selected | 18 | 20 | 22 | dB |
| Master volume (Mono, Stereo, True Line Level Out) :  1.5dB x 32 step | | | | |
| Step Size | | -1.5 | | dB |
| Attenuation Control Range | -46.5 | | 0 | dB |
| Load Resistance | 10 | | | kΩ |
| PC Beep :  3dB x 16 step | | | | |
| Step Size | | -3.0 | | dB |
| Attenuation Control Range | -45 | | 0 | dB |
| Analog Mixer :  1.5dB x 32 step | | | | |
| Step Size | | -1.5 | | dB |
| Gain Control Range | -34.5 | | +12 | dB |
| Record Gain :  1.5dB x 16 step | | | | |
| Step Size | | +1.5 | | dB |
| Gain Control Range | 0 | | +22.5 | dB |
| Mixer | | | | |
| Input Voltage (except for MIC) | | 1.0 | | Vrms |
| Input Voltage       MIC : Gain =  0dB | | 1.0 | | Vrms |
|                        MIC : Gain = 20dB | | 0.1 | | Vrms |
| S/N(A weighed) : 0dB setting, 1 path is selected at Mixer<br>    CD to AOUT: | 85 | 95 | | dB |
|     Other analog input to AOUT | | 95 | | dB |
| Input Impedance (Input gain=0dB,Rec_MUTE=off)<br>    PC_BEEP only | (10) | 80 | | kΩ |
|     Others(PHONE, LINE, CD, AUX, VIDEO) | (10) | 40 | | kΩ |
| Input Impedance (MIC1 and MIC2) | (10) | 22 | | kΩ |
| Power Supplies | | | | |
| Analog Power Supply Current(AVdd1 & AVdd2)<br>   All ON mode(all PR_bits are 0) | | 36 | 54 | mA |
|    Cold Reset status(Reset#=L, Vref is ON) | | 2.5 | 5 | mA |
|    All OFF mode(all PR_bits are 1) | | 0 | 0.2 | mA |
| Digital Power Supply Current(DVdd1 & DVdd2)<br>   All ON mode(all PR_bits are 0) at DVDD=5V | | 13 | 20 | mA |
|    All ON mode(all PR_bits are 0) at DVDD=3.3V | | 6.6 | 10 | mA |
|    All OFF mode(all PR_bits are 1) | | 0 | 0.2 | mA |

| Filter Characteristics | | | | |
|---|---|---|---|---|
| Ta=25°C,AVdd=5.0V±5%, DVdd=3.3V±5% or 5V±5% , fs=48KHz(fixed) | | | | |
| Parameter | min | typ | Max | Units |
| ADC Digital Filter (Decimation LPF) | | | | |
| Passband (±0.2dB) | 0 | | 19.2 | kHz |
| Stopband | 28.8 | | | kHz |
| Stopband Attenuation | 70 | | | dB |
| Group Delay | | | 0.5 | ms |
| ADC Digital Filter (HPF) | | | | |
| Frequency Response;      -3dB | | 7.5 | | Hz |
|               -0.5dB | | 21 | | |
|               -0.1dB | | 49 | | |
| DAC Digital Filter | | | | |
| Passband (±0.2dB) | 0 | | 19.2 | kHz |
| Stopband | 28.8 | | | kHz |
| Group Delay | | | 0.5 | ms |
| Stopband Rejection | 70 | | | dB |
| DAC Post filter | | | | |
| Passband Frequency Response (0 - 19.2kHz) | | ±0.1 | | dB |

| AK4543  DC Characteristics | | | | | |
|---|---|---|---|---|---|
| Ta=-10~70°C, VD=5V±5%(SEL_CMOS=L) or 3.3V±5%(SEL_CMOS=H: Open), VA=5V±5%,  50pF external load | | | | | |
| Parameter | Symbol | min | Typ | Max | Units |
| "H" level input voltage | VIH | | - | - | |
|   XTAL_IN | | 0.7xVD | | | V |
|   RESET#, SYNC, SDATA_OUT, BIT_CLK | | | | | |
|     At SEL_COMS=L(GND) | | 2.2 | | | V |
|     At SEL_COMS=H(Open) | | 0.7xVD | | | V |
|   ID0#, ID1#, SEL_CMOS(Pull up) | | 0.8xVD | | | V |
| "L" level input voltage | VIL | - | - | | |
|   XTAL_IN | | | | 0.3xVD | V |
|   RESET#, SYNC, SDATA_OUT, BIT_CLK | | | | | |
|     At SEL_COMS=L(GND) | | | | 0.8 | V |
|     At SEL_COMS=H(Open) | | | | 0.3xVD | V |
|   ID0#, ID1#, SEL_CMOS(Pull up) | | | | 0.2xVD | V |
| "H" level output voltage          Iout= -1mA | VOH | VD-0.55 | - | - | V |
| "L" level output voltage          Iout=  1mA | VOL | - | - | 0.55 | V |
| Input leakage current(exclude pull up pins) | Iin | - | - | ±10 | μA |
| Pull up resistance | Rup | 50 | 100 | 200 | kΩ |

| Parameter | Symbol | min | Typ | max | Units |
|---|---|---|---|---|---|
| Switching Characteristics | | | | | |
| Ta=25°C, AVdd=5.0V±5%, DVdd=3.3V±5% or 5V±5%, 50pF external load | | | | | |
| Master Clock Frequency     Note) | Fmclk | - | 24.576 | - | MHz |
| If Crystal is not used. | | 45 | 50 | 55 | % |
| AC link Interface Timing | | | | | |
| BIT_CLK frequency | Fbclk | | 12.288 | | MHz |
| BIT_CLK clock Period(Tbclk=1/Fbclk) | Tbclk | - | 81.38 | | ns |
| BIT_CLK low pulse width | Tclk_low | 36.0 | 40.7 | 45 | ns |
| BIT_CLK high pulse width | Tclk_high | 36.0 | 40.7 | 45 | ns |
| BIT_CLK rise time | Trise_clk | - | - | 6 | ns |
| BIT_CLK fall time | Tfall_clk | - | - | 6 | ns |
| SYNC frequency | | - | 48 | - | kHz |
| SYNC low pulse width | Tsync_low | - | 19.5 (240 cycle) | - | μs (Tbclk) |
| SYNC high pulse width | Tsync_high | - | 1.3 (16 cycle) | - | μs (Tbclk) |
| SYNC rise time | Trise_sync | - | - | 6 | ns |
| SYNC fall time | Tfall_sync | - | - | 6 | ns |
| Setup time(SYNC, SDATA_OUT) | Tsetup | 10.0 | - | - | ns |
| Hold time(SYNC, SDATA_OUT) | Thold | 25.0 | - | | ns |
| SDATA_IN delay time from BIT_CLK rising edge | Tdelay | - | - | 15 | ns |
| SDATA_IN rise time | Trise_din | - | - | 6 | ns |
| SDATA_IN fall time | Tfall_din | - | - | 6 | ns |
| SDATA_OUT rise time | Trise_dout | - | - | 6 | ns |
| SDATA_OUT fall time | Tfall_dout | - | - | 6 | ns |
| Cold Rest  (SDATA_OUT=L, SYNC=L) | | | | | |
| RESET# active low pulse width | Trst_low | 1.0 | - | - | μs |
| RESET# inactive to BIT_CLK delay | Trst2clk | 162.8 (2 cycle) | | | ns (Tbclk) |
| Warm Rest Timing | | | | | |
| SYNC active low pulse width | Tsync_high | 1.0 | 1.3 (16 cycle) | - | μs (Tbclk) |
| SYNC inactive to BIT_CLK delay | Tsync2clk | 162.8 (2 cycle) | | | ns (Tbclk) |
| AC-link Low Power Mode Timing | | | | | |
| End of Slot 2 to BIT_CLK, SDATA_IN Low | Ts2_pdwn | - | - | 1.0 | μs |
| Activate Test Mode Timing | | | | | |
| Setup to trailing edge of RESET# | Tsetup2rst | 15.0 | - | - | ns |
| Hold from RESET# rising edge | Thold2rst | 100 | - | - | ns |
| Rising edge of RESET# to Hi-Z | Toff | - | - | 50 | ns |
| Falling edge of RESET# to "L" | Tlow | - | - | 50 | ns |

Note ) The use of a crystal is recommended.  If a master clock is supplied (or if an external oscillator is used), Master Clock should be supplied to XTAL_IN and XTAL_OUT should be left open.

■ Power On

Note that a AK4543 must be in cold reset at power on and RESET# must be low until master clock becomes stable, or a reset must be done once master clock is stable. AVdd or DVdd can be powered from independent supplies.

Vdd

RESET#

SDATA_OUT="L"

SYNC="L"

BIT_CLK

Initialize Registers
start up crystal oscillation     $T_{rst2clk}$
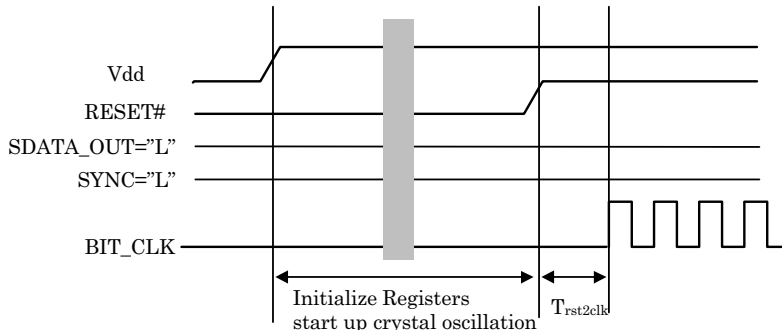
When using the AK4543 in the multiple codec mode, all codec's connected to the AC-link are waken up at the same time. A common reset line should be used to insure clock synchronization after power up.

■Cold Reset Timing

Note that both SDATA_OUT and SYNC must be low at the rising edge of RESET# for a cold reset to occur.
The AK4543 initializes all registers including the Powerdown Control Registers, BIT-CLK is reactivated and each analog output is in Hi-Z state except for PC Beep while RESET# pin is low. The PC Beep is directly routed to L & R line outputs when AK4543 is in Cold Reset. This is done to allow system sounds to be passed to speaker removing for an internal redundant speaker.
At the rising edge of RESET#, the AK4543 initiates the initialization of analog circuit, which takes 516fs cycles. After that, the mixer of the AK4543 is ready for normal operation.

Status bit in the slot 0 is "0" (not ready) when the AK4543 is in RESET period ("L") or in initialization process. After initialization cycles, the status bit goes to "1" indicating a ready condition.

$T_{rst\_low}$     $T_{rst2clk}$

RESET#

$V_{IL}$

SDATA_OUT="L"

SYNC="L"

BIT_CLK
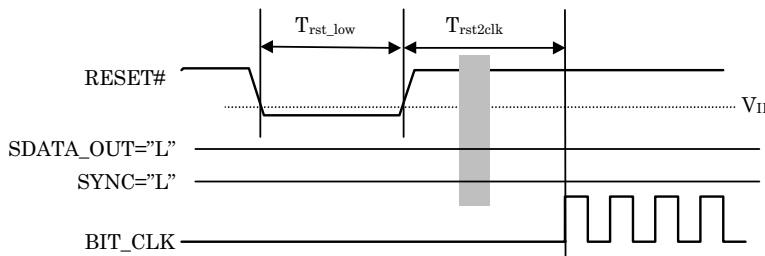
When the AK4543 is used under the multiple codec configuration and when cold reset is issued, all AK4543 connected to the AC-link will execute a cold reset concurrently.
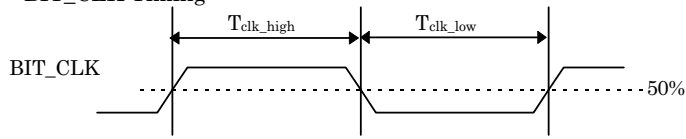
■Warm Reset

The AK4543 initiates a warm reset process by receiving a single pulse on the sync(Pin10). The AK4543 then clears PR4 bit and PR5 bit in the Powerdown Control Register. However, warm reset does not influence PR0~PR3 or PR6,7 bits in Powerdown Control Register(26h). Note that SYNC signal should synchronize with BIT_CLK after AK4543 starts to output BIT_CLK clock. And if an external clock is used, an external clock should be supplied before issuing a sync pulse for warm reset.

$T_{sync\_high}$     $T_{sync2clk}$
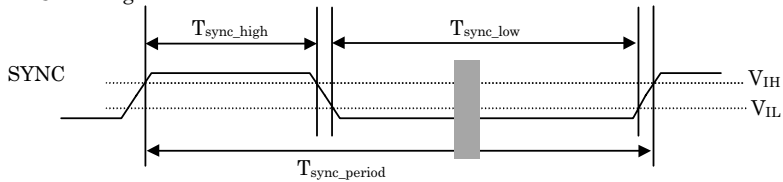
SYNC

$V_{IH}$
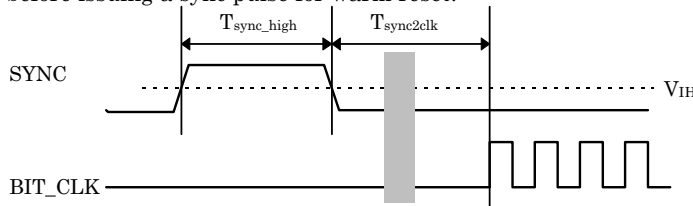
BIT_CLK

Please refer to Powerdown/Powerup sequence of multiple codec configuration on the warm reset when the AK4543 is used under the multiple codec configuration .(See page 24, 25)
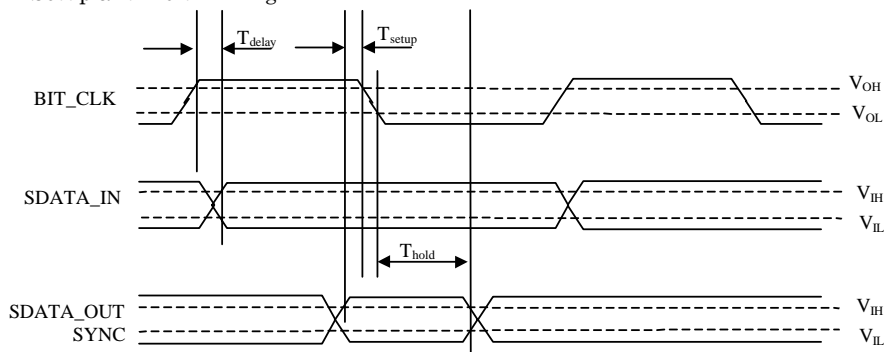
■BIT_CLK Timing

BIT_CLK

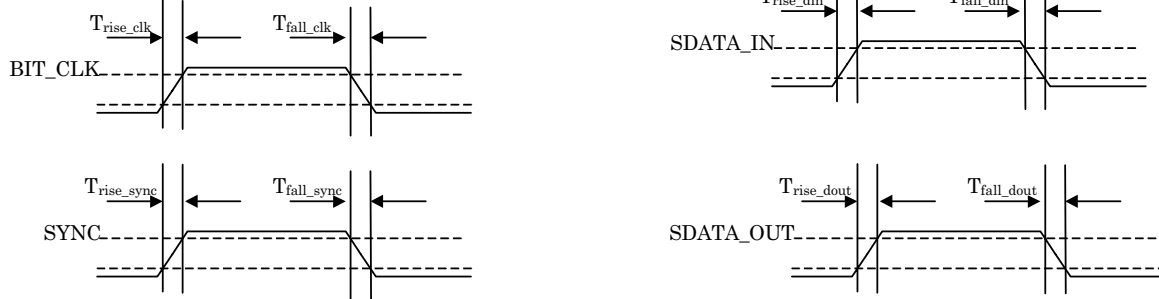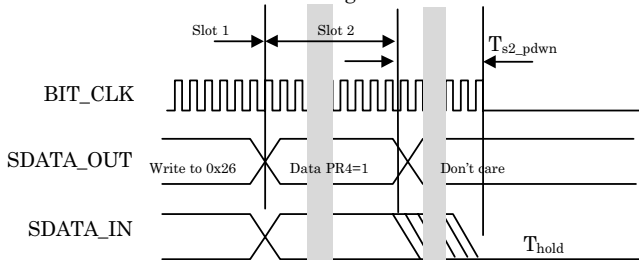$T_{clk\_high}$   $T_{clk\_low}$

50%

■SYNC Timing

SYNC

$T_{sync\_high}$   $T_{sync\_low}$

$V_{IH}$
$V_{IL}$

$T_{sync\_period}$

■Setup and Hold Timing

BIT_CLK

$T_{delay}$   $T_{setup}$

$V_{OH}$
$V_{OL}$

SDATA_IN

$V_{IH}$
$V_{IL}$

$T_{hold}$

SDATA_OUT
SYNC

$V_{IH}$
$V_{IL}$

■Signal Rise and Fall Times
(50pF external load : from 10%  90% of DVdd)

BIT_CLK

$T_{rise\_clk}$   $T_{fall\_clk}$

SDATA_IN

$T_{rise\_din}$   $T_{fall\_din}$

SYNC

$T_{rise\_sync}$   $T_{fall\_sync}$

SDATA_OUT

$T_{rise\_dout}$   $T_{fall\_dout}$

■AC-link Low Power Mode Timing

BIT_CLK

Slot 1   Slot 2   $T_{s2\_pdwn}$

SDATA_OUT

Write to 0x26   Data PR4=1   Don't care

SDATA_IN

$T_{hold}$

■Activate Test Mode

RESET# .......... $V_{IH}$

SDATA_OUT .......... $V_{IH}$

$T_{setup2rst}$

SDATA_IN
BIT_CLK

HI-Z

$T_{off}$

■AKM Test Mode

RESET# .......... $V_{IH}$

SDATA_OUT="L"

SYNC .......... $V_{IH}$

$T_{setup2rst}$
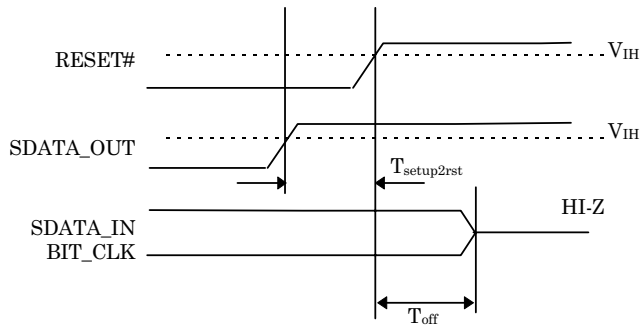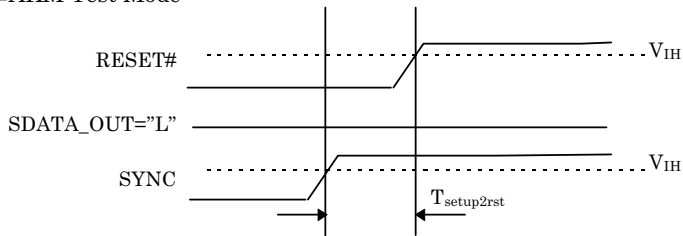
*Notes:[1]*
*1. All AC-link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the rising edge of RESET# causes the AK4543 AC-link outputs to go high impedance which is suitable for ATE in circuit testing.* Note that the AK4543 enters in the ATE test mode regardless SYNC is high or low.
2. Bringing both SYNC high and SDATA_OUT low for the rising edge of RESET# causes AKM test mode.
*3.* Once test modes have been entered, the only way to return to the normal operating state is to issue "cold reset" which issues RESET# with both SYNC and SDATA_OUT low.

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[1] All the following sentences written with small italic font in this document quote the AC'97 component specification.

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General Description

## ■AC '97 Connection to the Digital AC '97 controller

[2]*AC '97 communicates with its companion AC '97 controller via a digital serial link, "AC-link". All digital audio streams, and command/status information are communicated over this point to point serial interconnect. A breakout of the signals connecting the two is shown in the following figure.*

AC'97
Controller                                          AC'97

SYNC

BIT_CLK

SDATA_OUT

SDATA_IN

RESET#
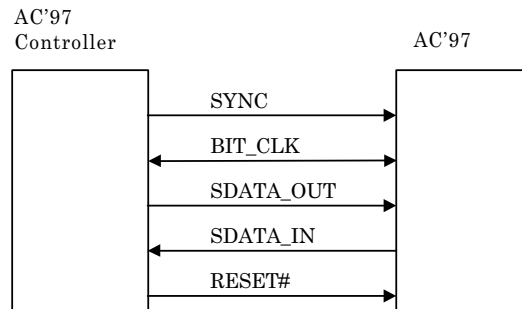
## ■AC'97 Digital Interface

*The AK4543 incorporates a 5 pin digital serial interface that links it to the AC '97 controller. AC-link is a bi-directional, fixed rate(48kHz), serial PCM digital stream. It handles multiple input, and output audio streams, as well as control register accesses employing a time division multiplexed (TDM) scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution. DAC and ADC resolution of the AK4543 is 18 bit resolution. The data streams currently defined by the AC '97 specification include:*

● *PCM Playback*                *2 output slots*
*2 channel composite PCM output stream*
● *PCM Record data*              *2 input slots*
*2 channel composite PCM input stream*
● *Control*                     *2 output slot*
*Control register write port*
● *Status*                      *2 input slots*
*Control register read port*

*SYNC, fixed at 48 KHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-link data, the AK4543 for outgoing data and AC '97 controller for incoming data, samples each serial bit on the falling edges of BIT_CLK.*
The AK4543 outputs BIT_CLK when it is assigned as Primary codec by the codec ID configuration ID1# and ID0#. The other hand, the AK4543 receives BIT_CLK when assigned as the Secondary codec from the Primary device.
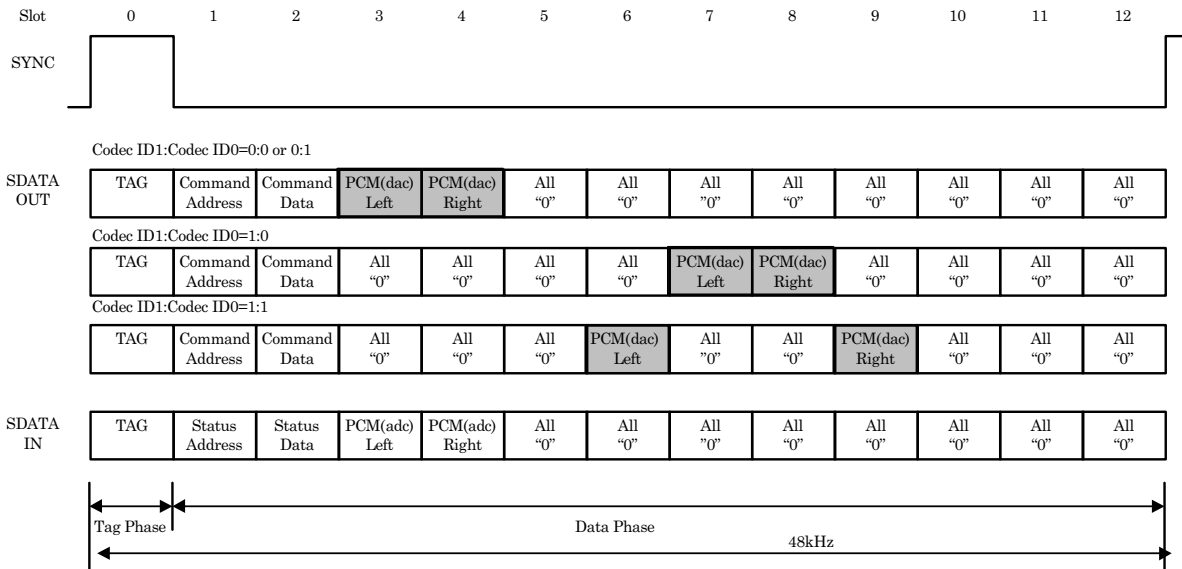*The AC-link protocol provides for a special 16-bit slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A "1" in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is "Tagged" invalid, it is the responsibility of the source of the data, (The AK4543 for the input stream, AC '97 controller for the output stream), to stuff all bit positions with 0's during that slot's active time.*
*SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the "Tag Phase". The remainder of the audio frame where SYNC is low is defined as the "Data Phase".*
Note that SDATA_OUT and SDATA_IN data is delayed one BIT_CLK because AC'97 controller causes SYNC signal high at a rising edge of BIT_CLK which initiates a frame.

"Output" stream means the direction from AC'97 controller to the AK4543, and "Input" stream means the direction from the AK4543 to AC'97 controller

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[2]All the following sentences written with small italic font in this document quote the AC'97 component specification.

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| Slot | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SYNC | | | | | | | | | | | | | |

Codec ID1:Codec ID0=0:0 or 0:1

| SDATA OUT | TAG | Command Address | Command Data | PCM(dac) Left | PCM(dac) Right | All "0" | All "0" | All "0" | All "0" | All "0" | All "0" | All "0" | All "0" |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Codec ID1:Codec ID0=1:0

| | TAG | Command Address | Command Data | All "0" | All "0" | All "0" | All "0" | PCM(dac) Left | PCM(dac) Right | All "0" | All "0" | All "0" | All "0" |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Codec ID1:Codec ID0=1:1

| | TAG | Command Address | Command Data | All "0" | All "0" | All "0" | PCM(dac) Left | All "0" | All "0" | PCM(dac) Right | All "0" | All "0" | All "0" |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

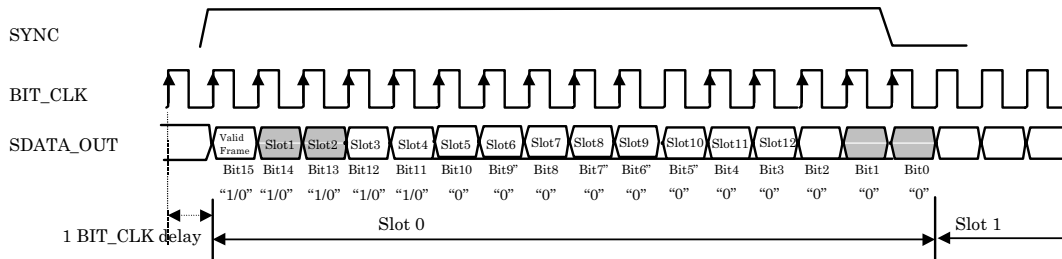| SDATA IN | TAG | Status Address | Status Data | PCM(adc) Left | PCM(adc) Right | All "0" | All "0" | All "0" | All "0" | All "0" | All "0" | All "0" | All "0" |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Tag Phase | Data Phase 48kHz

AC-link protocol identifies 13slots of data per frame. The frequency of sync is fixed to 48kHz. Only Slot 0, which is the Tag phase, is 16bits, all other slots are 20bits in length. These slots are explained in later sections.
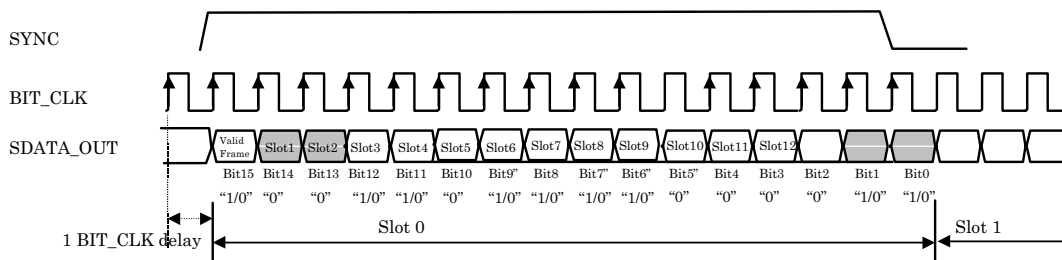
*AC-link Audio Output Frame (SDATA_OUT)*

a)Slot 0

Primary codec (Codec ID1: Codec ID0 = 0 : 0)

SYNC

BIT_CLK

SDATA_OUT | Valid Frame | Slot1 | Slot2 | Slot3 | Slot4 | Slot5 | Slot6 | Slot7 | Slot8 | Slot9 | Slot10 | Slot11 | Slot12

| Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| "1/0" | "1/0" | "1/0" | "1/0" | "1/0" | "0" | "0" | "0" | "0" | "0" | "0" | "0" | "0" | "0" | "0" | "0" |

1 BIT_CLK delay | Slot 0 | Slot 1

Secondary codec (Codec ID1 : Codec ID0 = 0 : 1 or 1 : 0 or 1 :1 )

SYNC

BIT_CLK

SDATA_OUT | Valid Frame | Slot1 | Slot2 | Slot3 | Slot4 | Slot5 | Slot6 | Slot7 | Slot8 | Slot9 | Slot10 | Slot11 | Slot12

| Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| "1/0" | "0" | "0" | "1/0" | "1/0" | "0" | "1/0" | "1/0" | "1/0" | "1/0" | "0" | "0" | "0" | "0" | "1/0" | "1/0" |

1 BIT_CLK delay | Slot 0 | Slot 1

The AK4543 checks bit15 (valid frame bit). Note that when the valid frame bit is "1", at least one bit14-6 (slot 1-9) or bit1-0 must be valid, bit5-2 will be "0"and should be ignored.
If bit15 is "0", the AK4543 ignores all following information in the frame.
The AK4543 then checks the validity of each bit in the TAG phase (slot 0).
If each bit is "0", the AK4543 ignores the slot indicated by "0". On the other hand, if each bit is "1", the slot is valid.
All bits in slot10-12(bit5-3) are "0" and bit2 is also "0".
The AK4543 monitors bit1 and 0, which are codec ID configuration bits used in multiple codec implementations.
These bits are used to identify which codec the frame data is issued to.

When codec ID configuration bits1 and 0 which are set by the codec ID configuration 45/46 strapping pins(codec ID0# and ID1#) are set to zero(00), the frame is aimed for the Primary codec. And when codec ID configuration bit1 and 0 are set to non-zero values(01, 10, or 11), the frame is meant for Secondary codec.

*A new audio output frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the AK4543 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AC '97 controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AK4543 on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.*

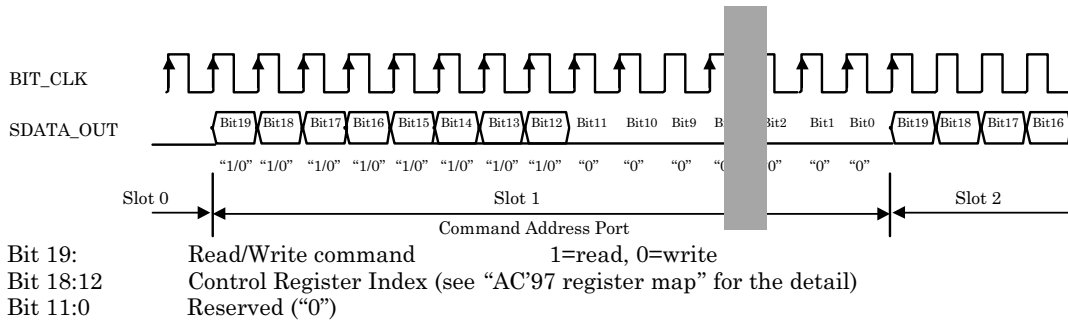Data should be sent to the AC'97 codec with MSB first through the Pin labled SDATA_OUT.

The following table shows the relationship of bits14&13 and the Read/Write operations depending on codec ID configuration.

| Bit 15 Valid Frame | Bit 14: Slot1 Valid Bit (Command Address) | Bit 13: Slot 2 Valid Bit (Command Data) | Read/Write Operation of Primary AK4543 | Read/Wirte Operation of Secondary AK4543 |
|---|---|---|---|---|
| 1 | 1 | 1 | Read/Write(Normal Operation) | Ignore |
| 1 | 0 | 1 | Ignore | Ignore |
| 1 | 1 | 0 | Read: Normal Operation Write: Ignore | Ignore |
| 1 | 0 | 0 | Ignore | Read/Write(Normal Operation) |

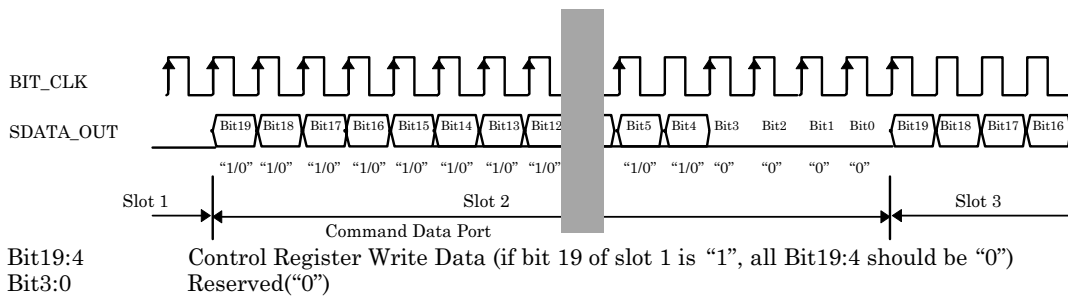AK4543 Addressing: Slot0 Tag Bits

b)Slot1:Command Address Port
Slot1 gives the address of the command data, which is given in the slot 2. The AK4543 has 20 valid registers of 16bit data. See Page17(See AC'97 register map).



| Bit 19: | Read/Write command | 1=read, 0=write |
| Bit 18:12 | Control Register Index (see "AC'97 register map" for the detail) |
| Bit 11:0 | Reserved ("0") |

Bit18 is equivalent to the most significant bit of the index register address.
The AK4543 ignores from bit11 to bit0. These bits will be reserved for future enhancement and must be stuffed with 0's by the AC'97 controller.

c)Slot2:Command Data Port



| Bit19:4 | Control Register Write Data (if bit 19 of slot 1 is "1", all Bit19:4 should be "0") |
| Bit3:0 | Reserved("0") |

If bit19 in slot1 is "0", a write command, the AC'97 controller must output Command Data Port data in slot 2 *of the same frame*. If the bit19 in slot1 is "1", a read, the AK4543 will ignore any Command Data Port data in slot2.

Bit19 is equivalent to D15 bit of mixer register value.

d)Slot3 PCM Playback Left Channel (18bits)
In the case of codec ID1:codec ID0=0:0 or 0:1, the AK4543 uses the playback(DAC) data format in slot3 for left channel.
Playback data format is 18bits MSB first 2's complement. The AC'97 controller should stuff bits1-0 with "0". If valid bit (slot3) in the slot 0 is invalid ("0"), the AK4543 interprets the data as all "0".
Bit19:2          Playback data
Bit 1:0          "0"

e)Slot4 PCM Playback Right Channel (18bits)
In the case of codec ID1:codec ID0=0:0 or 0:1, the AK4543 uses the playback(DAC) data format in the slot4 for right channel. Playback data format is MSB first. Data format is 18bits 2's complement. The AC'97 controller should stuff bits1-0 with "0". If valid bit (slot 4) in the slot 0 is invalid ("0"), the AK4543 interprets the data as all "0".
Bit19:2          Playback data
Bit 1:0          "0"

f)Slot5 is Not used in the AK4543
The AK4543 will ignore stuffed in this slot.

g)Slot6 PCM Playback Left Channel (18bits)
In case of codec ID1:codec ID0=1:1, the AK4543 uses the playback(DAC) data in slot 6 for left channel.
Playback data format is 18bits MSB first 2's complement. The AC'97 controller should stuff bit1-0 with "0". If valid bit (slot6) in the slot 0 is invalid ("0"), the AK4543 interprets the data as all "0".
Bit19:2          Playback data
Bit 1:0          "0"

h)Slot7 PCM Playback Left Channel (18bits)
In case of codec ID1:codec ID0=1:0, the AK4543 uses the playback(DAC) data in slot7 for left channel.
Playback data format is 18bits MSB first 2's complement. The AC'97 controller should stuff bit1-0 with "0". If valid bit (slot7) in the slot 0 is invalid ("0"), the AK4543 interprets the data as all "0".
Bit19:2          Playback data
Bit 1:0          "0"

i)Slot8 PCM Playback Right Channel (18bits)
In case of codec ID1:codec ID0=1:0, the AK4543 uses the playback(DAC) data in slot8 for right channel.
Playback data format is 18bits MSB first 2's complement. The AC'97 controller should stuff bit1-0 with "0". If valid bit (slot8) in the slot 0 is invalid ("0"), the AK4543 interprets the data as all "0".
Bit19:2          Playback data
Bit 1:0          "0"

j)Slot9 PCM Playback Right Channel (18bits)
In case of codec ID1:codec ID0=1:1, the AK4543 uses the playback(DAC) data in slot 9 for right channel.
Playback data format is 18bits MSB first 2's complement. The AC'97 controller should stuff bit1-0 with "0". If valid bit (slot9) in the slot 0 is invalid ("0"), the AK4543 interprets the data as all "0".
Bit19:2          Playback data
Bit 1:0          "0"

k)Slot10-12 is Not used in the AK4543
The AK4543 will ignore stuffed in these data slots.

■AC-link Input Frame(SDATA_IN)
  Each AC-link frame consists of one 16bit tag phase and twelve 20bit slots used for data and control.

a)Slot0
Slot0 is a special frame, and consists of 16bit s. Slot0 is also called the "Tag phase". The AK4543 supports bits 15-11 and bits1-0. Each bit indicates "1"=valid(normal operation) or ready, "0"=invalid(abnormal operation) or not ready.
 If the first bit in the slot 0 is valid, the AK4543 is ready for normal operation. [3]If the "Codec Ready" bit is invalid, the following bits and remaining slots are all "0". The AC'97 controller should ignore the following bits in the slot 0 and all other slots.
Bit 14 means that Slot 1(Status Address) output is valid or invalid. And Bit 13 means that Slot 2(Status Data ) is valid or invalid.
The following table shows the relationship between Bit 14,13 and each Status of the AK4543.

| Bit 15 (Codec Ready) | Bit 14 (Status Address) | Bit 13 (Status Data) | Status |
|---|---|---|---|
| 1 | 1 | 1 | There is a Read Command in the previous frame. Then both Slot 1 and Slot 2 output normal data. If the access to non-implemented register or odd register is requested, the AK4543 returns "valid 7-bit register address in slot 1 and returns "valid"0000h data in slot 2 on the next AC-link frame. |
| 1 | 1 | 0 | Prohibited or non-existing |
| 1 | 0 | 0 | There is no Read Command in the previous frame. Both Slot 1 and Slot 2 output All"0". |
| 1 | 0 | 1 | Prohibited or non-existing |

Note    1). The above Read sequence is done as response for previous frames read command. That is, if the previous frame is a Write Command, AK4543 outputs bit1 4 ="0", bit13 ="0" and slot 1&2 = All"0".

Bit12 means the output of Slot 3(PCM(ADC) Left) is valid or invalid. And Bit 11 means the output of Slot 4(PCM(ADC)Left) is valid or invalid.  Bits10-0 are filled with "0".

*A new audio input frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the AK4543 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AK4543 transitions SDATA_IN into the first bit position of slot 0 ("Codec Ready" bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AC'97 controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.*
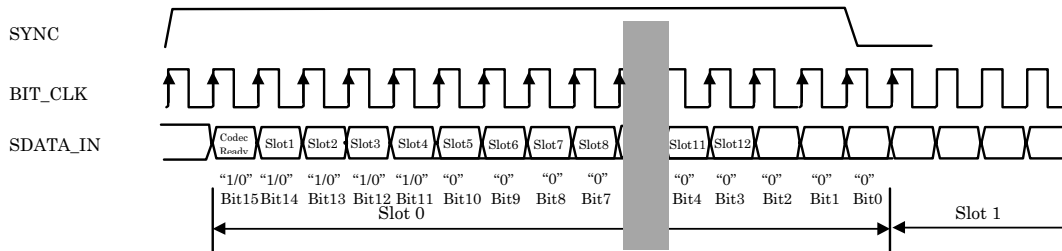


b)Slot1        Status Address Port
*Audio input frame slot1's stream echoes the control register index, for historical reference, for the data to be returned in slot2. (Assuming that slots1 valid bit and slot2 valid bit in the slot0 had been tagged "valid" by the AK4543)*



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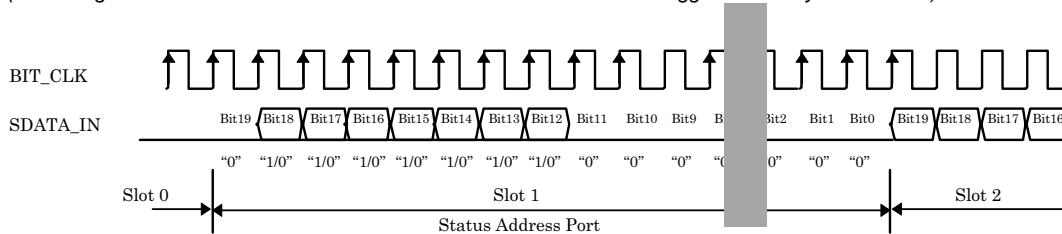
[3] When the AC'97 is not ready for normal operation, output bits are not specified in this documents and should be considered as invalid.

This address shows the register index for which data is being returned in the slot2.
This address port is a copy of slot1 of the output frame, and index address input to SDATA_OUT is loop ed back to the AC'97 controller through SDATA_IN.  This allows the controller to insure the AK4543 receives the correct data.


c)Slot2:  Status Data Port
Status data addressed by the command address port of Output Stream is output through SDATA_IN pin.
Bit19:4          Control Register Read Data (the contents of indexed address in the slot 1)
Bit3:0          "0"


Note that the address of Status Data Port data is consistent with Status Address Port data of slot 1 *in the same frame*.  If the read operation is issued in the frame N by the AC'97 controller, Status Data Port data is output through SDATA_IN in the frame N+1. Note that data is only available in this frame, only one time and that the following frames are invalid if another read operation is not issued.

d)Slot3: PCM Record Left Channel
Record(ADC) data format is 18bits MSB first 2's complement.  Lower 2bits of the frame are ignored.   If ADC block is powered down, slot-3 valid bit in the slot 0 is invalid ("0"), and data is as all "0".

Bit19:2          Audio ADC left channel output
Bit1:0          "0"


e)Slot4: PCM Record Right Channel
Record(ADC) data format is 18bits MSB first 2's complement.  Lower 2bits of the frame are ignored.  If ADC block is powered down, slot-4 valid bit in the slot 0 is invalid ("0"), and data is as all "0".
Bit19:2          Audio ADC right channel output
Bit1:0          "0"


f)Slot5: Modem Line Codec
The AK4543 does not incorporate the modem codec, all bits are stuffed with "0" in this slot.
Bit19:0          "0"


g)Slot6: Microphone Record Data
The AK4543 does not incorporate the 3rd ADC for microphone, all bits are stuffed with "0" in this slot.
Bit19:0          "0"


h)Slots7-12          Reserved for future enhancement
Bits19:0          "0"

■AC'97 Register Map

Each Register is a 16bit word.

Note: The AK4543 outputs "valid" 0000h if the controller reads an unused or invalid register address.

| Reg Num | Name | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00h | Reset | 0 | "0" | "1" | "0" | "1" | "1" | "0" | "1" | "0" | "1" | "0" | "1" | "0" | "0" | "0" | "0" | 2D50h |
| 02h | Master Volume | Mute | X | ML5 | ML4 | ML3 | ML2 | ML1 | ML0 | X | X | MR5 | MR4 | MR3 | MR2 | MR1 | MR0 | 8000h |
| 04 | LINVL Volume | Mute | X | ML5 | ML4 | ML3 | ML2 | ML1 | ML0 | X | X | MR5 | MR4 | MR3 | MR2 | MR1 | MR0 | 8000h |
| 06h | Master Volume Mono | Mute | X | X | X | X | X | X | X | X | X | MR5 | MR4 | MR3 | MR2 | MR1 | MR0 | 8000h |
| 0Ah | PC_BEEP Volume | Mute | X | X | X | X | X | X | X | X | X | X | PV3 | PV2 | PV1 | PV0 | X | 0000h |
| 0Ch | Phone Volume | Mute | X | X | X | X | X | X | X | X | X | X | GN4 | GN3 | GN2 | GN1 | GN0 | 8008h |
| 0Eh | Mic Volume | Mute | X | X | X | X | X | X | X | X | 20dB | X | GN4 | GN3 | GN2 | GN1 | GN0 | 8008h |
| 10h | Line In Volume | Mute | X | X | GL4 | GL3 | GL2 | GL1 | GL0 | X | X | X | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |
| 12h | CD Volume | Mute | X | X | GL4 | GL3 | GL2 | GL1 | GL0 | X | X | X | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |
| 14h | Video Volume | Mute | X | X | GL4 | GL3 | GL2 | GL1 | GL0 | X | X | X | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |
| 16h | Aux Volume | Mute | X | X | GL4 | GL3 | GL2 | GL1 | GL0 | X | X | X | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |
| 18h | PCM Out Volume | Mute | X | X | GL4 | GL3 | GL2 | GL1 | GL0 | X | X | X | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h |
| 1Ah | Record Select | X | X | X | X | X | SL2 | SL1 | SL0 | X | X | X | X | X | SR2 | SR1 | SR0 | 0000h |
| 1Ch | Record Gain | Mute | X | X | X | GL3 | GL2 | GL1 | GL0 | X | X | X | X | GR3 | GR2 | GR1 | GR0 | 8000h |
| 20h | General Purpose | POP | X | 3D | X | X | X | MIX | MS | LPBK | X | X | X | X | X | X | X | 0000h |
| 22h | 3D Control | X | X | X | X | X | X | X | X | X | X | X | X | X | X | DP1 | DP0 | 0000h |
| 26h | Powerdown Ctrl/Stat | PR7 | PR6 | PR5 | PR4 | PR3 | PR2 | PR1 | PR0 | X | X | X | X | REF | ANL | DAC | ADC | na |
| 28h | Extended Audio ID | ID1 | ID0 | X | X | X | X | AMAP | X | X | X | X | X | X | X | X | X | x200h |
| 7Ch | Vendor ID1 | "0" | "1" | "0" | "0" | "0" | "0" | "0" | "1" | "0" | "1" | "0" | "0" | "1" | "0" | "1" | "1" | 414Bh |
| 7Eh | Vendor ID2 | "0" | "1" | "0" | "0" | "1" | "1" | "0" | "1" | "0" | "0" | "0" | "0" | "0" | "0" | "1" | "0" | 4D02h |

*) Vender ID of AKM is "AKM" :This ID has been approved by Intel.

*) The AK4543 outputs "X" bits as "0".

*) A write on "Invalid" registers will not affect the operation of the AK4543.

*) ANL, DAC, ADC Bit in register 26h are all "0" following cold reset. When each section is ready for normal operation, the coresponding bit becomes "1". The Powerdown register(26h) is not affected by a write to Reset register(0h). See "Mixer Registers" in AC'97 specification for details. Vref is controlled only by PR3.

■Reset Register (Index 00h)

<Write>

When any value is written to this register, all registers in the AK4543 except for register "26h" Powerdown Ctrl/Stat Register are reset to the default values. The value of this register is not altered.

<Read>

Reading this register returns "2D50h"composed of the ID code of the part, a code for the type of 3D enhancement, 18 bit ADC/DAC resolution, and a code for True Line Level Out.

*Setting D14 – D10 "01011" means AKM 3D enhancement which is registered in Audio Codec '97 Component Specification Rev 1.03 and 2.1 .

*Setting D8 "1" indicates 18bit ADC resolution and D6"1" does DAC resolution.

*Setting D4 "1" means True Line Level Out is supported with Volume Control(Index 04h).

■ Play Master Volume Registers (Index 02h ,06h) and LINVL(True Line Level Out) Volume Register(Index 04h)

The following table shows the relationship between bits and the attenuation value with step size of 1.5dB. The AK4543 has a range of 0dB to –46.5dB. The AK4543 does not support the optional MX5 bit.

**The AK4543** detect**s** when MX5 is set and set all 5 LSBs to 1s. Example: When the driver writes a "01xxxxx" the AK4543 interpret that as "0011111". When this register is read, the returned value is "0011111".

| Mute | MX5 | MX4 | MX3 | MX2 | MX1 | MX0 | Att. |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0dB |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | -1.5dB |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | -3.0dB |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | -4.5dB |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | -45.0dB |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | -46.5dB |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 1 | X | X | X | X | X | -46.5dB |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | X | X | X | X | X | X | Mute |

■ PC Beep Register (Index 0Ah)

The following table shows the relationship between bits and the attenuation value.   The attenuation step is -3dB with a range of 0 to –45dB.  PC_BEEP of the AK4543 is mute off at default state.

*The PC Beep is routed to L & R Line outputs directly when AK4543 is in a RESET State(Reset# is "L").  This is so that Power on Self Test(POST) codes can be heard by the user in case of a hardware problem with the PC. After Reset# goes "H", direct PC beep pass thru becomes OFF.*

| Mute | PV3 | PV2 | PV1 | PV0 | Att. |
|------|-----|-----|-----|-----|------|
| 0 | 0 | 0 | 0 | 0 | 0dB |
| 0 | 0 | 0 | 0 | 1 | -3.0dB |
| 0 | 0 | 0 | 1 | 0 | -6.0dB |
| ----- | ----- | ----- | ----- | ----- | ----- |
| 0 | 1 | 1 | 1 | 1 | -45.0dB |
| 1 | X | X | X | X | Mute |

■ Analog Mixer Input Gain Registers (Index 0Ch-18h)

The following table shows the relationship between bits and the gain/attenuation value.  Attenuation step is 1.5dB with a range of +12dB to –34.5dB.

| Mute | Gx4 | Gx3 | Gx2 | Gx1 | Gx0 | Att. |
|------|-----|-----|-----|-----|-----|------|
| 0 | 0 | 0 | 0 | 0 | 0 | +12dB |
| 0 | 0 | 0 | 0 | 0 | 1 | +10.5dB |
| ----- | ----- | ----- | ----- | ----- | ----- | ----- |
| 0 | 0 | 1 | 0 | 0 | 0 | 0dB |
| 0 | 0 | 1 | 0 | 0 | 1 | -1.5dB |
| ----- | ----- | ----- | ----- | ----- | ----- | ----- |
| 0 | 1 | 1 | 1 | 1 | 0 | -33.0dB |
| 0 | 1 | 1 | 1 | 1 | 1 | -34.5dB |
| 1 | X | X | X | X | X | Mute |

■ Record Select Control Register (Index 1Ah)

| SR2 | SR1 | SR0 | Att. |
|-----|-----|-----|------|
| 0 | 0 | 0 | Mic |
| 0 | 0 | 1 | CD In (R) |
| 0 | 1 | 0 | Video In (R) |
| 0 | 1 | 1 | Aux In (R) |
| 1 | 0 | 0 | Line In (R) |
| 1 | 0 | 1 | Stereo Mix (R) |
| 1 | 1 | 0 | Mono Mix |
| 1 | 1 | 1 | Phone |

| SR2 | SL1 | SL0 | Att. |
|-----|-----|-----|------|
| 0 | 0 | 0 | Mic |
| 0 | 0 | 1 | CD In (L) |
| 0 | 1 | 0 | Video In (L) |
| 0 | 1 | 1 | Aux In (L) |
| 1 | 0 | 0 | Line In (L) |
| 1 | 0 | 1 | Stereo Mix (L) |
| 1 | 1 | 0 | Mono Mix |
| 1 | 1 | 1 | Phone |

■ Record Gain Register (Index 1Ch)

| Mute | Gx3 | Gx2 | Gx1 | Gx0 | Gain |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0dB |
| 0 | 0 | 0 | 0 | 1 | 1.5dB |
| 0 | 0 | 0 | 1 | 0 | 3.0dB |
| -------- | -------- | -------- | -------- | -------- | -------- |
| 0 | 1 | 1 | 1 | 1 | 22.5dB |
| 1 | X | X | X | X | Mute |

■ General Purpose Register (Index 20h)

The following table indicates how to control several miscellaneous functions of the AK4543.

| | Bit | Function |
|---|---|---|
| POP | D15 | PCM(DAC) Bypass 3D |
| | | 0= Via 3D Path, 1= 3D Bypass |
| 3D | D13 | 3D Stereo Enhancement |
| | | 0=Off, 1=On |
| MIX | D9 | Mono Output Select |
| | | 0=Mix, 1=Mic |
| MS | D8 | Mic Select |
| | | 0=Mic1, 1 =Mic2 |
| LPBK | D7 | ADC/DAC Loopback Mode |
| | | 1= Loopback |

An active bit("1") in D15(POP) will pass DAC output to Line_OUT or LNLVL_OUT directly, while a "0" in D15 will put DAC output into Input Mixers or AKM's 3D enhancement circuit.

D13(3D) will activate the AKM's 3D enhancement.

LPBK(ADC/DAC Loopback Mode) bit enables loopback of the ADC output to slot3 &4 of DAC input for both the Primary codec and Secondary codec on the same AC-Link Generally done for system testing.

■ 3D Control Register (Index 22h)

The following table shows the relationship between the bit and depth of 3D enhancement.

| DP1 | DP0 | Depth | Recommended Application |
|---|---|---|---|
| 0 | 0 | 0% | Off |
| 0 | 1 | 50% | Audio |
| 1 | 0 | 70% | Audio |
| 1 | 1 | 100% | Game |

■ Powerdown Control/Status Register (Index 26h)

BitsD0 to D3 are read only status bits. Any write to these bits will not affect the operation of the AK4543. These bits are used as status bits to subsections of the AC'97 codec. A "1" indicates the subsection of the AK4543 is "ready" or that is capable of performing in normal operation.

|  | Bit | Function |
|---|---|---|
| REF | D3 | Vref up to nominal state<br>0=NOT ready, 1=ready, |
| ANL | D2 | Analog mixers, etc ready<br>0=NOT ready, 1=ready |
| DAC | D1 | DAC section ready to accept data<br>0=NOT ready, 1=ready |
| ADC | D0 | ADC section ready to transmit data<br>0=NOT ready, 1=ready |

The power down modes are as follows.

|  | Bit | Function |
|---|---|---|
| PR0 | D8 | PCM in ADC's & Input Mux Powerdown |
| PR1 | D9 | PCM out DACs Powerdown |
| PR2 | D10 | Analog Mixer Powerdown (Vref still on) |
| PR3 | D11 | Analog Mixer Powerdown (Vref off) |
| PR4 | D12 | Digital Interface (AC-link) Powerdown |
| PR5 | D13 | Internal Clk disable |
| PR6 | D14 | True Line Level Out Powerdown |
| PR7 | D15 | EAPD(External Amplifier Powerdown) |

When PR3 is set to "1", the ADC, DAC, Mixer, True Line Level Out, and VREF are powered down even if any PRx bit are "0". When PR3 bit is reset to "0", the AK4543 resumes the previous state by referencing previous PRx bit. In this case, the AK4543 outputs corresponding slot-x valid bits in the slot 0 as "0" until the AK4543 results in normal operation(Codec Ready).

EAPD(External Amplifier Power Down) bit controls an external audio amplifier. EAPD="0" places a "0"(L) on the output pin, enabling an external audio amplifier, EAPD="1"(H) shuts it down. Powered up default is EAPD="0"(external audio amplifier enabled).

■ Extended Audio ID(Index 28h)

The Extended Audio ID(28h) is a read only register. 2bits D15&D14 can be read for codec identification. D15 ,14 are automatically set with the codec ID1#(46pin) and ID0#(45pin). ID1# and ID0# can be strapped and adopt inverted polarity and default to 00=Primary(via internal pull up) when left floating. Depended on codec ID configuration, the AK4543 is assigned to Primary codec or Secondary codec. Note that codec ID configuration has to be fixed before Powering up of the device.

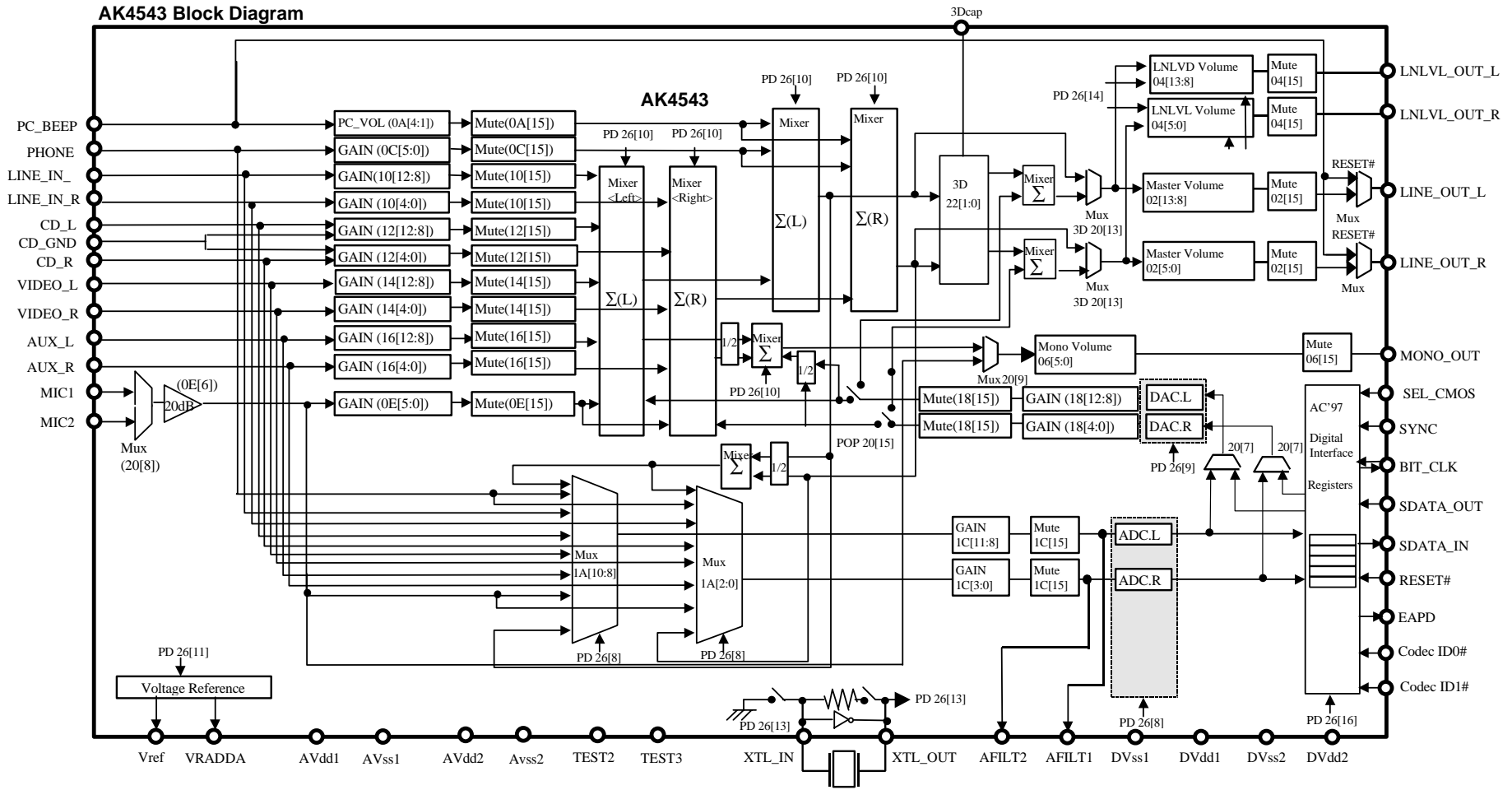| ID1#(pin 46) | | ID0#(pin45) | | Configuration<br>(Codec ID) |
|---|---|---|---|---|
| Physical<br>Connection | Logic<br>Value | Physical<br>Connection | Logic<br>Value |  |
| NC | 0 | NC | 0 | Primary    ID00 |
| NC | 0 | GND | 1 | Secondary ID01 |
| GND | 1 | NC | 0 | Secondary ID10 |
| GND | 1 | GND | 1 | Secondary ID11 |

The AMAP (bit D9 of this read only register) will always be set to "1" indicating that DAC input slot will follow to AC'97 recommendation as shown in next table.(CODEC ID is configured via ID1#m ID0# pins)
The audio DAC mapping can be changed based on the codec ID configuration.

| Codec ID | AC-link Frame Data used for DACs | | Comments |
|---|---|---|---|
|  | PCM Left DAC uses<br>data from Slot# | PCM Right DAC<br>uses data from Slot# | Expected use |
| 00 | 3 | 4 | Original Definition(Master) |
| 01 | 3 | 4 | Original Definition(Docking) |
| 10 | 7 | 8 | Left/Right surround channels |
| 11 | 6 | 9 | Center/LFE channels |

■ Vendor ID Registers (Index 7Ch, 7Eh)

*This register is a read only register that is used to determine the specific vendor identification. The ID method is Microsoft Plug and Play Vendor ID code with upper byte of 7Ch register, the first character of that id, lower byte of 7Ch register, the second character and upper byte of 7Eh register  the third character. These three characters are ASCII encoded. Lower byte of 7E register is for the Vendor Revision number.*

AKM's  vender ID is "AKM", and revision number is 02.  As ASCII code "A" is 41h, "K" is 4Bh, and "M" is 4Dh, Vendor ID registers are 414Bh and 4D02h respectively.

**AK4543 Block Diagram**

**AK4543**

3Dcap

Left side inputs:
- PC_BEEP
- PHONE
- LINE_IN_
- LINE_IN_R
- CD_L
- CD_GND
- CD_R
- VIDEO_L
- VIDEO_R
- AUX_L
- AUX_R
- MIC1
- MIC2

Right side outputs:
- LNLVL_OUT_L
- LNLVL_OUT_R
- LINE_OUT_L
- LINE_OUT_R
- MONO_OUT
- SEL_CMOS
- SYNC
- BIT_CLK
- SDATA_OUT
- SDATA_IN
- RESET#
- EAPD
- Codec ID0#
- Codec ID1#

Blocks:
- PC_VOL (0A[4:1])  Mute(0A[15])
- GAIN (0C[5:0])  Mute(0C[15])
- GAIN (10[12:8])  Mute(10[15])
- GAIN (10[4:0])  Mute(10[15])
- GAIN (12[12:8])  Mute(12[15])
- GAIN (12[4:0])  Mute(12[15])
- GAIN (14[12:8])  Mute(14[15])
- GAIN (14[4:0])  Mute(14[15])
- GAIN (16[12:8])  Mute(16[15])
- GAIN (16[4:0])  Mute(16[15])
- GAIN (0E[5:0])  Mute(0E[15])

Mux (20[8])
(0E[6]) 20dB

Mixer <Left>  Mixer <Right>
$\Sigma$(L)  $\Sigma$(R)

Mixer  Mixer  PD 26[10]
$\Sigma$(L)  $\Sigma$(R)

3D 22[1:0]

Mixer $\Sigma$  Mux 3D 20[13]
Mixer $\Sigma$  Mux 3D 20[13]

LNLVD Volume 04[13:8]  Mute 04[15]
PD 26[14]  LNLVL Volume 04[5:0]  Mute 04[15]

Master Volume 02[13:8]  Mute 02[15]  RESET#  Mux
Master Volume 02[5:0]  Mute 02[15]  RESET#  Mux

1/2  Mixer $\Sigma$  1/2  Mux 20[9]  Mono Volume 06[5:0]  Mute 06[15]
PD 26[10]

Mute(18[15])  GAIN (18[12:8])  DAC.L
Mute(18[15])  GAIN (18[4:0])  DAC.R
PD 26[9]

POP 20[15]

Mixer $\Sigma$  1/2

20[7]  20[7]

AC'97 Digital Interface Registers

GAIN 1C[11:8]  Mute 1C[15]  ADC.L
GAIN 1C[3:0]  Mute 1C[15]  ADC.R

Mux 1A[10:8]  Mux 1A[2:0]
PD 26[8]  PD 26[8]

PD 26[11]
Voltage Reference

PD 26[13]  PD 26[13]

PD 26[8]  PD 26[16]

Bottom pins:
Vref  VRADDA  AVdd1  AVss1  AVdd2  Avss2  TEST2  TEST3  XTL_IN  XTL_OUT  AFILT2  AFILT1  DVss1  DVdd1  DVss2  DVdd2

■Power Management/Low Power Modes
*The AK4543 is capable of operating at multiple reduced power modes for when no activity is required. The state of power down is controlled by the Powerdown Register (26h). There are 8 separate commands for power down. See the table below for the different modes. As the AK4543 operates at static mode, the registers will not lose their values even if the master clock is stopped only upon power.*

Powerdown Mode Truth Table

|  | ADC | DAC | Mixer | VREF | ACLINK | Internal CLK | LNLVL_OUT | EAPD |
|---|---|---|---|---|---|---|---|---|
| PR0="1" | PD | don't care | don't care | don't care | Don't care | don't care | don't care | don't care |
| PR1="1" | don't care | PD | don't care | don't care | Don't care | don't care | don't care | don't care |
| PR2="1" | don't care | don't care (No DAC out) | PD | don't care | Don't care | don't care | PD | don't care |
| PR3="1" | PD | PD | PD | PD | Don't care | don't care | PD | don't care |
| PR4="1" | PD | PD | don't care | don't care | PD | don't care | don't care | don't care |
| PR5="1" | PD | PD | don't care | don't care | PD | PD | don't care | don't care |
| PR6="1" | don't care | don't care | don't care | don't care | Don't care | don't care | PD | don't care |
| PR7="1" | don't care | don't care | don't care | don't care | Don't care | don't care | don't care | PD |

*: PD means Powerdown .
*: No DAC out means that there is no PCM out because mixer is disabled.*

*From normal operation sequential writes to the Powerdown Register are performed to power down subsections of the AK4543 one at a time. After everything has been shut off, a final write (of PR4) can be executed to shut down the AC '97 digital interface (AC-link). The part will remain in sleep mode with all its registers holding their static values. To wake up, the AC '97 controller will send a pulse on the sync line issuing a warm reset. This will restart the AK4543 digital (resetting PR4 to zero). The AK4543 can also be woken up with a cold reset. A cold reset will cause a loss of values of the registers as a cold reset will set them to their default states. When a subsection is powered back on the Powerdown Control/Status register (index 26h) should be read to verify that the section is ready (i.e. stable) before attempting any operation that requires its normal operation.*

*And the below figure illustrates one example of procedure to do a complete  powerdown/power up of AK4543.*
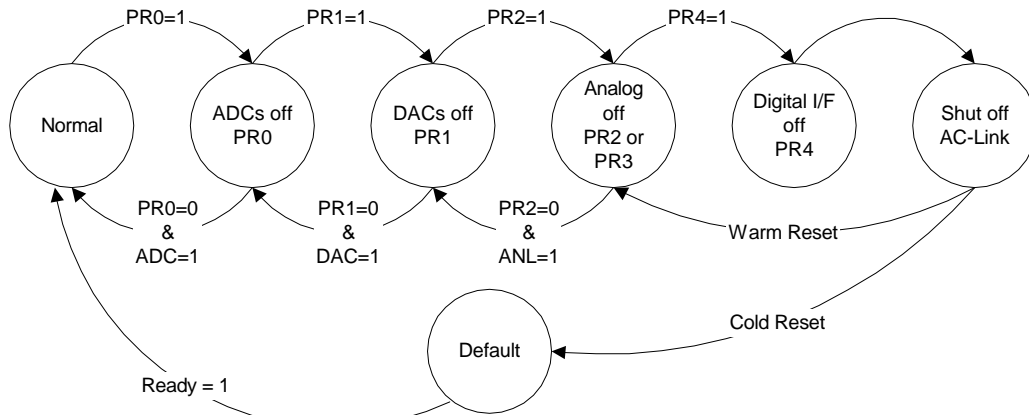


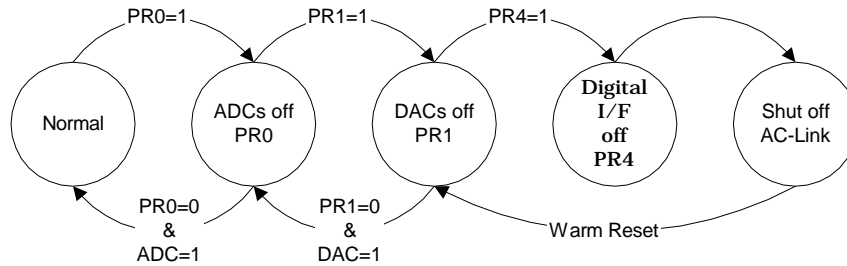One example of AK4543 Powerdown/Powerup flow

When PR3 bit is set to "1", the ADC, DAC, Mixer, True Line Level Out, and VREF will be powered down even if any PRx bits are "0".  When PR3 bit is reset to "0", the AK4543 resumes with the previous state by referencing PRx bit. In this case, the AK4543 outputs "0" (invalid) for  corresponding slot-x valid bits in the slot 0 until  the corresponding block of the AK4543 is operating with normal operation.
Setting the PR4 bit causes the Powerdown mode of AK4543 and AC-Link of AK4543 shut down. In this case, when Warm Reset is executed,  PR4 bit is cleared and the AC-Link is reactivated. A cold reset is issued , the AK4543 is restored to operation with the default register settings.
In addition, setting PR5 bit causes the Powerdown mode of AK4543 and the internal clock of AK4543 to be stopped. When a warm reset is done in this case, PR5 bit is cleared to 0 and internal clock and AC-Link are reactivated. When Cold reset is executed, AK4543 is set up to the operation with default register setting, no  powerdown modes active.

The next figure illustrates a  state when all the mixers should work with the static volume settings that are contained in their associated registers.  This is used when the user  is playing a CD (or external LINE_IN source) through the AC '97 codec to the speakers but has most of the system in  a low power mode.  The procedure for this follows the previous except that the analog mixer is never shut down.



*AK4543 Powerdown/Powerup flow with analog still alive*

■Powerdown/Powerup sequence of multiple codec configuration

*There can be up to 4 Codecs on the extended AC-link. Multiple Codec AC-link implementations must run off a common BIT_CLK. The Primary Codec generates the master AC-link BIT_CLK for both the AC  '97 Digital Controller and any Secondary  Codecs. The AK4543 may be used as a master or slave in any systems using more than one codec.*
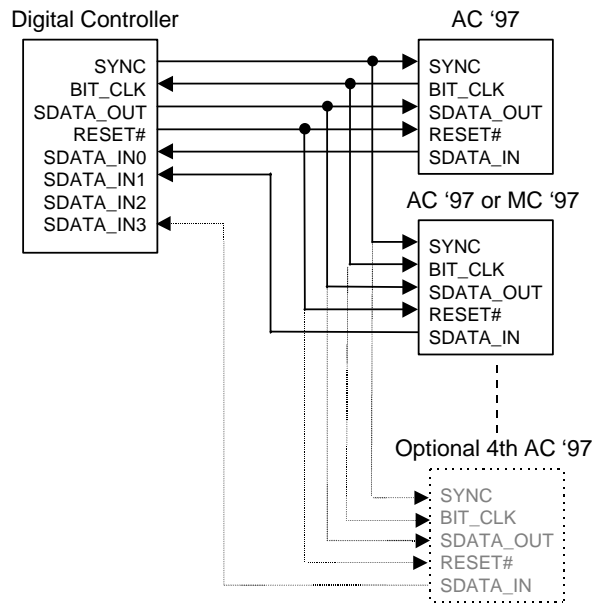


*Multiple Codec Example*

Under the multiple codec circumstances, there is no restriction on setting PR0(ADC), PR1(DAC), PR2(Mixer), PR6(LNLVL_OUT) and PR7(EAPD) to "1" or "0".

As suggested in  the AC'97 Specification Rev2.1, the AC-Link Powerdown(PR"4") and Vref Powerdown(PR5="1")  under the Multiple codec configuration are NOT recommended in order to continue supplying  BIT_CLK to the Secondary codecs.

The below table shows the relationship for the AC-Link Powerdown/Powerup procedure.

| AC-Link Powerdown Procedure | Subsequent Procedure for Powerup | Comments |
| --- | --- | --- |
| RESET#=L | Cold Reset | Cold Reset wakes up all of codecs with default register setting concurrently. |
| Shutdown(Complete Powerdown) | Cold Reset | Cold Reset wakes up all of codecs with default register setting concurrently. |

Note:
1) The AC-Link Powerdown of Primary AC'97 will stop supplying the BIT_CLK to the Secondary AC'97.
2) When the AC-Link Powerdown is issued to the Secondary of AC'97, the Secondary of AC'97 will go to the AC-Link Powerdown and Warm Reset will be followed by Syn signal at the next time frame.


■Testability

**Activating the Test Modes**
*AC '97 has two test modes. One is for ATE in circuit test and the other is for vendor specific tests. AC '97 enters the ATE in circuit test mode regardless of SYNC signal (high or low) if SDATA_OUT is sampled high at the trailing edge of RESET#. If AC '97 enters AKM test mode when coming out of RESET if SYNC is high with SDATA_OUT low. These cases will never occur during standard operating conditions.*
*Regardless of the test mode, the AC '97 controller must issue a "Cold" reset to resume normal operation of the AC '97 Codec.*

**Test Mode Functions**
*ATE in circuit test mode*

*When AC '97 is placed in the ATE test mode, its digital AC-link outputs (i.e. BIT_CLK and SDATA_IN) are driven to a high impedance state. This allows ATE in circuit testing of the AC '97 controller.*

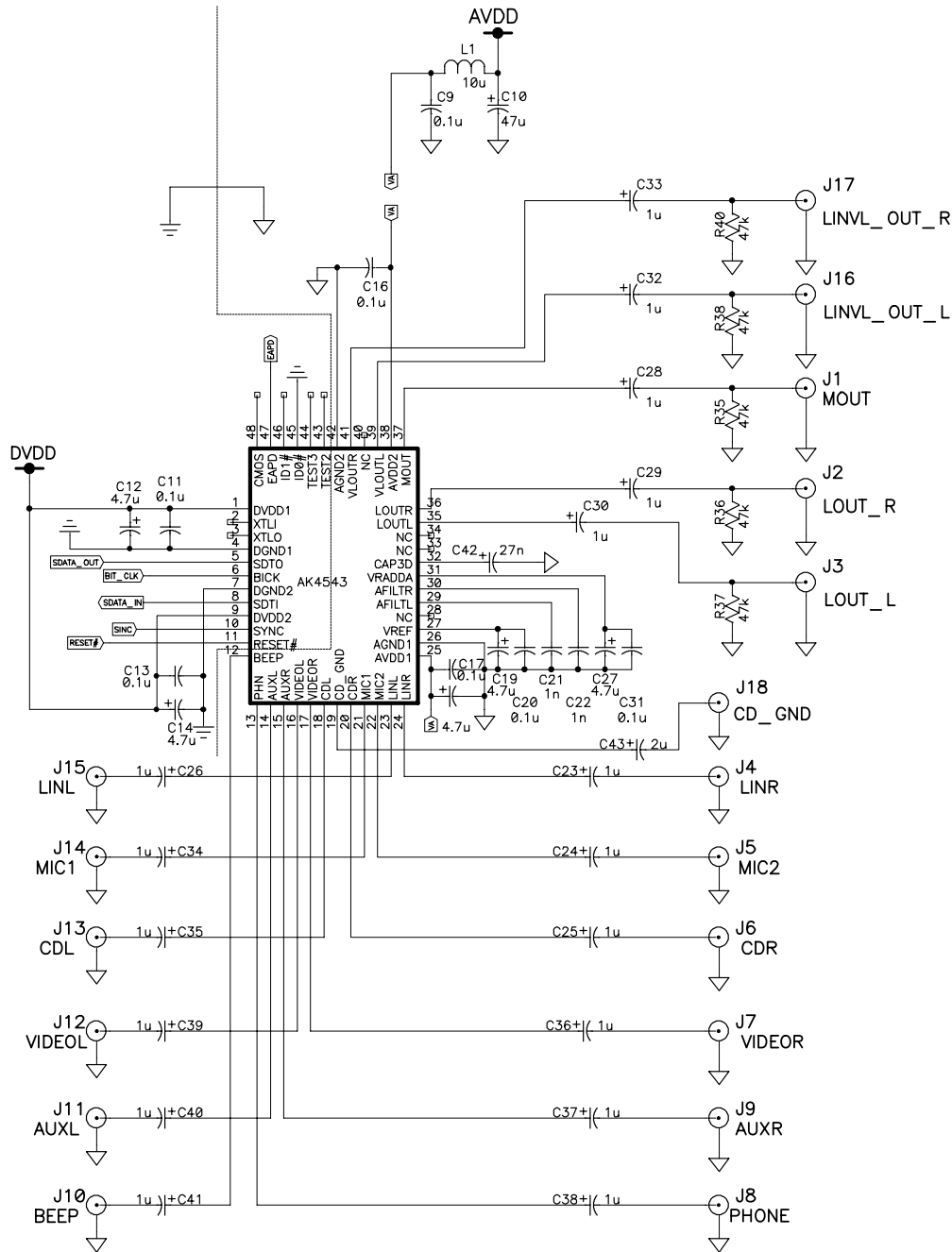## System Design

The following figure shows the system connection diagram.

Primary codec: codec ID1:codecID0=0:0
    AVDD: 5V
   DVDD: 3.3V or 5V
        3.3V : 48pin open
        5.0V : 48pin DGND
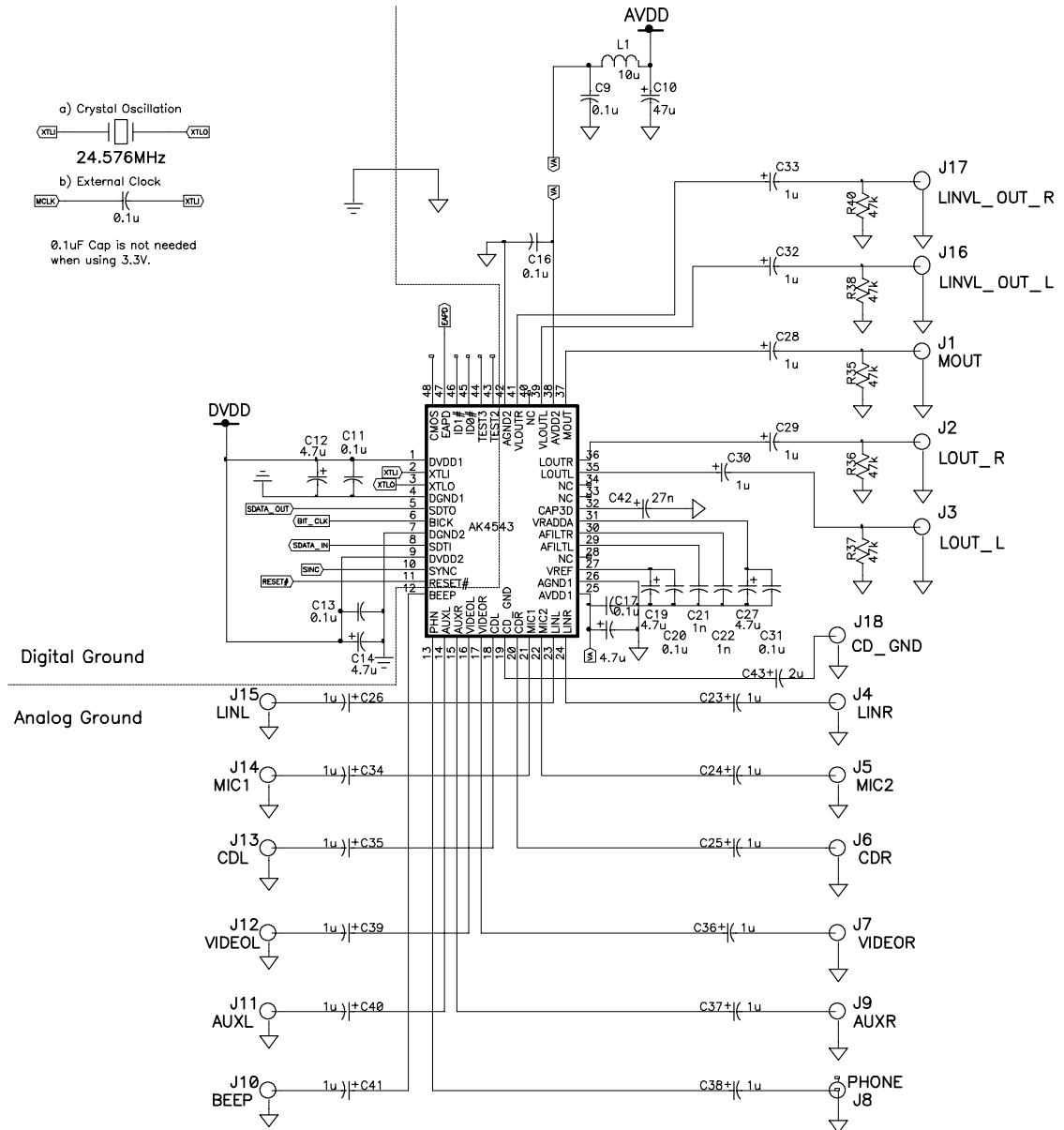
Secondary codec codec ID1:codecID0=0:1,1:0 or 1:1
This figure is the case of ID1 =0 and ID0=1.

   AVDD: 5V
  DVDD: 3.3V or 5V
          3.3V : 48pin open
          5.0V : 48pin DGND

1. Grounding and Power Supply Decoupling
AVdd1 and AVdd2 should be connected and derived from same AVdd. And DVdd1 and DVdd2 also should be connected and derived from same DVdd. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4543 as possible, with the small value ceramic capacitor being the nearest.The most important capacitor placements are on the Vref pin and AVdd pins.
No specific power supply sequencing is required on the AK4543.

2. On-chip Voltage Reference
The on-chip voltage reference is output on the VRADDA, Vref pins are used for decoupling. A electrolytic capacitor less than 10uF in parallel with a 0.1 uF ceramic capacitor attached to these pins eliminates the effects of high frequency noise. No load current may be drawn from VRADDA, or Vref pins. All signals, especially clocks, should be kept away from the VRADDA, and Vref pins in order to avoid unwanted coupling into delta-sigma modulators.

3. Codec ID configuration Pin 45,46

| ID1#(pin 46) | | ID0#(pin45) | | Configuration |
|---|---|---|---|---|
| Physical Connection | Logic Value | Physical Connection | Logic Value | |
| NC | 0 | NC | 0 | Primary |
| NC | 0 | GND | 1 | Secondary ID01 |
| GND | 1 | NC | 0 | Secondary ID10 |
| GND | 1 | GND | 1 | Secondary ID11 |

4.Anlog input
Since many analog levels can be as high as 2Vrms, the circuit shown below can be used to attenuate the analog input 2Vrms to 1Vrms which is the maximum voltage allowed for all the stereo line-level inputs.
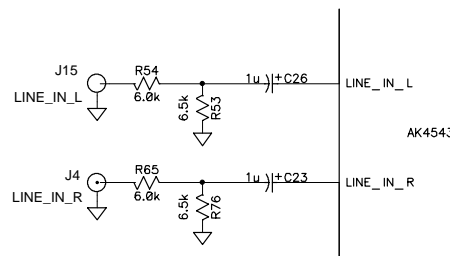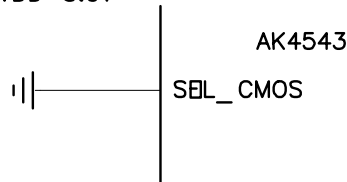


5.SEL_CMOS#(48pin)
When DVDD is 3.3V for support of CMOS level, Pin 48 must be open.

Pin 48 must be DGND as the below figure in the case of DVDD is 5.0V for TTL level
This SEL_COMS# has to be fixed before powering up the AK4543.



6.PC_BEEP
If PC_BEEP isn't used, this input pin should be NC(open) or connected to Analog-Ground via capacitor. In this case, the register for PC-Beep(04h,D15) should be set to mute on"1". (Note that the default of PC_BEEP is mute off.)
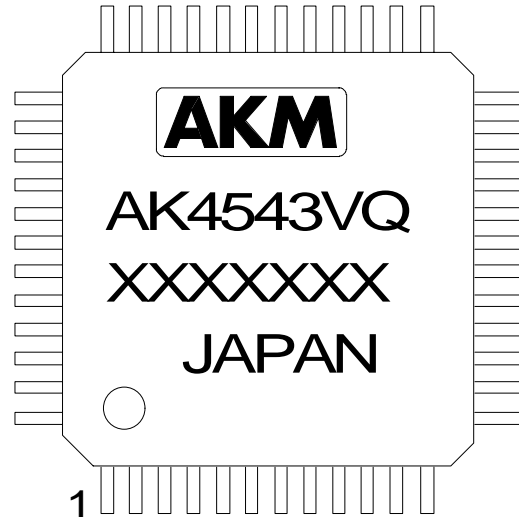In addition, when PC_BEEP is connected through capacity to Analog-Ground, PC_BEEP is recommended to be separated from other non-used input pins.

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**Package**

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48pin LQFP(Unit:mm)

| **Marking** |
| --- |

AKM

AK4543VQ

XXXXXXX

JAPAN

1
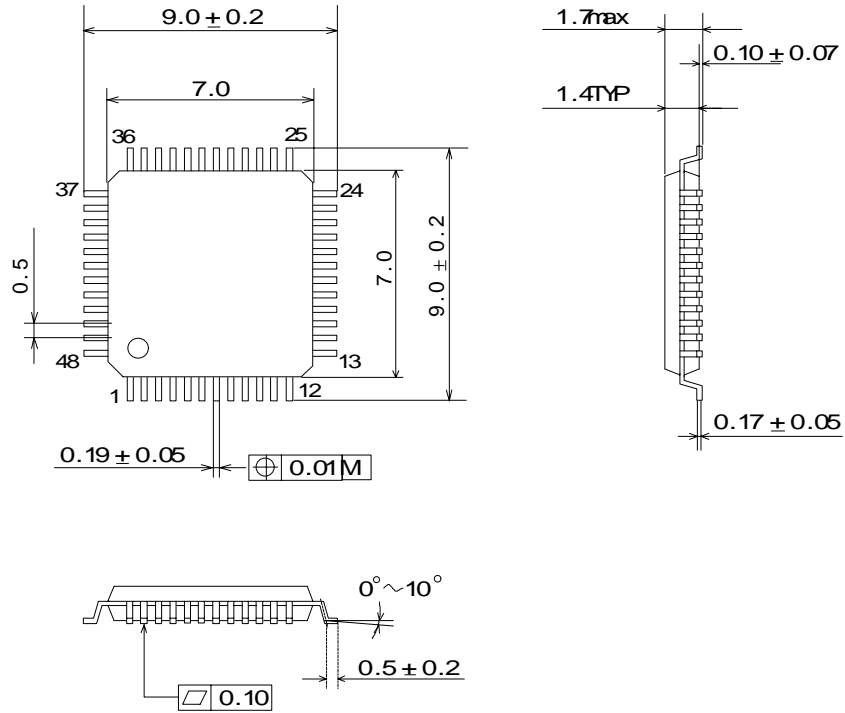
1)    Pin #1 indication
2)    Date Code : XXXXXXX (7 digits)
3)    Marketing Code : AK4543VQ
4)    Country of Origin
5)    Asahi Kasei  Logo

---

| **Appendix** |
|---|

1. Summary of the relationship of Slot 0 tag bit between SDATA_OUT and SDATA_IN

Whenever the AC '97 Digital Controller addresses the Primary AK4543 or the AK4543 responds to a read command, Slot 0 tag bits should always be set to indicate actual Slot 1 and Slot 2 data validity.

| Function | Slot 0, bit 15 (Valid Frame) | Slot 0, bit 14 (Valid Slot 1 Address) | Slot 0, bit 13 (Valid Slot 2 Data) | Slot 0, Bits 1-0 (Codec ID) |
|---|---|---|---|---|
| AC'97 Digital Controller Primary Read Frame N, SDATA_OUT | 1 | 1 | 0 | 00 |
| AC'97 Digital Controller Primary Write Frame N, SDATA_OUT | 1 | 1 | 1 | 00 |
| AK4543 Status Frame N+1, SDATA_IN | 1 | 1 | 1 | 00 |

Primary AK4543 Addressing: Slot 0 tag bits

When the AC '97 Digital Controller addresses a Secondary AK4543, the Slot 0 Tag bits for Address and Data must be "0". A non-zero 2-bit Codec ID in the LSBs of Slot 0 indicates a valid Read or Write Address in Slot 1, and the Slot 1 R/W bit indicates presence or absence of valid Data in Slot 2.

| Function | Slot 0, bit 15 (Valid Frame) | Slot 0, bit 14 (Valid Slot 1 Address) | Slot 0, bit 13 (Valid Slot 2 Data) | Slot 0, Bits 1-0 (Codec ID) |
|---|---|---|---|---|
| AC'97 Digital Controller Secondary Read Frame N, SDATA_OUT | 1 | 0 | 0 | 01, 10, or 11 |
| AC'97 Digital Controller Secondary Write Frame N, SDATA_OUT | 1 | 0 | 0 | 01, 10, or 11 |
| AK4543 Status Frame N+1, SDATA_IN | 1 | 1 | 1 | 00 |

Secondary AK4543 Addressing: Slot 0 tag bits

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