MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX602

Calling Line Identifier / Calling Line Identifier on Call Waiting

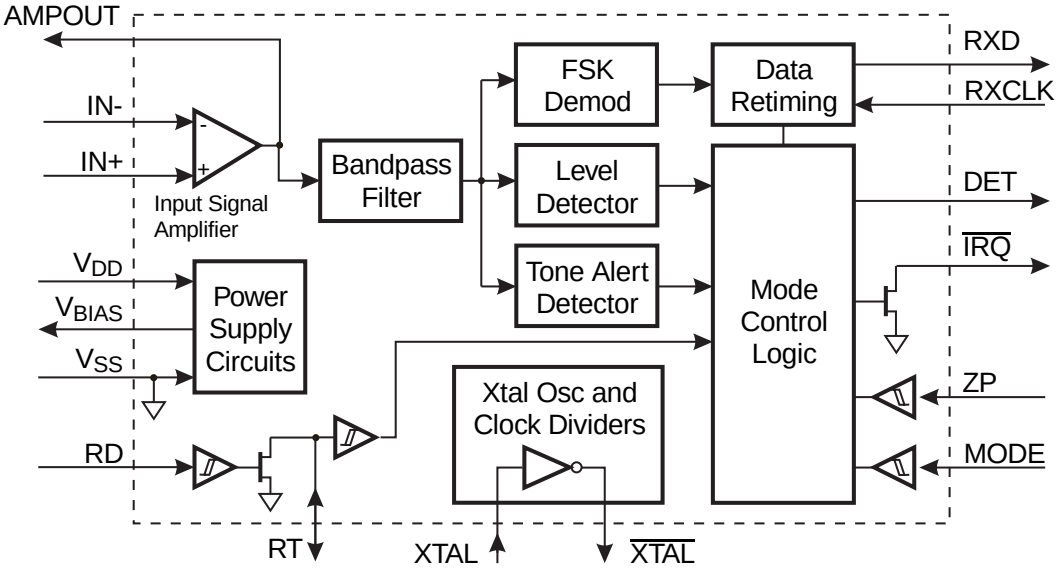
PRELIMINARY INFORMATION

Features

- **'Zero-Power' Ring or Line Polarity Reversal Detector**
- **V23/Bell202 FSK Demodulator with Data Retiming facility**
- **Dual-Tone Alert Detector**
- **µC Interrupt / Wake-up output to minimize system operating power**
- **Low Power Operation 0.5mA/1.0mA at 3.3V/5.5V$_{DD}$**
- **1µA max. 'Zero-Power' current**

Applications

- **Caller ID**
- **Caller ID on Call Waiting (Telephones and Adjunct Boxes)**



The MX602 is a low power CMOS device used for the reception of physical layer signals in Bellcore's Calling Identity Delivery (CID) and Calling Identity on Call Waiting (CIDCW) systems, British Telecom Calling Line Identification Service (CLIP), the Cable Communications Association's Caller Display Services (CDS), and similar evolving services.

The device includes a 'zero-power' ring or line polarity reversal detector, a dual-tone (2130Hz plus 2750Hz) Tone Alert Signal detector and a 1200-baud FSK V23/Bell202 compatible asynchronous data demodulator with a data retiming circuit which removes the need for a UART in the associated µC.

It is suitable for 'on-hook' use in systems using Bellcore specifications TR-NWT-000030 and SR-TSV-002476, British Telecom specifications SIN227 and SIN242, CCA TW/P&E/312, ETSI ETS 300 659-1 and ETS 300 659-2 and Mercury Communications MNR 19. It is also suitable for 'off-hook' use in some of those systems.

The MX602 may be used with a 3.0V to 5.0V supply and is available in the following packages: 16-pin SOIC (MX602DW) and a 16-pin PDIP (MX602P).

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1. Block Diagram

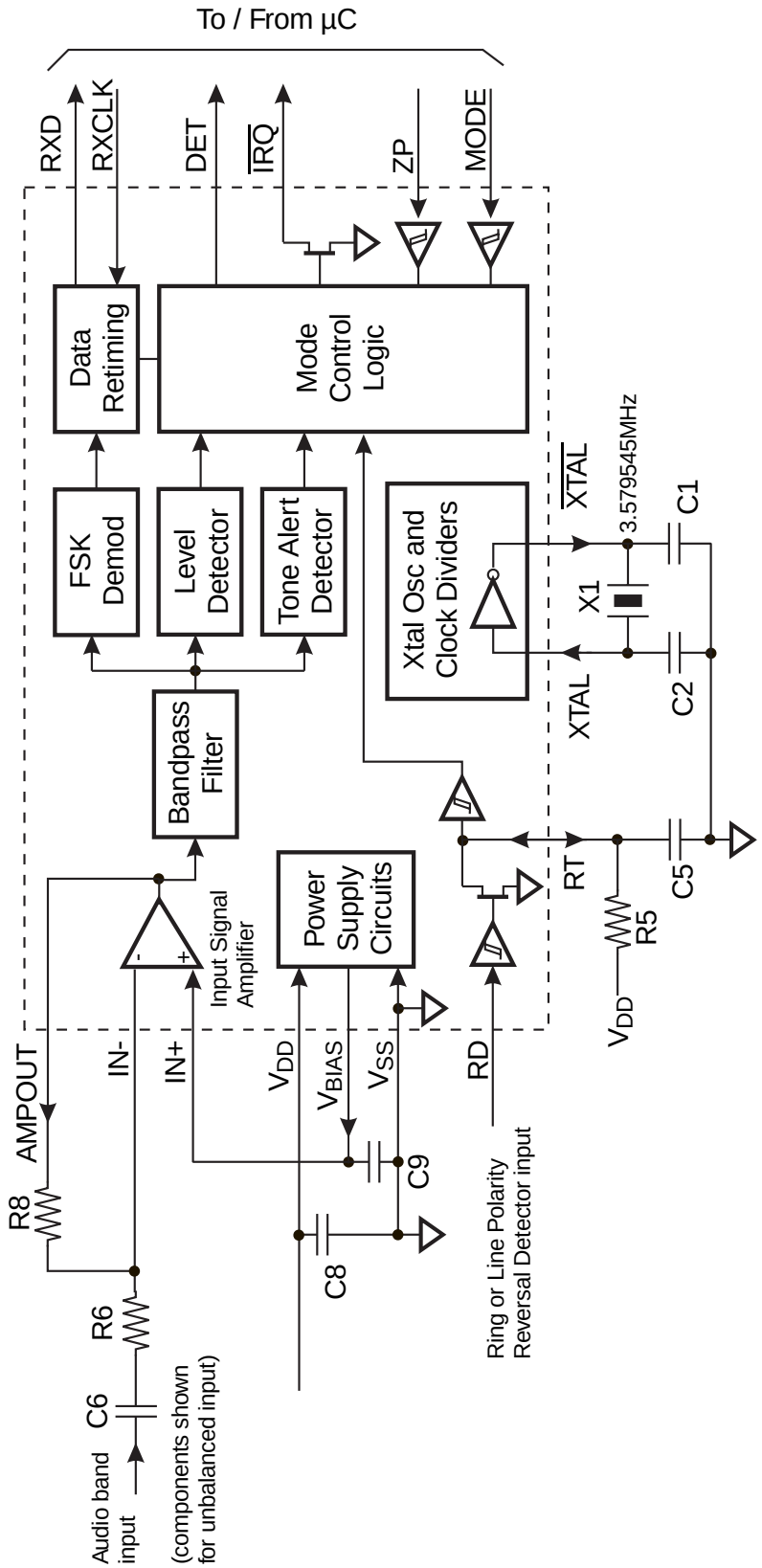


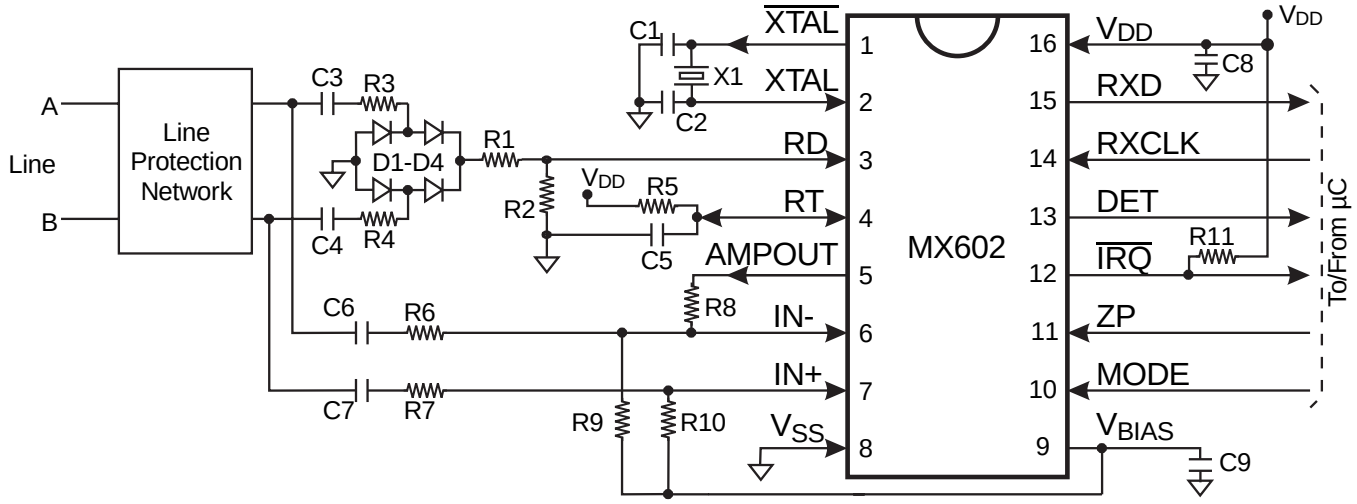
Figure 1: Block Diagram

2. Signal List

Pin No.	Signal	Type	Description
1	$\overline{XTAL}$	output	Output of the on-chip Xtal oscillator inverter
2	XTAL	input	Input to the on-chip Xtal oscillator inverter
3	RD	input (S)	Input to the Ring or Line Polarity Reversal Detector
4	RT	input / output	Open-drain output and Schmitt trigger input forming part of the Ring or Line Polarity Reversal detector. An external resistor to V_{DD} and a capacitor to V_{SS} should be connected to RT to filter and extend the RD input signal
5	AMPOUT	output	Output of the on-chip Input Signal Amplifier
6	IN -	input	Inverting input to the on-chip Input Signal Amplifier
7	IN +	input	Non-inverting input to the on-chip Input Signal Amplifier
8	V_{SS}	power	Negative supply
9	V_{BIAS}	output	Internally generated bias voltage, held at $V_{DD}/2$ when the device is not in 'Zero-Power' mode. Should be bypassed to V_{SS} by a capacitor mounted close to the device pins.
10	MODE	input (S)	Input used to select the operating mode.
11	ZP	input (S)	High level on this input selects 'Zero-Power' mode.
12	$\overline{IRQ}$	output	Open-drain output (active low) that may be used as an Interrupt Request / Wake-up input to the associated µC. An external pull-up resistor should be connected between this output and V_{DD}.
13	DET	output	Logic level output driven by the Ring or Line Polarity Reversal Detector, the Tone Alert Detector or the FSK Level detect circuits, depending on the operating mode.
14	RXCLK	input	Logic level input which may be used to clock received data bits out of the FSK Data Retiming block
15	RXD	output	Logic level output carrying either the raw output of the FSK Demodulator or re-timed 8-bit characters depending on the state of the RXCLK input
16	V_{DD}	power	Positive supply. Levels and thresholds within the device are proportional to this voltage. Should be bypassed to V_{SS} by a capacitor mounted close to the device pins.

Notes: input (S) = Schmitt trigger input

3. External Components



R1		470kΩ	±1%
R2	Note 1		±1%
R3, R4 R5, R6 R7		470kΩ	±1%
R8	Note 2, 3	470kΩ @ 3.3V 680kΩ @ 5.0V	±1%
R9	Note 2	240kΩ@ 3.3V 200kΩ@ 5.0V	±1%
R10		160kΩ	±1%

R11		100kΩ	±20%
C1, C2		18pF	±20%
C3, C4		0.1µF	±20%
C5		0.33µF	±20%
C6, C7		680pF	±20%
C8,C9		0.1µF	±20%
X1	Note 4	3.579545MHz	±0.1%
D1 - D4		1N4004	

Figure 2 : Recommended External Components for Dual Bellcore and British Telecom Application

Recommended External Component Notes:

1. See section 4.8
2. See section 4.2
3. The recommended values of R8 were selected for applications in both Bellcore and British Telecom Systems. Optimum Bellcore-only operation may be achieved by reducing the value of R8 e.g. to 656kΩ @ 5.0V.
4. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

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4. General Description

4.1 Mode Control Logic

The MX602's operating mode and the source of the DET and $\overline{IRQ}$ outputs are determined by the logic levels applied to the MODE and ZP input pins;

ZP	MODE	Mode	DET output from	$\overline{IRQ}$ output from
0	0	Tone Alert Detect	Tone Alert Signal Detection	End of Tone Alert Signal Ring or Line Polarity Reversal Detector
0	1	FSK Receive	FSK Level Detector	FSK Data Retiming (if enabled) and Ring or Line Polarity Reversal Detector
1	0	Zero-Power	Ring or Line Polarity Reversal Detector	Ring or Line Polarity Reversal Detector
1	1	Zero-Power	Ring or Line Polarity Reversal Detector	None

In the 'Zero-Power' modes, power is removed from all of the internal circuitry except for the Ring or Line Polarity Reversal Detector and the DET and $\overline{IRQ}$ outputs.

4.2 Input Signal Amplifier

This amplifier is used to convert the balanced FSK and Tone Alert signals received over the telephone line to an unbalanced signal of the correct amplitude for the FSK receiver and Tone Alert Detector circuits.

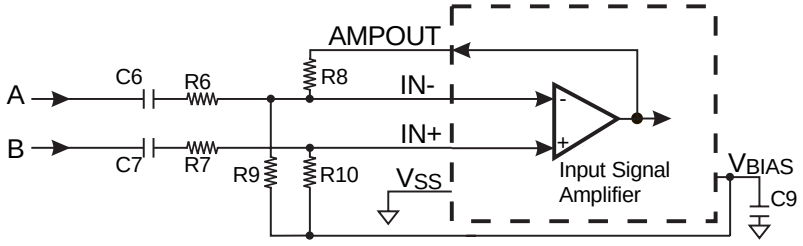


Figure 3: Input Signal Amplifier, balanced input configuration

The design equations for this circuit are:

$$\text{Differential Voltage Gain } \frac{V_{AMPOUT}}{V_{(B-A)}} = \frac{R8}{R6} \qquad R9 = \frac{R8 \times R10}{(R8 - R10)}$$

$$R6 = R7 = 470k\Omega \qquad R10 = 160k\Omega$$

The target differential voltage gain depends on the expected signal levels between the A and B wires and the MX602's internal overload and threshold levels, which are proportional to the supply voltage.

The MX602 has been designed to meet the related specifications when R8 = 470kΩ at V_{DD} = 3.3V nominal, rising to 680kΩ at V_{DD} = 5.0V (see note) and R9 = 240kΩ at V_{DD} = 3.3V dropping to 200kΩ at V_{DD} = 5.0V as shown in section 4.2 Figure 5

Notes:

1. The recommended values of R8 were selected for applications in both Bellcore and British Telecom Systems. Optimum Bellcore-only operation may be achieved by reducing the value of R8 e.g. to 656kΩ @ 5.0V.

The Input Signal Amplifier may also be used, with different external components, to allow the MX602 to operate from an unbalanced signal source as shown in Figure 4. In this unbalanced signal configuration, the values of R6 and R8 are the same as used for the balanced input configuration @ 3.3V nominal.

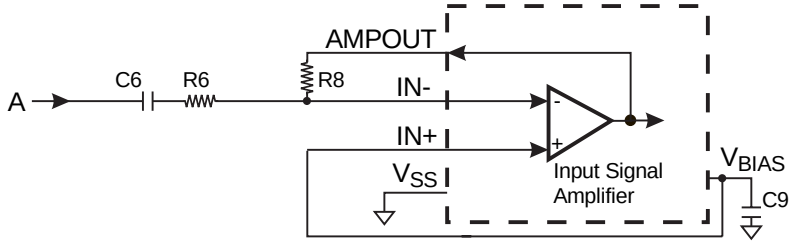


Figure 4: Input Signal Amplifier, unbalanced input configuration

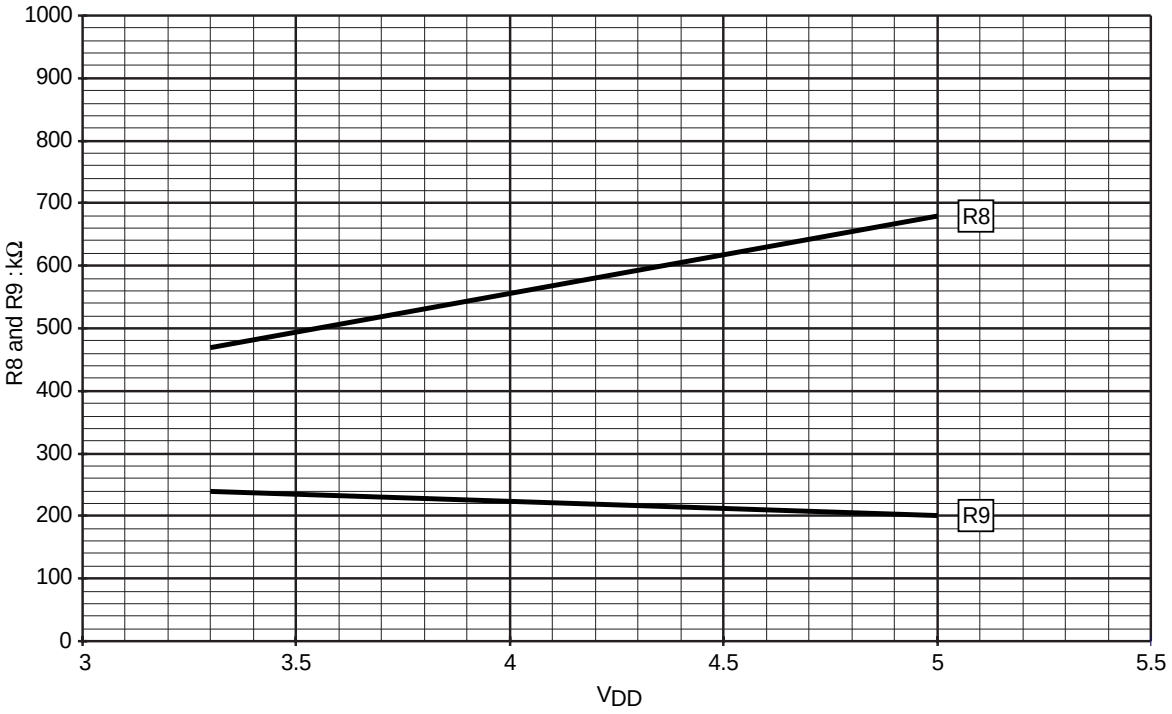


Figure 5: Input Signal Amplifier, optimum values of R8 and R9 vs. V_{DD}

4.3 Bandpass Filter

Is used to attenuate out of band noise and interfering signals from reaching the FSK Demodulator, Tone Alert Detector and Level Detector circuits. The characteristics of this filter, differs between FSK and Tone Alert modes. Switched Capacitor filter stages clocked at 57.7kHz provide primary filtering. If the input signal is band limited to 28.85kHz then no anti-aliasing filtering is required.

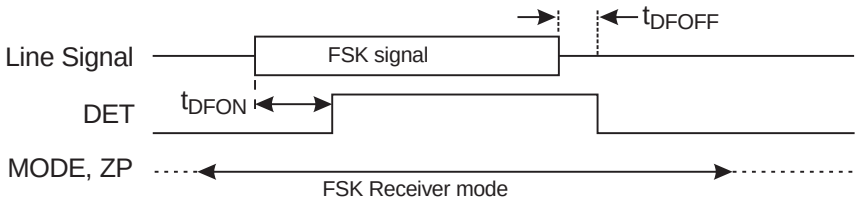
4.4 Level Detector

This block operates by measuring the level of the signal at the output of the Bandpass Filter. It then compares it against a threshold which depends on whether FSK Receive or Tone Alert Detect mode has been selected.

In Tone Alert Detect mode the output of the Level Detector block provides an input to the Tone Alert Signal Detector.

In FSK Receive mode the MX602 DET output will be set high when the level has exceeded the threshold for a sufficient duration. Amplitude and time hysteresis are used to reduce chattering of the DET output in marginal conditions.

Note: In FSK Receive mode, this circuit may also respond to non-FSK signals such as speech.



See section 6.1 for definitions of t_{DFON} and t_{DFOFF}

Figure 6: FSK Level Detector operation

4.5 FSK Demodulator

This block converts the 1200 baud FSK input signal to a digital data stream which is output via the RXD pin as long as the Data Retiming function is not enabled (see section 4.6). This output does not depend on the state of the FSK Level Detector output.

Note: In the absence of a valid FSK signal, the demodulator may falsely interpret speech or other extraneous signals as data.

4.6 FSK Data Retiming

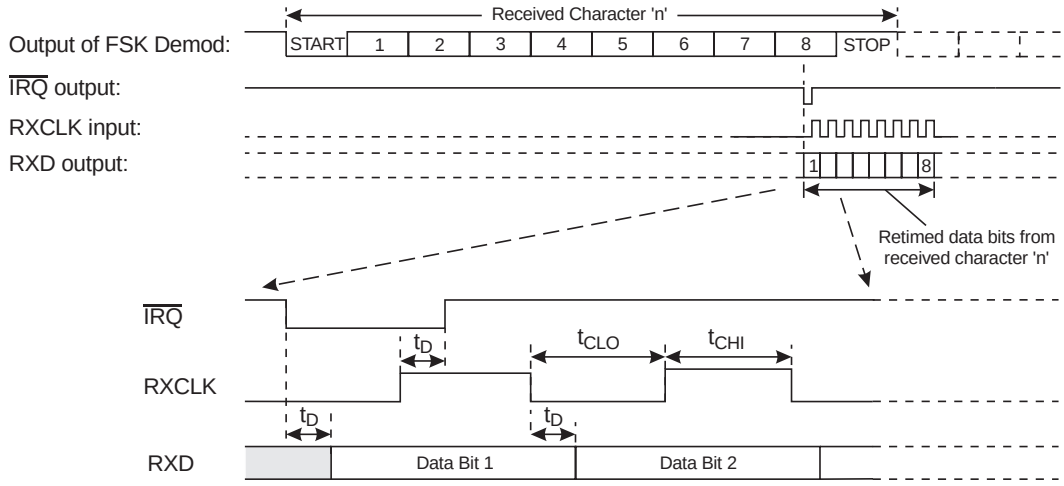
The Data Retiming block extracts the 8 data bits of each character from the received asynchronous data stream, and presents them to the µC under the control of strobe pulses applied to the RXCLK input. The timing of these pulses is not critical and they may easily be generated by a simple software loop. This facility removes the need for a UART in the µC without incurring an excessive software overhead.

The block operates on a character by character basis by first looking for the mark to space transition which signals the beginning of the start bit. Using this transition as a timing reference, the block samples the output of the FSK Demodulator in the middle of each of the following 8 received data bits, and stores the results in an internal 8-bit shift register.

When the eighth data bit has been clocked into the internal shift register, the MX602 examines the RXCLK input. If this is low then the $\overline{IRQ}$ output will be pulled low and the first of the stored data bits put onto the RXD output pin. On detecting that the $\overline{IRQ}$ output has gone low, the µC should pulse the RXCLK pin high 8 times. The high to low transition at the end of the first 7 of these pulses will be used by the MX602 to shift the next data bit from the shift register onto the RXD output. At the end of the eighth pulse the FSK Demodulator output will be reconnected to the RXD output pin. The $\overline{IRQ}$ output will be cleared the first time the RXCLK input goes high.

Thus to use the Data Retiming function, the RXCLK input should be kept low until the $\overline{IRQ}$ output goes low; if the Data Retiming function is not required the RXCLK input should be kept high.

The only restrictions on the timing of the RXCLK waveform are those shown in Figure 7 and the need to complete the transfer of all eight bits into the µC within 8.3mSec (the time of a complete character at 1200 baud).



t_D = Internal MX602 delay (max 1µS); t_{CLO} = RXCLK low time (min 1µS); t_{CHI} = RXCLK high time (min 1µS)

Figure 7: FSK Operation with Data Retiming

Note: If enabled, the Data Retiming block will interpret the FSK Channel Seizure signal (a sequence of alternating mark and space bits) as valid received characters, with values of 55 (hex). Similarly it may interpret speech or other signals as random characters. If the Data Retiming facility is not required, the RXCLK input to the MX602 should be kept high. The asynchronous data from the FSK Demodulator will then be connected directly to the RXD output pin, and the $\overline{IRQ}$ output will not be activated by the FSK signal. This case is illustrated in Figure 8.

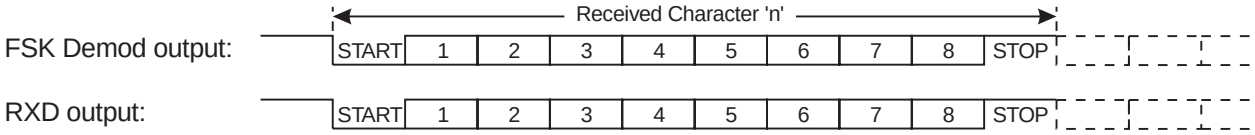
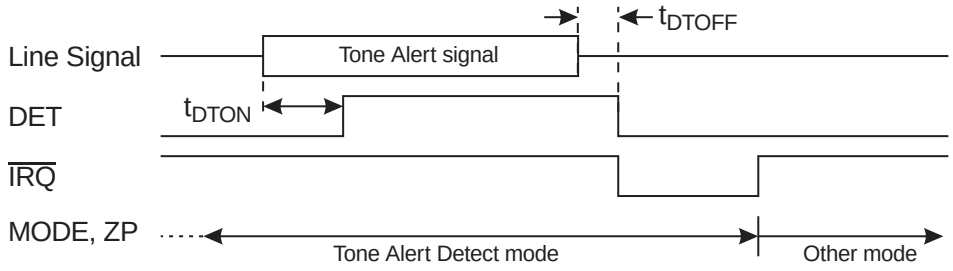


Figure 8: FSK Operation without Data Retiming (RXCLK always high)

4.7 Tone Alert Detector

This block is enabled when the MX602 is set to Tone Alert Detector operating mode. It then monitors the received signal for the presence of simultaneous 2130Hz and 2750Hz tones of sufficient level and duration.

The MX602 DET output will be set high while a valid Tone Alert signal is detected. At the end of the Tone Alert signal the DET output will go low and the $\overline{IRQ}$ output will be pulled low until the MX602 is switched out of Tone Alert Detector mode.



See section 6.1 for definitions of t_{DTON} and t_{DTOFF}

Figure 9: Tone Alert Detector Operation

4.8 Ring or Line Polarity Reversal Detector

These circuits are used to detect the Line Polarity Reversal and Ringing signals associated with the Calling Line Identification protocol. Figure 10 illustrates their use in a typical application.

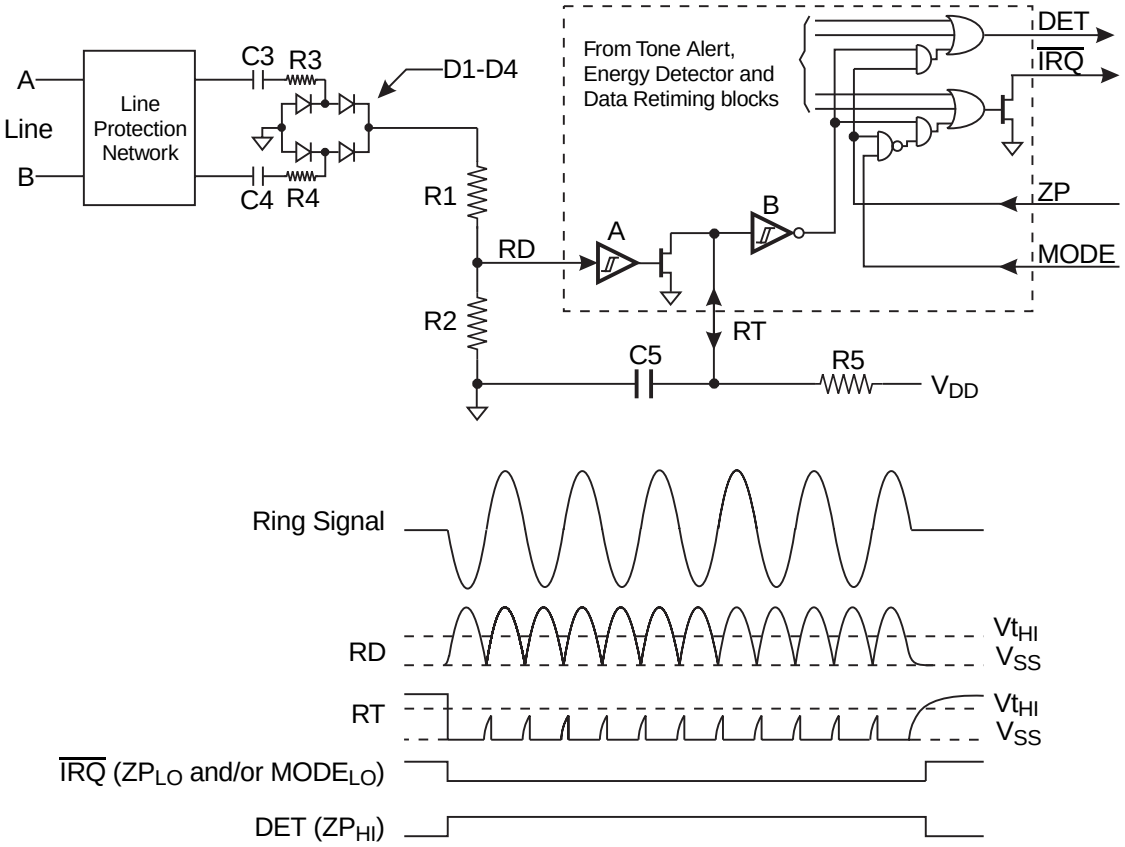


Figure 10: Ring or Line Polarity Reversal Operation

When no signal is present on the telephone line, RD will be at V_{SS} and RT pulled to V_{DD} by R5 so the output of the Schmitt trigger 'B' will be low.

The ring signal is usually applied at the subscriber's exchange as an ac voltage inserted in series with one of the telephone wires and will pass through either C3 and R3 or C4 and R4 to appear at the top end of R1 (point X in Figure 10) in a rectified and attenuated form.

When the amplitude of the signal appearing at RD is greater than the input threshold (Vt_{HI}) of Schmitt trigger 'A' then the N transistor connected to RT will be turned on, pulling the voltage at RT to V_{SS} by discharging the external capacitor C5.

The output of the Schmitt trigger 'B' will then go high, activating the DET and/or $\overline{IRQ}$ outputs depending on the states of the MODE and ZP inputs.

The minimum amplitude ringing signal that is certain to be detected is :

$$\left(0.7 + Vt_{HI}\frac{(R1+R2+R3)}{R2}\right)(0.707V_{RMS})$$

Where Vt_{HI} is the high-going threshold voltage of the Schmitt trigger A (see section 6.1).

With R1, R3 and R4 all 470kΩ as indicated in Figure 2, then setting R2 to 68kΩ will guarantee detection of ringing signals of $40V_{RMS}$ and above, for V_{DD}, over the range 3.0 to 5.5V.

A line polarity reversal may be detected using the same circuit but there will be only one pulse at RD. The British Telecom specification SIN242 says that the circuit must detect a +15V to -15V reversal between the two lines slewing in 30msec. For a linearly changing voltage at the input to C3 (or C4), then the voltage appearing at the RD pin will be

$$\frac{dV}{dt}C3\left(1-e^{-\frac{t}{T}}\right)R2 \text{ where } T = C3(R1+R2+R3) \text{ and } \frac{dV}{dt} \text{ is the input slew rate.}$$

For dV/dt = 500V/sec (15V in 30msec), R1, R3 and R4 all 470kΩ and C3, C4 both 0.1µF as indicated in Figure 2, then setting R2 to 390kΩ will guarantee detection at V_{DD} = 5.5V.

If the time constant of R5 and C5 is large enough then the voltage on RT will remain below the threshold of the 'B' Schmitt trigger keeping the DET and/or $\overline{IRQ}$ outputs active for the duration of a ring cycle

The time for the voltage on RT to charge from V_{SS} towards V_{DD} can be derived from the formula

$$V_{RT} = V_{DD}\left(1-e^{-\frac{t}{R5C5}}\right)$$

As the Schmitt trigger high-going input threshold voltage (Vt_{HI}) has a minimum value of 0.56 x V_{DD} , then the Schmitt trigger B output will remain high for a time of at least 0.821 x R5 x C5 following a pulse at RD.

Using the values given in Figure 2(470kΩ and 0.33µF) gives a minimum time of 100 msec (independent of V_{DD}), which is adequate for ring frequencies of 10Hz or above.

If necessary, the µC can distinguish between a ring and a reversal by timing the length of the $\overline{IRQ}$ or DET output.

4.9 Xtal Osc and Clock Dividers

Frequency and timing accuracy of the MX602 is determined by a 3.579545MHz clock present at the XTAL pin. This may be generated by the on-chip oscillator inverter using the external components C1, C2 and X1 of Figure 2, or may be supplied from an external source to the XTAL input, in which case C1, C2 and X1 should not be fitted.

The oscillator is turned off in the 'Zero-Power' modes.

If the clock is provided by an external source which is not always running, then the ZP input must be set high when the clock is not available. Failure to observe this rule may cause a significant rise in the supply current drawn by MX602 as well as generating undefined states of the RXD, DET and $\overline{IRQ}$ outputs.

5. Application Notes

5.1 Typical Caller Identity Delivery (Caller ID) System Signals

Figure 11, Figure 12, and Figure 13 illustrate the line signaling and MX602 input and output signals for typical Bellcore and British Telecom system use.

The Data Retiming function is not used in these examples (RXCLK kept high).

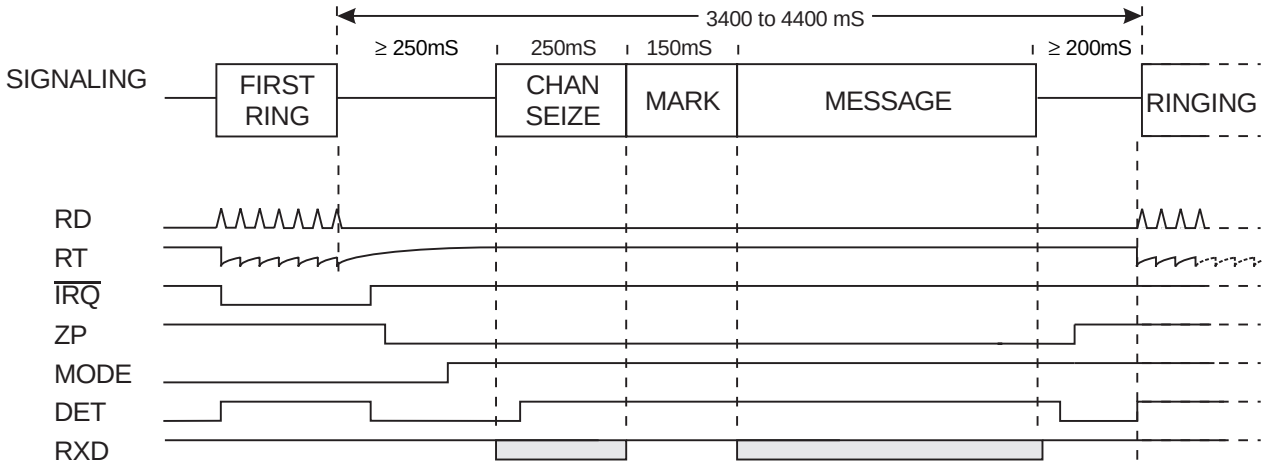


Figure 11: Bellcore System Signals

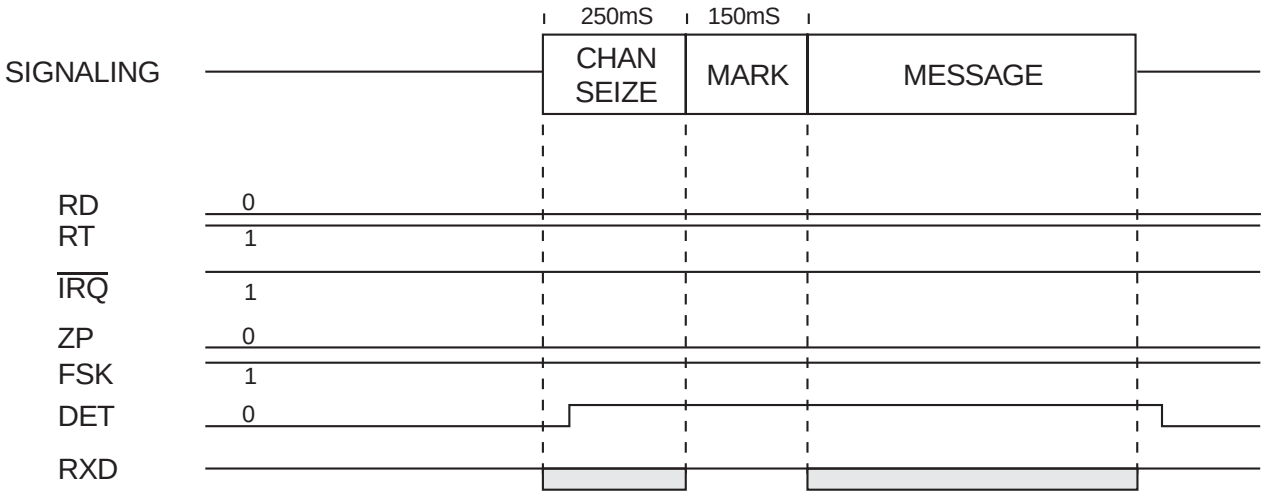
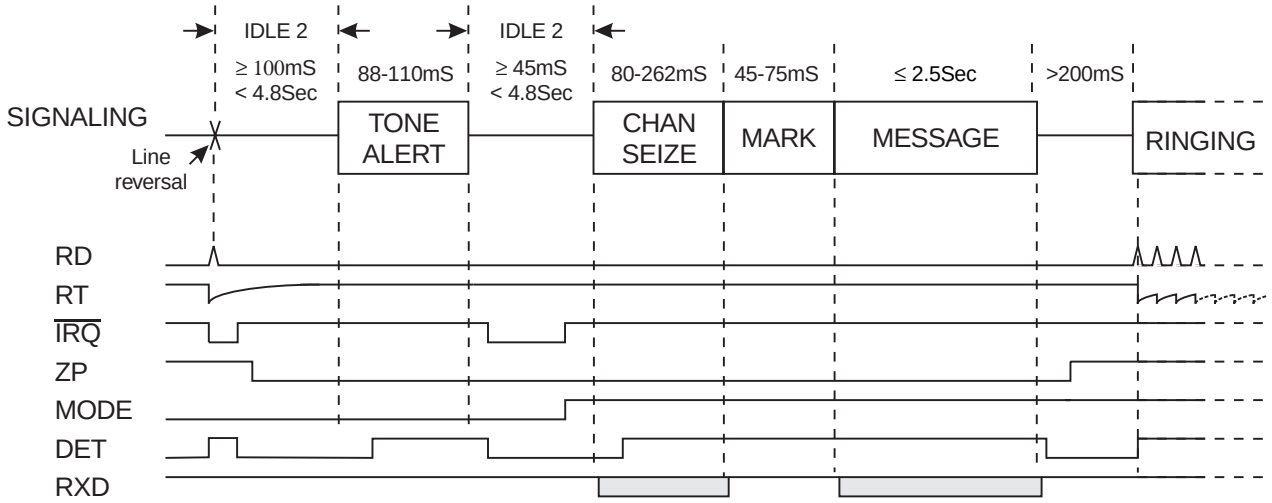


Figure 12: Bellcore System Signals (without ring)

The British Telecom Tone Alert signal consists of simultaneous 2130Hz and 2750Hz tones. The 'Chan Seize' signal consists of a '1010..' FSK bit sequence in all cases.



Note: IDLE 1 + IDLE 2 ≤ 5 sec

Figure 13: British Telecom System Signals

5.2 MX602 CIDCW (Calling Line Identity on Call Waiting) Operation

5.2.1 Introduction

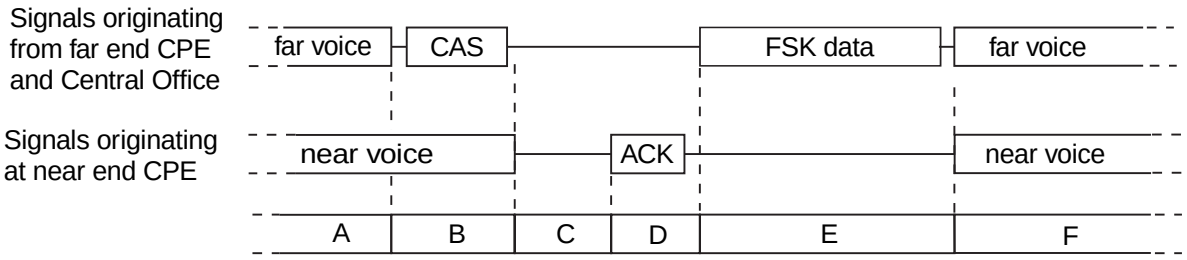
CIDCW is a telephone service which identifies a waiting caller without interrupting your current call. It eliminates the 'blind spot' in traditional Call Waiting by giving a telephone user the informed choice of whether or not to take the incoming call.

To support CIDCW, the circuits of Caller ID compatible telephone equipment and adjunct 'boxes' must detect a subtle CPE Alert Signal (CAS), a dual tone injected into phone conversations. The CAS is transmitted by the central office to initiate a CIDCW transaction consisting of an 80ms burst of simultaneous 2130Hz and 2750Hz tones. CAS detection accuracy is very important because both missed and false signal detection is evident and annoying to telephone users. Missed signal detection causes Caller ID information to be lost. False signal detection produces a disruptive tone which is heard by the far end caller. Because the tone signals must be detected in the presence of conversations which both mask and masquerade as the tone signals, this function is very difficult to accurately achieve.

This application note describes the use of the MX602 for CIDCW CAS detection. The MX602's 1µA ring detect supply current, 3.3 to 5.5 volt supply range, and 16 pin package offer significant advantages in battery life and final product size.

5.2.2 Overview

A successful CIDCW transaction as described by Bellcore SR-TSV-002476, consists of a sequence of actions between the CPE (Customer Premises Equipment - e.g. a telephone) and the Central Office as indicated in Figure 14.



A. Normal conversation with both near and far voice present.
B. Central Office mutes far end voice, emits CAS and becomes silent
C. CPE recognizes CIDCW initiation and mutes near end voice and keypad
D. CPE emits DTMF ACK to Central Office to signal its readiness to receive Caller ID data stream
E. Central Office recognizes ACK and emits FSK Data stream of Caller ID data which is received and decoded by CPE
F. CIDCW transaction is complete. CPE unmutes near end voice and Central Office unmutes far end voice returning to normal conversation with both near and far voice present.

Figure 14, CIDCW Transaction From Near End CPE Perspective

From the near end CPE's perspective, the initiation of a CIDCW transaction is characterized by two events occurring in sequence: (1) a CAS dual tone is received, and (2) a subsequent quiet period passes as far end speech continues to be muted. These two events can be detected by the MX602's Dual Tone Alert detector and FSK level detector, respectively.

Caller ID and CIDCW end products typically use a microcontroller to manage the transfer and display of Caller ID data. The same microcontroller is easily used to observe and control the MX602 CIDCW transaction initiation detection process. It measures an MX602 DET output pulse duration, mutes near end voice, subsequently watches for DET output activity, and controls whether the MX602 is in Dual Tone Alert or FSK Receive modes as shown in Figure 15.

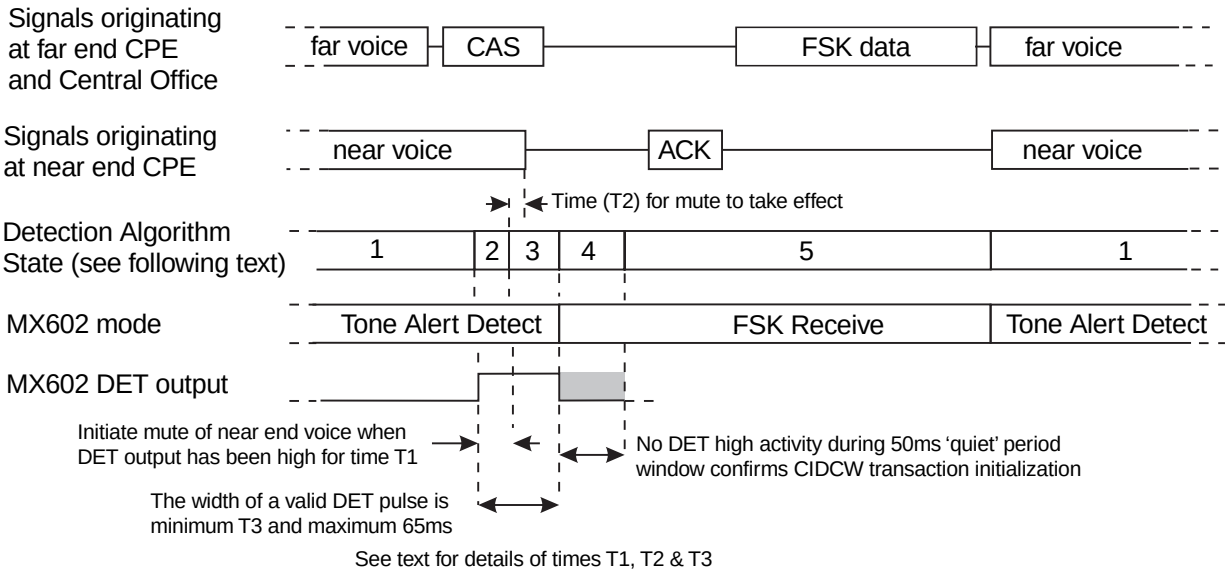


Figure 15, CIDCW Transaction Initiation with MX602 Operation

Different strategies may be used for CIDCW transaction initiation detection. The simplest strategy detects only the CAS dual tone. More complex strategies may detect both the CAS dual tone as well as the following far end voice quiet period

if near end voice is muted. The choice of a specific strategy involves several tradeoffs which must be considered by the end product designer.

As previously described, the MX602 dual tone detector and FSK energy level detector functions provide the tools to implement a range of strategies. It is important to note that CIDCW transaction detection performance is influenced by factors which are external to the MX602 and under the control of its surrounding circuit. Such factors may include: (1) Input signal levels provided to the MX602, (2) The functional 'cost' associated with missed and false CIDCW transaction detections, (3) Pulse width measurement accuracy, and (4) Noise or other disturbances introduced by muting or other external circuits. The remainder of this section provides examples to assist end product designers develop their specific designs.

CIDCW Transaction Initiation Detection Algorithm

The following State Transition Diagram Figure 16 and following text provide a detailed description of the CIDCW detection procedure as shown in Figure 15.

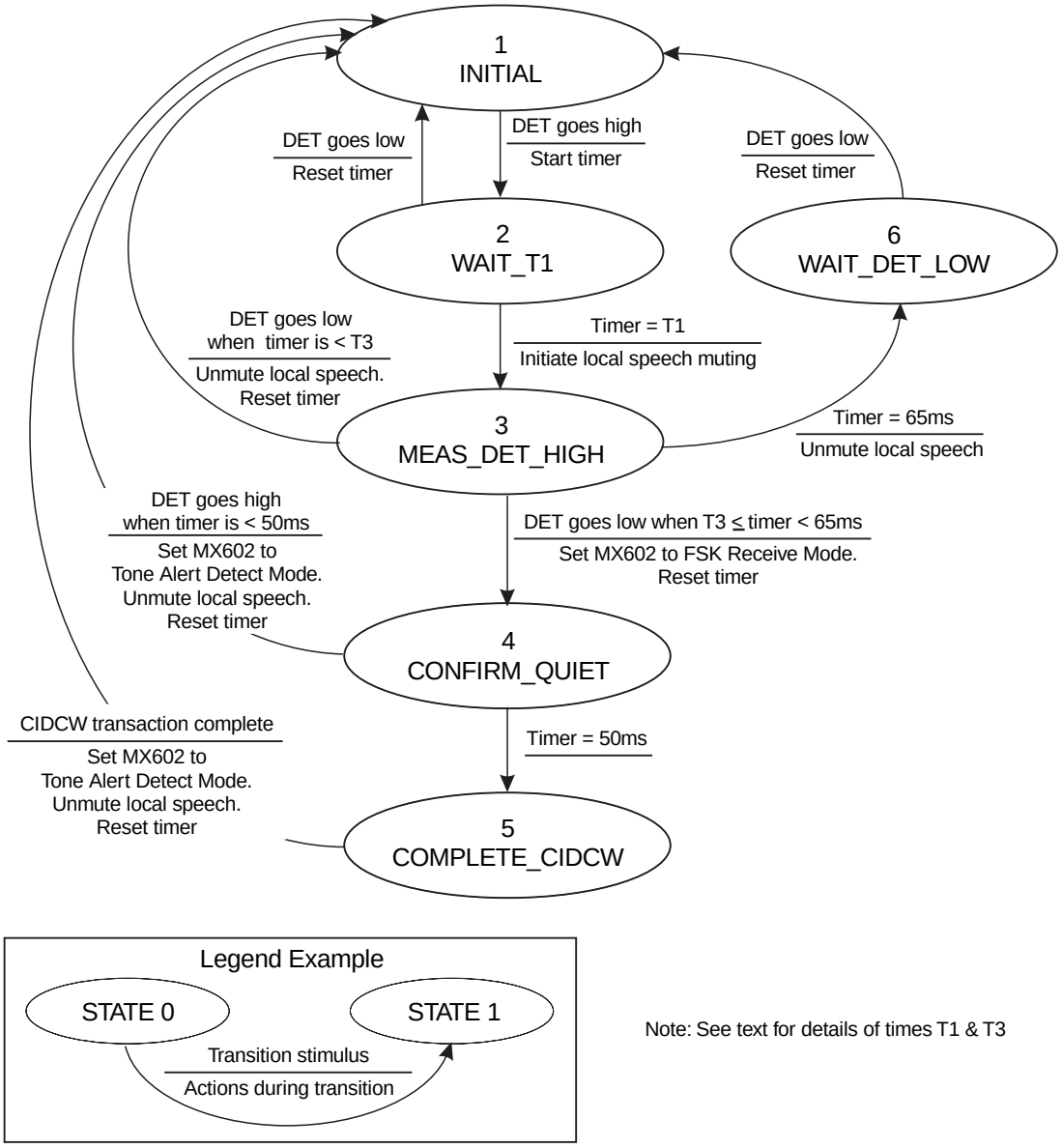


Figure 16, CIDCW State Flow Diagram

5.2.3 Detailed Procedure for CIDCW Transaction Initiation Detection

1. INITIAL state
The MX602 is in the Tone Alert Detect mode. On the rising edge of the DET line, start the timer, and transition to the WAIT_T1 state.

2. WAIT_T1 state
During this state, the DET output high time is measured so that pulses lasting less than T1 may be ignored.
WHILE Timer < T1
    IF DET goes low
        Reset the timer.
        Transition to the INITIAL state.
Initiate local speech muting.
Transition to MEAS_DET_HIGH state.

3. MEAS_DET_HIGH state
WHILE Timer < 65ms
    IF DET goes low
        IF Timer < T3
            Unmute local speech.
            Reset the timer.
            Transition to the INITIAL state.
        ELSE
            Set MX602 to FSK Receive Mode.
            Reset the timer.
            Transition to the CONFIRM_QUIET state.
Unmute local speech.
Transition to the WAIT_DET_LOW state.

4. CONFIRM_QUIET state
WHILE Timer < 50ms
    IF DET goes high
        Set MX602 to Tone Alert Detect Mode.
        Unmute local speech.
        Reset the timer.
        Transition to the INITIAL state.
Transition to the COMPLETE_CIDCW state.

5. COMPLETE_CIDCW state
This state handles the remaining CIDCW transaction functions e.g. determine that no near end extensions are off hook, emit a CPE ACK to Central Office via a DTMF D tone signal, receive the FSK Caller ID data stream, etc.
WHEN CIDCW transaction is complete
    Set the MX602 to Tone Alert Detect Mode.
    Unmute local speech.
    Reset the timer.
    Transition to the INITIAL state.

6. WAIT_DET_LOW state
WHEN DET goes low
    Reset the timer
    Transition to the INITIAL state.

Times T1, T2, & T3
The values given below have been selected to give an extremely low incidence of false CAS detections while maintaining a high probability of decoding correct CIDCW initiation signals by taking advantage of the specific profile of MX602's responses to typical speech and CAS signals. Two timing options are given, Telephone Set and Adjunct Box, the choice being determined principally by how easily local speech can be muted. The Adjunct Box option reduces the frequency of short speech mutes by a factor of about 5 at the expense of a small increase in the number of missed CAS signals when compared to the Telephone Set option.

Adjunct Box Timing

When the CIDCW circuits are housed in an adjunct box so that muting is only possible by interrupting the 2-wire connection to the telephone set, then it is recommended that:

T1 should be 15ms i.e. speech muting should only be initiated after the DET output has been high for 15ms.

T2, the time for speech muting to take effect, should be as short as possible and in any case not more than 5ms.

T3, the minimum length of a valid DET output high time, should be equal to T1 plus T2 plus 10ms, i.e. between 25 and 30ms.

Telephone Set Timing

When the CIDCW circuits are built into the telephone set so that locally generated speech can be muted quickly and without injecting noise then it is recommended that:

T1 should be zero, i.e. muting should be initiated as soon as the MX602 DET output goes high.

T2, the time for local speech muting to take effect, should be as short as possible and in any case not more than 5ms.

T3, the minimum length of a valid DET output high time, should be 15ms.

Notes:

1. The T1, T2, and T3 time values are intended to provide guidance, however, different times may be required for optimal operation in specific end product designs.
2. For optimum performance, the system transition times from tone detect to muting and tone detect de-response to FSK mode should be minimized. Tests have been performed with sub-millisecond response times but longer times may be used with some degradation in performance.
3. The 50ms monitoring period of the CONFIRM_QUIET state, when added to the 0.5 to 10ms de-response time of the MX602 in Tone Alert Detect and a nominal 0 to 5ms delay in changing from TONE mode to FSK mode, results in a valid CAS detection occurring at between 50 and 65ms after the end of the CAS. This leaves at least 35ms to mute the local handset fully, test for off-hook extensions, and initiate the DTMF ACK tone within the time permitted by CIDCW specifications.
4. During the CONFIRM_QUIET state, any high pulses on the DET output will last for at least 8ms (or until the mode is changed). This makes it simple to monitor and detect any DET high output pulses when in this state.
5. In adjunct box applications, it is important to avoid injecting noise to the MX602 input signal when performing near end voice muting because such noise could disrupt MX602 operation and reduce performance. Alternate approaches can be used which would delay such voice muting until after the CAS tone. One example would first qualify dual tone detector output pulses of 20ms to 65ms nominal duration as CAS tone indications and follow such pulses with near end voice muting and silence confirmation to further enhance performance.

5.2.4 Block Diagrams of Adjunct Box and Telephone Set Interfaces

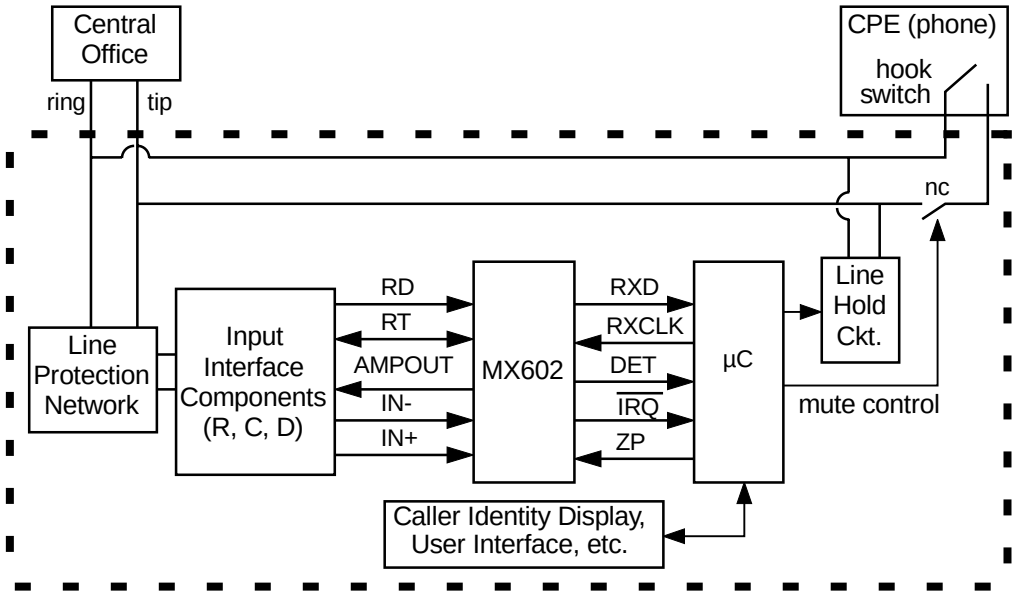


Figure 17: Adjunct Box Interface

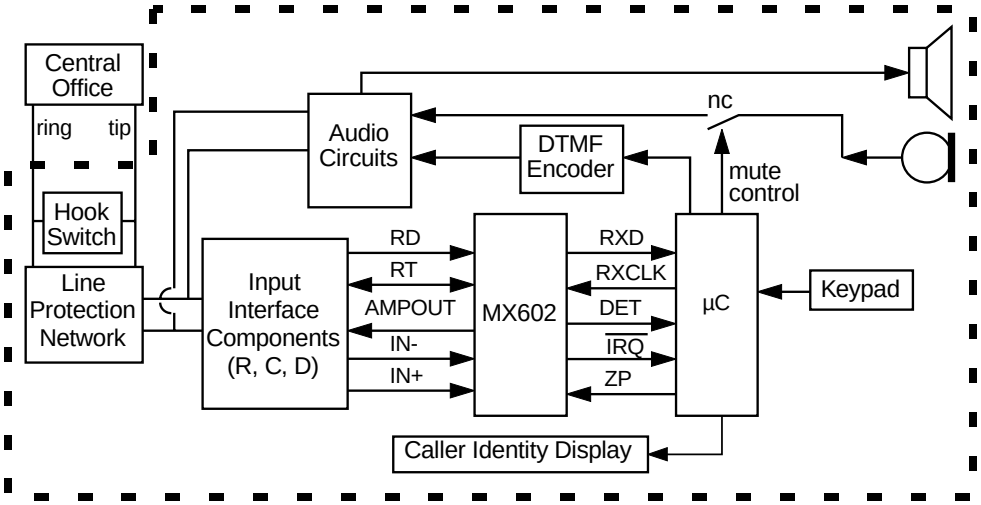
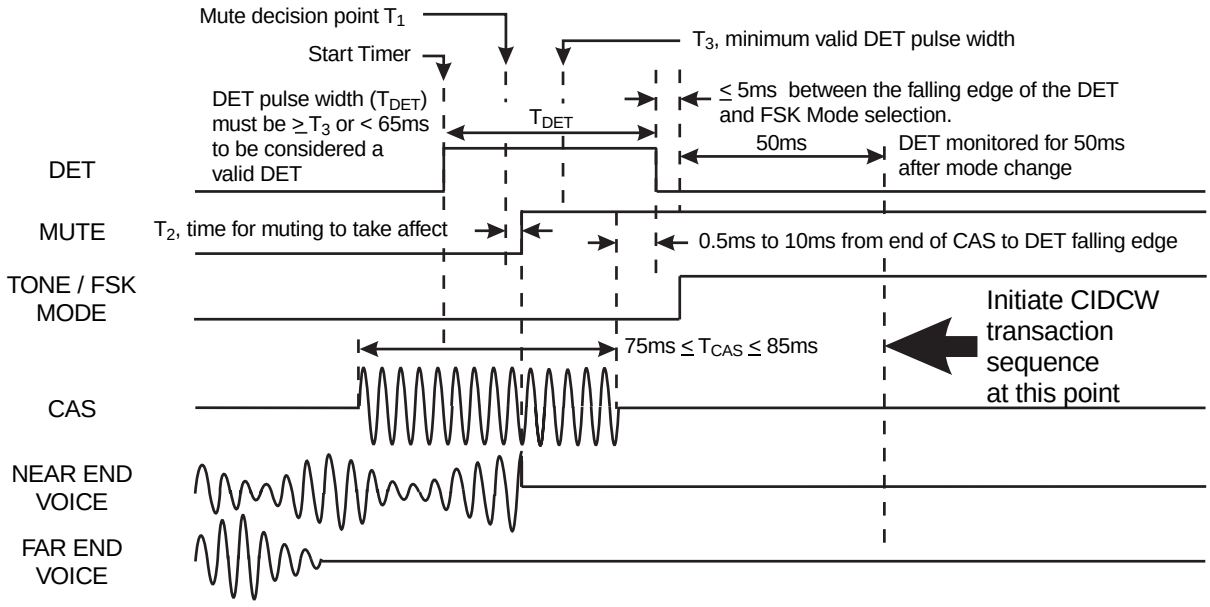


Figure 18: Telephone Set Interface

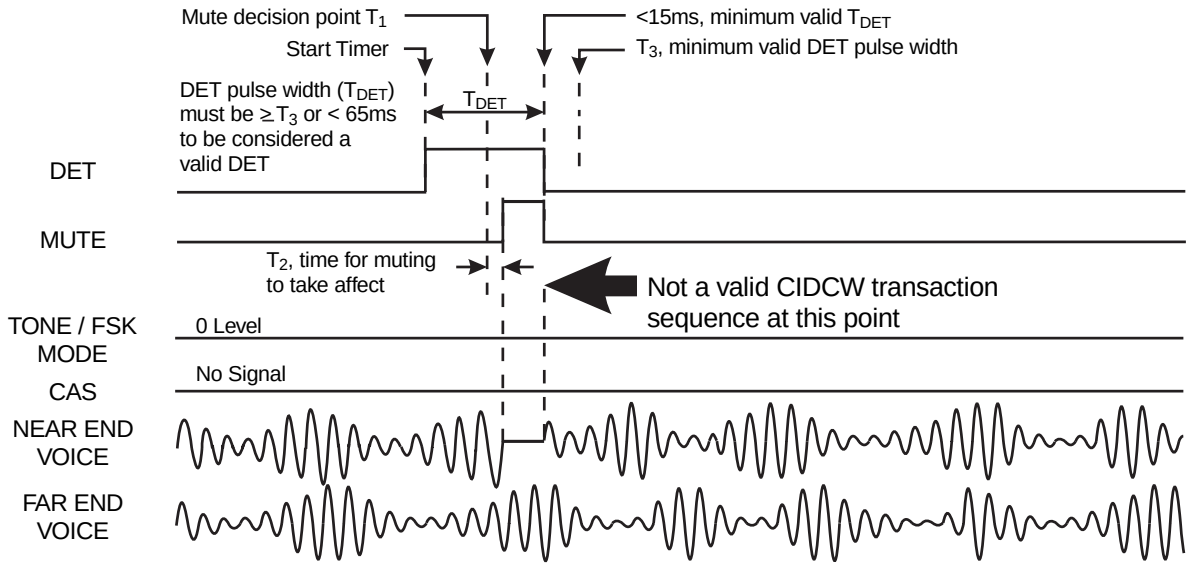
5.2.5 Timing Diagrams

Figure 19, Figure 20, Figure 21, Figure 22, Figure 23, Figure 24, Figure 25, and Figure 26 are timing diagrams which illustrate the CIDCW transaction initiation sequence for various cases.



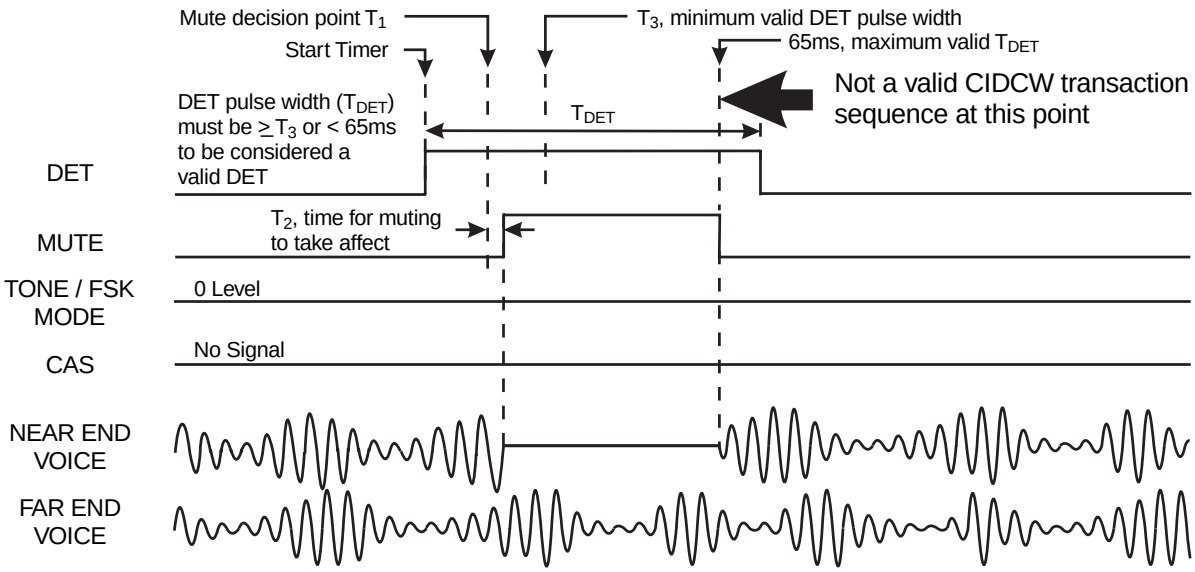
Note: The actual signal received by the MX602 is the sum of the CAS, Near-End Voice, and Far-End Voice signals.

Figure 19, Valid CIDCW Transaction Initiation Adjunct Box Timing Sequence



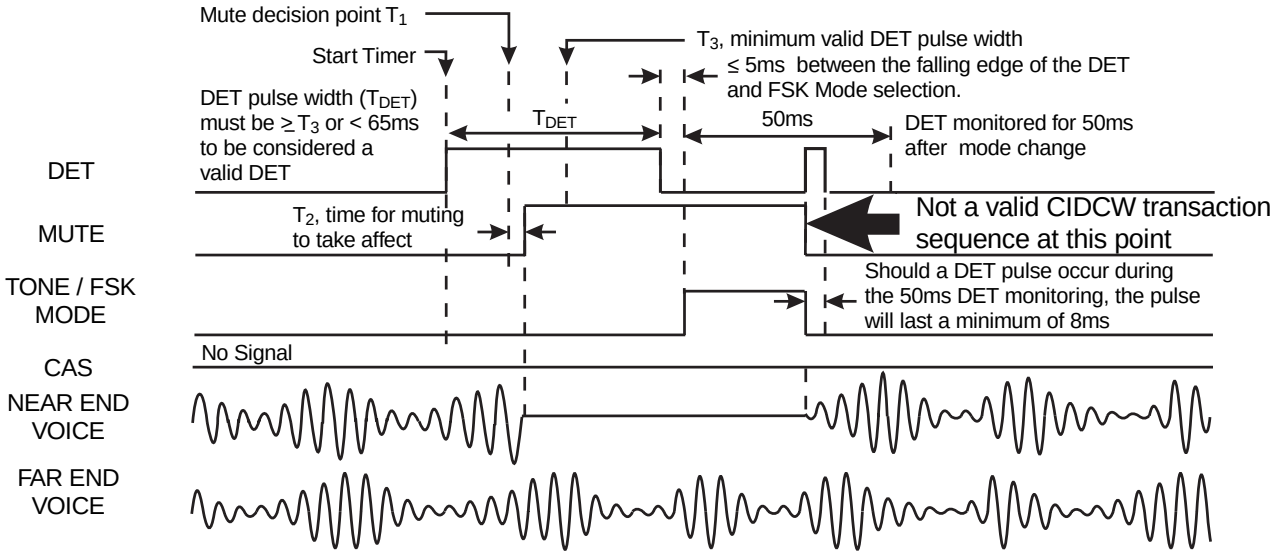
Note: The actual signal received by the MX602 is the sum of the CAS, Near-End Voice, and Far-End Voice signals.

Figure 20, Invalid CIDCW Transaction Initiation Adjunct Box Timing Sequence (DET pulse < 15ms)



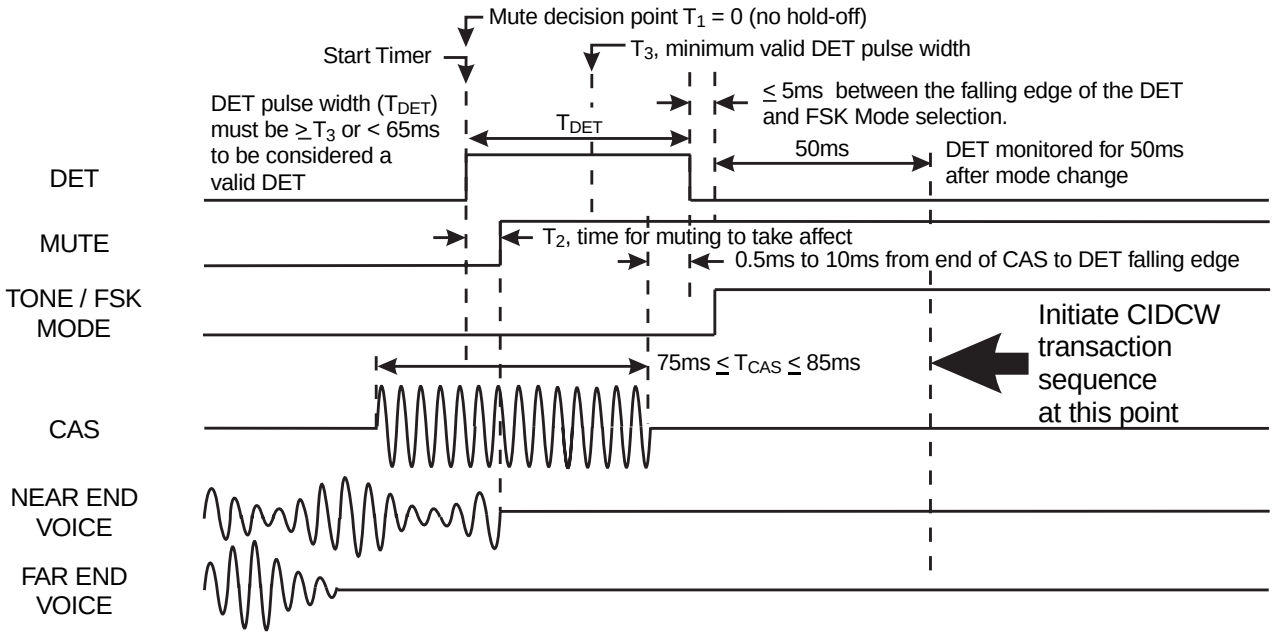
Note: The actual signal received by the MX602 is the sum of the CAS, Near-End Voice, and Far-End Voice signals.

Figure 21, Invalid CIDCW Transaction Initiation Adjunct Box Timing Sequence (DET pulse ≥ 65ms)



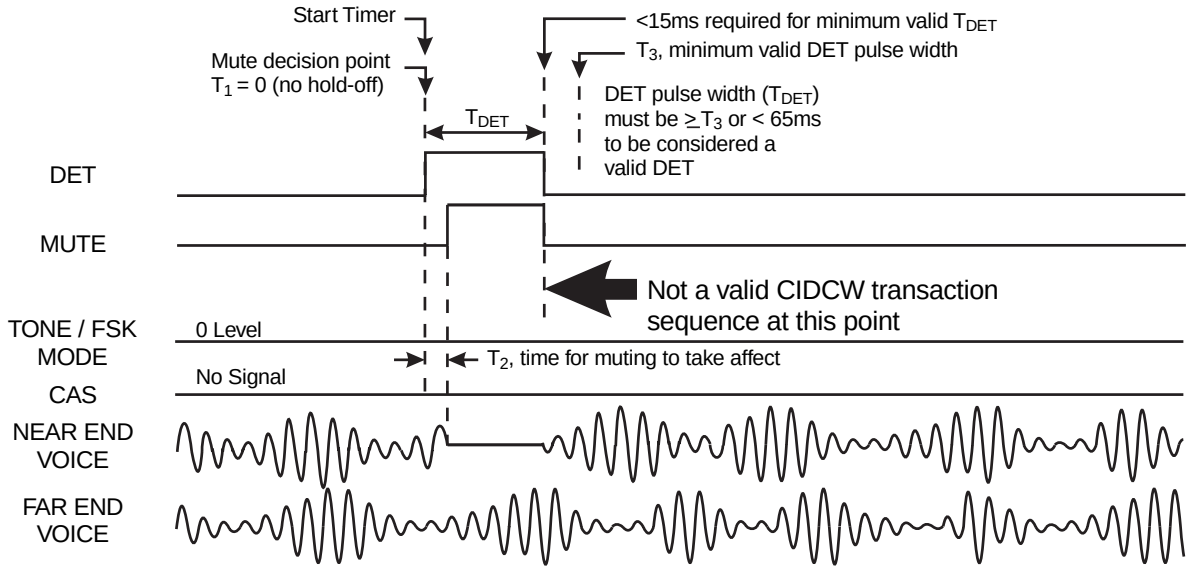
Note: The actual signal received by the MX602 is the sum of the CAS, Near-End Voice, and Far-End Voice signals.

Figure 22, Invalid CIDCW Transaction Initiation Adjunct Box Timing Sequence (DET output goes high during 50ms quiet period)



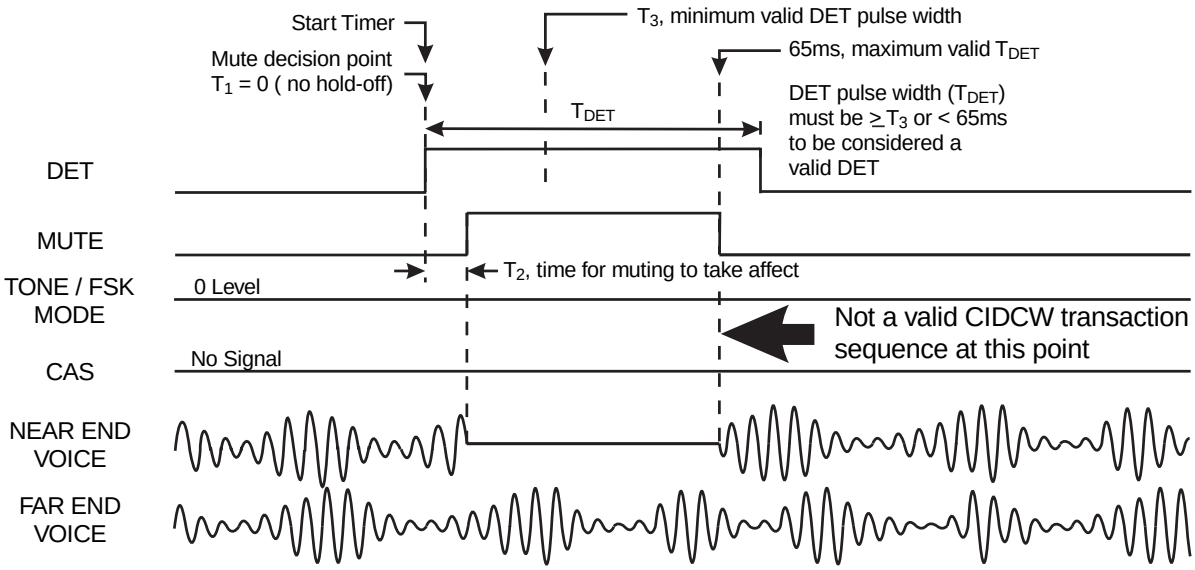
Note: The actual signal received by the MX602 is the sum of the CAS, Near-End Voice, and Far-End Voice signals.

Figure 23: Valid CIDCW Transaction Initiation Telephone Set Timing Sequence



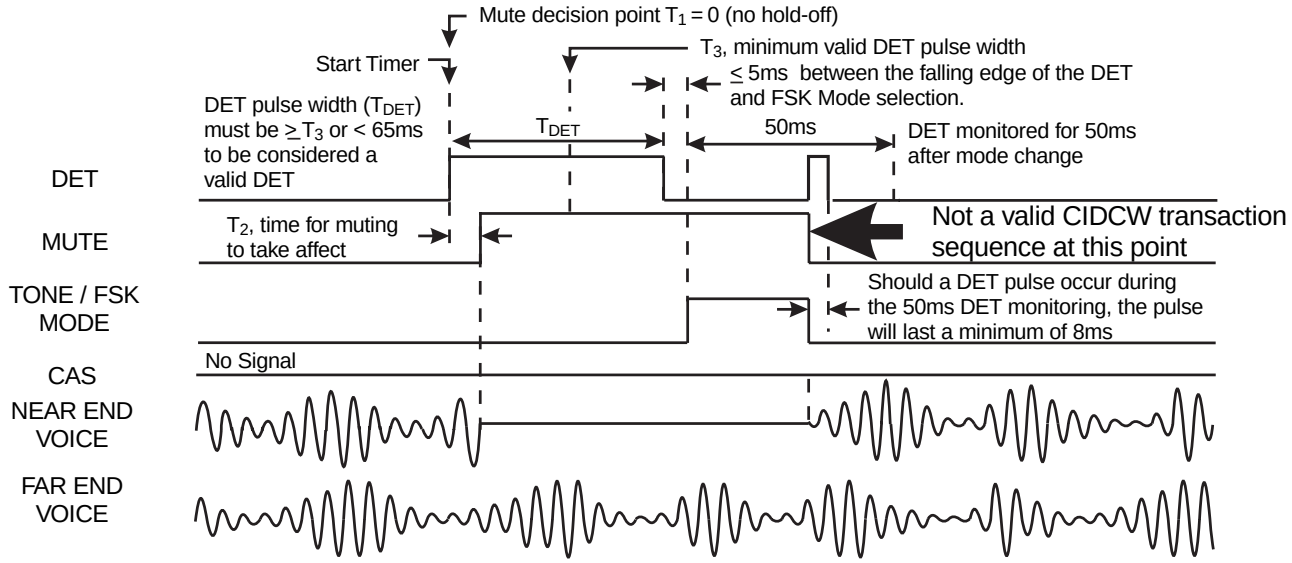
Note: The actual signal received by the MX602 is the sum of the CAS, Near-End Voice, and Far-End Voice signals.

Figure 24: Invalid CIDCW Transaction Initiation Telephone Set Timing Sequence (DET pulse < 15ms)



Note: The actual signal received by the MX602 is the sum of the CAS, Near-End Voice, and Far-End Voice signals.

Figure 25: Invalid CIDCW Transaction Initiation Telephone Set Timing Sequence (DET pulse ≥ 65ms)



Note: The actual signal received by the MX602 is the sum of the CAS, Near-End Voice, and Far-End Voice signals.

Figure 26: Invalid CIDCW Transaction Initiation Telephone Set Timing Sequence (DET output goes high during 50ms quiet period)

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - VSS)	-0.3	7.0	V
Voltage on any pin to VSS	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and VSS pins	-30	30	mA
Current into or out of any other pin	-20	20	mA
DW /DIP Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C°		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - VSS)		3.0	5.5	V
Operating Temperature		-40	85	°C
Xtal frequency	1	3.575965	3.583125	MHz

Operating Limits Notes:

1. A Xtal frequency of 3.579545MHz ±0.1% is required for correct Tone Alert and FSK detection.

Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 3.0V at T_{AMB} = 25°C and V_{DD} = 3.3V to 5.5V at T_{AMB} = - 40 to +85°C, V_{SS} = 0V
Xtal Frequency = 3.579545MHz ± 0.1%, 0dBV corresponds to 1.0V_{RMS}

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (ZP input high) at V_{DD} = 5.0V	1,2			1.0	µA
I_{DD} (ZP input low) at V_{DD} = 3.0V	1		0.5	1.0	mA
I_{DD} (ZP input low) at V_{DD} = 5.0V	1		1.0	2.0	mA
Logic 1 input level (RXCLK and XTAL inputs)		70%			V_{DD}
Logic 0 input level (RXCLK and XTAL inputs)				30%	V_{DD}
Logic input leakage current (V_{IN} = 0 to V_{DD}), XTAL input		-1.0		1.0	µA
Output logic 1 level (I_{OH} = 360µA)		V_{DD} - 0.4			V
Output logic 0 level (I_{OL} = 360µA)				0.4	V
$\overline{IRQ}$ output 'off' state current (V_{OUT} = V_{DD})				1.0	µA
Schmitt Trigger input thresholds (Figure 27)					
High going (Vt_{HI})		(0.56)(V_{DD})		(0.56)(V_{DD}) + 0.6	V
Low going (Vt_{LO})		(0.44)(V_{DD}) - 0.6		(0.44)(V_{DD})	V
Tone Alert Detector					
'Low' tone nominal frequency			2130		Hz
'High' tone nominal frequency			2750		Hz
Start of Tone Alert signal to DET high time (t_{DTON} Figure 9)			40		msec
End of Tone Alert signal to DET and $\overline{IRQ}$ low time (t_{DTOFF} Figure 9)		0.5		10.0	msec
To ensure detection:	3				
'Low' tone frequency tolerance				±20	Hz
'High' tone frequency tolerance				±30	Hz
Tone level of each simultaneously applied tone	4	-40.0		-2.2	dBV
2750Hz tone level with respect to 2130Hz tone level		-7.0		7.0	dB
Signal to Noise ratio	5	20.0			dB
Dual Tone Burst Duration		75			msec
To ensure non-detection:	6				
'Low' tone frequency tolerance		±75			Hz
'High' tone frequency tolerance		±95			Hz
Level (total)	4			-46.0	dBV
Dual Tone Burst Duration				25	msec
FSK Receiver					
Transmission rate		1188	1200	1212	Baud
V23 Mark (logic 1) frequency		1280	1300	1320	Hz
V23 Space (logic 0) frequency		2068	2100	2132	Hz
Bell202 Mark (logic 1) frequency		1188	1200	1212	Hz
Bell202 Space (logic 0) frequency		2178	2200	2222	Hz
Valid input level range	4	-40.0		-8.0	dBV

	Notes	Min.	Typ.	Max.	Units
Acceptable twist (mark level with respect to space level)					
V23s		-7.0		7.0	dB
Bell202		-10.0		10.0	dB
Acceptable Signal to Noise ratio					
V23	5	20.0			dB
Bell202	5	30.0			dB
Level Detector 'on' threshold level	4			-40.0	dBV
Level Detector 'off' to 'on' time (t_{FDON} Figure 6)				25.0	msec
Level Detector 'on' to 'off' time (t_{FDOFF} Figure 6)		8.0			msec
Input Signal Amplifier					
Input impedance	7	10.0			MΩ
Voltage gain			500		V/V
XTAL Input					
'High' pulse width	8	100			ns
'Low' pulse width	8	100			ns

Operating Characteristics Notes:

1. At 25°C, not including any current drawn from the MX602 pins by external circuitry other than X1, C1 and C2.
2. RD, MODE, RXCLK inputs at V_{SS}, ZP input at V_{DD}. See Figure 28
3. All conditions must be met to ensure detection.
4. For V_{DD} = 5.0V with equal level tones and with the input signal amplifier external components as section 3. The internal threshold levels are proportional to V_{DD}. For other supply voltages or different signal level ranges the voltage gain of the input signal amplifier should be adjusted by selecting the appropriate external components as described in section 4.2
5. Noise (either impulsive or random type that has a flat frequency spectrum at the frequency range of interest) in the 300Hz-3400Hz band for V23 and 200Hz-3200Hz for Bell202.
6. Meeting any of these conditions will ensure non-detection.
7. Open loop, small signal, low frequency measurements.
8. Timing for an external input to the CLOCK/XTAL pin.

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4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA

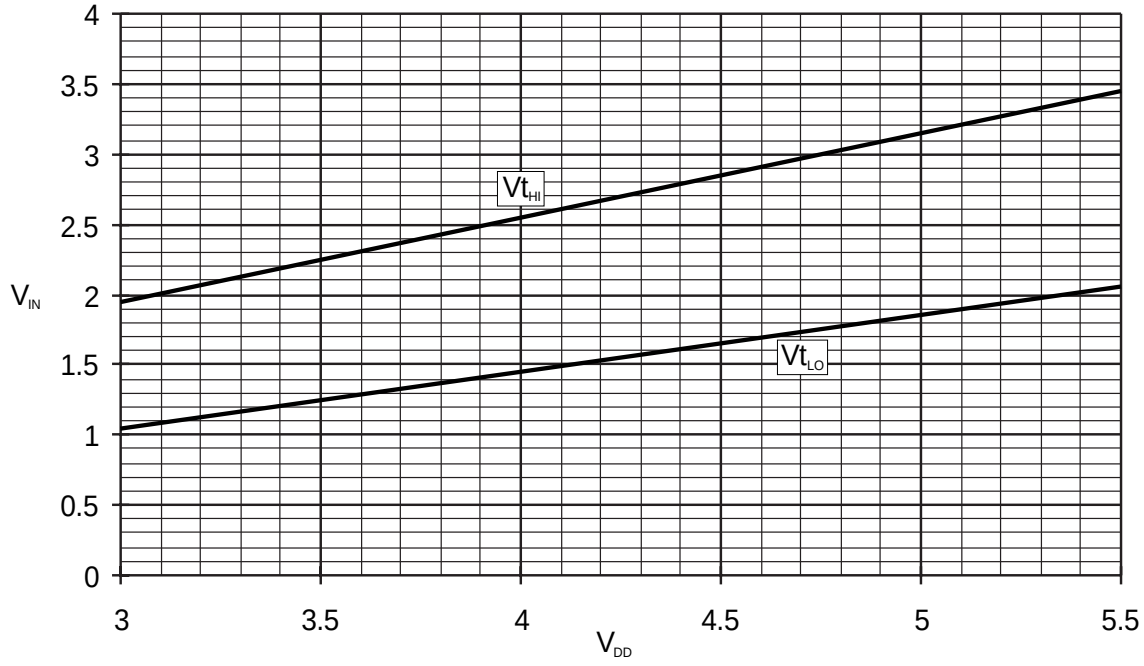


Figure 27: Schmitt Trigger typical input voltage thresholds vs. V_{DD}

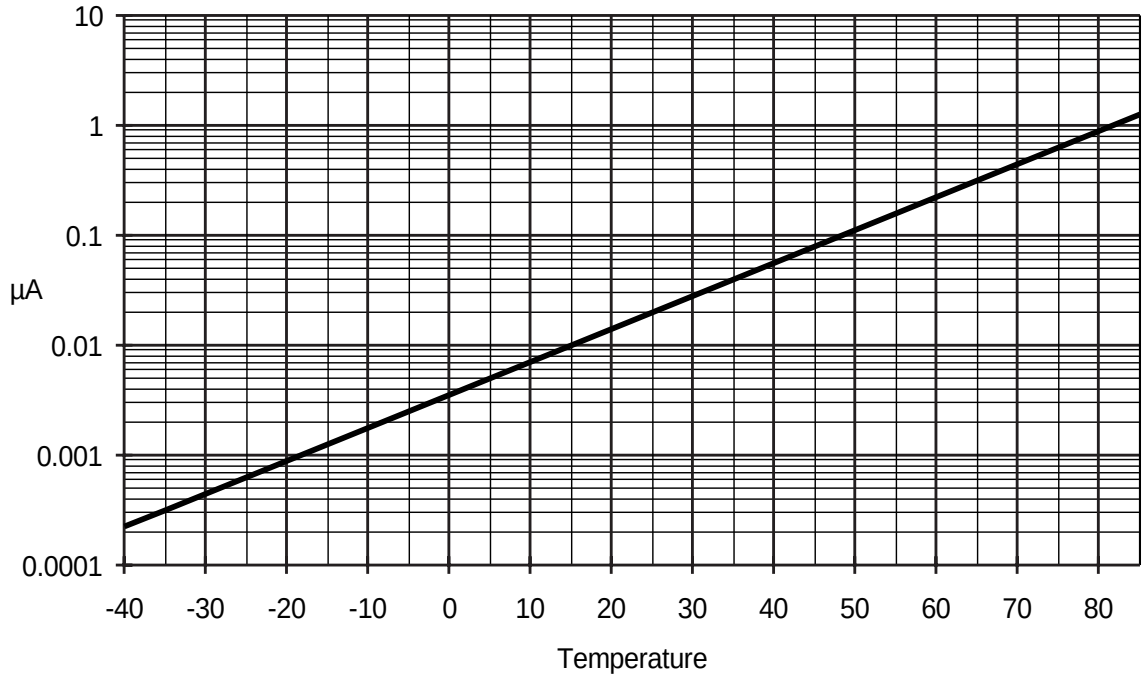
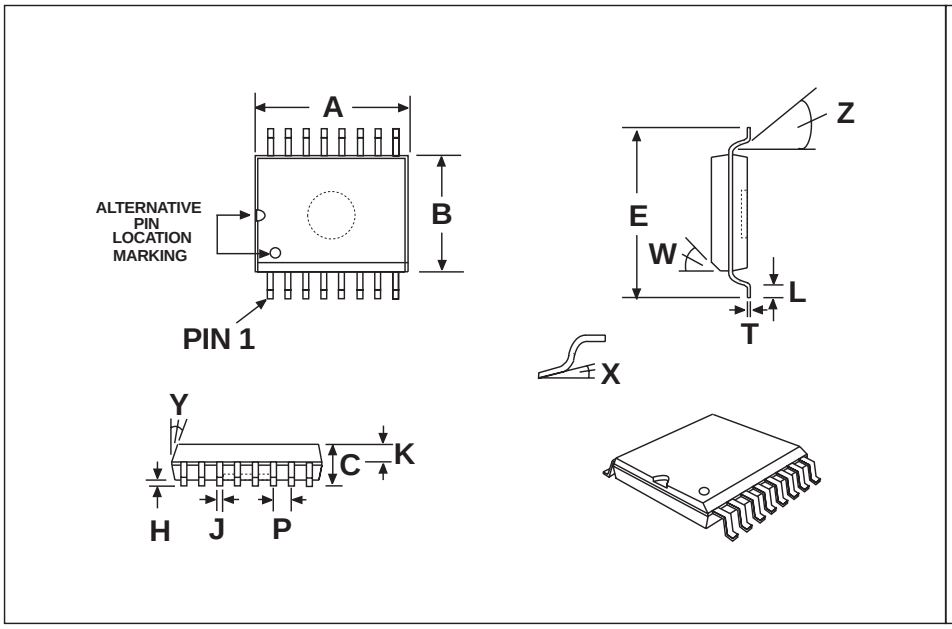


Figure 28: Typical 'Zero-Power' I_{DD} vs. Temperature (V_{DD} = 5.0V)

6.2 Packaging

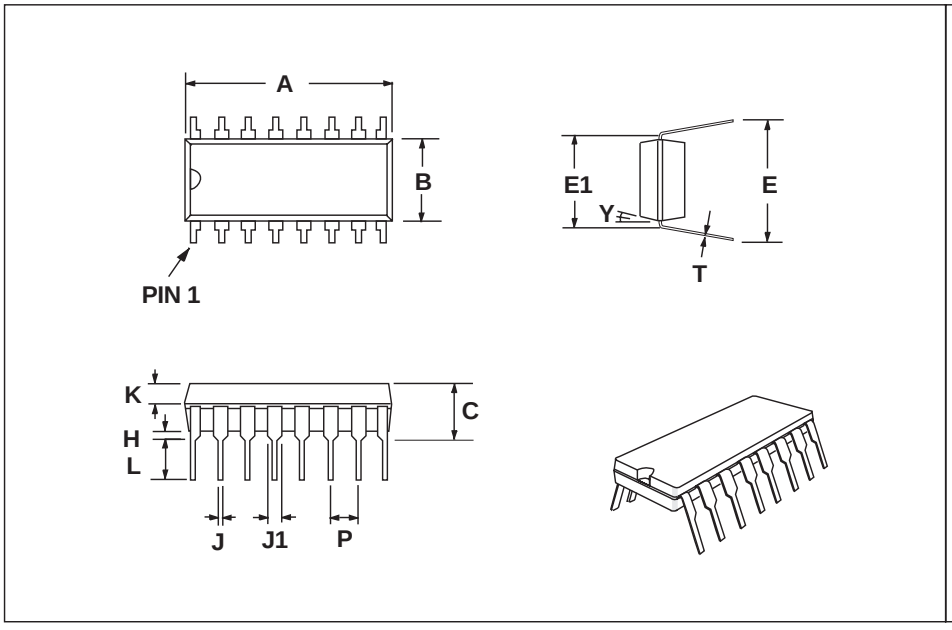


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 29 : 16-pin SOIC Mechanical Outline: ***Order as part no. MX602DW***



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 30 : 16-pin PDIP Mechanical Outline: ***Order as part no. MX602P***

CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.
These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

CML Microcircuits (USA) [formerly MX-COM, Inc.] Product Textual Marking

On CML Microcircuits (USA) products, the **'MX-COM'** textual logo is being replaced by a **'CML'** textual logo.

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