HT9288A/HT9288B

Dual PLLs for 45/48MHz Cordless Phone

Features

- Single 2.5 to 5.5V power supply
- On chip oscillator circuits with external X-TAL (10.240MHz)
- Synthesizer up to 10-channel pairs
- Base/Handset selected by MODE pin
- Maximum operating frequency: 60MHz@ Vin= 200mV$_{P-P}$
- Standby mode for power saving by $\overline{SB}$ pin
- Lock detect signal
- 5 kHz output for guard tone
- Standard 16-pin DIP/SOP/NSOP packages

Application

- Cordless phone System

General Description

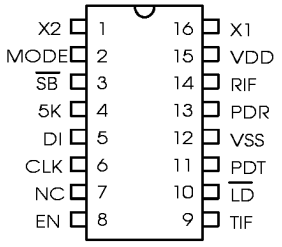
The HT9288A/9288B are dual phase-locked loop frequency synthesizers developed for 45/48MHz of 10-channel band frequency of cordless phone which are used in Mainland China.

These devices contain two mask-programmable counter ROMs for receive and transmit loops with two independent phase detect circuits.

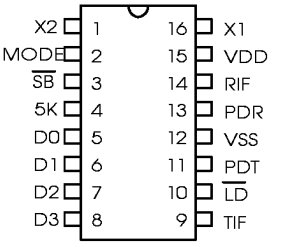
Frequency selection are accomplished by 4-bit parallel input for the HT9288B and serial interface for the HT9288A.

Other features include a lock detect circuit for the transmit loop and a 5.0 kHz tone output.

Pin Assignment



HT9288A
–16 DIP/SOP/NSOP



HT9288B
–16 DIP/SOP/NSOP

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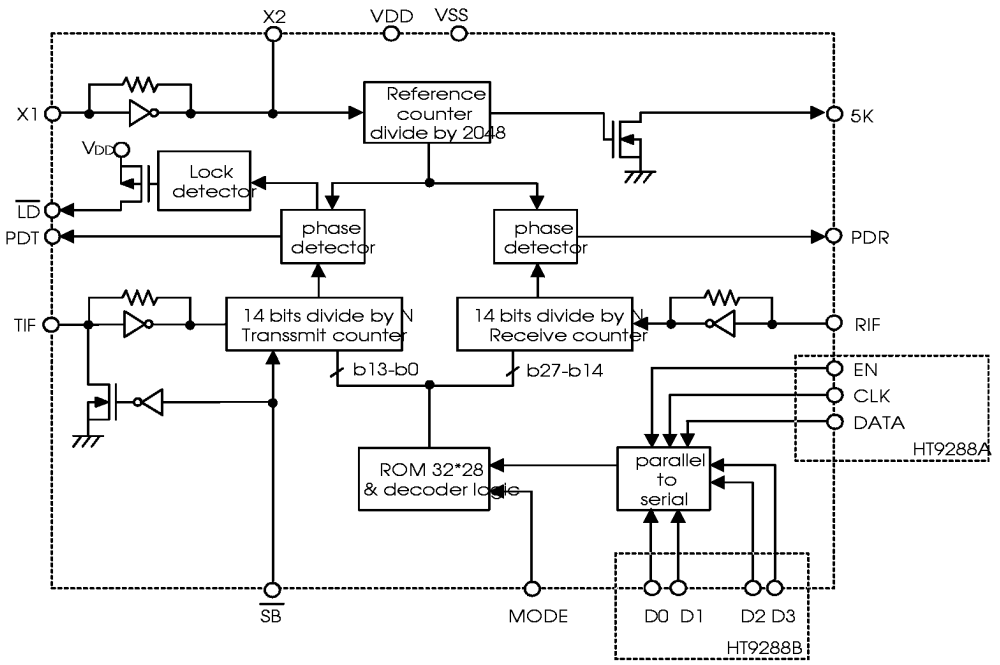
Block Diagram



Pad Description

Pin No	Pin Name	I/O	Function Description
1	X2	O	The output pin gererates reference frequency when it is connected to pin 16 with an external parallel-resonant crystal. For a 46/49MHz cordless phone application, a 10.24MHz crystal is need.
2	MODE	I	Mode is for determining whether this chip is to be used in the base or handset of a cordless phone. Internal, this pin is used in the decoding logic for selecting the ROM address. When V_{DD}=base mode, and when Vss=handset mode.
3	$\overline{SB}$	I	This pin is used to save power while no transmit and internal pull down. $\overline{SB}$: High, transmit and receive active. $\overline{SB}$: Low, receive acts only.
4	5K	O	The signal derived from the reference oscillator and reference divider, this output is n-channel open drain.

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Pin No	Pin Name	I/O	Function Description
5	D0 (LSB)	I	These inputs provide the BCD code for selecting the one of ten channels to be locked in both the transmit and received loop. When address data selects over 1-10, the decoding logic defaults to channel 10. The frequency assignments with D0-D3 are shows in Table 1. These inputs have internal pull down devices.
6	D1	I	
7	D2	I	
8	D3 (MSB)	I	
9	TIF	I	Input to 14-bit programmable transmit counter. The output signal from external VCO circuit can be ac coupled to this pin,the minimum input level is 200m V_{P-P}.
10	$\overline{LD}$	O	Lock detect signal associated with the transmit loop. V_{DD} level: indicate an out-off--lock condition. This is a p-channel open-drain output.
11	PDT	O	Phase detector output for transmit. PDT detects the phase error from transmit PLL and it's output is connected to external low pass filter.
12	VSS	—	Ground
13	PDR	I	Phase detector output for receive. PDR detects the phase error from receive PLL and it's output is connected to external low pass filter.
14	RIF	I	Input to 14-bit programmable receive counter. The output signal from external VCO circuit can be ac coupled to this pin, the minimum input level is 200m V_{P-P}.
15	VDD	—	Power supply
16	X1	I	Connect to the pin 1, external parallel-resonant crystal and capacitor.
5	DI (HT9288A only)	I	The serial input data pin.
6	CLK (HT9288A only)	I	Clock input. Each low to high trnasition of the clock shifts one bit of data into the on-chip shift register.
7	NC	—	No connection
8	EN (HT 9288A only)	I	The enable pin controls the data transfer from the shift register to the 4-bit latch. A low to high transition latches the data.

Absolute Maximum Ratings

DC supply voltage.....–0.5 to 6V
Input voltage ..... –0.5 to V_{DD}+0.5V
DC current drain per pin 10mA
Operating temperature range..... –30 to 75°C
Storage temperature range ..... –65 to 150°C
DC current drain V_{DD} or V_{SS} pins.....30mA

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D. C. Characteristics

(T_A=25°C)

Symbol	Characteristic	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Power Supply Voltage	—	—	2.5	—	5.5	V
V_{OH}	Output Voltage	2.5V 5.5V	—	2.45 5.45	— —	— —	V
V_{OL}		2.5V 5.5V	—	— —	— —	0.05 0.05	
V_{IH}	Input Voltage	2.5V 5.5V	—	1.75 3.85	— —	— —	V
V_{IL}		2.5V 5.5V	—	— —	— —	0.75 1.65	
I_{OH}	Output Current	2.5V 5.5V	V_{OUT}= 2.2V V_{OUT}= 5.0V	–0.18 –0.55	— —	— —	mA
I_{OL}		2.5V 5.5V	V_{OUT}= 0.3V V_{OUT}= 0.5V	— —	— —	0.18 0.55	
I_{IH}	Input Current	2.5V 5.5V	X_1, TIF, RIF	— —	— —	–30 –66	µA
		2.5V 5.5V	DATA, $\overline{SB}$, MODE	— —	— —	–0.05 –0.11	
I_{IL}		2.5V 5.5V	X_1, TIF, RIF	— —	— —	30 66	
		2.5V 5.5V	DATA, $\overline{SB}$, MODE	— —	— —	50 121	
I_{STB}	Standby Current	2.5V 5.5V	Note 1	— —	— —	1.4 3.6	mA
I_{DD}	Operating Current	2.5V 5.5V	Note 2	— —	— —	2.8 6.2	mA
I_{OZ}	Three-State Leakage Current	5.5V	—	—	—	±1	µA

Note 1: X1: 10.240MHz; MODE: V_{DD}; $\overline{SB}$: V_{SS}; others are open.

Note 2: X2: 10.240MHz; MODE: V_{DD}; $\overline{SB}$: V_{DD}; others are open. (200 mV_{P-P} input at RIF, TIF)

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A. C. Characteristics

Symbol	Characteristic	Test Condition		Min	Typ.	Max	Unit
		V_{DD}	Condition				
t_{TLH}	Output Rise Time	3V 5V	Figure 1	—	— —	200 100	ns
t_{THL}	Output Fall Time	3V 5V	Figure 1	—	— —	200 100	ns
T_R	Input Rise Time	3V 5V	Figure 2	—	— —	5 4	μA
T_F	Input Fall Time	3V 5V	Figure 2	—	— —	5 4	μA
F_{MAX}	Input Frequency	3V 5V	X1 TIF input= Sine Wave 200 mV_{P-P} RIF	—	— —	12 60 60	MHz
t_{SU}	Setup Time: data to clock (HT9288A) Setup Time: enable to clock (HT9288A)	3V 3V	Figure 3	100 200	— — — —	— — — —	ns
t_H	Hold Time: clock to data (HT9288A)	3V	Figure 3	80	— —	— —	ns
t_{REC}	Recovery Time: enable to clock (HT9288A)	3V	Figure 4	80	— —	— —	ns
t_W	Input pulse width: clock and enable (HT9288A)	3V	Figure 4	80	— —	— —	ns

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Function Description

The HT9288A/HT9288B are dual phase-locked loop frequency synthesizers developed for 45/48MHz of 10-channel band frequency of cordless phone which are used in Mainland China.

To accomplish the duplex communication in cordless phone system it must use two different channels to reach the function.

See the table 1 which show the receive channel and transmit channel between base and handset. If any channel of base and handset account inter fereuce while radio link, these devices can select another pair to improve the quality of communication.

The $\overline{SB}$ pin is used to save power when not transmitting. IF $\overline{SB}$ is high both the transmit and receive loops are in operating eles transmit loop is disabled Figure 5 show the cordless phone opplication diagram.

Table 1 Divide Ratios and VCO Frequencies Base (MODE=1)

Input				CH	Rx (Fref=5KHz)			Tx=(Fref=5KHz)		
D3	D2	D1	D0		FR_X (MHz)	FVCO (MHz)	N	FT_X (MHz)	FVCO (MHz)	N
0	0	0	1	1	48.250	37.555	7511	45.250	45.250	9050
0	0	1	0	2	48.275	37.580	7516	45.275	45.275	9055
0	0	1	1	3	48.300	37.605	7521	45.300	45.300	9060
0	1	0	0	4	48.325	37.630	7526	45.325	45.325	9065
0	1	0	1	5	48.350	37.655	7531	45.350	45.350	9070
0	1	1	0	6	48.375	37.680	7536	45.375	45.375	9075
0	1	1	1	7	48.400	37.705	7541	45.400	45.400	9080
1	0	0	0	8	48.425	37.730	7546	45.425	45.425	9085
1	0	0	1	9	48.450	37.755	7551	45.450	45.450	9090
1	0	1	0	10	48.475	37.780	7556	45.475	45.475	9095
1	0	1	1	10	48.475	37.780	7556	45.475	45.475	9095
1	1	0	0	10	48.475	37.780	7556	45.475	45.475	9095
1	1	0	1	10	48.475	37.780	7556	45.475	45.475	9095
1	1	1	0	10	48.475	37.780	7556	45.475	45.475	9095
1	1	1	1	10	48.475	37.780	7556	45.475	45.475	9095
0	0	0	0	10	48.475	37.780	7556	45.475	45.475	9095

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Remote (MODE=0)

Input				CH	Rx (Fref=5KHz)			Tx=(Fref=5KHz)		
D3	D2	D1	D0		$FR_{X(MHz)}$	FVCO (MHz)	N	FTX(MHz)	FVCO (MHz)	N
0	0	0	1	1	45.250	34.555	6911	48.250	48.250	9650
0	0	1	0	2	45.275	34.580	6916	48.275	48.275	9655
0	0	1	1	3	45.300	34.605	6921	48.300	48.300	9660
0	1	0	0	4	45.325	34.630	6926	48.325	48.325	9665
0	1	0	1	5	45.350	34.655	6931	48.350	48.350	9670
0	1	1	0	6	45.375	34.680	6936	48.375	48.375	9675
0	1	1	1	7	45.400	34.705	6941	48.400	48.400	9680
1	0	0	0	8	45.425	34.730	6946	48.425	48.425	9685
1	0	0	1	9	45.450	34.755	6951	48.450	48.450	9690
1	0	1	0	10	45.475	34.780	6956	48.475	48.475	9695
1	0	1	1	10	45.475	34.780	6956	48.475	48.475	9695
1	1	0	0	10	45.475	34.780	6956	48.475	48.475	9695
1	1	0	1	10	45.475	34.780	6956	48.475	48.475	9695
1	1	1	0	10	45.475	34.780	6956	48.475	48.475	9695
1	1	1	1	10	45.475	34.780	6956	48.475	48.475	9695
0	0	0	0	10	45.475	34.780	6956	48.475	48.475	9695

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Timing Diagram

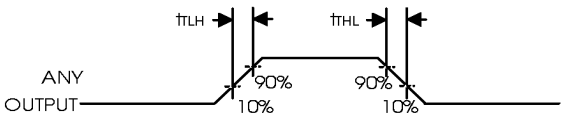

Figure 1

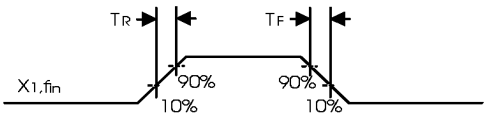

Figure 2

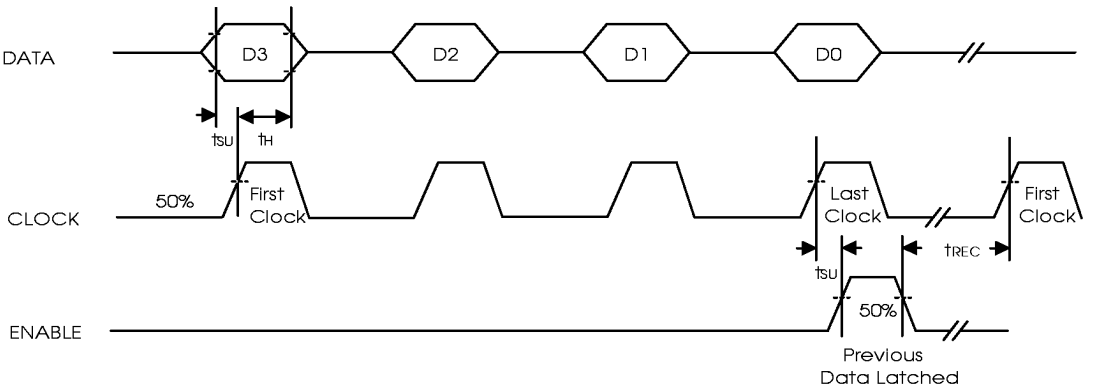

Figure 3

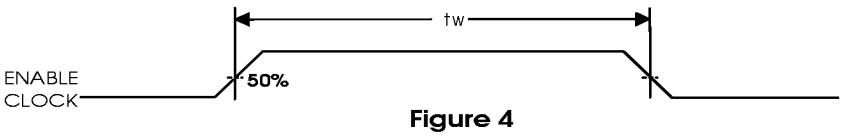

Figure 4

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Application Circuit

HT9288A/HT9288B

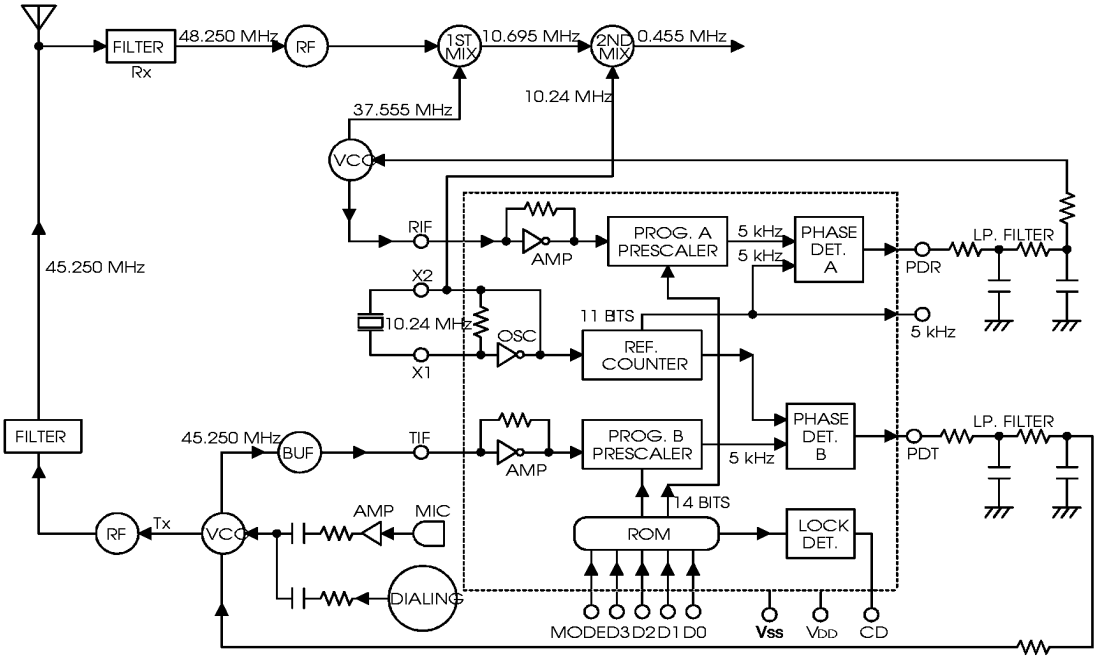

Figure 5

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