IXYS

IXLD426/427/428
Dual Power MOSFET Driver
• Low Power Latch Resistant CMOS
• 30 ns Rise Time

General Description

The IXLD426/427/428 are dual CMOS high speed drivers. A TTL/CMOS input voltage level is translated into an output voltage level swing equalling the supply. The CMOS output will be within 25 mV of ground or positive supply. Bipolar designs are capable of swinging only within 1 volt of the supply.

The low impedance high current driver outputs will swing a 1000 pf load 18 V in 30 ns. The unique current and voltage drive qualities make the IXLD426/427/428 ideal power MOSFET drivers, line drivers and DC to DC converter building blocks.

Input logic signals may equal the power supply voltage. Input current is a low 1 μA making direct interface to CMOS/BIPOLAR switch mode power supply control integrated circuits possible as well as open collector analog comparators.

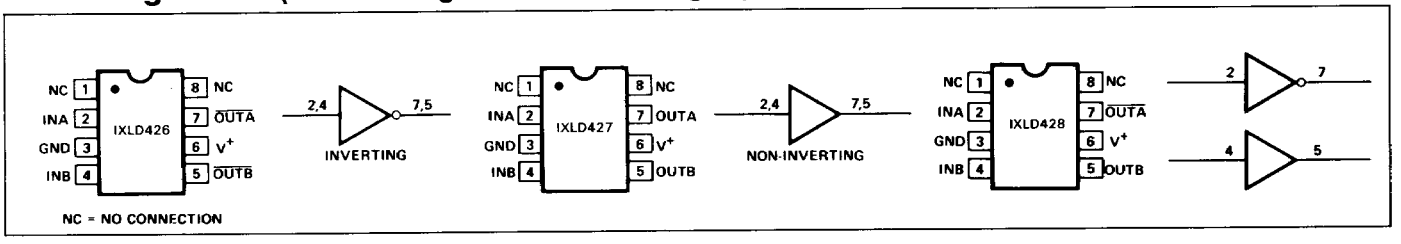
Quiescent power supply current is 8 mA maximum. The IXLD426 requires 1/5 the current of the pin compatible bipolar DS0026 device. This is important in DC to DC converter applications with power efficiency constraints and high frequency switch mode power supply applications. Quiescent current is typically 6 mA when driving a 1000 pf load 18 V at 100 kHz.

The inverting IXLD426 driver is pin compatible with the bipolar DS0026 and MMH0026 devices. The IXLD427 is non-inverting; the IXLD428 contains an inverting and non-inverting driver.

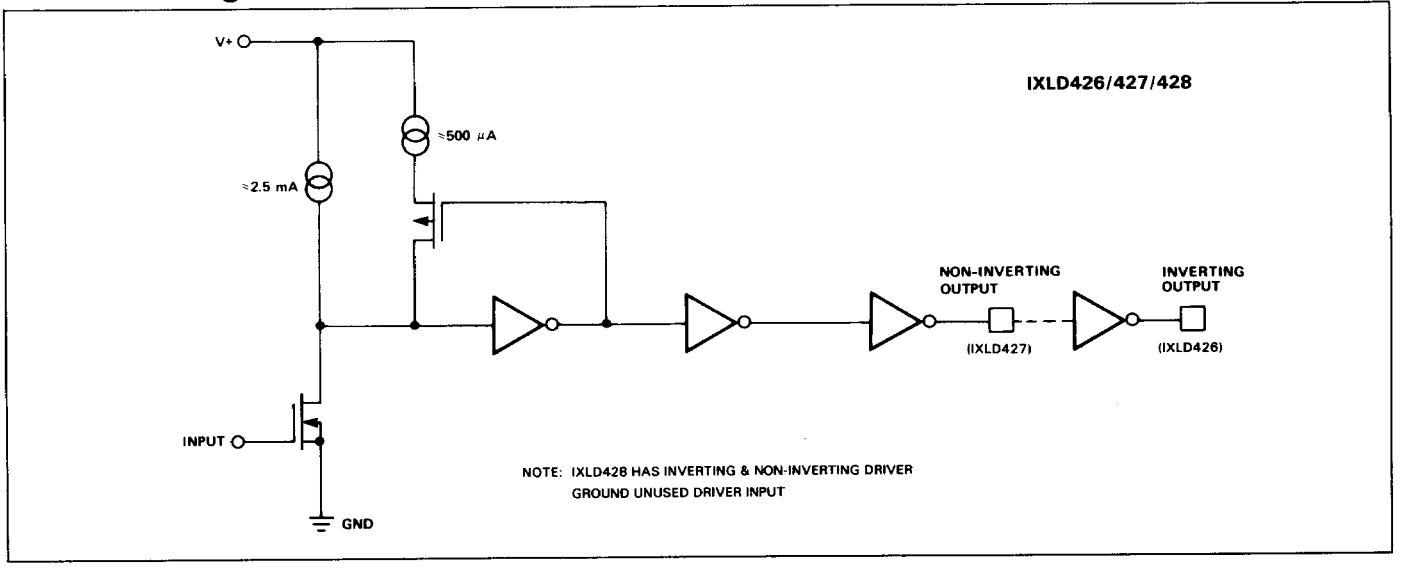
Features

- High Speed Switching (C_L = 1000 pf) . . . . . 30 ns
- High Peak Output Current . . . . . 1.5 A
- High Output Voltage Swing . . . . . V_S – 25 mV
  GND + 25 mV
- Low Input Current (Logic "0" or "1") . . . . . 1 μA
- TTL/CMOS Input Compatible
- Available in Inverting & Non-Inverting Configurations
- Wide Operating Supply Voltage . . . . . 4.5 V to 18 V
- Low Power Consumption (Inputs Low) . . . . . 0.4 mA
  (Inputs High) . . . . . 8 mA
- Single Supply Operation
- Low Output Impedance . . . . . 6 Ω
- Pin Out Equivalent to DS0026 & MMH0026

Pin Configuration (See Ordering Information on Page 6)



Functional Diagram



Absolute Maximum Ratings (Notes 1, 2, 3)

Power Dissipation
- Plastic . . . . . 500 mW
- CerDIP . . . . . 800 mW

Derating Factors
- Plastic . . . . . 5.6 mW/°C Above 36°C
- CerDIP . . . . . 6.0 mW/°C

Supply Voltage . . . . . 20 V

Input Voltage Any Terminal . . Vs + 0.3 V to Ground −0.3 V

Operating Temperature
- M Version . . . . . −55°C to +125°C
- I Version . . . . . −25°C to +85°C
- C Version . . . . . 0°C to +70°C

Maximum Chip Temperature . . . . . +150°C

Storage Temperature . . . . . −55°C to +150°C

Lead Temperature (10 Sec) . . . . . 300°C

IXLD426
Electrical Characteristics: T_A = 25°C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	IXLD426 MIN	IXLD426 TYP	IXLD426 MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	2	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	3	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	−1	—	1	µA
OUTPUT	4	V_{OH}	High Output Voltage		V_S − 0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V
	6	R_O	Output Resistance	V_{IN} = 0.8 V, I_{OUT} = 10 mA, V_S = 18 V	—	10	15	Ω
	7	R_O	Output Resistance	V_{IN} = 2.4 V, I_{OUT} = 10 mA, V_S = 18 V	—	6	10	Ω
	8	I_{PK}	Peak Output Current		—	1.5	—	A
SWITCHING TIME	9	T_R	Rise Time	Test Figure 1	—	—	30	ns
	10	T_F	Fall Time	Test Figure 1	—	—	20	ns
	11	T_{D1}	Delay Time	Test Figure 1	—	—	40	ns
	12	T_{D2}	Delay Time	Test Figure 1	—	—	75	ns
POWER SUPPLY	13	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	8.0	mA
	14	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.4	mA

IXLD426
Electrical Characteristics: Over operating temperature range with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	IXLD426 MIN	IXLD426 TYP	IXLD426 MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	2	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	3	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	−10	—	10	µA
OUTPUT	4	V_{OH}	High Output Voltage		V_S − 0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V

Dual Power MOSFET Driver

- Low Power Latch Resistant CMOS
- 30 ns Rise Time

IXLD426/427/428

IXLD426

Electrical Characteristics: Over operating temperature range with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	IXLD426 MIN	IXLD426 TYP	IXLD426 MAX	UNIT
OUTPUT	6	R_O	Output Resistance	V_{IN} = 0.8 V, I_{OUT} = 10 mA, V_S = 18 V	—	13	20	Ω
	7	R_O	Output Resistance	V_{IN} = 2.4 V, I_{OUT} = 10 mA, V_S = 18 V	—	8	15	Ω
SWITCHING TIME	8	T_R	Rise Time	Test Figure 1	—	—	60	ns
	9	T_F	Fall Time	Test Figure 1	—	—	40	ns
	10	T_{D1}	Delay Time	Test Figure 1	—	—	60	ns
	11	T_{D2}	Delay Time	Test Figure 1	—	—	120	ns
POWER SUPPLY	12	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	12.0	mA
	13	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.6	mA

IXLD427

Electrical Characteristics: T_A = 25°C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	IXLD427 MIN	IXLD427 TYP	IXLD427 MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	2	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	3	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	−1	—	1	μA
OUTPUT	4	V_{OH}	High Output Voltage		V_S − 0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V
	6	R_O	Output Resistance	V_{IN} = 2.4 V, I_{OUT} = 10 mA, V_S = 18 V	—	10	15	Ω
	7	R_O	Output Resistance	V_{IN} = 0.8 V, I_{OUT} = 10 mA, V_S = 18 V	—	6	10	Ω
	8	I_{PK}	Peak Output Current		—	1.5	—	A
SWITCHING TIME	9	T_R	Rise Time	Test Figure 1	—	—	30	ns
	10	T_F	Fall Time	Test Figure 1	—	—	20	ns
	11	T_{D1}	Delay Time	Test Figure 1	—	—	40	ns
	12	T_{D2}	Delay Time	Test Figure 1	—	—	75	ns
POWER SUPPLY	13	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	8.0	mA
	14	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.4	mA

NOTES:

1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Switching times guaranteed by design.

IXLD427

Electrical Characteristics: Over operating temperature range with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	IXLD427 MIN	TYP	MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	–	–	V
	2	V_{IL}	Logic 0 Input Voltage		–	–	0.8	V
	3	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	–10	–	10	µA
OUTPUT	4	V_{OH}	High Output Voltage		V_S –0.025	–	–	V
	5	V_{OL}	Low Output Voltage		–	–	0.025	V
	6	R_O	Output Resistance	V_{IN} = 2.4 V I_{OUT} = 10 mA, V_S = 18 V	–	13	20	Ω
	7	R_O	Output Resistance	V_{IN} = 0.8 V I_{OUT} = 10 mA, V_S = 18 V	–	8	15	Ω
SWITCHING TIME	8	T_R	Rise Time	Test Figure 1	–	–	60	ns
	9	T_F	Fall Time	Test Figure 1	–	–	40	ns
	10	T_{D1}	Delay Time	Test Figure 1	–	–	60	ns
	11	T_{D2}	Delay Time	Test Figure 1	–	–	120	ns
POWER SUPPLY	12	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	–	–	12.0	mA
	13	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	–	–	0.6	mA

IXLD428

Electrical Characteristics: T_A = 25°C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	IXLD428 MIN	TYP	MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	–	–	V
	2	V_{IL}	Logic 0 Input Voltage		–	–	0.8	V
	3	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	–1	–	1	µA
OUTPUT	4	V_{OH}	High Output Voltage		V_S –0.025	–	–	V
	5	V_{OL}	Low Output Voltage		–	–	0.025	V
	6	R_O	Output Resistance	Output High I_{OUT} = 10 mA, V_S = 18 V	–	10	15	Ω
	7	R_O	Output Resistance	Output Low I_{OUT} = 10 mA, V_S = 18 V	–	6	10	Ω
	8	I_{PK}	Peak Output Current		–	1.5	–	A

NOTES:
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Switching times guaranteed by design.

IXLD428
Electrical Characteristics: T_A = 25°C with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	IXLD428 MIN	IXLD428 TYP	IXLD428 MAX	UNIT
SWITCHING TIME	9	T_R	Rise Time	Test Figure 1	—	—	30	ns
	10	T_F	Fall Time	Test Figure 1	—	—	20	ns
	11	T_{D1}	Delay Time	Test Figure 1	—	—	40	ns
	12	T_{D2}	Delay Time	Test Figure 1	—	—	75	ns
POWER SUPPLY	13	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	8.0	mA
	14	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.4	mA

IXLD428
Electrical Characteristics: Over operating temperature range with 4.5 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	IXLD428 MIN	IXLD428 TYP	IXLD428 MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	—	—	V
	2	V_{IL}	Logic 0 Input Voltage		—	—	0.8	V
	3	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	−10	—	10	µA
OUTPUT	4	V_{OH}	High Output Voltage		V_S −0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V
	6	R_O	Output Resistance	Output High I_{OUT} = 10 mA, V_S = 18 V	—	13	20	Ω
	7	R_O	Output Resistance	Output Low I_{OUT} = 10 mA, V_S = 18 V	—	8	15	Ω
SWITCHING TIME	8	T_R	Rise Time	Test Figure 1	—	—	60	ns
	9	T_F	Fall Time	Test Figure 1	—	—	40	ns
	10	T_{D1}	Delay Time	Test Figure 1	—	—	60	ns
	11	T_{D2}	Delay Time	Test Figure 1	—	—	120	ns
POWER SUPPLY	12	I_S	Power Supply Current	V_{IN} = 3.0 V (Both Inputs)	—	—	12.0	mA
	13	I_S	Power Supply Current	V_{IN} = 0.0 V (Both Inputs)	—	—	0.6	mA

NOTES:
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Switching times guaranteed by design.

Ordering Information

Part No.	Package	Configuration	Temperature Range
IXLD426CPA	8-Pin Plastic Dip	Inverting	0°C to +70°C
IXLD426IJA*	8-Pin CerDIP	Inverting	−25°C to +85°C
IXLD426MJA*	8-Pin CerDIP	Inverting	−55°C to +125°C
IXLD427CPA	8-Pin Plastic Dip	Non-Inverting	0°C to +70°C
IXLD427IJA*	8-Pin CerDIP	Non-Inverting	−25°C to +85°C
IXLD427MJA*	8-Pin CerDIP	Non-Inverting	−55°C to +125°C
IXLD428CPA	8-Pin Plastic Dip	Non-Inv. & Inv.	0°C to +70°C
IXLD428IJA*	8-Pin CerDIP	Non-Inv. & Inv.	−25°C to +85°C
IXLD428MJA*	8-Pin CerDIP	Non-Inv. & Inv.	−55°C to +125°C
IXLD426C/Y	CHIP	Inverting	25°C
IXLD427C/Y	CHIP	Non-Inverting	25°C
IXLD428C/Y	CHIP	Non-Inv. & Inv.	25°C

* For devices with 125°C, 160 Hour Burn In add /BI to part number suffix.

Switching Time Test Circuits

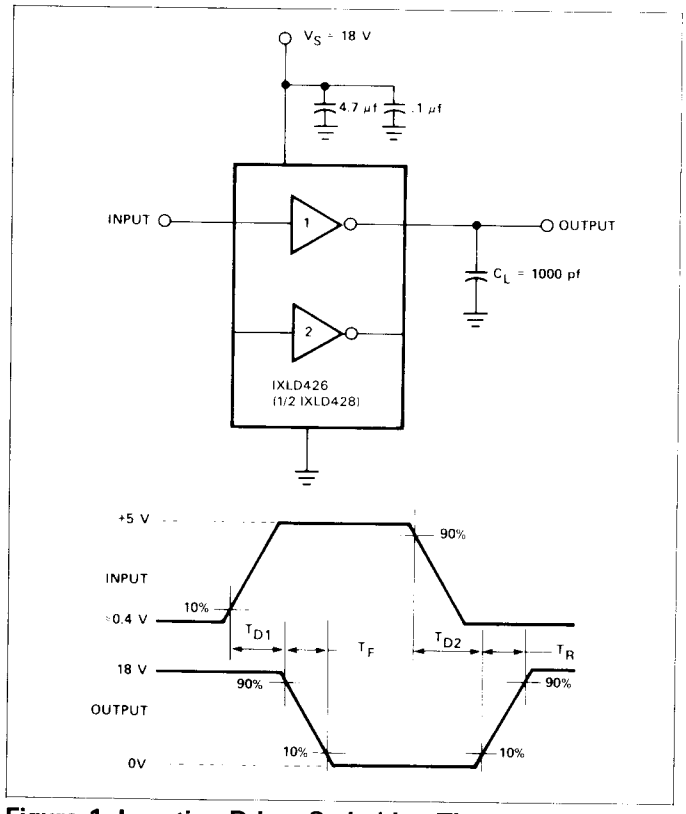


Figure 1: Inverting Driver Switching Time

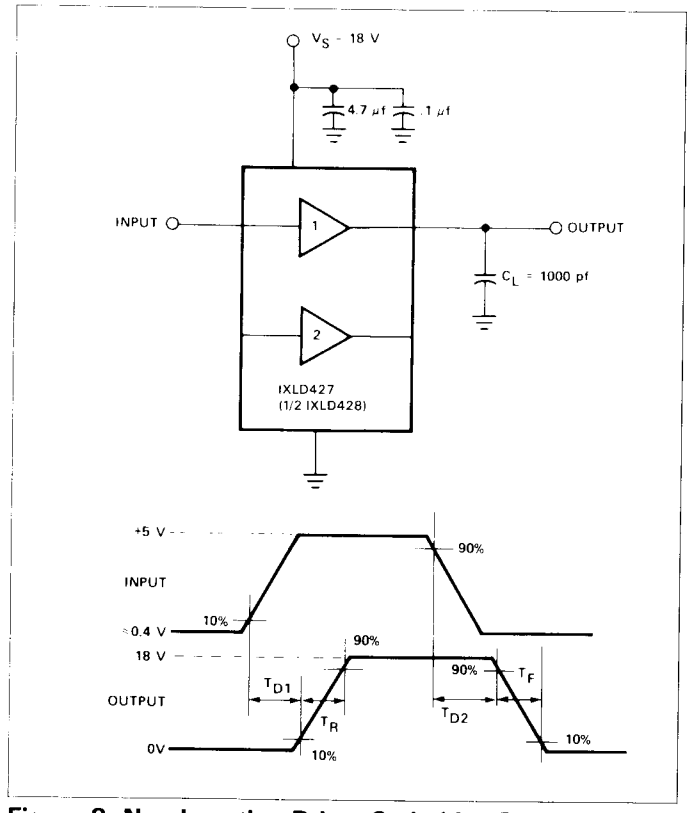
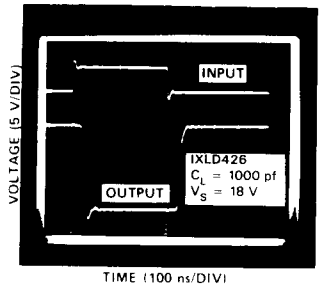
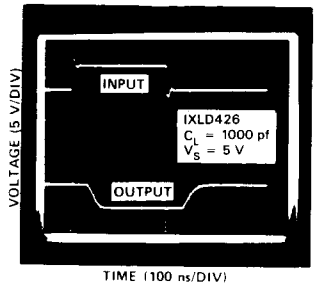


Figure 2: Non-Inverting Driver Switching Time

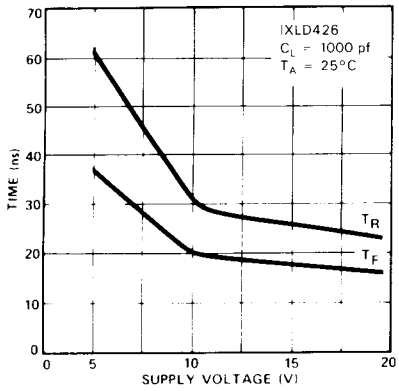


IXLD426 Switching Speed

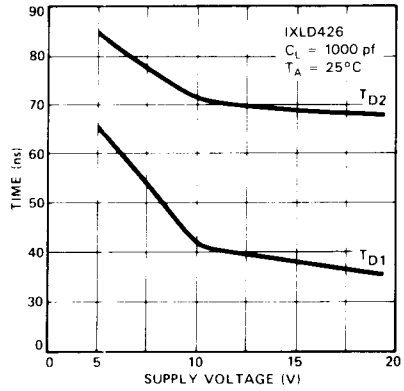


Typical Characteristic Curves

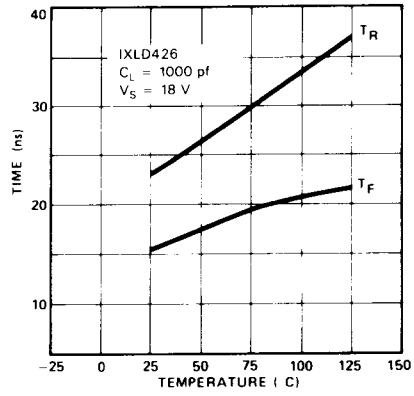
Rise and Fall Time vs Supply Voltage



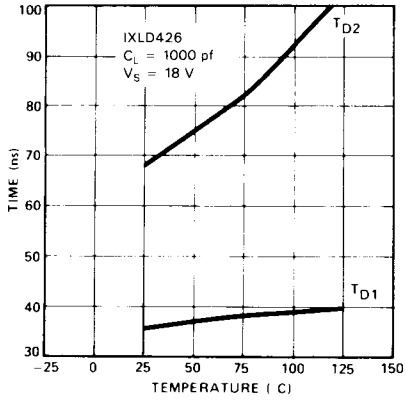
Delay Time vs Supply Voltage



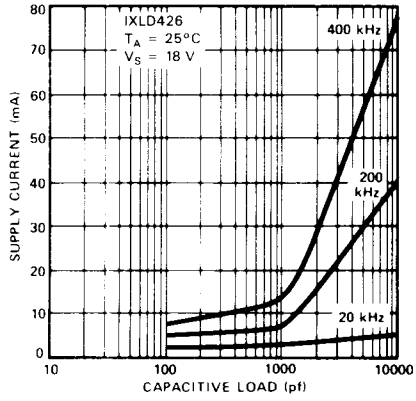
Rise and Fall Time vs Temperature



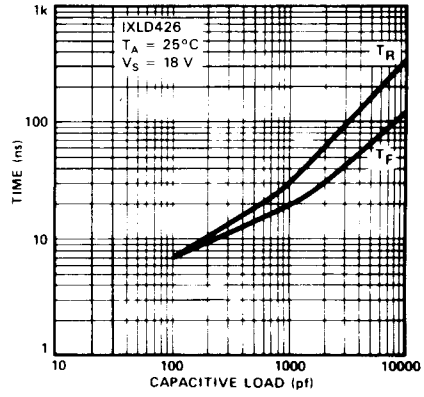
Delay Time vs Temperature



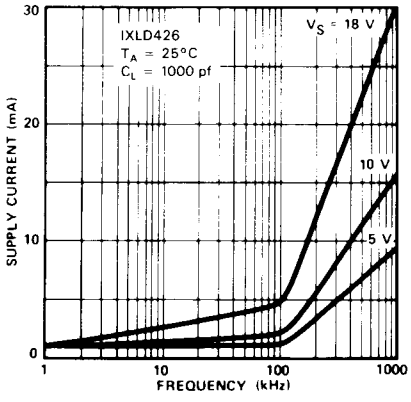
Supply Current vs Capacitive Load



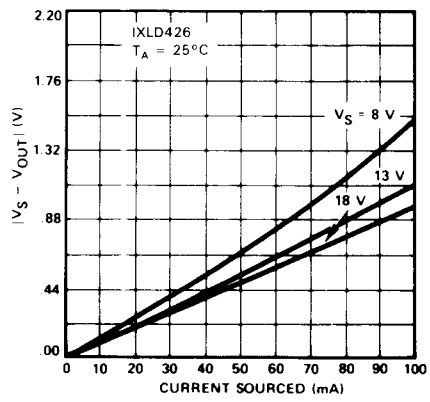
Rise and Fall Time vs Capacitive Load



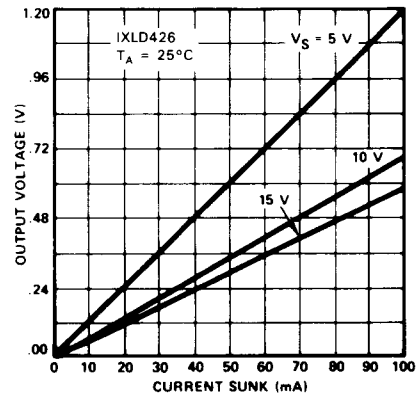
Supply Current vs Frequency



High Output vs Voltage

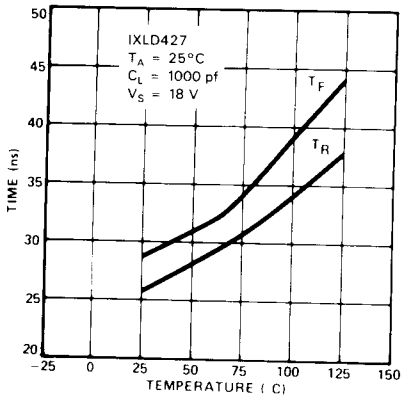


Low Output Voltage

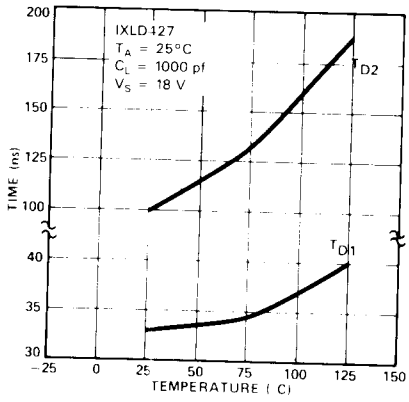


Typical Characteristic Curves

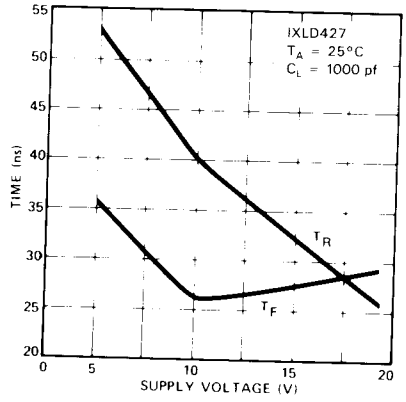
Rise and Fall Time vs Temperature



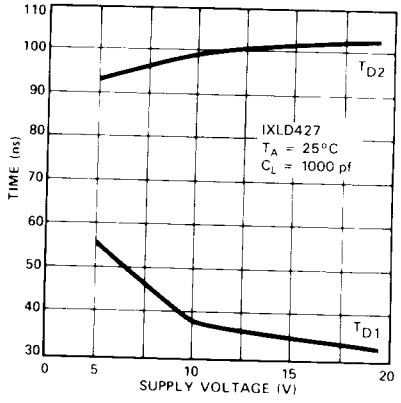
Delay Time vs Temperature



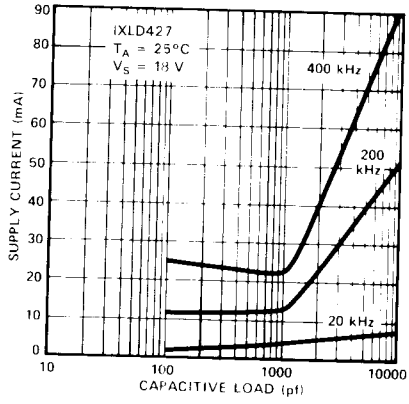
Rise and Fall Time vs Supply Voltage



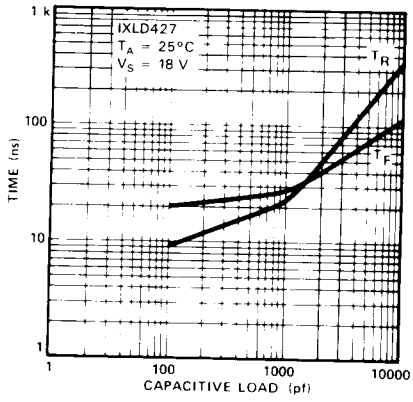
Delay Time vs Supply Voltage



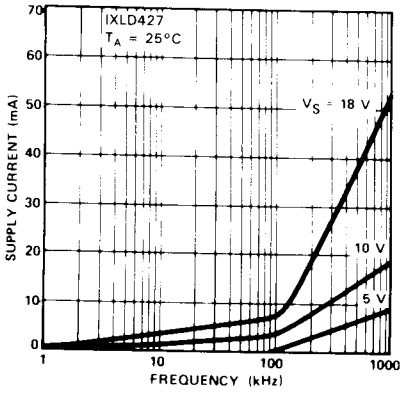
Supply Current vs Capacitive Load



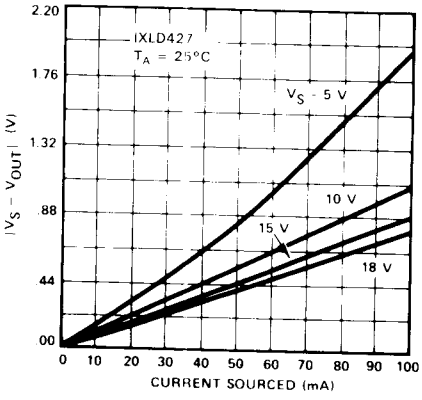
Rise and Fall Time vs Capacitive Load



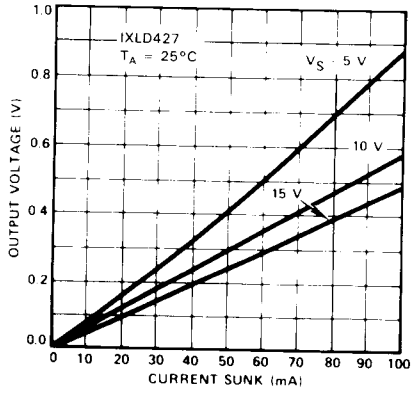
Supply Current vs Frequency



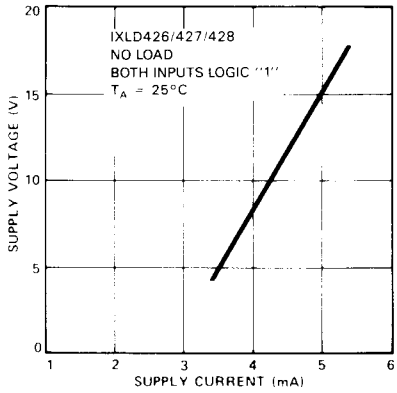
High Output Voltage



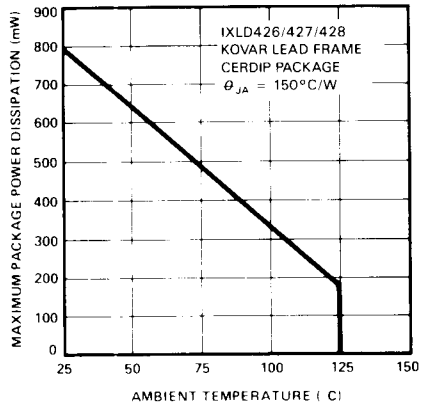
Low Output Voltage



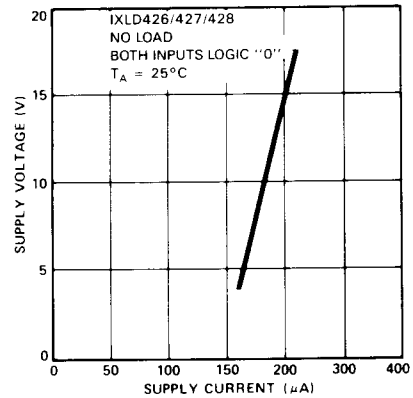
Quiescent Power Supply Current vs Supply Voltage



Package Power Dissipation



Quiescent Power Supply Current vs Supply Voltage



Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, changing a 1000 pf load 18 volts in 25 ns requires a 0.8 A current from the device power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitors with short lead lengths (<0.5 inch) should be used. A 4.7 μf solid tantalum capacitor in parallel with one or two 0.1 uf ceramic disk capacitors normally provides adequate bypassing.

Grounding

The IXLD426 and IXLD428 contain inverting drivers. Ground potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics.

Individual ground returns for the input and output circuits or a ground plane should be used.

Input Stage

The input voltage level changes the no load or quiescent supply current. The N channel MOSFET input stage transistor drives a 2.5 mA current source load. With a logic "1" input, the maximum quiescent supply current is 8 mA. Logic "0" input level signals reduce quiescent current to 400 μA maximum. Minimum power dissipation occurs for logic "0" inputs for the IXLD426/427/428; unused driver inputs **must be grounded or tied to the positive supply.**

The drivers are designed with 100 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5 V making the device TTL compatible over the 4.5 V to 18 V operating supply range. Input current is less than 1 μA over this range.

The IXLD426/427/428 may be directly driven by the TL494, SG1526/1527, SG1524, SE5560 and similar switch mode power supply integrated circuits.

Power Dissipation

The supply current vs frequency and supply current vs capacitive load characteristic curves will aid in determining power dissipation calculations.

The IXLD426/427/428 CMOS drivers have greatly reduced quiescent DC power consumption. Maximum quiescent current is 8 mA compared to the DS0026 40 mA specification. For a 15 V supply, power dissipation is typically 40 mW.

Two other power dissipation components are:

- Output stage AC and DC load power.
- Transition state power.

Output stage power is:

$$P_O = P_{DC} + P_{AC}$$
$$= V_O (I_{DC}) + f C_L V_S^2$$

Where:

V_O = DC output voltage
I_{DC} = DC output load current
f = Switching frequency
V_S = Supply voltage

In power MOSFET drive applications the P_{DC} term is negligible. MOSFET power transistors are high impedance, capacitive input devices. In applications where resistive loads or relays are driven the P_{DC}component will normally dominate.

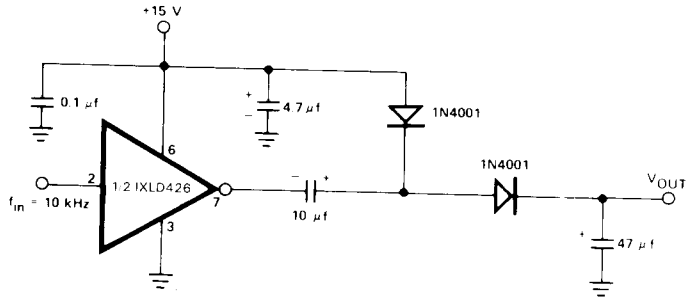
The magnitude of P_{AC} is readily estimated for several cases:

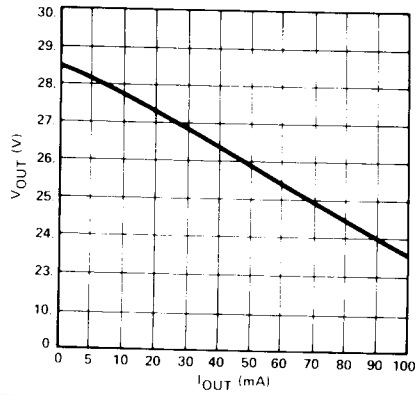
A.
1. f = 200 kHz
2. C_L = 1000 pf
3. V_S = 18 V
4. P_{AC} = 65 mW

B.
1. f = 200 kHz
2. C_L = 1000 pf
3. V_S = 15 V
4. P_{AC} = 45 mW

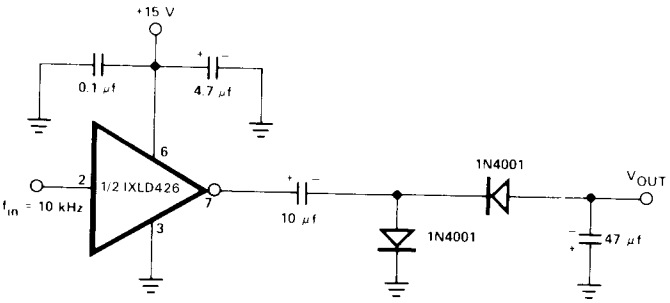
During output level state changes, a current surge will flow through the series connected N and P channel output MOSFETS as one device is turning "ON" while the other is turning "OFF." The current spike flows only during output transitions. The input levels should not be maintained between the logic "0" and logic "1" levels. **Unused driver inputs must be tied to ground and not be allowed to float.** Average power dissipation will be reduced by minimizing input rise times. As shown in the characteristic curves, average supply current is frequency dependent.

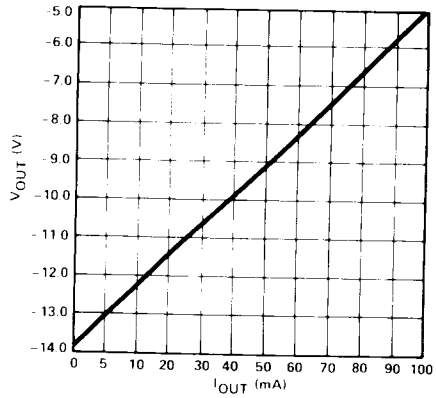
Voltage Doubler





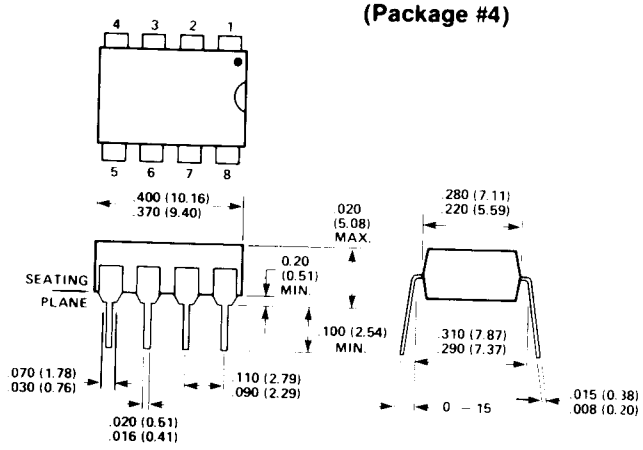
Voltage Inverter



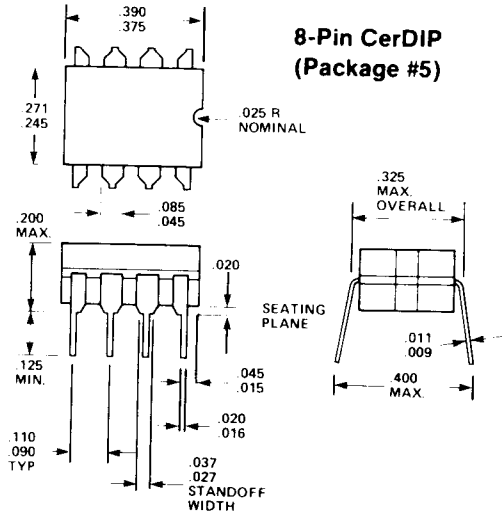


Package Information

8-Pin Plastic Dip
(Package #4)



8-Pin CerDIP
(Package #5)



IXLD429
High Speed Single Latch Resistant CMOS Power MOSFET Driver
• 25 ns Rise/Fall Time with C_L = 2500 pF
• 6 A Peak Drive Current

General Description

The IXLD429 is a single high speed CMOS level translator and driver. Designed specifically to drive highly capacitive power MOSFET gates, the IXLD429 features a 2.5Ω output impedance and 6 A peak output current drive.

A 2500 pF capacitive load will be driven 18 V in 25 ns. Delay time through the device is 60 ns. The rapid switching times with large capacitive loads minimize power MOSFET transition power loss.

A TTL/CMOS input logic level is translated into an output voltage swing that equals the supply. The output will swing to within 25 mV of ground or V_S^+. Input voltage swing may equal the supply. Logic input current is under 10 μA making direct interface to CMOS/Bipolar switch mode power supply controllers easy. Input "speed-up" capacitors are not required.

The CMOS design minimizes quiescent power supply current. With a logic 1 input, power supply current is 5 mA maximum and decreases to 0.5 mA for logic 0 inputs.

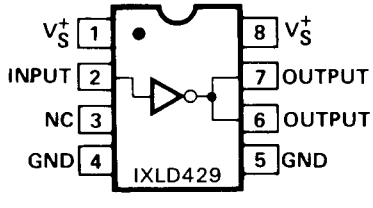
For dual devices see the IXLD426/427/428 product data sheet.

Ordering Information

Part No.	Package	Temperature Range
IXLD429CPA	8-Pin Plastic DIP	0°C to 70°C
IXLD429IJA*	8-Pin CerDIP	−25°C to 85°C
IXLD429MJA*	8-Pin CerDIP	−55°C to 125°C
IXLD429Y	CHIP	25°C

* For devices with 125°C, 160 Hour Burn In add /BI to part number suffix.

Pin Configuration



NC = NO INTERNAL CONNECTION

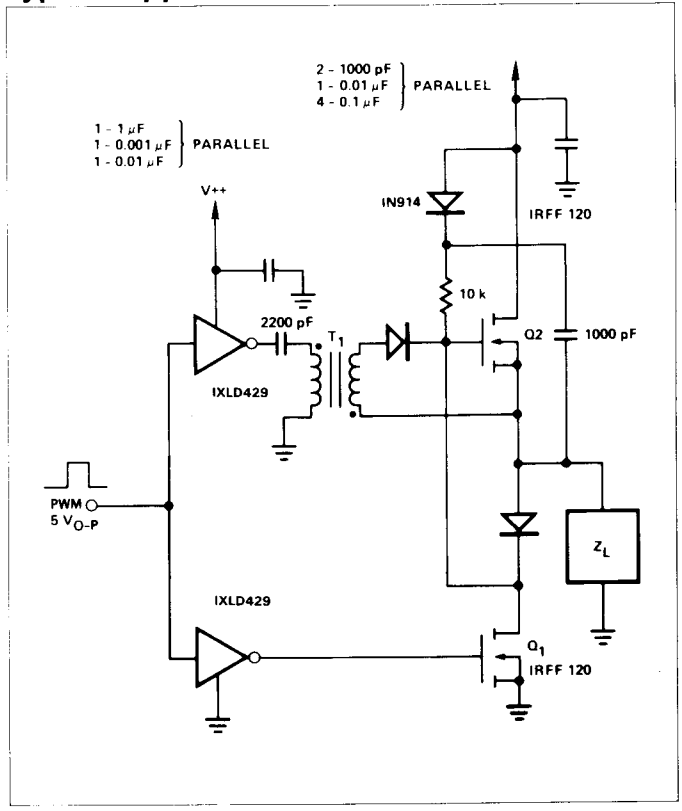
Features

- Wide Operating Range . . . . . 7 V to 18 V
- High Impedance CMOS Logic Input
- Logic Input Threshold Independent of Supply Voltage
- Low Supply Current
  - 5 mA Maximum with Logic 1 Input
- — 0.5 mA Maximum with Logic 0 Input
- Output Voltage Swing Within 25 mV of Ground or V_S^+
- Low Delay Time . . . . . 75 ns Max.
- High Capacitive Load Drive Capability
  — t_{RISE}, t_{FALL} = 35 ns Max with C_{LOAD} = 2500 pF

Applications

- Switch Mode Power Supplies
- CCD Drivers
- Pulse Transformer Drive
- Class D Switching Amplifiers

Typical Application



IXLD429

High Speed Single Latch Resistant CMOS Power MOSFET Driver
- 25 ns Rise/Fall Time with C_L = 2500 pF
- 6 A Peak Drive Current

Absolute Maximum Ratings (Notes 1, 2, 3)

Power Dissipation
- Plastic . . . . . 500 mW
- CerDIP . . . . . 800 mW

Derating Factors
- Plastic . . . . . 5.6 mW/°C Above 36°C
- CerDIP . . . . . 6.0 mW/°C

Supply Voltage . . . . . 20 V

Input Voltage Any Terminal . . Vs + 0.3 V to Ground −0.3 V

Operating Temperature
- M Version . . . . . −55°C to +125°C
- I Version . . . . . −25°C to +85°C
- C Version . . . . . 0°C to +70°C

Maximum Chip Temperature . . . . . +150°C

Storage Temperature . . . . . −55°C to +150°C

Lead Temperature (10 Sec) . . . . . 300°C

IXLD429
Electrical Characteristics: T_A = 25°C with 7.0 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	IXLD429 MIN	IXLD429 TYP	IXLD429 MAX	UNIT
INPUT	1	V_{IH}	Logic 1 Input Voltage		2.4	1.8	–	V
	2	V_{IL}	Logic 0 Input Voltage		–	1.3	0.8	V
	3	I_{IN}	Input Current	0 ≤ V_{IN} ≤ V_S	−10	–	10	µA
OUTPUT	4	V_{OH}	High Output Voltage		V_S −0.025	–	–	V
	5	V_{OL}	Low Output Voltage		–	–	0.025	V
	6	R_O	Output Resistance	V_{IN} = 0.8 V I_{OUT} = 10 mA, V_S = 18 V	–	1.8	2.5	Ω
	7	R_O	Output Resistance	V_{IN} = 2.4 V I_{OUT} = 10 mA, V_S = 18 V	–	1.5	2.5	Ω
	8	I_{PK}	Peak Output Current	V_S = 18 V	–	6	–	A
SWITCHING TIME	9	T_R	Rise Time	Test Figure 1, C_L = 2500 pF	–	23	35	ns
	10	T_F	Fall Time	Test Figure 1, C_L = 2500 pF	–	25	35	ns
	11	T_{D1}	Delay Time	Test Figure 1	–	53	75	ns
	12	T_{D2}	Delay Time	Test Figure 1	–	60	75	ns
POWER SUPPLY	13	I_S	Power Supply Current	V_{IN} = 3.0 V	–	3.5	5.0	mA
	14	I_S	Power Supply Current	V_{IN} = 0.0 V	–	0.3	0.5	mA

High Speed Single Latch Resistant CMOS Power MOSFET Driver

- 25 ns Rise/Fall Time with C_L = 2500 pF
- 6 A Peak Drive Current

IXLD429

Electrical Characteristics: Over operating temperature range with 7.0 V ≤ V_S ≤ 18 V unless otherwise specified.

TYPE	NO.	SYMBOL	PARAMETER	CONDITIONS	IXLD429 MIN	IXLD429 TYP	IXLD429 MAX	UNIT
OUTPUT	4	V_{OH}	High Output Voltage		V_S −0.025	—	—	V
	5	V_{OL}	Low Output Voltage		—	—	0.025	V
	6	R_O	Output Resistance	V_{IN} = 0.8 V, I_{OUT} = 10 mA, V_S = 18 V	—	—	5.0	Ω
	7	R_O	Output Resistance	V_{IN} = 2.4 V, I_{OUT} = 10 mA, V_S = 18 V	—	—	5.0	Ω
SWITCHING TIME	8	T_R	Rise Time	Test Figure 1, C_L = 2500 pF	—	—	70	ns
	9	T_F	Fall Time	Test Figure 1, C_L = 2500 pF	—	—	70	ns
	10	T_{D1}	Delay Time	Test Figure 1	—	—	100	ns
	11	T_{D2}	Delay Time	Test Figure 1	—	—	120	ns
POWER SUPPLY	12	I_S	Power Supply Current	V_{IN} = 3.0 V	—	—	12.0	mA
	13	I_S	Power Supply Current	V_{IN} = 0.0 V	—	—	1.0	mA

NOTES:
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Switching times guaranteed by design.

Switching Time Test Circuit

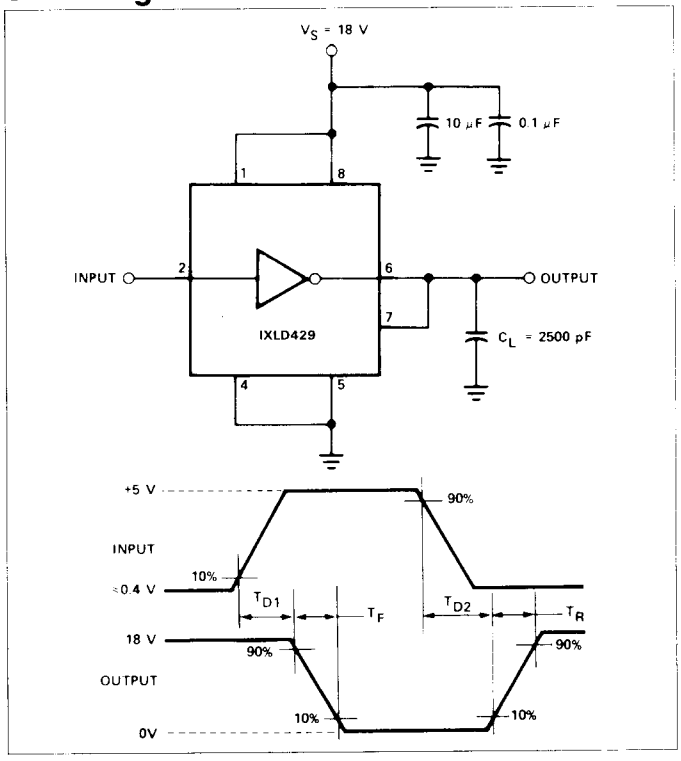
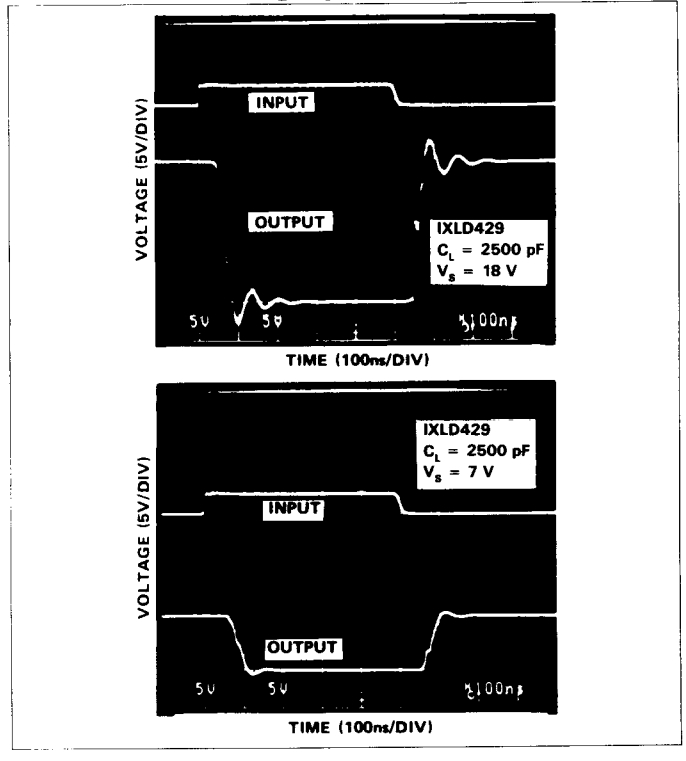


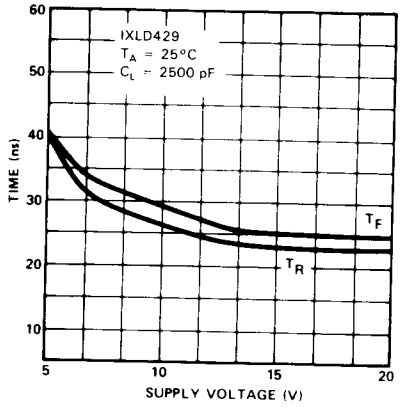
Figure 1: Inverting Driver Switching Time

IXLD429 Switching Speed

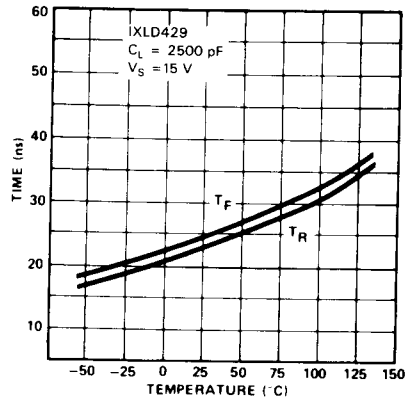


Typical Characteristic Curves

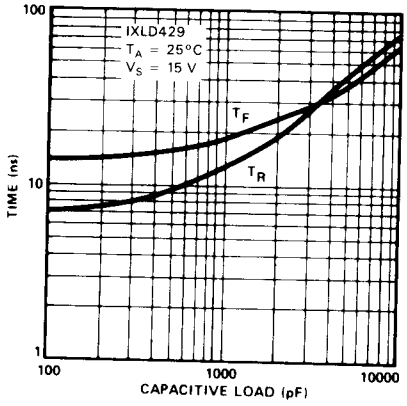
Rise and Fall Time vs Supply Voltage



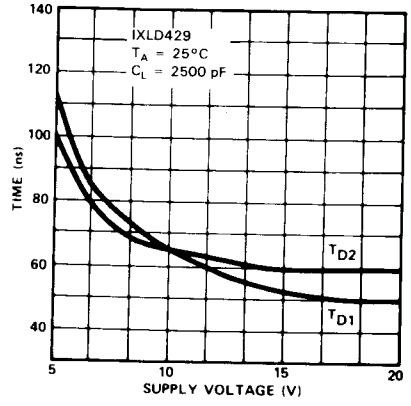
Rise and Fall Time vs Temperature



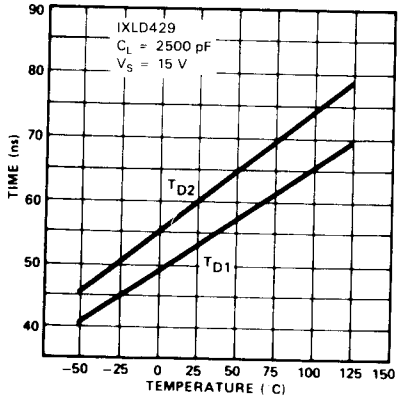
Rise and Fall Time vs Capacitive Load



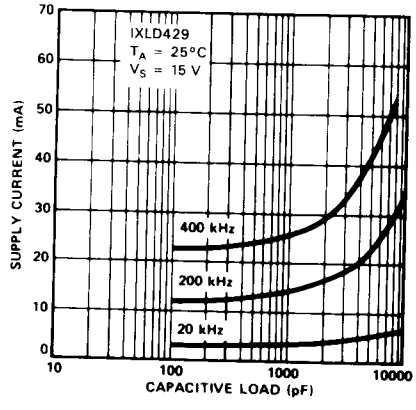
Delay Time vs Supply Voltage



Delay Time vs Temperature



Supply Current vs Capacitive Load



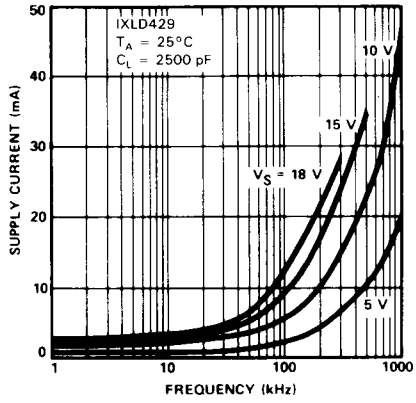
High Speed Single Latch Resistant CMOS Power MOSFET Driver

- 25 ns Rise/Fall Time with C_L = 2500 pF
- 6 A Peak Drive Current

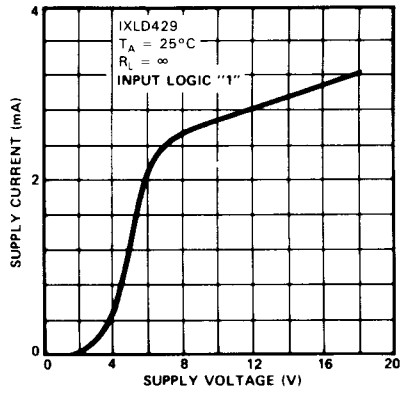
IXLD429

Typical Characteristic Curves

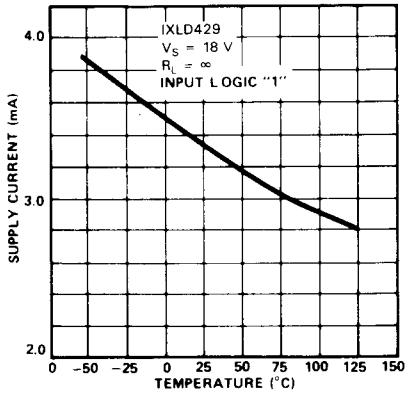
Supply Current vs Frequency



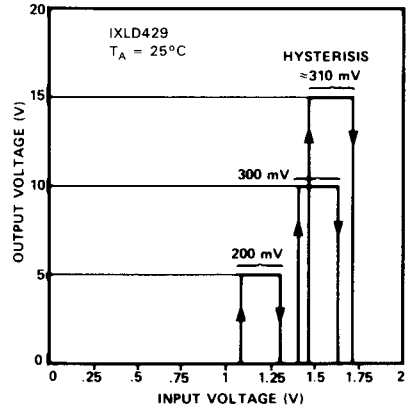
Quiescent Power Supply Current vs Supply Voltage



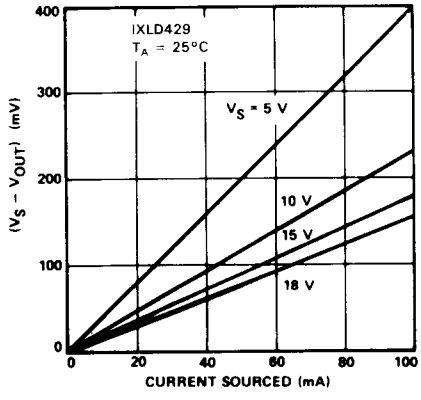
Quiescent Power Supply Current vs Temperature



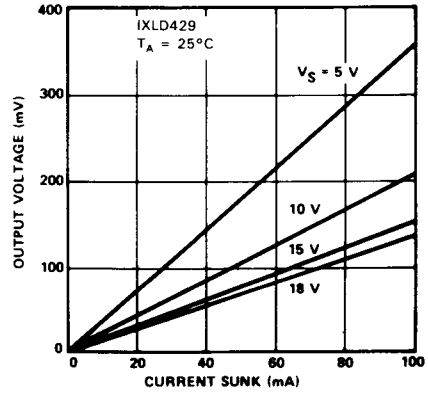
Voltage Transfer Characteristic



High Output Voltage vs Current



Low Output Voltage vs Current



Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 2500 pF load 18 volts in 25 ns requires a 1.8 A current from the device power supply.

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitors with short lead lengths (<0.5 inch) should be used. A 10 μF solid tantalum capacitor in parallel with one or two 0.1 μF ceramic disk capacitors normally provides adequate bypassing.

Grounding

The high current capability of the IXLD429 demands careful PC board layout for best performance. Since the IXLD429 is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade switching speed. The feedback is especially noticeable with slow-risetime inputs, such as are produced by an open collector output with resistor pullup. The IXLD429 input structure includes about 300 mV of hysteresis to ensure clean transitions and freedom from oscillation, but attention to layout is still recommended.

Figure 2 shows the feedback effect in detail. As the IXLD429 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05 Ω of PC trace resistance can produce hundreds of millivolts at the IXLD429 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and slow switching speed may result.

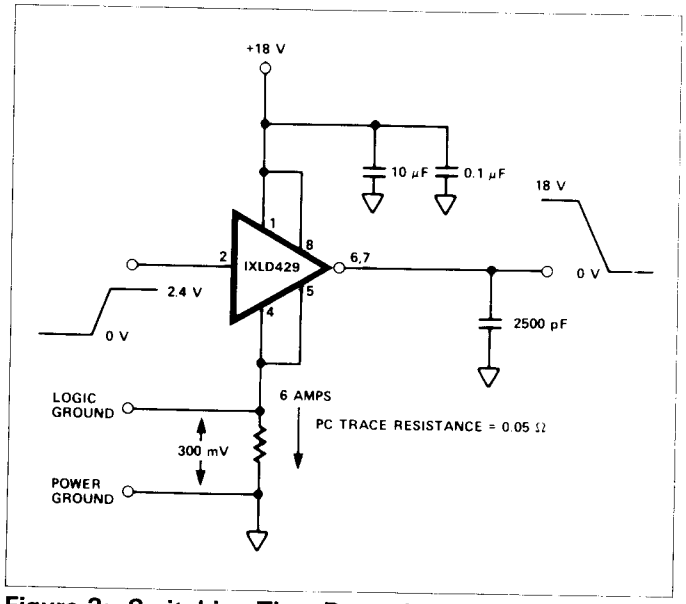


Figure 2: Switching Time Degradation Due to Negative Feedback

To ensure optimum performance, separate ground traces should be provided for the logic and power connections. Connecting the logic ground directly to the IXLD429 GND pins will ensure full logic drive to the input and ensure fast output switching. Both of the IXLD429 GND pins should be connected to power ground.

Input Stage

The input voltage level changes the no load or quiescent supply current. The N channel MOSFET input stage transistor drives a 3 mA current source load. With a logic "1" input, the maximum quiescent supply current is 5 mA. Logic "0" input level signals reduce quiescent current to 500 μA maximum.

The IXLD429 input is designed to provide 300 mV of hysteresis. This provides clean transitions and minimizes output stage current spiking when changing states. Input voltage levels are approximately 1.5 V, making the device TTL compatible over the 7 V to 18 V operating supply range. Input current is less than 10 μ A over this range.

The IXLD429 can be directly driven by the TL494, SG1526/1527, SG1524, SE5560 and similar switch mode power supply integrated circuits. By offloading the power-driving duties to the IXLD429, the power supply controller can operate at lower dissipation. This can improve performance and reliability.

Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 and 74C have outputs which can only supply a few milliamperes of current, and even shorting outputs to ground will not force enough current to destroy the device. The IXLD429, on the other hand, can source or sink several amperes and drive large capacitive loads at high frequency. The package power dissipation limit can easily be exceeded. Therefore, some attention should be given to power dissipation when driving low impedance loads and/or operating at high frequency.

The supply current vs frequency and supply current vs capacitive load characteristic curves will aid in determining power dissipation calculations. Also, Table 1 lists the maximum operating frequency for several power supply voltages when driving a 2500 pF load. More accurate power dissipation figures can be obtained by summing the three power sources.

Input signal duty cycle, power supply voltage, and capacitive load influence package power dissipation. Given power dissipation and package thermal resistance the maximum ambient operation temperature is easily calculated. The CerDIP 8-pin package junction to ambient thermal resistance is 150° C/W. At 25°C the package is rated at 800 mW maximum dissipation. Maximum allowable chip temperature is 150°C.

High Speed Single Latch Resistant CMOS Power MOSFET Driver

- 25 ns Rise/Fall Time with C_L = 2500 pF
- 6 A Peak Drive Current

Three components make up total package power dissipation:

- Capacitive load dissipation (P_C)
- Quiescent power (P_Q)
- Transition power (P_T)

The capacitive load caused dissipation is a direct function of frequency, capacitive load, and supply voltage. The package power dissipation is:

EQ. 1: $P_C = f\ C\ V_S^2$

where: F = switching frequency
C = capacitive load
V_S = supply voltage

Quiescent power dissipation depends on input signal duty cycle. A logic low input results in a low power dissipation mode with only 0.5 mA total current drain. Logic high signals raise the current to 5 mA maximum. The quiescent power dissipation is:

EQ. 2: $P_Q = V_S\ (D\ (I_H) + (1\text{-}D)\ I_L)$

where: I_H = quiescent current with input high (5 mA Max)
I_L = quiescent current with input low (0.5 mA Max)
D = duty cycle

Transition power dissipation arises because the output stage N and P channel MOS transistors are "on" simultaneously for a very short period when the output changes. The transition package power dissipation is approximately:

EQ. 3: $P_T = f\ V_S\ (30 \times 10^{-9})$

An example shows the relative magnitude for each term.

Example 1:
C = 2500 pF
V_S = 15 V
D = 50%
f = 200 kHz
P_D = Package power dissipation = $P_C + P_T + P_Q$
= 113 mW + 90 mW + 26 mW
= 229 mW
Max. operating temperature = $T_J - \theta_{JA}\ (P_D)$
= 115°C

where:
T_V = Max. allowable junction temperature (150°C)
θ_{JA} = Junction to ambient thermal resistance (150°C/W, CerDIP)

NOTE: Ambient operating temperature should not exceed 85°C for "IJA" device or 125°C for "MJA" device.

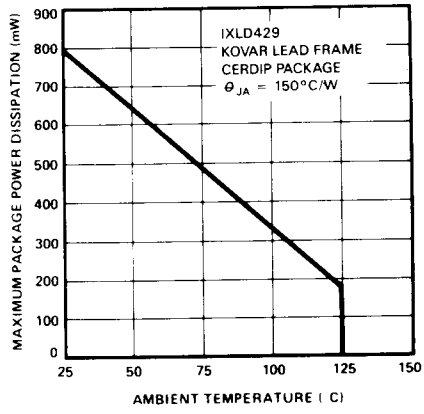
IXLD429 Maximum Operating Frequency

V_S	f_{Max}
18V	500 kHz
15V	700 kHz
10V	1.3 MHz
5V	> 2MHz

Table 1

Conditions: 1. CerDIP Package (θ_{JA} = 150°C/W)
2. T_A = 25°C
3. C_L = 2500 pF

Package Power Dissipation

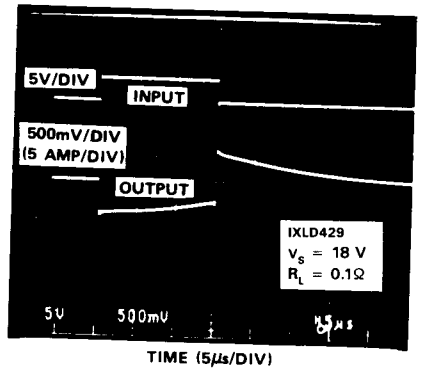


IXLD429

High Speed Single Latch Resistant CMOS Power MOSFET Driver

- 25 ns Rise/Fall Time with C_L = 2500 pF
- 6 A Peak Drive Current

Peak Output Current Capability



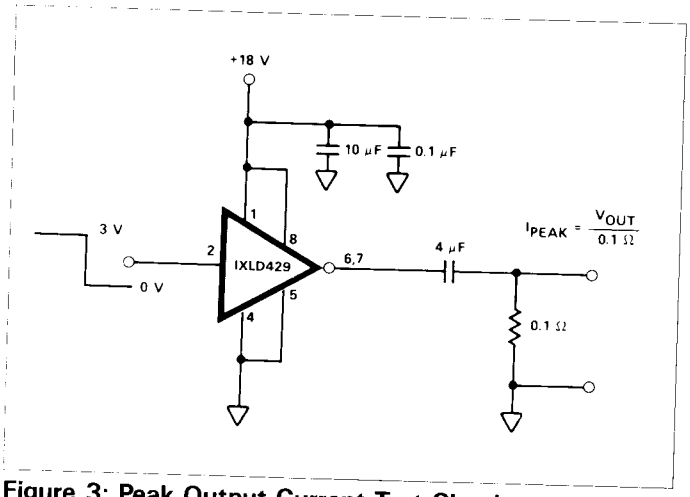
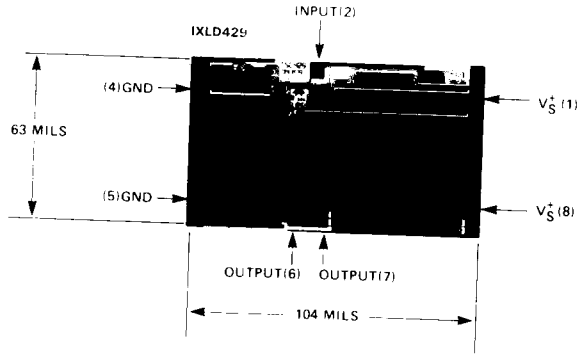


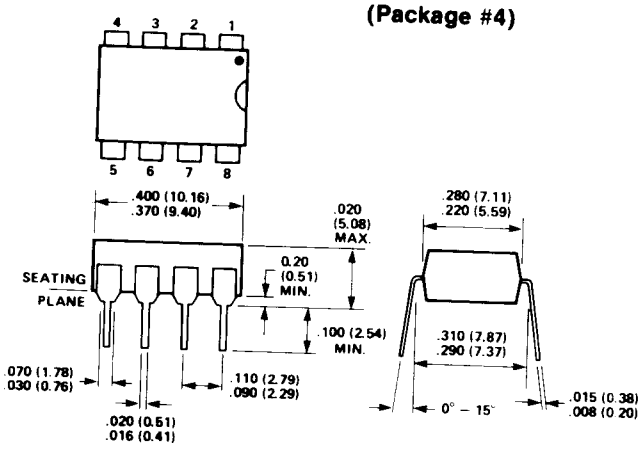
Figure 3: Peak Output Current Test Circuit

Chip Pad Layout

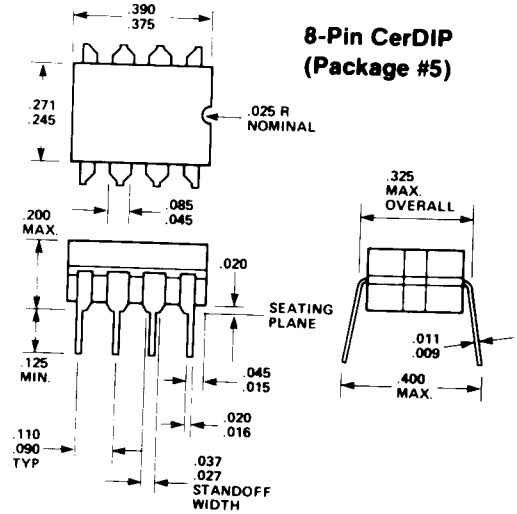


Package Information

8-Pin Plastic DIP (Package #4)



8-Pin CerDIP (Package #5)



MOSFET DRIVERS

The following families of power drivers are made with a CMOS process to inferface between low-level control functions and high-power switching devices, particularly power MOSFETs. The devices are also an optimum choice for capacitive line drivers where 1.2 A-6 A may be switched. With both inverting and non-inverting inputs available, logic signals of either polarity may be accepted.

Selecting MOSFET Drivers

Device	Drive Current	Output No. & Type Invert.	Non-Invert	Rated Load (pF)	Rise Time @ Rated Load (nS)	Rise Time @ Rated Load (nS)	Rising Edge Prop. Delay* (nS)	Falling Edge Prop. Delay (nS)	Latch	Input Protected to 6 V Below Gnd Rail
IXLD1426	1.2 A Peak	dual		1000	30	20	55	80	Resistant	NO
IXLD1427	1.2 A Peak		dual	1000	30	20	55	80	Resistant	NO
IXLD1428	1.2 A Peak	single &	single	1000	30	20	55	80	Resistant	NO
IXLD426	1.5 A Peak	dual		1000	30	20	40	75	Resistant	NO
IXLD427	1.5 A Peak		dual	1000	30	20	40	75	Resistant	NO
IXLD428	1.5 A Peak	single &	single	1000	25	20	40	75	Resistant	NO
IXLD4426	1.5 A Peak	dual		1000	25	25	18	38	Immune	YES
IXLD4427	1.5 A Peak		dual	1000	25	25	18	38	Immune	YES
IXLD4428	1.5 A Peak	single &	single	1000	25	25	18	38	Immune	YES
IXLD4423	3.0 A Peak	dual		2200	25	25	18	38	Immune	YES
IXLD4424	3.0 A Peak		dual	2200	25	25	18	38	Immune	YES
IXLD4425	3.0 A Peak	single &	single	2200	25	25	18	38	Immune	YES
IXLD429	6.0 A Peak	single	inverting	2200	25	35	53	60	Resistant	NO
IXLD4420	6.0 A Peak	single	non-invert	2200	25	25	18	38	Immune	YES
IXLD4429	6.0 A Peak	single	inverting	2200	25	25	18	38	Immune	YES

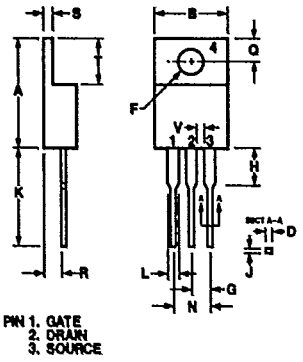
MOSFET Die Size vs. Suggested Driver Family

MOSFET Size	Suggested Driver (@ 12 V)	Typical t_r/t_f	Suggested Driver for faster speed (@ 12 V)	Typical t_r/t_f
Size 3	IXLD426/1426/4426	10/26	IXLD4423	7/18
Size 4	IXLD426/1426/4426	26/31	IXLD4420/4429	12/26
Size 5	IXLD426/1426/4426	40/40	IXLD4420/4429	15/15
Size 6	IXLD4420/4429	25/20	—	—
Size 7	IXLD4420/4429	36/35	—	—
Size 8	IXLD4420/4429	50/50	—	—

DETAILED PACKAGE OUTLINES

T-91-20

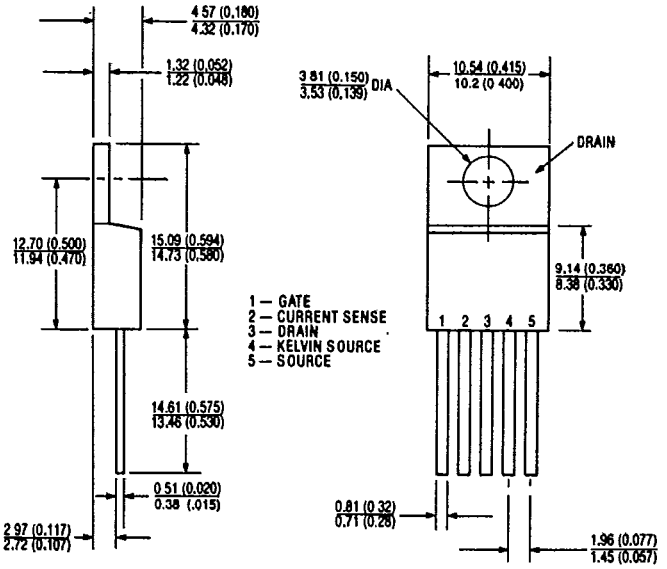
TO-220 AB



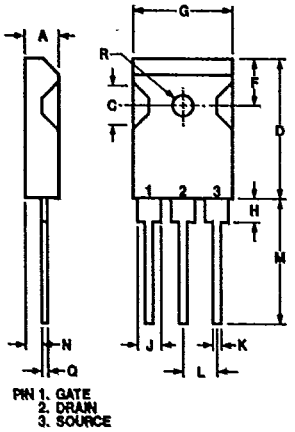
Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	14.23	16.51	.560	.650
B	9.66	10.66	.380	.420
C	3.56	4.82	.140	.190
D	0.64	0.89	.025	.035
F	3.54	4.08	.139	.161
G	2.29	2.79	.090	.110
H	–	6.35	–	250
J	0.51	.76	.020	030
K	12.70	14.73	.500	.580
L	1.15	1.77	045	.070
N	4.83	5.33	.190	.210
Q	2.54	3.42	.100	135
R	2.04	2.49	080	115
S	0.64	1.39	025	.055
T	5.85	6.85	2.30	2.70
V	1.15	–	.045	–

CONFORMS TO OUTLINE TO-220 (IR H-7)

Dimensions in Millimeters (Inches)

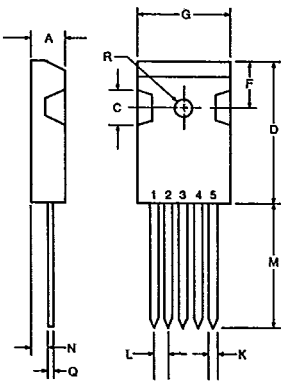


TO-247 (3 LEADED)



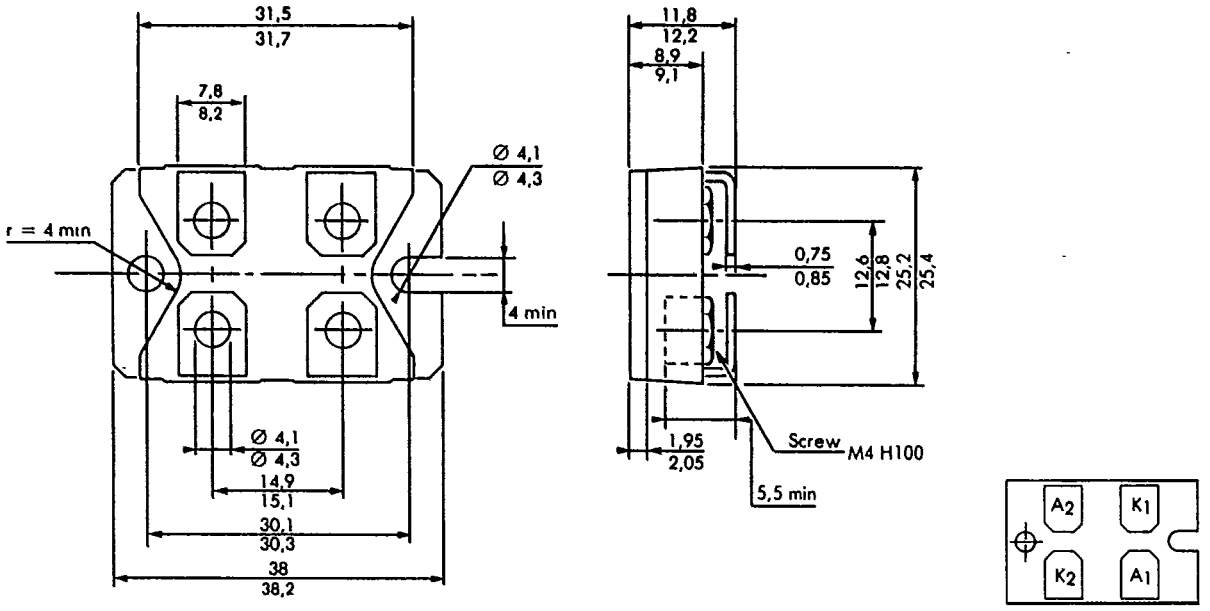
Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.7	5.3	.185	.209
C	4.5	6.0	.178	.236
D	19.7	21.4	.776	.843
F	5.3	6.1	.209	.240
G	15.3	15.9	.602	.625
H	3.7	4.3	.146	.169
J	1.95	2.4	.077	.094
J_1	2.97	3.4	.117	.134
K	1.0	1.4	.040	.055
L	5.4	5.5	.213	.217
M	19.9	20.2	.783	.795
N	2.2	2.6	.087	.102
Q	0.4	0.8	.016	.031
R	2.9	3.3	.114	.129

TO-247 (5 LEADED)

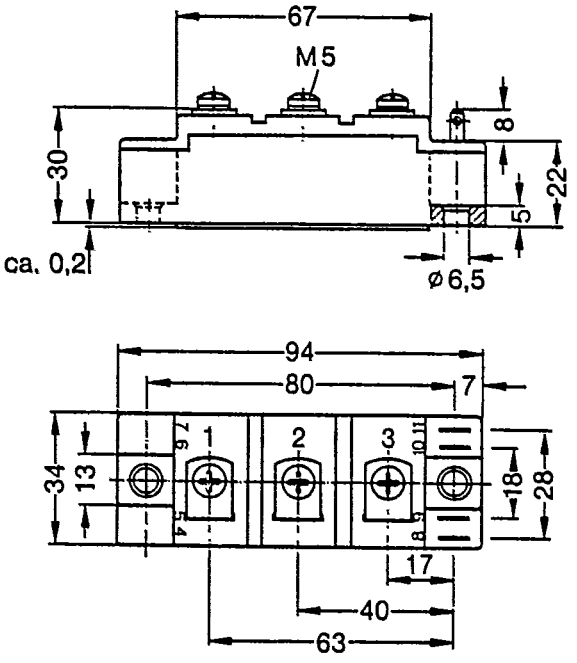


Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.7	5.3	.185	.209
C	4.5	6.0	.178	.236
D	19.7	21.4	.776	.843
F	5.3	6.1	.209	.240
G	15.3	15.9	.602	.625
K	1.1	1.3	.043	.051
L	2.51	2.56	.099	.101
M	19.9	20.2	.783	.795
N	2.2	2.6	.087	.102
Q	0.4	0.8	.016	.031
R	2.9	3.3	.114	.129

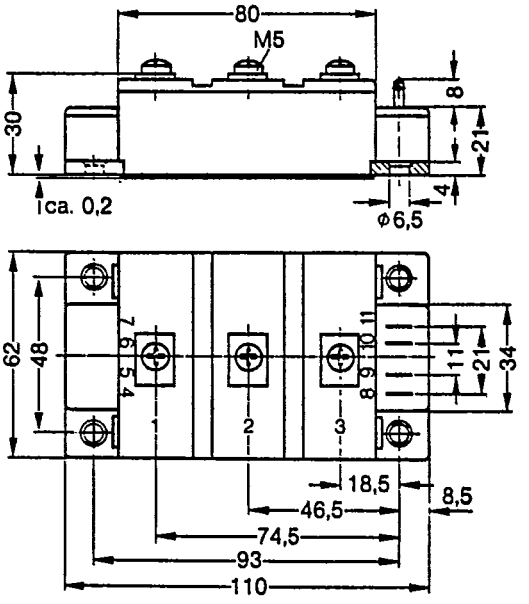
TO-238
Dimensions in Millimeters



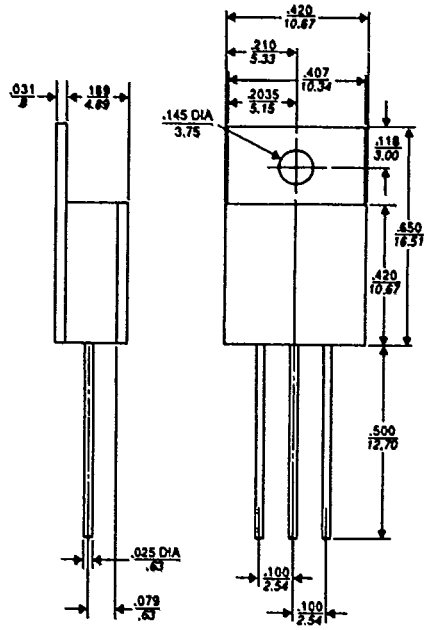
Y-4
Dimensions in Millimeters



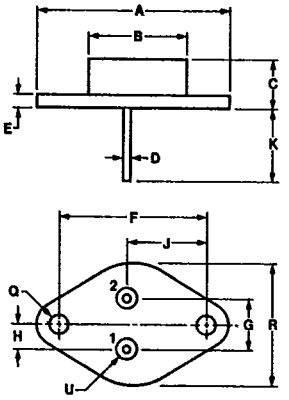
Y-3
Dimensions in Millimeters



TO-220 HERMETIC



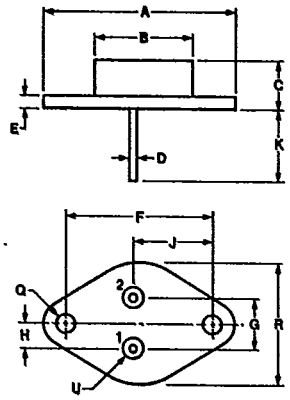
TO-204 AE



PIN 1. GATE
2. SOURCE
CASE–DRAIN

Dim.	Millimeter Min.	Millimeter Max.	Inches Min.	Inches Max.
A	–	39.37	–	1.55
B	–	19.71	–	.776
C	7.62	10.16	.300	.400
D	1.47	1.57	.058	.062
E	1.52	3.43	.060	.135
F	30.15	BSC	1.187	BSC
G	10.67	11.18	.420	.440
H	5.33	6.10	.210	.240
J	16.68	17.12	.657	.674
K	11.20	11.98	.441	.472
Q	3.86	4.11	.152	.162
R	24.84	25 27	.978	.995

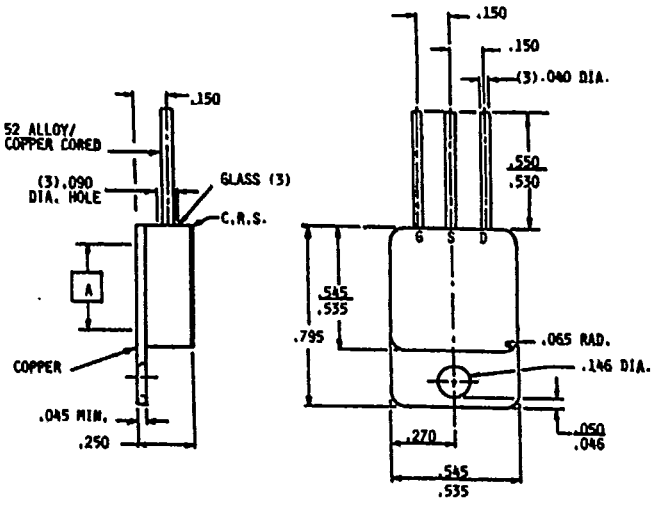
TO-204 AA



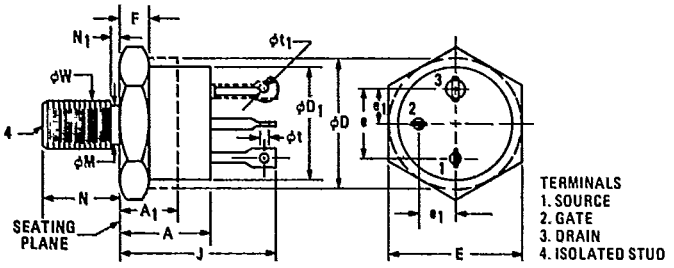
PIN 1. GATE
2. SOURCE
CASE–DRAIN

Dim.	Millimeter Min.	Millimeter Max.	Inches Min.	Inches Max.
A	–	39.37	–	.155
B	–	19.71	–	.776
C	6.35	8.89	.250	.350
D	.097	1.09.	.038	.043
E	–	3.43	–	.135
F	30.15	BSC	1.187	BSC
G	10.67	11.18	.420	.440
H	5.33	6.10	.210	.240
J	16.68	17.12	.657	.674
K	11.20	11.98	.441	.472
Q	3.86	4.11	.152	.162
R	24.84	25.47	.978	1.00

TO-254 HERMETIC



CONFORMS TO JEDEC OUTLINE TO-210AC (TO-61)
Dimensions in Millimeters (Inches)

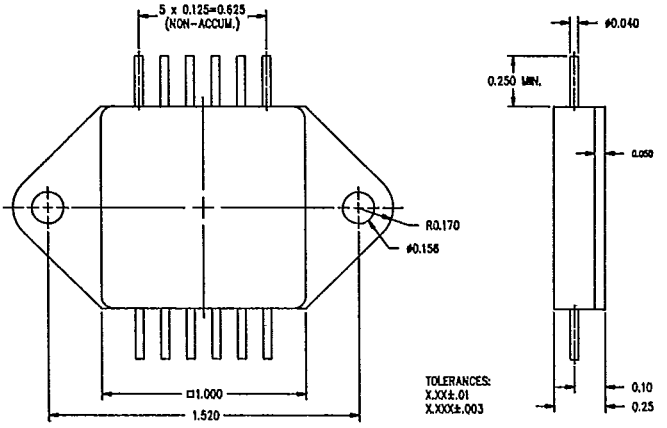


Symbol	Inches Min.	Inches Max.	Millimeters Min.	Millimeters Max.	Notes
A	0.325	0.460	8.26	11.68	
A_1		0.270		6.86	2
øD	0.610	0.687	15.49	17.45	2
$øD_1$	0.570	0.610	14.48	15.49	
E	0.667	0.687	16.94	17.45	
e	0.340	0.415	8.64	10.54	5
e_1	0.170	0.213	4.32	5.41	5
F	0.090	0.150	2.29	3.81	1

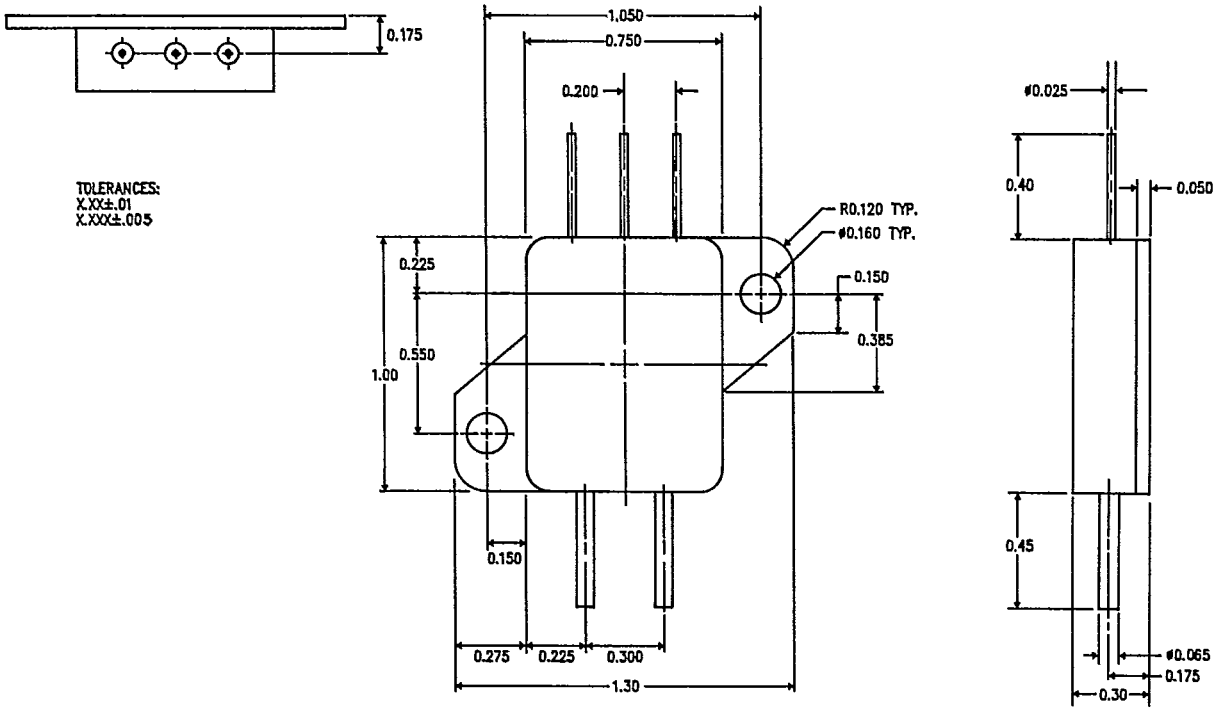
Symbol	Inches Min.	Inches Max.	Millimeters Min.	Millimeters Max.	Notes
J	0.640	0.875	16.26	22.23	
øM	0.220	0.249	5.59	6.32	
N	0.422	0.455	10.72	11.56	
N_1		0.090		2.29	
øt	0.055	0.072	1.19	1.83	
$øt_1$	0.046	0.077	1.17	1.96	4
øW	0.2225	0.2268	5.561	5.761	3

NOTES
1. DIMENSION DOES NOT INCLUDE SEALING FLANGES.
2. PACKAGE CONTOUR OPTIONAL WITHIN DIMENSIONS SPECIFIED.
3. PITCH DIAMETER – THREAD 1/4 28 UNF 2A (COATED).
   REFERENCE ISCREW THREAD STANDARDS FOR FEDERAL SERVICES - HANDBOOK H 28).
4. THIS TERMINAL CAN BE FLATTENED AND PIERCED OR HOOK TYPE.
5. POSITION OF LEADS IN RELATION TO THE HEXAGON IS NOT CONTROLLED.

QUADPAC



Z-Pac

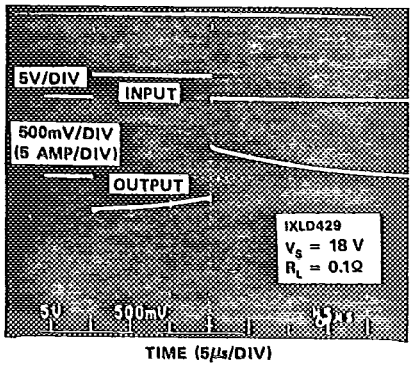


High Speed Single Latch Resistant CMOS Power MOSFET Driver

- 25 ns Rise/Fall Time with C_L = 2500 pF
- 6 A Peak Drive Current

IXLD429

Peak Output Current Capability



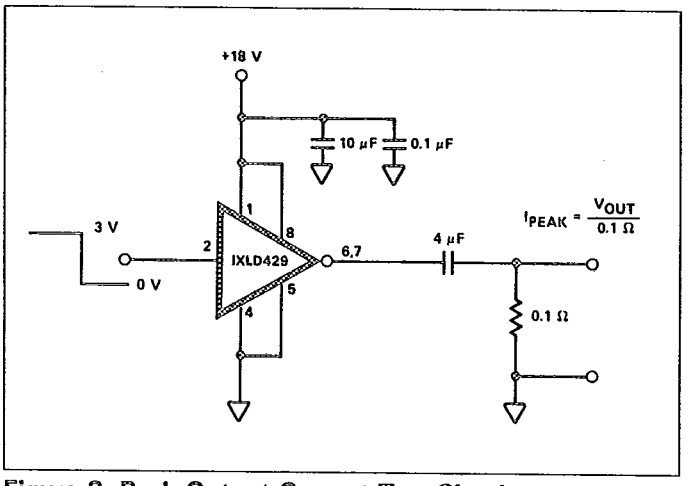
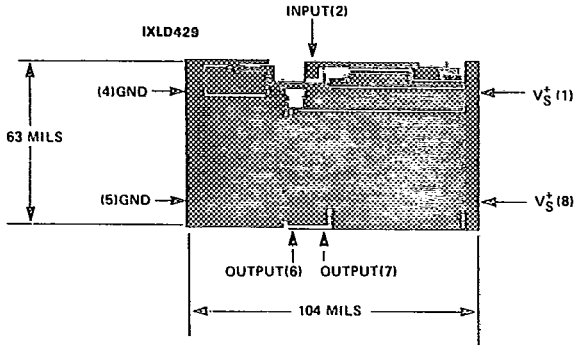


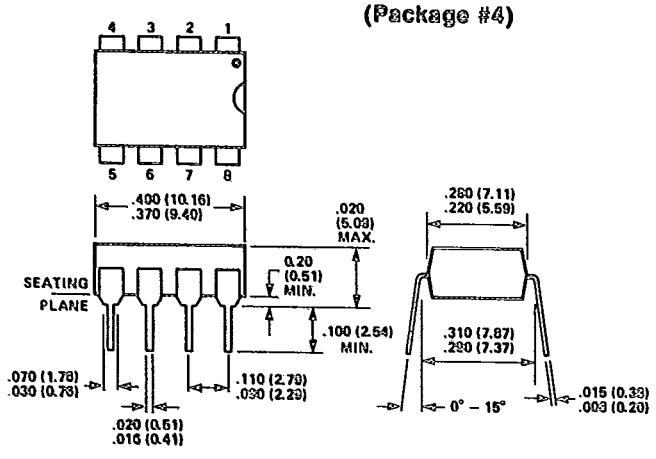
Figure 3: Peak Output Current Test Circuit

Chip Pad Layout



Package Information

8-Pin Plastic DIP (Package #4)



8-Pin CerDIP (Package #5)