

# MJF31C (NPN), MJF32C (PNP)

Preferred Device

## Complementary Silicon Plastic Power Transistors for Isolated Package Applications

Designed for use in general purpose amplifier and switching applications.

### Features

- Collector–Emitter Saturation Voltage –  
 $V_{CE(sat)} = 1.2 \text{ Vdc (Max) @ } I_C = 3.0 \text{ Adc}$
- Collector–Emitter Sustaining Voltage –  
 $V_{CEO(sus)} = 100 \text{ Vdc (Min)}$
- High Current Gain – Bandwidth Product  
 $f_T = 3.0 \text{ MHz (Min) @ } I_C = 500 \text{ mA}$
- UL Recognized, File #E69369, to 3500  $V_{RMS}$  Isolation
- Pb–Free Packages are Available\*

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	100	Vdc
Collector–Base Voltage	$V_{CB}$	100	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current Unclamped Inductive Load Energy (Note 1)	$I_C$	3.0 5.0	Adc
			– Continuous
			– Peak
Base Current	$I_B$	1.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	28 0.22	W W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016	W W/ $^\circ\text{C}$
Unclamped Inductive Load Energy (Note 1)	E	32	mJ
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Ambient	$R_{\theta JC}$	62.5	$^\circ\text{C/W}$
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	4.46	$^\circ\text{C/W}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1.  $I_C = 1.8 \text{ A}$ ,  $L = 20 \text{ mH}$ ,  $P.R.F. = 10 \text{ Hz}$ ,  $V_{CC} = 10 \text{ V}$ ,  $R_{BE} = 100 \Omega$ .

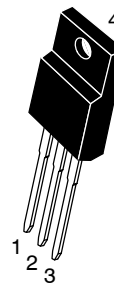
\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

<http://onsemi.com>

## 3.0 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON 100 VOLTS, 28 WATTS



TO-220 FULLPAK  
CASE 221D  
STYLE 2

### MARKING DIAGRAM



x = 1 or 2  
G = Pb–Free Package  
A = Assembly Location  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MJF31C	TO–220 FULLPAK	50 Units/Rail
MJF31CG	TO–220 FULLPAK (Pb–Free)	50 Units/Rail
MJF32C	TO–220 FULLPAK	50 Units/Rail
MJF32CG	TO–220 FULLPAK (Pb–Free)	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

# MJF31C (NPN), MJF32C (PNP)

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Sustaining Voltage (Note 2) ( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	100	-	Vdc
Collector Cutoff Current ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$I_{CEO}$	-	0.3	mAdc
Collector Cutoff Current	$I_{CES}$	-	200	$\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	-	1.0	mAdc
<b>ON CHARACTERISTICS (Note 2)</b>				
DC Current Gain ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	25 10	- 50	-
Collector-Emitter Saturation Voltage ( $I_C = 3.0\text{ Adc}$ , $I_B = 375\text{ mAdc}$ )	$V_{CE(sat)}$	-	1.2	Vdc
Base-Emitter On Voltage ( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	-	1.8	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current-Gain - Bandwidth Product ( $I_C = 500\text{ mAdc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )	$f_T$	3.0	-	MHz
Small-Signal Current Gain ( $I_C = 0.5\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )	$h_{fe}$	20	-	-

2. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

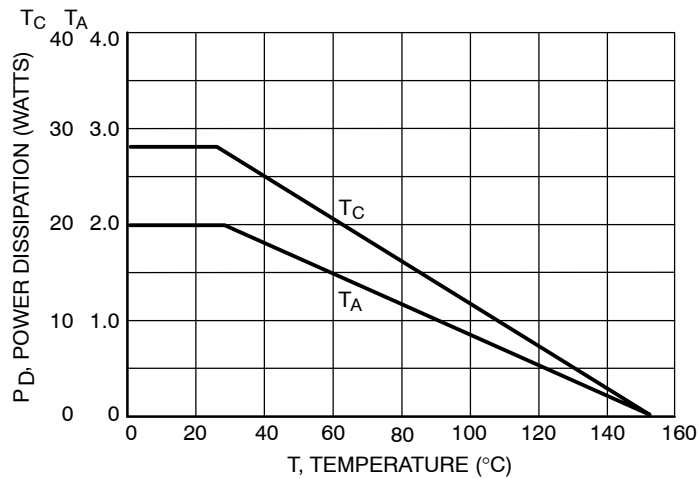
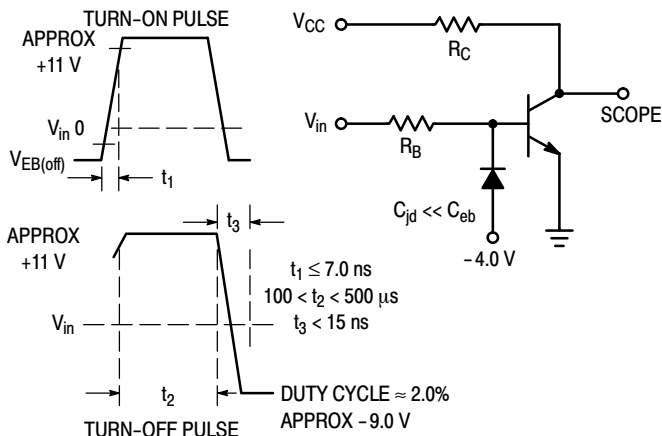


Figure 1. Power Derating



$R_B$  and  $R_C$  VARIED TO OBTAIN DESIRED CURRENT LEVELS  
Figure 2. Switching Time Equivalent Circuit

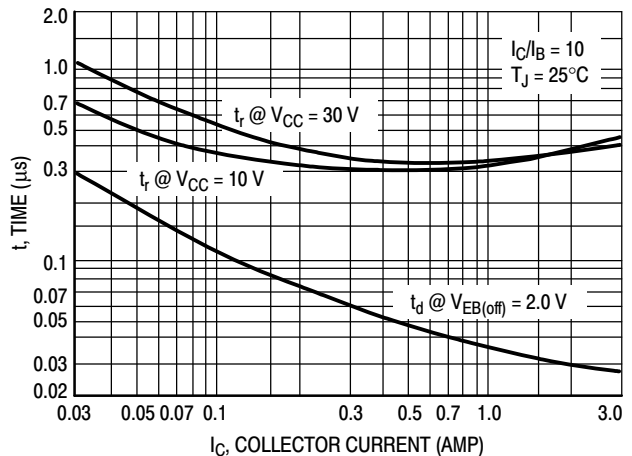


Figure 3. Turn-On Time

# MJF31C (NPN), MJF32C (PNP)

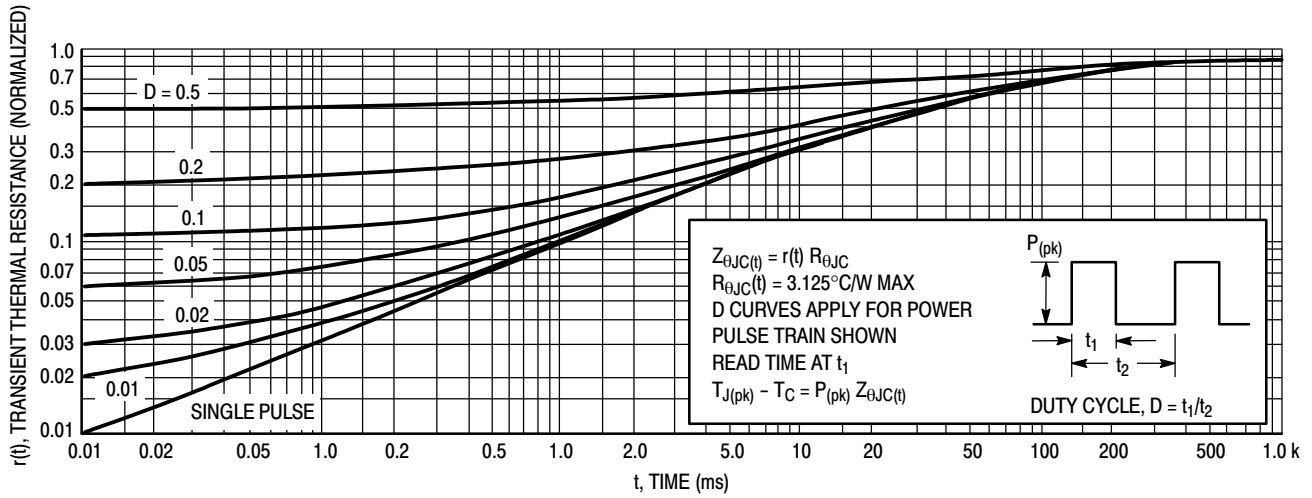


Figure 4. Thermal Response

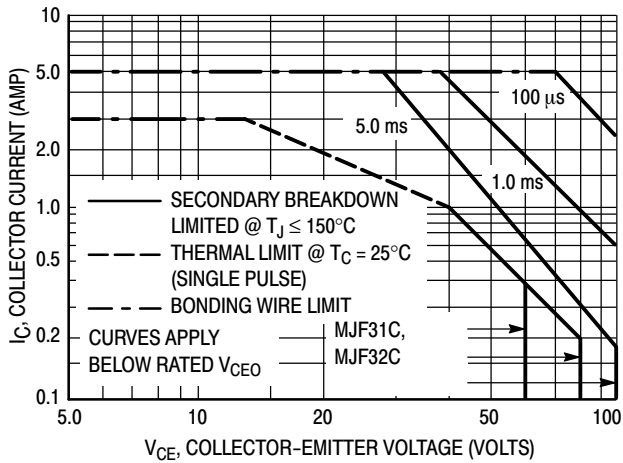


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^{\circ}\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

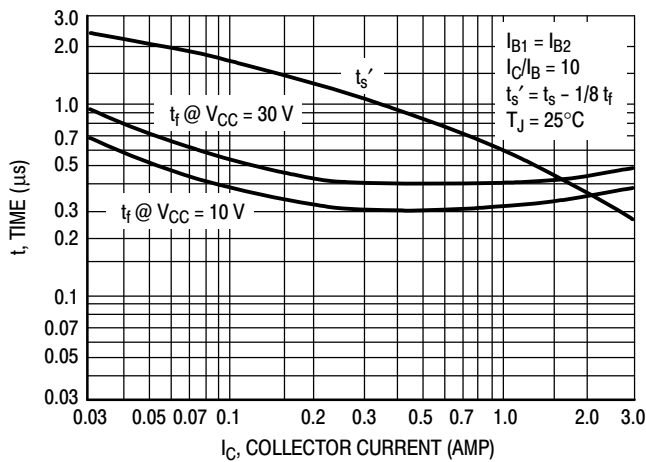


Figure 6. Turn-Off Time

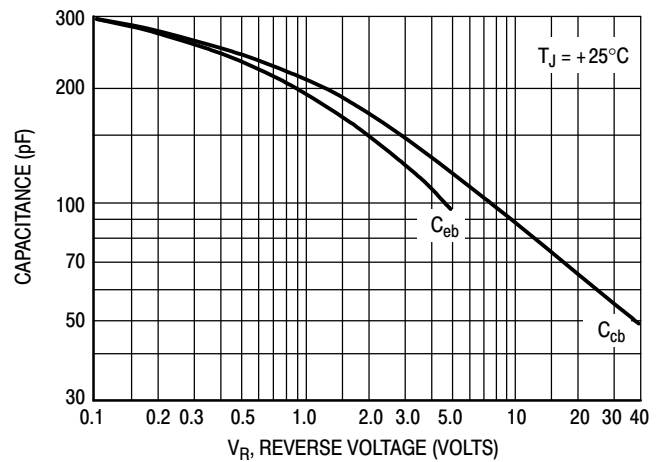


Figure 7. Capacitance

# MJF31C (NPN), MJF32C (PNP)

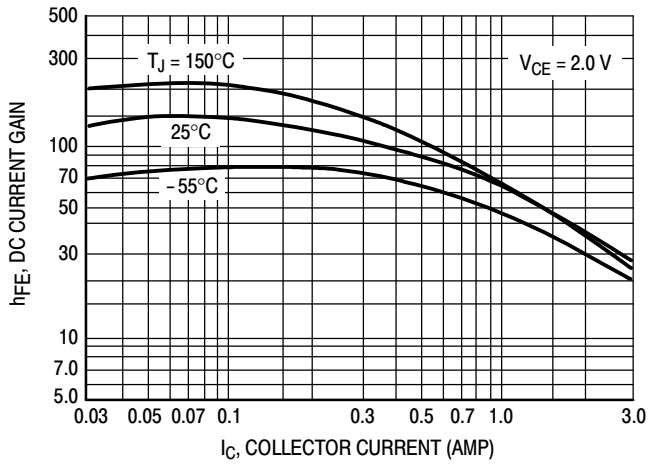


Figure 8. DC Current Gain

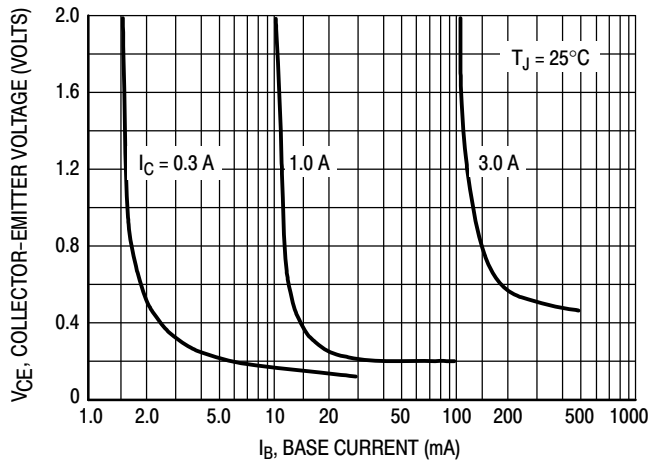


Figure 9. Collector Saturation Region

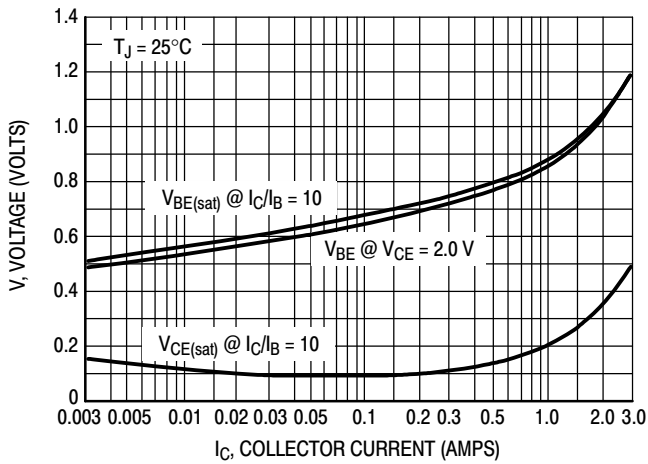


Figure 10. "On" Voltages

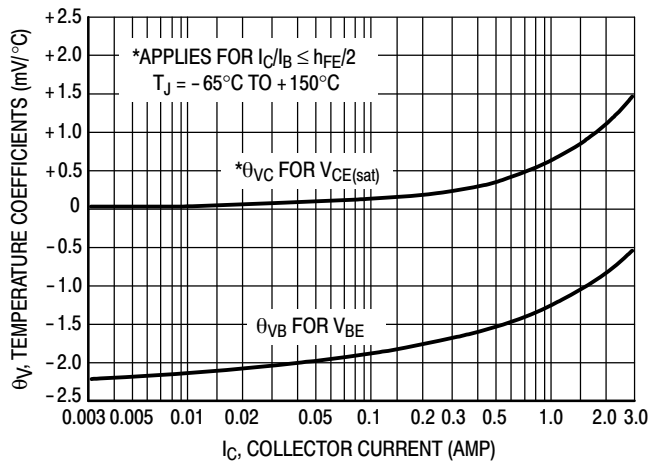


Figure 11. Temperature Coefficients

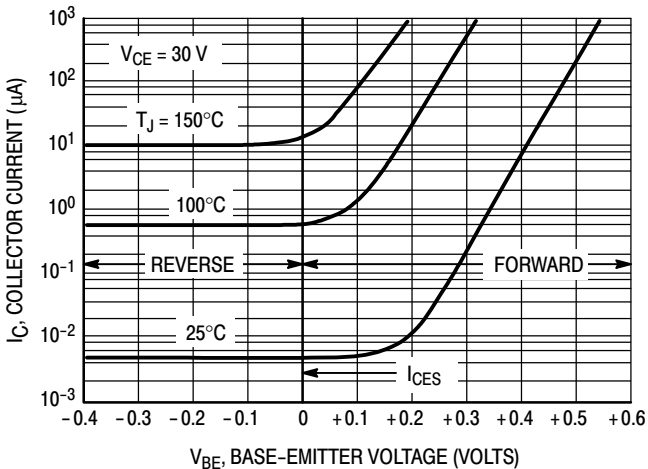


Figure 12. Collector Cut-Off Region

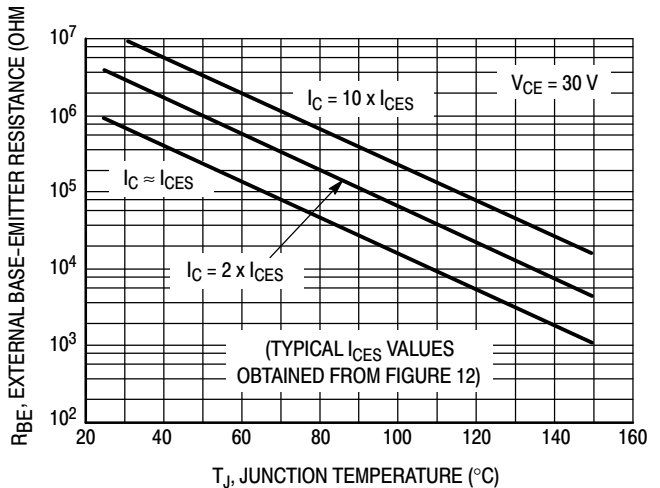
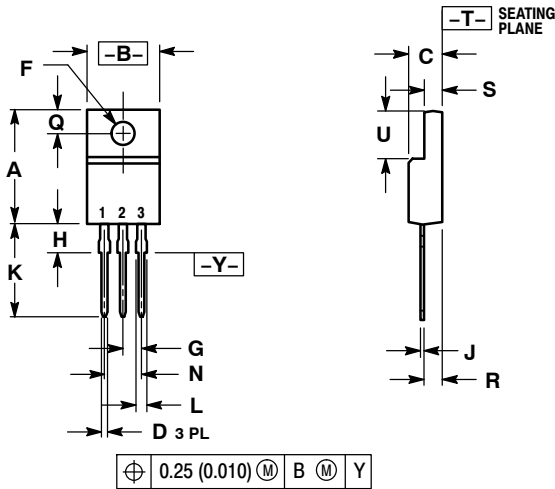


Figure 13. Effects of Base-Emitter Resistance

# MJF31C (NPN), MJF32C (PNP)

## PACKAGE DIMENSIONS

TO-220 FULLPAK  
CASE 221D-03  
ISSUE J



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

### STYLE 2:

- PIN 1. BASE  
2. COLLECTOR  
3. EMITTER

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative