



32K x 68-bit Entry NETWORK SEARCH ENGINE

PRELIMINARY DATA

FEATURES SUMMARY

- 32K DATA ENTRIES IN 68-BIT MODE
- TABLE MAY BE PARTITIONED INTO UP TO FOUR (4) QUADRANTS
(Data entry width in each octant is configurable as 34, 68, 136, or 272 bits.)
- UP TO 83 MILLION SUSTAINED SEARCHES PER SECOND IN 68-BIT and 136-BIT CONFIGURATIONS
- UP TO 41.5 MILLION SEARCHES PER SECOND IN 34-BIT and 272-BIT CONFIGURATIONS
- SEARCHES ANY SUB-FIELD IN A SINGLE CYCLE
- OFFERS BIT-BY-BIT and GLOBAL MASKING
- SYNCHRONOUS, PIPELINED OPERATION
- UP TO 31 SEARCH ENGINES CASCADABLE WITHOUT PERFORMANCE DEGRADATION
- WHEN CASCADED, THE DATABASE ENTRIES CAN SCALE FROM 248K TO 1984K DEPENDING ON THE WIDTH OF THE ENTRY
- GLUELESS INTERFACE TO INDUSTRY-STANDARD SRAMS
- SIMPLE HARDWARE INSTRUCTION INTERFACE
- IEEE 1149.1 TEST ACCESS PORT
- OPERATING SUPPLY VOLTAGES INCLUDE:
 V_{DD} (Operating Supply Voltage) = 1.8V
 V_{DDQ} (Operating Supply Voltage for I/O) = 2.5 or 3.3V
- 272 PBGA, 27mm x 27mm

Figure 1. 272-ball PBGA Package

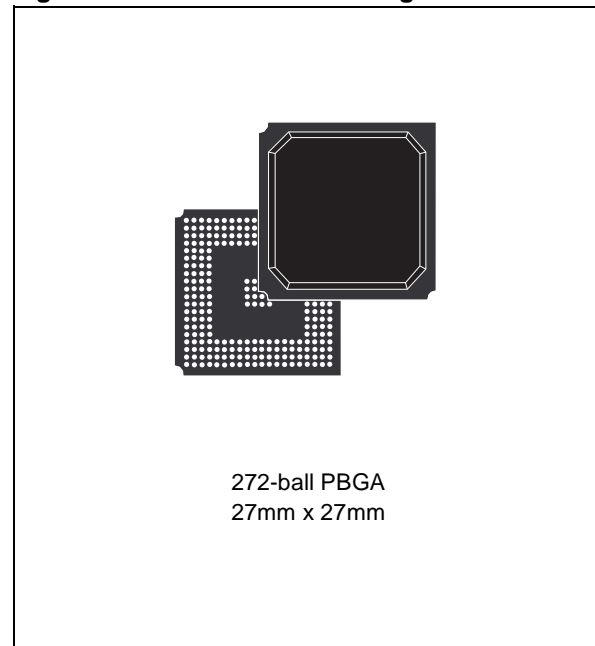


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M7020R

DESCRIPTION

Overview

ST Microelectronics, Inc.'s M7020R Search Engine incorporates patent-pending Associative Processing Technology™ (APT) and is designed to be a high-performance, pipelined, synchronous, 32K-entry network database search engine. The M7020R database entry size can be 68 bits, 136 bits, or 272 bits. In the 68-bit entry mode, the size of the database is 32K entries. In the 136-bit mode, the size of the database is 16K entries, and in the 272-bit mode, the size of the database is 8K entries. The M7020R is configurable to support multiple databases with different entry sizes. The 34-bit entry table can be implemented using the Global Mask Registers (GMRs) building-database size of 64K entries with a single device.

Performance

The Search Engine can sustain 83 million transactions per second when the database is programmed or configured as 68 or 136 bits. When the database is programmed to have an entry size

of 34 or 272 bits, the Search Engine will perform at 41.5 million transactions per second. STM's M7020R can be used to accelerate network protocols such as Longest-prefix Match (CIDR), ARP, MPLS, and other Layer 2, 3, and 4 protocols.

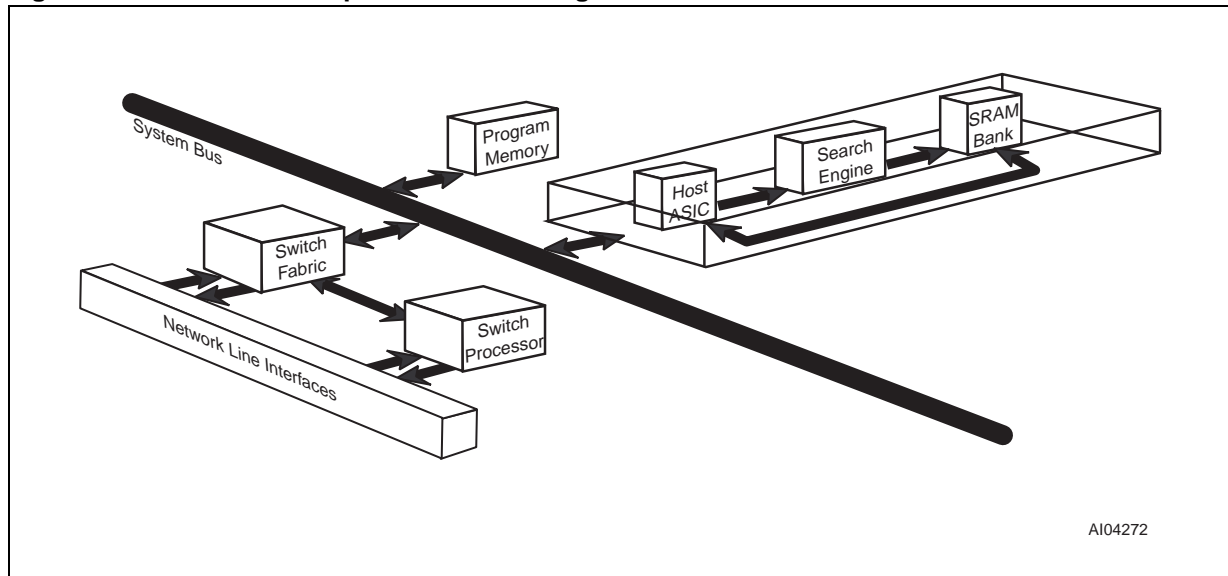
Applications

This high-speed, high-capacity Search Engine can be deployed in a variety of networking and communications applications. The performance and features of the M7020R make it attractive in applications such as Enterprise LAN switches and routers and broadband switching and/or routing equipment supporting multiple data rates at OC-48 and beyond. The Search Engine is designed to be scalable in order to support network database sizes to 1984K entries specifically for environments that require large network policy databases. Figure 4, page 11 shows the block diagram for the M7020R device.

Table 1. Product Range

Part Number	Operating Supply Voltage	Operating I/O Voltage	Speed	Temperature Range
M7020R-083ZA1	1.8V	2.5 or 3.3V	83MHz	Commercial
M7020R-066ZA1	1.8V	2.5 or 3.3V	66MHz	Commercial
M7020R-050ZA1	1.8V	2.5 or 3.3V	50MHz	Commercial

Figure 2. Switch/Router Implementation Using the M7020R



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Table 2. Signal Names

Symbol	Type ⁽¹⁾	Description
Clocks and Reset		
CLK2X	I	Master Clock
PHS_L	I	Phase
TEST	I	Test Input
RST_L	I	Reset
Command and DQ Bus		
CMD[8:0]	I	Command Bus
CMDV	I	Command Valid
DQ[67:0]	I/O	Address/Data Bus
ACK ⁽⁴⁾	T	READ Acknowledge
EOT ⁽⁴⁾	T	End of Transfer
SSF	T	SEARCH Successful Flag
SSV	T	SEARCH Successful Flag Valid
SRAM Interface		
SADR[21:0]	T	SRAM Address
CE_L	T	SRAM Chip Enable
WE_L	T	SRAM Write Enable
OE_L	T	SRAM Output Enable
ALE_L	T	Address Latch Enable

Cascade Interface		
LHI[6:0]	I	Local Hit In
LHO[1:0]	O	Local Hit Out
BHI[2:0]	I	Block Hit In
BHO[2:0]	O	Block Hit Out
FULI[6:0]	I	Full In
FULO[1:0]	O	Full Out
FULL	O	Full Flag
Device Identification		
ID[4:0]	I	Device Identification
Supplies		
V _{DD}	n/a	Chip Core Supply (1.8V)
V _{DDQ}	n/a	Chip I/O Supply (2.5 or 3.3V)
Test Access Port		
TDI	I	Test Access Port's Test Data In
TCK	I	Test Access Port's Test Clock
TDO	T	Test Access Port's Test Data Out
TMS	I	Test Access Port's Test Mode Select
TRST_L	I	Test Access Port's Reset

Note: 1. Signal types are: I = Input only; I/O = Input or Output; O = Output; and T = Tristate
2. "CLK" is an internal clock signal. Any reference to "CLK Cycles" means one cycle of CLK.
3. ACK and EOT Signals require a weak, external pull-down resistor of 47 K Ω or 100 K Ω .

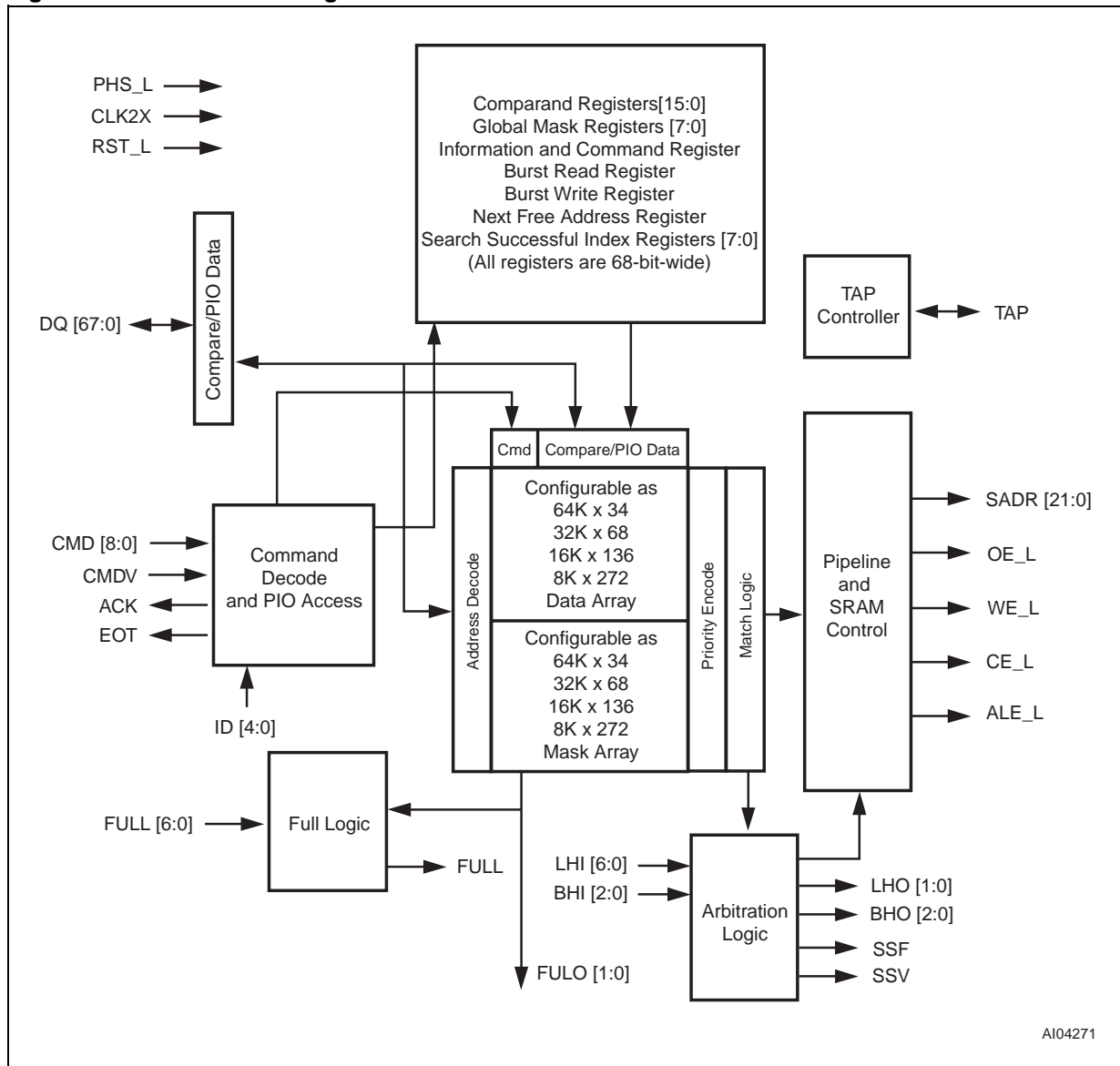
Figure 3. Connections

NC	GND	EOT	NC	NC	V _{DD}	FULI5	FULI4	FULI1	BHO0	V _{DD}	BHI0	LHI6	NC	V _{DD}	ID2	ID0	TDO	NC	NC	
NC	NC	ACK	FULL	NC	FULO1	NC	FULI6	FULI2	BHO1	BHI2	V _{DDQ}	LHI5	LHI3	LHI2	ID3	TMS	TDI	V _{DD}	NC	
DQ64	NC	NC	V _{DDQ}	V _{DD}	V _{DDQ}	NC	NC	V _{DDQ}	BHO2	V _{DD}	LHO1	LHI4	V _{DDQ}	LHI0	ID1	TCK	NC	NC	DQ65	
DQ62	NC	V _{DD}	GND	RSTL	NC	FULO0	GND	FULI3	FULI0	BHI1	LHO0	GND	LHI1	ID4	^T RST_L	GND	DQ63	DQ61	DQ57	
DQ60	V _{DDQ}	NC	DQ66	TOP												DQ67	DQ59	NC	DQ53	
V _{DD}	NC	DQ56	DQ58													V _{DDQ}	DQ55	DQ49	V _{DD}	
DQ50	V _{DDQ}	DQ52	DQ54													DQ47	V _{DDQ}	DQ51	V _{DDQ}	
NC	DQ46	DQ48	GND													GND	NC	DQ45	DQ43	
DQ40	DQ42	V _{DDQ}	DQ44													DQ41	DQ39	V _{DD}	DQ37	
V _{DD}	NC	DQ36	DQ38	LEFT	GND				GND				RIGHT				V _{DDQ}	DQ35	DQ33	DQ31
V _{DDQ}	DQ34	DQ32	DQ30													V _{DDQ}	NC	DQ29	V _{DD}	
NC	DQ28	V _{DDQ}	DQ26													NC	DQ23	DQ25	DQ27	
DQ24	V _{DD}	DQ20	GND													GND	DQ19	V _{DDQ}	DQ21	
DQ22	DQ16	DQ14	V _{DDQ}													V _{DDQ}	NC	DQ15	DQ17	
V _{DD}	DQ18	V _{DDQ}	DQ6													DQ9	DQ11	DQ13	V _{DD}	
NC	DQ12	DQ8	DQ0													DQ1	DQ5	DQ7	NC	
BOTTOM																				
DQ10	NC	V _{DDQ}	GND	NC	CMD4	CMD2	GND	WE_L	CLK2X	V _{DD}	SADR ₁₅	GND	V _{DDQ}	SADR ₅	V _{DDQ}	GND	NC	NC	V _{DDQ}	
DQ2	DQ4	V _{DD}	SSF	CMD6	CMD3	CMD0	AE_L	OE_L	SADR ₂₁	SADR ₁₈	SADR ₁₆	SADR ₁₂	SADR ₉	SADR ₇	SADR ₆	NC	SADR ₀	V _{DD}	DQ3	
NC	NC	NC	SSV	CMD5	CMD1	CMDV	V _{DDQ}	PHS_L	V _{DDQ}	SADR ₁₉	V _{DDQ}	NC	SADR ₁₀	SADR ₁₁	NC	SADR ₄	SADR ₃	NC	NC	
NC	NC	CMD8	CMD7	V _{DDQ}	V _{DD}	NC	CE_L	NC	V _{DD}	SADR ₂₀	SADR ₁₇	SADR ₁₄	SADR ₁₃	V _{DD}	SADR ₈	V _{DDQ}	SADR ₂	SADR ₁	NC	

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Figure 4. M7020R Block Diagram



MAXIMUM RATING

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is

not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature (V _{DD} Off)	–0 to 70	°C
T _{SLD} ⁽¹⁾	Lead Solder Temperature for 10 seconds	235	°C
V _{DD}	V _{DD} Operating Supply Voltage	1.9	V
V _{DDQ}	V _{DDQ} Voltage for I/O (3.3V)	3.465	V
V _{DDQ}	V _{DDQ} Voltage for I/O (2.5V)	2.6	V
I _O	Output Current	200	mA
P _D	Power Dissipation	< 5	W

Note: 1. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measure-

ment Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 4. DC and AC Measurement Conditions

Sym	Parameter	Min	Max	Units
V _{DD}	V _{DD} Operating Supply Voltage	1.7	1.9	V
V _{DDQ}	V _{DDQ} Voltage for I/O (3.3V)	3.135	3.465	V
V _{DDQ}	V _{DDQ} Voltage for I/O (2.5V)	2.4	2.6	V
t _A	Ambient Operating Temperature	0	70	°C
	Supply Voltage Tolerance	-5	+5	%
	Input Pulse Levels (V _{DDQ} = 3.3V)		GND to 3.0	V
	Input Pulse Levels (V _{DDQ} = 2.5V)		GND to 2.5	V
	Input Rise and Fall Times at 0.3V and 2.7V (V _{DDQ} = 3.3V)		≤ 2ns (see Figure 6, page 14)	ns
	Input Rise and Fall Times at 0.25V and 2.25V (V _{DDQ} = 2.5V)		≤ 2ns (see Figure 6, page 14)	ns
	Input Timing Reference Levels (V _{DDQ} = 3.3V)		1.5	V
	Input Timing Reference Levels (V _{DDQ} = 2.5V)		1.25	V
	Output Timing Reference Levels (V _{DDQ} = 3.3V)		1.5	V
	Output Timing Reference Levels (V _{DDQ} = 2.5V)		1.25	V
	Output Load		(see Figure 5 and Figure 7, page 14)	V

Note: 1. Maximum allowable applies to overshoot only (V_{DDQ} is 3.3V supply).
 2. Minimum allowable applies to undershoot only.

M7020R

Figure 5. M7020R 2.5, or 3.3V AC Testing Load

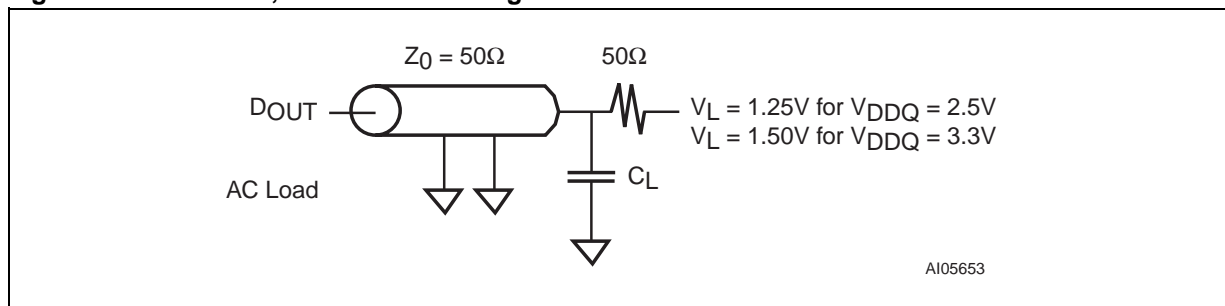


Figure 6. M7020R 2.5, or 3.3V Input Waveform

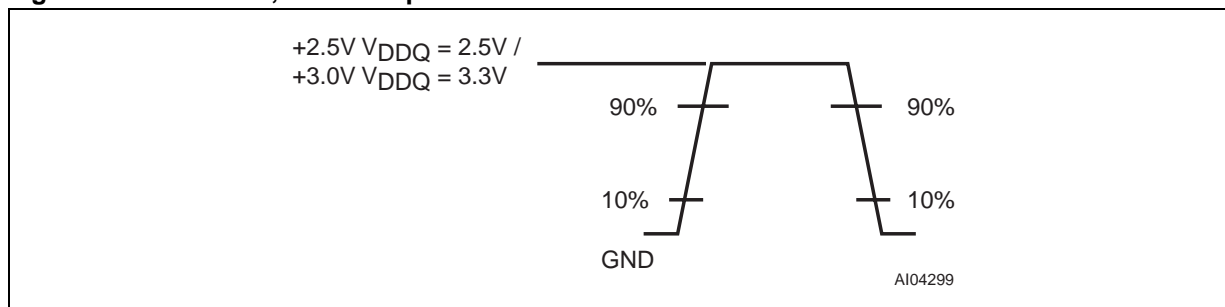
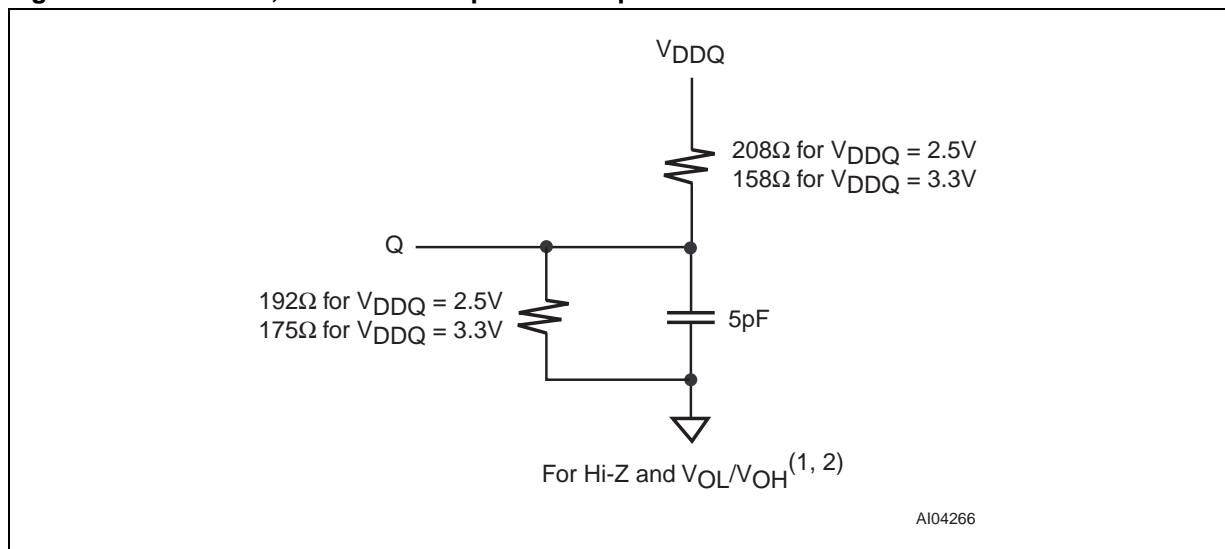


Figure 7. M7020R 2.5, or 3.3V I/O Output Load Equivalent



Note: 1. Output loading is specified with $C_L = 5pF$ as in Figure 7. Transition is measured at ± 200 mV from steady-state voltage.
 2. The load used for V_{OH} , V_{OL} testing is shown in Figure 7.

Table 5. Capacitance

Symbol	Parameter	Test Condition ^(1,2)	Min	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		6	pF
$C_{IO}^{(3)}$	Output Capacitance	$V_{OUT} = 0V$		6	pF

Note: 1. Effective capacitance measured with power supply. Sampled only, not 100% tested.

2. At 25°C, $f = 1\text{MHz}$.

3. Outputs deselected.

Table 6. DC Characteristics

Sym	Parameter	Test Condition ⁽¹⁾	Min	Max	Unit
I_{LI}	Input Leakage Current	$V_{DDQ} = V_{DDQ}(\text{max}), V_{IN} = 0 \text{ to } V_{DDQ}(\text{max})$		± 10	μA
I_{LO}	Output Leakage Current	$V_{DDQ} = V_{DDQ}(\text{max}), V_{IN} = 0 \text{ to } V_{DDQ}(\text{max})$		± 10	μA
V_{IL}	Input Low Voltage ($V_{DDQ} = 3.3V$)		-0.3	0.8	V
V_{IH}	Input High Voltage ($V_{DDQ} = 3.3V$)		2.0	$V_{DDQ} + 0.3$	V
V_{IL}	Input Low Voltage ($V_{DDQ} = 2.5V$)		-0.3	0.7	V
V_{IH}	Input High Voltage ($V_{DDQ} = 2.5V$)		1.7	$V_{DDQ} + 0.3$	V
V_{OL}	Output Low Voltage ($V_{DDQ} = 3.3V$)	$V_{DDQ} = V_{DDQ}(\text{min}), I_{OL} = 8\text{mA}$		0.4	V
V_{OH}	Output High Voltage ($V_{DDQ} = 3.3V$)	$V_{DDQ} = V_{DDQ}(\text{min}), I_{OH} = 8\text{mA}$	2.4		V
V_{OL}	Output Low Voltage ($V_{DDQ} = 2.5V$)	$V_{DDQ} = V_{DDQ}(\text{min}), I_{OL} = 8\text{mA}$		0.4	V
V_{OH}	Output High Voltage ($V_{DDQ} = 2.5V$)	$V_{DDQ} = V_{DDQ}(\text{min}), I_{OH} = 8\text{mA}$	2.0		V
I_{DD1}	1.8V Supply Current at $V_{DD}(\text{max})$	66MHz Search Rate		2300	mA
		50MHz Search Rate		1800	mA
I_{DD2}	3.3V Supply Current at $V_{DD}(\text{max})$	66MHz Search Rate, $I_{OUT} = 0\text{mA}$		200	mA
		50MHz Search Rate, $I_{OUT} = 0\text{mA}$		150	mA
I_{DD2}	2.5V Supply Current at $V_{DD}(\text{max})$	66MHz Search Rate, $I_{OUT} = 0\text{mA}$		160	mA
		50MHz Search Rate, $I_{OUT} = 0\text{mA}$		120	mA

Note: 1. Valid for Ambient Operating Temperature: $T_A = 0 \text{ to } 70^\circ\text{C}$; $V_{DD} = 1.5V$.

Figure 8. AC Timing Waveforms with CLK2X

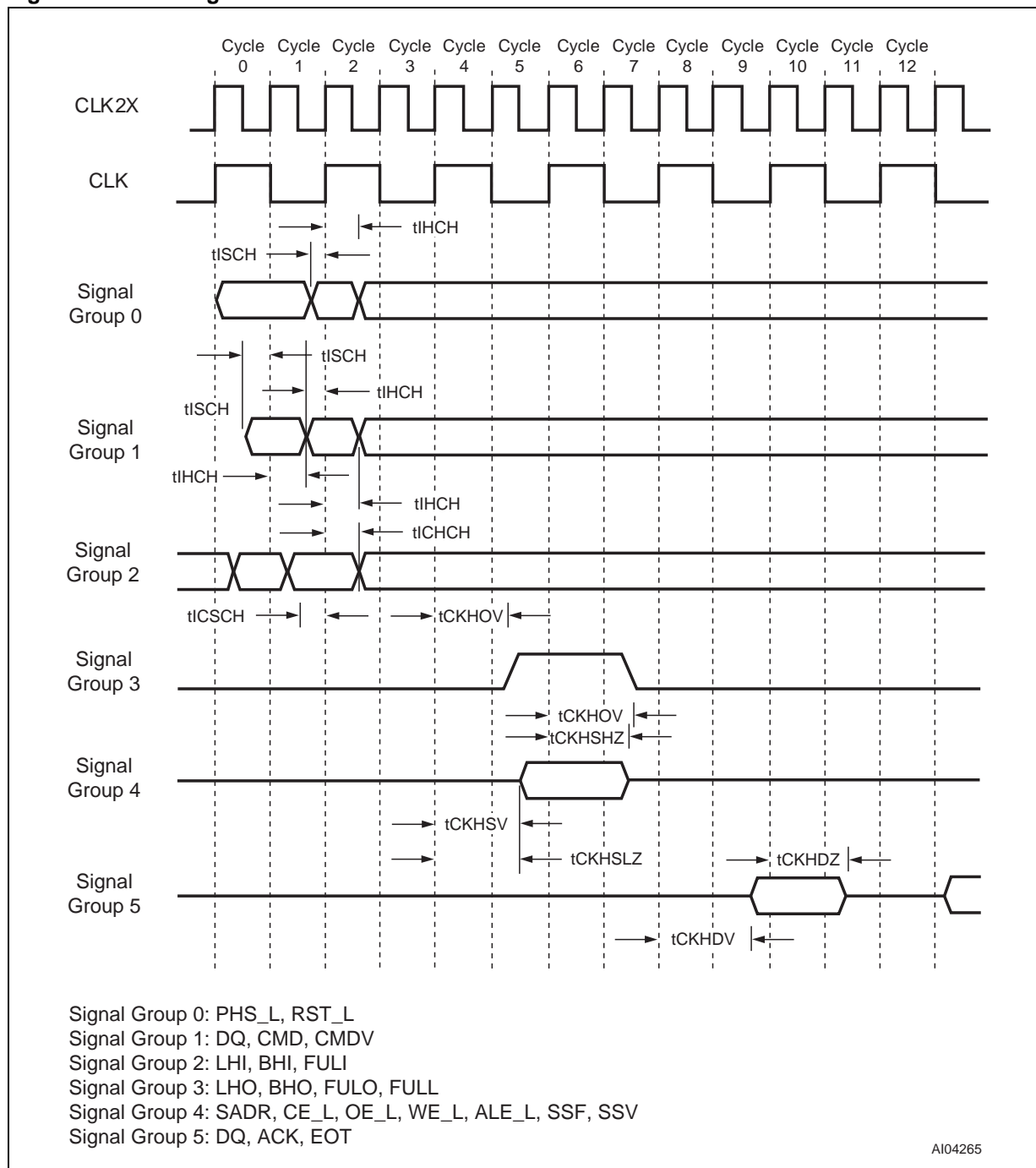


Table 7. AC Timing Parameters with CLK2X

Row	Symbol	M7020R-050		M7020R-066		M7020R-083		Unit	Description ⁽¹⁾
		Min	Max	Min	Max	Min	Max		
1	f _{CLOCK}		100		133		166	MHz	CLK2X frequency
2	t _{CLK}	10		7.5				ns	CLK2X period
3	t _{CKHI}	4.0		3.0				ns	CLK2X high pulse ⁽²⁾
4	t _{CKLO}	4.0		3.0				ns	CLK2X low pulse ⁽²⁾
5	t _{ISCH}	2.5		2.5		2.5		ns	Input Setup Time to CLK2X rising edge. ⁽²⁾
6	t _{IHCH}	0.6		0.6		0.6		ns	Input Hold Time to CLK2X rising edge. ⁽²⁾
7	t _{ICSCH}	4.2		4.2		4.2		ns	Cascaded Input Setup Time to CLK2X rising edge. ⁽²⁾
8	t _{ICHCH}	0.6		0.6		0.6		ns	Cascaded Input Hold Time to CLK2X rising edge. ⁽²⁾
9	t _{CKHOV}		9.5		8.5			ns	Rising edge of CLK2X to LHO, FULO, BHO, FULL valid. ⁽³⁾
10	t _{CKHDV}		10.0		9.0			ns	Rising edge of CLK2X to DQ valid. ⁽²⁾
11	t _{CKHDZ}	1.2	9.5	1.2	9.5	1.2	9.5	ns	Rising edge of CLK2X to DQ high-Z. ⁽⁴⁾
12	t _{CKHSV}		10.0		9.0			ns	Rising edge of CLK2X to SRAM Bus valid. ⁽²⁾
13	t _{CKHSHZ}		7.0		6.5			ns	Rising edge of CLK2X to SRAM Bus high-Z. ^(2,4)
14	t _{CKHSLZ}	7.5		7.0				ns	Rising edge of CLK2X to SRAM Bus low-Z. ^(2,4)

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{DD} = 1.8V.

2. Values are based on 50% signal levels.

3. Based on an AC load of CL = 30pF (see Figure 5, Figure 6, and Figure 7, page 14).

4. These parameters are sampled and not 100% tested, and are based on an AC load of 5pF.

OPERATION

The following subsections contain command (CMD and DQ Bus (command and databus), database entry, arbitration logic, pipeline, and SRAM control, and full logic descriptions.

CMD Bus and DQ Bus

CMD[8:0] carries the CMD and its associated parameter. DQ[67:0] is used for data transfer to and from the database entries, which comprise a data and a mask field that are organized as data and mask arrays. The DQ Bus carries the SEARCH data (of the data and mask arrays and internal registers) during the SEARCH command as well as the address and data during READ and/or WRITE operations. The DQ Bus can also carry the address information for the flow-through accesses to the external SRAMs and/or SSRAMs.

Database Entry (Data Array and Mask Array)

Each database entry comprises a data and a mask field. The resultant value of the entry is '1,' '0,' or 'X (don't care),' depending on the value in the data and mask bits. The on-chip priority encoder selects the first matching entry in the database that is nearest to location '0.'

Arbitration Logic

When multiple Search Engines are cascaded to create large databases, the data being searched is presented to all search engines simultaneously in the cascaded system. If multiple matches occur within the cascaded devices, arbitration logic on the search engines will enable the winning device (with a matching entry that is closest to address "0" of the cascaded database) to drive the SRAM bus.

Pipeline and SRAM Control

Pipeline latency is added to give enough time to a cascaded system's arbitration logic to determine the device that will drive the index of the matching entry on the SRAM bus. Pipeline logic adds latency to both the SRAM access cycles and the SSF and SSV signals to align them to the host ASIC receiving the associated data.

Full Logic

Bit[0] in each of the 68-bit entries has a special purpose for the LEARN command (0 = empty, 1 = full). When all the data entries have bit[0] = 1, the database asserts the FULL Flag, indicating all the search engines in the depth-cascaded array are full.

CONNECTION DESCRIPTIONS

Clocks and Reset

Master Clock (CLK2X). M7020R samples all the data and control pins on the positive edge of CLK2X. All signals are driven out of the device on the rising edge of CLK2X (when PHS_L is low).

Phase (PHS_L). This signal runs at half the frequency of CLK2X and generates an internal CLK from CLK2X see Figure 9, page 20.

Test Input (TEST - for Cypress Semiconductor Use Only). This signal should be connected to ground.

Reset (RST_L). Driving RST_L low initializes the device to a known state.

CMD and DQ Bus

CMD Bus (CMD[8:0]). [1:0] specifies the command; [8:2] contains the CMD parameters. The descriptions of individual commands explains the details of the parameters. The encoding of commands based on the [1:0] field are:

- 00: PIO READ
- 01: PIO WRITE
- 10: SEARCH
- 11: LEARN

CMD Valid (CMDV). Qualifies the CMD bus:

- 0: No Command
- 1: Command

Address/Data Bus (DQ[67:0]). This signal carries the READ and WRITE address and data during register, data, and mask array operations. It carries the compare data during SEARCH operations. It also carries the SRAM address during SRAM PIO accesses.

READ Acknowledge (ACK). This signal indicates that valid data is available on the DQ Bus during register, data, and mask array READ operations, or the data is available on the SRAM data bus during SRAM READ operations.

Note: ACK Signals require a weak external pull-down resistor such as 47 or 100 K Ω .

End of Transfer (EOT). This signal indicates the end of burst transfer to the data or mask array during READ or WRITE burst operations.

Note: EOT Signals require a weak external pull-down resistor such as 47 K Ω or 100 K Ω .

SEARCH Successful Flag (SSF). When asserted, this signal indicates that the device is the global winner in a SEARCH operation.

SEARCH Successful Flag Valid (SSV). When asserted, this signal qualifies the SSF signal.

SRAM Interface

SRAM Address (SADR[21:0]). This bus contains address lines to access off-chip SRAMs that contain associative data. See Table 50, page 127 for the details of the generated SRAM address. In a database of multiple M7020Rs, each corresponding bit of SADR from all cascaded devices must be connected.

SRAM Chip Enable (CE_L). This is chip enable control for external SRAMs. In a database of multiple M7020Rs, CE_L of all cascaded devices must be connected. This signal is then driven by only one of the devices.

SRAM Write Enable (WE_L). This is write enable control for external SRAMs. In a database of multiple M7020Rs, WE_L of all cascaded devices must be connected together. This signal is then driven by only one of the devices.

SRAM Output Enable (OE_L). This is output enable control for external SRAMs. Only the last device drives this signal (with the LRAM bit set).

Address Latch Enable (ALE_L). When this signal is low, the addresses are valid on the SRAM Address Bus. In a database of multiple M7020Rs, the ALE_L of all cascaded devices must be connected. This signal is then driven by only one of the devices.

Cascade Interface

Local Hit In (LHI[6:0]). These pins depth-cascade the device to form a larger table size. One signal of this bus is connected to the LHO[1] or LHO[0] of each of the upstream devices in a block. All unused LHI pins are connected to a logic '0.' (For more information, see DEPTH-CASCADING, page 122.)

Local Hit Out (LHO[1:0]). LHO[1] and LHO[0] are the same logical signal. LHO[1] or LHO[0] is connected to one input of the LHI bus of up to four downstream devices in a block of up to eight devices. (For more information, see DEPTH-CASCADING, page 122.)

Block Hit In (BHI[2:0]). Inputs from the previous BHO[2:0] are tied to the BHI[2:0] of the current device. In a four-block system, the last block can contain only seven devices because the ID code 1111 is used for broadcast access.

Block Hit Out (BHO[2:0]). These outputs from the last device in a block are connected to the BHI[2:0] inputs of the devices in the downstream blocks.

Full In (FULI[6:0]). Each signal in this bus is connected to FULO[0] or FULO[1] of an upstream device to generate the FULL signal for the depth-cascaded block.

Full Out (FULO[1:0]). FULO[1] and FULO[0] are the same logical signal. One of these two signals must be connected to the FULL of up to four downstream devices in a depth-cascaded table. Bit [0] in the data array indicates if the entry is full (1) or empty (0). This signal is asserted if all of the bits in the data array are '1s.' Refer to Depth-Cascading to Generate a "FULL" Signal, page 122.

Full Flag (FULL). When asserted, this signal indicates that the table consisting of many depth-cascaded devices is full.

Device Identification

Device Identification (ID[4:0]). The binary-encoded device ID for a depth-cascaded system starts at 00000 and goes up to 11110. 11111 is reserved for a special broadcast address that selects all cascaded search engines in the system.

On a broadcast READ-only, the device with the LDEV bit set to '1' responds.

Supplies

Chip Core Supply (VDD). This is equal to 1.8V.

Chip I/O Supply (VDDQ). This is equal to either 2.5 or 3.3V.

Test Access Port

Test Data In (TDI). This is the Test Access Port's Test Data In.

Test Clock (TCK). This is the Test Access Port's Test Clock.

Test Data Out (TDO). This is the Test Access Port's Test Data Out.

Test Mode Select (TMS). This is the Test Access Port's Test Mode Select.

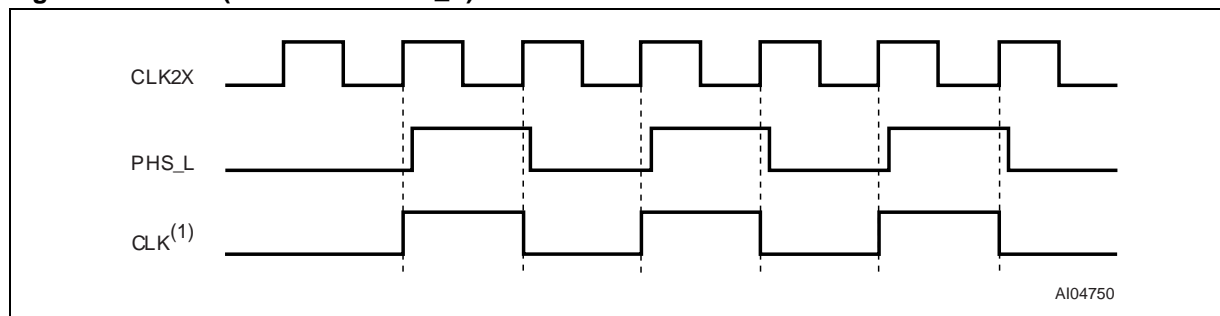
Test Reset (TRST_L). This is the Test Access Port's Test Reset.

CLOCKS

The M7020R receives the CLK2X and PHS_L signals. It uses the PHS_L signal to divide CLK2X and generate an internal clock (CLK), as shown in

Figure 9. The M7020R uses CLK2X and CLK for internal operations.

Figure 9. Clocks (CLK2X and PHS_L)



Note: Any reference to "CLK Cycles" means 1 cycle of the signal, "CLK."
 1. "CLK" is an internal signal.

REGISTERS

All registers in the M7020R are 68 bits wide. The M7020R contains 8 pairs of comparand storage registers, 16 pairs of global mask registers (GMRs), eight search successful index registers and one each of CMD, information, burst READ,

burst WRITE, and next-free address registers. Table 8 provides an overview of all the M7020R registers. The registers are ordered in ascending address order. Each register group is then described in the following subsections.

Table 8. Register Overview

Address	Abbreviation	Type	Name
0–31	COMP0–31	R	16 Comparand Registers. Stores comparands from the DQ Bus for learning later.
32–47	MASKS	RW	8 Global Mask Registers Array.
48–55	SSR0–7	R	8 SEARCH Successful Index Registers.
56	COMMAND	RW	Command Register.
57	INFO	R	Information Register.
58	RBURREG	RW	Burst Read Register.
59	WBURREG	RW	Burst Write Register.
60	NFA	R	Next Free Address Register.
61–63	–	–	Reserved

Comparand Registers

The device contains 32 68-bit comparand registers (16 pairs) dynamically selected in every SEARCH operation to store the comparand presented on the DQ Bus. The LEARN command will later use these registers when executed. The M7020R stores the SEARCH command's Cycle A comparand in the even-numbered register and the Cycle B comparand in the odd-numbered register, as shown in Figure 10.

Mask Registers

The device contains 16 68-bit global mask registers (8 pairs) dynamically selected in every SEARCH operation to select the search subfield. The addressing of these registers is explained in Figure 11. The three-bit GMR Index supplied on the CMD bus can apply 8 pairs of global masks during the SEARCH and WRITE operations, as shown in Figure 11.

Note: In 68-bit SEARCH and WRITE operations, the host ASIC must program both the even and odd mask registers with the same values.

Each mask bit in the GMRs is used during SEARCH and WRITE operations. In SEARCH operations, setting the mask bit to '1' enables compares; setting the mask bit to '0' disables compares (forced match) at the corresponding bit position. In WRITE operations to the data or mask array, setting the mask bit to '1' enables WRITES; setting the mask bit to '0' disables WRITES at the corresponding bit position.

Figure 10. Comparand Register Selection During SEARCH and LEARN Instructions

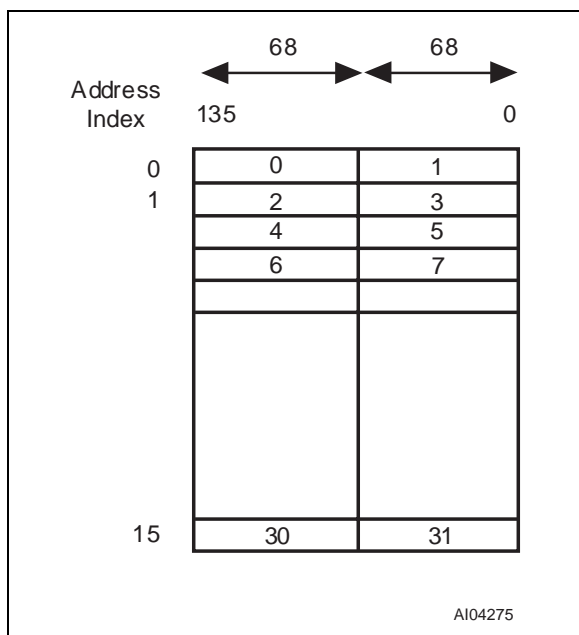
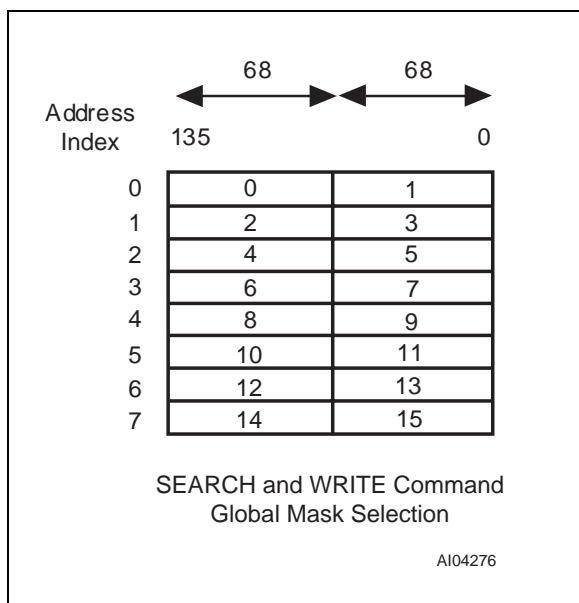


Figure 11. Addressing the Global Masks Register Array



SEARCH-Successful Registers (SSR[0:7])

The device contains eight search successful registers (SSRs) to hold the index of the location where a successful search occurred. The format of each register is described in Table 9. The SEARCH command specifies which SSR stores the index of a specific SEARCH command in Cycle B of the SEARCH Instruction. Subsequently, the host ASIC can use this register to access that

data array, mask array, or external SRAM using the index as part of the indirect access address (see Table 19, page 32 and Table 22, page 35).

The device with a valid bit set performs a READ or WRITE operation. All other devices suppress the operation.

Table 9. SEARCH-Successful Register (SSR) Description

Field	Range	Initial Value	Description
INDEX	[14:0]	X	Index. This is the address of the 68-bit entry where a successful search occurs. The device updates this field only when a search is successful. If a hit occurs in a 136-bit entry-size quadrant, the LSB is '0.' If a hit occurs in a 272-bit entry size quadrant, the two LSBs are '00.' This index updates if the device is either a local or global winner in a SEARCH operation.
–	[30:15]	0	Reserved.
VALID	[31]	0	Valid. During SEARCH operation in a depth-cascaded configuration, the device that is a global winner in a match sets this bit to '1.' This bit updates only when the device is a global winner in a SEARCH operation.
–	[67:32]	0	Reserved.

The Command Register

Table 10. Command Register Field Descriptions

Field	Range	Initial Value	Description								
SRST	[0]	0	Software Reset. If '1,' this bit resets the device, with the same effect as the hardware reset. Internally, it generates a reset pulse lasting for eight CLK cycles. This bit automatically resets to a '0' the reset cycle has completed.								
DEVE	[1]	0	Device Enable. If '0,' it keeps the SRAM Bus (SADR, WE_L, CE_L, OE_L, and ALE_L), SSF, and SSV signals in 3-state condition and forces the cascade interface output signals LHO[1:0] and BHO[2:0] to '0.' It also keeps the DQ Bus in input mode. The purpose of this bit is to make sure that there are no bus contentions when the devices power up in the system.								
TLSZ	[3:2]	01	Table Size. The host ASIC must program this field to configure the chips into a table of a certain size. This field affects the pipeline latency of the SEARCH and LEARN operations as well as the READ and WRITE accesses to the SRAM (SADR[21:0], CE_L, OE_L, WE_L, ALE_L, SSV, SSF, and ACK). Once programmed, the search latency stays constant.								
TLSZ	[3:2]	01	<p style="text-align: center;">Latency in # of CLK Cycles</p> <table> <tr> <td>00: 1 device</td> <td style="text-align: right;">4</td> </tr> <tr> <td>01: 2-8 devices</td> <td style="text-align: right;">5</td> </tr> <tr> <td>10: 9-31 devices</td> <td style="text-align: right;">6</td> </tr> <tr> <td>11: Reserved</td> <td></td> </tr> </table>	00: 1 device	4	01: 2-8 devices	5	10: 9-31 devices	6	11: Reserved	
00: 1 device	4										
01: 2-8 devices	5										
10: 9-31 devices	6										
11: Reserved											
HLAT	[6:4]	000	<p>Latency of Hit Signals. This field adds latency to the SSF and SSV signals during SEARCH, and ACK signal during SRAM READ access by the following number of CLK cycles.</p> <table> <tr> <td>000: 0</td> <td style="text-align: right;">100: 4</td> </tr> <tr> <td>001: 1</td> <td style="text-align: right;">101: 5</td> </tr> <tr> <td>010: 2</td> <td style="text-align: right;">110: 6</td> </tr> <tr> <td>011: 3</td> <td style="text-align: right;">111: 7</td> </tr> </table>	000: 0	100: 4	001: 1	101: 5	010: 2	110: 6	011: 3	111: 7
000: 0	100: 4										
001: 1	101: 5										
010: 2	110: 6										
011: 3	111: 7										
LDEV	[7]	0	<p>Last Device in the Cascade. When set, this device is the last device on the SRAM bus in the depth-cascaded table and is the default driver for the SSF and SSV signals.</p> <p>In the event of a SEARCH failure, the device with this bit set drives the hit signals as follows: SSF = 0, SSV = 1</p> <p>During non-SEARCH cycles, the device with this bit set drives the signals as follows: SSF = 0, SSV = 0</p>								
LRAM	[8]	0	<p>Last device on this SRAM Bus. When set, this device is the last device on this SRAM bus in the depth-cascaded table and is the default driver for the SADR, CE_L, WE_L, and ALE_L signals. In cycles where no M7020R device in a depth-cascaded table drives these signals, this device drives the signals as follows: SADR = 3FFFFFF, CE_L = 1 WE_L = 1 ALE_L = 1 OE_L is always driven by the device for which this bit is set.</p>								

Field	Range	Initial Value	Description
CFG	[16:9]	0000 0000	Database Configuration. The device is internally divided into four quadrants of 8K x 68, each of which can be configured as 8K x 68, 4K x 136, or 2K x 272 as follows: 00: 8K x 68 01: 4K x 136 10: 2K x 272 11: Reserved Bits [10:9] apply to configuring the 1st quadrant in the address space. Bits [12:11] apply to configuring the 2nd quadrant in the address space. Bits [14:13] apply to configuring the 3rd quadrant in the address space. Bits [16:15] apply to configuring the 4th quadrant in the address space.
	[67:17]	0	Reserved.

The Information Register

Table 11. Information Register Field Descriptions

Field	Range	Initial Value	Description
Revision	[3:0]	0001 ⁽¹⁾	Revision Number. This is the current device revision number. Numbers start from one and increment by one for each revision of the device.
Implementation	[6:4]	001	This is the M7020R implementation number.
Reserved	[7]	0	Reserved.
Device ID	[11:8]	0001 or 0010	This is the Device Identification Number.
Device ID	[12]		Reserved
Device ID	[15:13]	00000100	This is the Device Identification Number.
MFID	[31:16]	1101_1100_0111_1111	Manufacturer ID. This field is the same as the manufacturer ID and continuation bits in the TAP controller.
	[67:32]		Reserved.

Note: 1. This field may change in future versions.

M7020R

The Read Burst Address Register (RBURREG)

These READ burst address register fields must be programmed before burst READ (see Table 12).

The Write Burst Address Register (WBURREG)

These WRITE burst address register fields must be programmed before burst WRITE (see Table 13).

The NFA Register

Bit [0] of each 68-bit data entry is a special bit designated for use in the operation of the LEARN command. In 68-bit quadrants, the bit[0] indicates whether a location is full (bit set to '1') or empty (bit

set to '0'). Every WRITE/LEARN command loads the address of first 68-bit location that contains a '0' in the entry's bit[0]. This is stored in the NFA register (see Table 14). If all the bits in a device are set to '1,' the M7020R asserts FULO[1:0] to '1.'

In 136-bit-configured quadrants, the LSB of this register is always set to '0.' The host ASIC must set bit '0' and Bit 68 in a 136-bit word to either '0' or '1' to indicate full/empty status.

Note: Both bits (0 and 68) must be set to '0' or '1' (e.g., '10' or '01' settings are invalid).

Table 12. Read Burst Register Description

Field	Range	Initial Value	Description
ADR	[14:0]	0	Address. This is the starting address of the data array or mask array during a burst READ operation. It automatically increments by 1 for each successive read of the data array or mask array. Once the operation is complete, the contents of this field must be reinitialized for the next operation.
	[18:15]		Reserved.
BLEN	[27:19]	0	Length of Burst Access. The device is capable of writing from 4 up to 511 locations in a single burst. The BLEN decrements automatically. Once the operation is complete, the contents of this field must be reinitialized for the next operation.
	[67:28]		Reserved.

Table 13. Write Burst Register Description

Field	Range	Initial Value	Description
ADR	[14:0]	0	Address. This is the starting address of the data array or mask array during a burst WRITE operation. It automatically increments by 1 for each successive write of the data array or mask array. Once the operation is complete, the contents of this field must be reinitialized for the next operation.
	[18:15]		Reserved.
BLEN	[27:19]	0	Length of Burst Access. The device is capable of writing from 4 up to 511 locations in a single burst. The BLEN decrements automatically. Once the operation is complete, the contents of this field must be reinitialized for the next operation.
	[67:28]		Reserved.

Table 14. NFA Register

Address	67 - 15	14 - 0
60	Reserved	Index

SEARCH ENGINE ARCHITECTURE

The M7020R consists of 32K x 68-bit storage cells referred to as data bits. There is a mask cell corresponding to each data cell. Figure 12 shows the three organizations of the device based on the value of the CFG bits in the command register.

During a SEARCH operation, the search data bit (S), data array bit (D), mask array bit (M) and the global mask bit (G) are used in the following manner to generate a match at that bit position (see Table 15, page 28).

The entry with all matched bit positions results in a successful search during a SEARCH operation.

In order for a successful search within a device to make the device the local winner in the SEARCH operation, all 68-bit positions must generate a match for a 68-bit entry in 68-bit-configured quadrants, or all 136-bit positions must generate a match for two consecutive even and odd 68-bit entries in quadrants configured as 136 bits, or all

272-bit positions must generate a match for 4 consecutive entries aligned to 4 entry-page boundaries of 68-bit entries in quadrants configured as 272 bits.

An arbitration mechanism using a cascade bus determines the global winning device among the local winning devices in a SEARCH cycle. The global winning device drives the SRAM Bus, SSV, and the SSF signals. In case of a SEARCH failure, the devices with the LDEV and LRAM bits set drive(s) the SRAM Bus, SSF, and SSV signals.

The M7020R device can be configured to contain tables of different widths, even within the same chip. Figure 13, page 28 shows a sample configuration of different widths.

Data and Mask Addressing

Figure 14, page 28 shows the M7020R data array and mask array addressing procedure.

Figure 12. M7020R Database Width Configuration

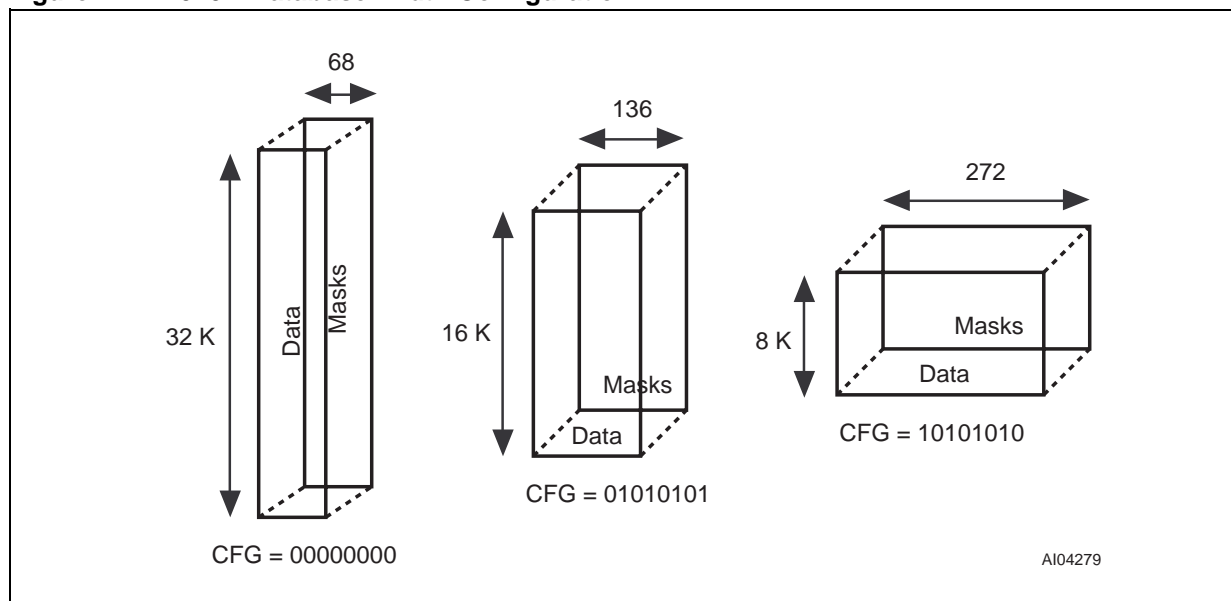


Table 15. Bit Position Match

G	M	D	S	Match
0	X	X	X	1
1	0	X	X	1
1	1	0	0	1
1	1	1	0	0
1	1	0	1	0
1	1	1	1	1

Figure 13. Multi-width Configuration Example

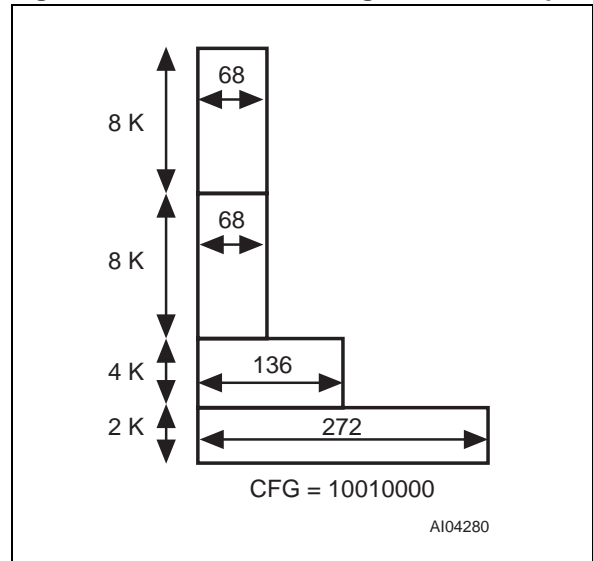
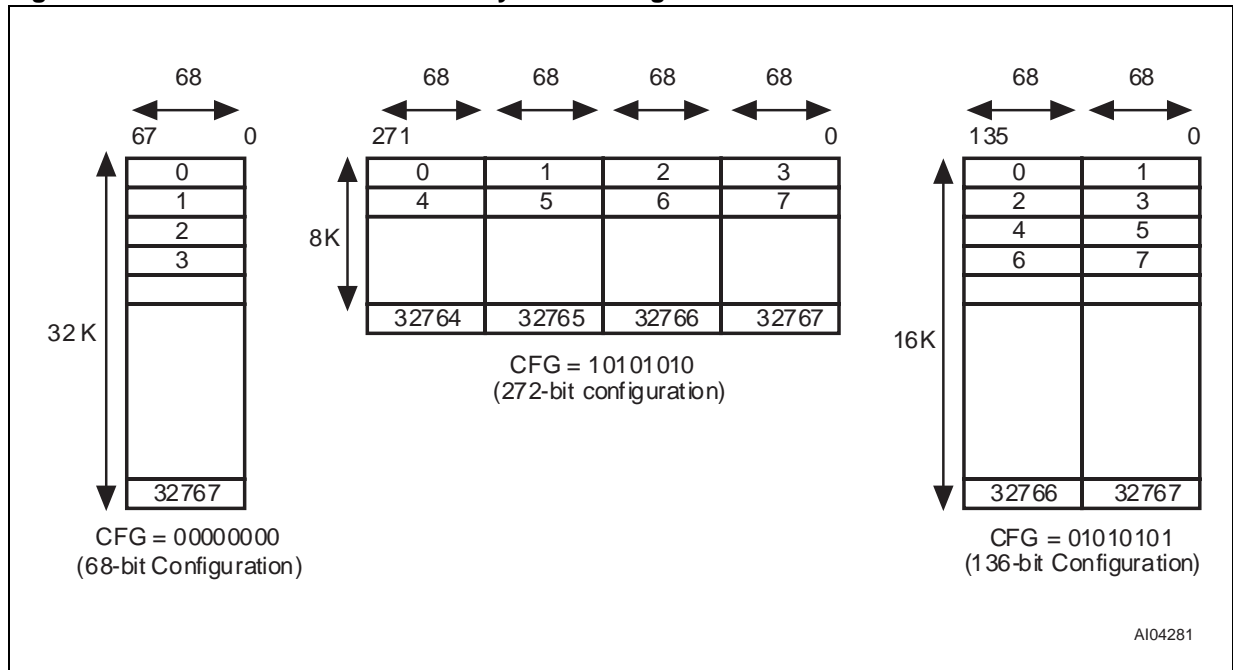


Figure 14. M7020R Data and Mask Array Addressing



COMMAND CODES AND PARAMETERS

A master device, such as an ASIC controller, issues commands to the M7020R using the Command Valid CMDV signal and the CMD Bus. The following subsections describe the functions of the commands.

Command Codes

The M7020R implements four basic commands shown in Table 16. The Command Code must be presented to CMD[1:0] while keeping the command valid (CMDV) signal high for two CLK2X cycles.

These two CLK2X cycles are designated as “Cycle A” and “Cycle B.” The controller ASIC must align the instructions with the PHS_L signal. The CMD[8:2] field passes the parameters of the command in Cycles A and B.

Commands and Command Parameters

Table 17, page 29 lists the CMD bus fields that contain the M7020R command parameters as well as their respective cycles.

Table 16. Command Codes

CMD Code	Command	Description
00	READ	Reads one of the following: data array, mask array, device registers, or external SRAM.
01	WRITE	Writes one of the following: data array, mask array, device registers, or external SRAM.
10	SEARCH	Searches the data array for a desired pattern using the specified register from the global mask register array and local mask associated with each data cell.
11	LEARN	The device has internal storage for up to 16 comparands that it can learn. The device controller can insert these entries at the next free address (as specified by the NFA register) using the LEARN Instruction.

Table 17. Command Parameters

Cmd	Cyc	8	7	6	5	4	3	2	1	0
READ	A	SADR[21]	SADR[20]	X	0	0	0	0 = Single 1 = Burst	0	0
	B	0	0	0	0	0	0	0 = Single 1 = Burst	0	0
WRITE	A	SADR[21]	SADR[20]	X	Global Mask Register Index [2:0]			0 = Single 1 = Burst	0	1
	B	0	0	0	Global Mask Register Index [2:0]			0 = Single 1 = Burst	0	1
SEARCH	A	SADR[21]	SADR[20]	SADR[19]	Global Mask Register Index [2:0]			68-bit or 136-bit: 0 272-bit: 1 in 1st Cycle 0 in 2nd Cycle	1	0
	B	Successful Search Register Index[2:0]			Comparand Register Index				1	0
LEARN ⁽¹⁾	A	SADR[21]	SADR[20]	X	Comparand Register Index				1	1
	B	0	0	Mode 0: 68-bit 1: 136-bit	Comparand Register Index				1	1

Note: 1. The 272-bit-configured devices or 272-bit-configured quadrants within devices do not support the LEARN Instruction.

READ COMMAND

The READ can be a single read of a data array, a mask array, an SRAM, or a register location (CMD[2] = 0). It can be a burst READ (CMD[2] = 1) or mask array locations using an internal auto-incrementing address register (RBURADR). Table 18, page 32 describes each type of READ command.

A single-location READ operation lasts six cycles, as shown in Figure 15, page 31. The burst READ adds two cycles for each successive READ. The SADR[21:20] bits supplied in the READ Instruction Cycle A drive SADR[21:20] signals during the READ of an SRAM location.

The single READ operation takes six CLK cycles, in the following sequence:

- **Cycle 1:** The host ASIC applies the READ Instruction on the CMD[1:0] (CMD[2] = 0), using CMDV = 1, and the DQ Bus supplies the address, as shown in Table 19, page 32 and Table 20, page 33. The host ASIC selects the M7020R for which ID[4:0] matches the DQ[25:21] lines. If the DQ[25:21] = 11111, the host ASIC selects the M7020R with the LDEV Bit set. The host ASIC also supplies SADR[21:20] on CMD[8:7] in Cycle A of the READ Instruction if the READ is directed to the external SRAM.
- **Cycle 2:** The host ASIC floats DQ[67:0] to 3-state condition.
- **Cycle 3:** The host ASIC keeps DQ[67:0] in 3-state condition.
- **Cycle 4:** The selected device starts to drive the DQ[67:0] Bus and drives the ACK signal from Z to low.
- **Cycle 5:** The selected device drives the read data from the addressed location on the DQ[67:0] Bus and drives the ACK signal high.
- **Cycle 6:** The selected device floats DQ[67:0] to 3-state condition and drives the ACK signal low.

At the termination of Cycle 6, the selected device releases the ACK line to 3-state condition. The READ Instruction is complete, and a new operation can begin.

Note: The latency of the SRAM READ will be different than the one described above (see SRAM PIO Access, page 126). Table 19, page 32 lists

and describes the format of the READ address for a data array, mask array, or SRAM.

In a burst READ operation, the READ lasts $4 + 2n$ CLK-cycles (where “n” stands for the number of accesses in the burst specified by the BLEN field of the RBURREG). Table 20, page 33 describes the READ address format for the internal registers. Figure 16, page 31 illustrates the timing diagram for the burst READ of the data or mask array. This operation assumes that the host ASIC has programmed the RBURREG with the starting address (ADR) and the length of transfer (BLEN) before initiating the burst READ command.

- **Cycle 1:** The host ASIC applies the READ Instruction on the CMD[1:0] (CMD[2] = 1), using CMDV=1 and the address supplied on the DQ Bus, as shown in Table 21, page 33. The host ASIC selects the M7020R for which ID[4:0] matches the DQ[25:21] lines. If the DQ[25:21] = 11111, the host ASIC selects the M7020R with the LDEV Bit set.
 - **Cycle 2:** The host ASIC floats DQ[67:0] to the 3-state condition.
 - **Cycle 3:** The host ASIC keeps DQ[67:0] in the 3-state condition.
 - **Cycle 4:** The selected device starts to drive the DQ[67:0] Bus and drives ACK and EOT from Z to low.
 - **Cycle 5:** The selected device drives the READ data from the addressed location on the DQ[67:0] Bus and drives the ACK signal high.
- Note:** Cycles four and five repeat for each additional access until all the accesses specified in the burst length (BLEN) field of RBURREG are complete. On the last transfer, the M7020R drives the EOT signal high.
- **Cycle (4 + 2n):** The selected device drives the DQ[67:0] to 3-state condition and drives the ACK and the EOT signals low.

At the termination of Cycle $4 + 2n$, the selected device floats the ACK line to 3-state condition. The burst READ Instruction is complete, and a new operation can begin (see Table 21, page 33 for burst READ address formats).

Figure 15. Single Location READ Cycle Timing

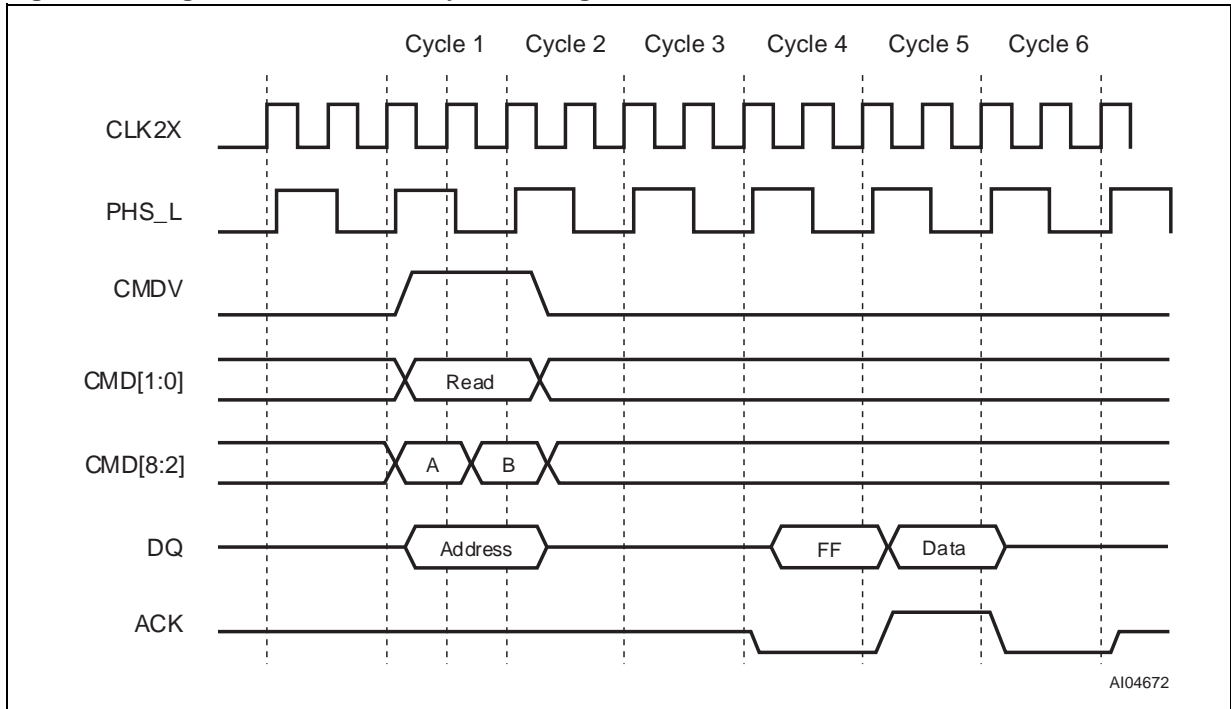


Figure 16. Burst READ of the Data and Mask Arrays (BLEN = 4)

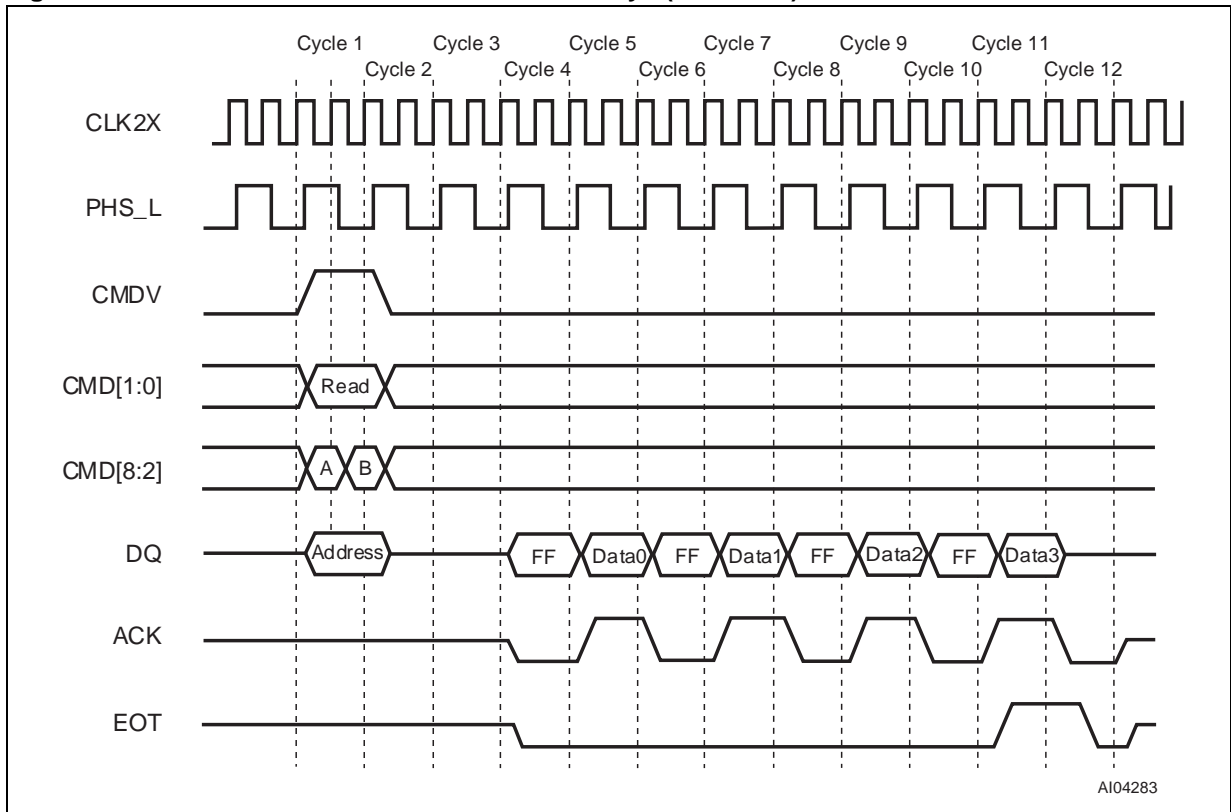


Table 18. READ Command Parameters

CMD Parameter CMD[2]	Read Command	Description
0	Single Read	Reads a single location of the data array, mask array, external SRAM, or device registers. All access information is applied on the DQ Bus.
1	Burst Read	<p>Reads a block of locations from the data array or mask array as a burst.</p> <p>The internal register (R BURADR) specifies the starting address and the length of the data transfer from the data array or mask array, and it auto-increments the address for each access.</p> <p>All other access information is applied on the DQ Bus.</p> <p>Note: The device registers and external SRAM can only be read in single-read mode.</p>

Table 19. Data and Mask Array, SRAM Read Address Format

DQ [67:30]	DQ [29]	DQ [28:26]	DQ [25:21]	DQ [20:19]	DQ [18:15]	DQ [14:0]
Reserved	0: Direct 1: Indirect	Successful SEARCH Register Index (Applicable if DQ[29] is indirect)	ID	00: Data Array	Reserved	If DQ[29] is '0,' this field carries address of data array location. If DQ[29] is '1,' the successful search register ID (SSRI) specified on DQ[28:26] supplies the address of the data array location: {SSR[14:2], SSR[1] DQ[1], SSR[0] DQ[0]} ⁽¹⁾
Reserved	0: Direct 1: Indirect	Successful SEARCH Register Index (Applicable if DQ[29] is indirect)	ID	01: Mask Array	Reserved	If DQ[29] is '0,' this field carries address of mask array location. If DQ[29] is '1,' the successful search register ID (SSRI) specified on DQ[28:26] supplies the address of the mask array location: {SSR[14:2], SSR[1] DQ[1], SSR[0] DQ[0]} ⁽¹⁾
Reserved	0: Direct 1: Indirect	Successful SEARCH Register Index (Applicable if DQ[29] is indirect)	ID	10: External SRAM	Reserved	If DQ[29] is '0,' this field carries address of SRAM location. If DQ[29] is '1,' the successful search register ID (SSRI) specified on DQ[28:26] supplies the address of the SRAM location: {SSR[14:2], SSR[1] DQ[1], SSR[0] DQ[0]} ⁽¹⁾

Note: 1. “|” stands for Logical OR operation. “{ }” stands for concatenation operator.

Table 20. READ Address Format for Internal Registers

DQ[67:26]	DQ[25:21]	DQ[20:19]	DQ[18:6]	DQ[5:0]
Reserved	ID	11: Register	Reserved	Register Address

Table 21. READ Address Format for Data and Mask Arrays

DQ[67:26]	DQ[25:21]	DQ[20:19]	DQ[18:15]	DQ[14:0]
Reserved	ID	00: Data Array	Reserved	Do not care. These 15 bits come from the internal register (R BURADR) which increments for each access.
Reserved	ID	01: Mask Array	Reserved	Do not care. These 16 bits come from the internal register (R BURADR) which increments for each access.

WRITE COMMAND

The WRITE can be a single write of a data array, mask array, register, or external SRAM location (CMD[2] = 0). It can be a burst WRITE (CMD[2] = 1) using an internal auto-incrementing address register (WBURADR) of the data array or mask array locations. A single-location WRITE is a three-cycle operation, shown in Figure 17, page 34. The burst WRITE adds one extra cycle for each successive WRITE.

The WRITE operation sequence is as follows:

- **Cycle 1A:** The host ASIC applies the WRITE Instruction on the CMD[1:0] (CMD[2] = 0), using CMDV=1 and the address supplied on the DQ Bus, as shown in Table 22, page 35. The host ASIC also supplies the index to the global mask register to mask the write to the data array or mask array location in CMD[5:3]. For SRAM WRITES, the host ASIC must supply the SADR[21:20] on CMD[8:6]. The host ASIC sets CMD[9] to '0' for the normal WRITE.
- **Cycle 1B:** The host ASIC continues to apply the WRITE Instruction to the CMD[1:0] (CMD[2] = 0), using CMDV = 1 and the address supplied on the DQ Bus. The host ASIC continues to supply the global mask register index to mask the WRITE to the data or mask array locations in CMD[5:3]. The host ASIC selects the device where ID[4:0] matches the DQ[25:21] lines, or it selects all the devices when DQ[25:21] = 11111.
- **Cycle 2:** The host ASIC drives the DQ[67:0] with the data to be written to the data array, mask array, external SRAM, or register location of the selected device.

- **Cycle 3:** Idle cycle. At the termination of this cycle, another operation can begin.

Note: The latency of the SRAM WRITE will be different than the one described above (see SRAM PIO Access, page 126).

The burst WRITE operation lasts for $n + 2$ CLK cycles (where n signifies the number of accesses in the burst as specified in the BLEN field of the WBURREG register, please see Figure 18, page 35).

This operation assumes that the host ASIC has programmed the WBURREG with the starting address (ADR) and the length of transfer (BLEN) before initiating the burst write command (see Table 24, page 36 for format). The sequence is as follows:

- **Cycle 1A:** The host ASIC applies the WRITE Instruction on the CMD[1:0] (CMD[2] = 1), using CMDV = 1 and the address supplied on the DQ Bus, as shown in Table 24, page 36. The host ASIC also supplies the index to the global mask register to mask the write to the data or mask array locations in CMD[5:3].
- **Cycle 1B:** The host ASIC continues to apply the WRITE Instruction on the CMD[1:0] (CMD[2] = 0), using CMDV = 1 and the address supplied on the DQ Bus. The host ASIC continues to supply the global mask register index to mask the WRITE to the data or mask array locations in CMD[5:3]. The host ASIC selects the device where ID[4:0] matches the DQ[25:21] lines, or it selects all the devices when DQ[25:21] = 11111.

M7020R

- **Cycle 2:** The host ASIC drives the DQ[67:0] with the data to be written to the data array or mask array location of the selected device. The M7020R writes the data from the DQ[67:0] Bus only to the subfield that has the corresponding mask bit set to '1' in the global mask register specified by the index CMD[5:3] and supplied in Cycle 1. The M7020R drives the EOT signal low from Cycle 3 to Cycle n; the M7020R drives the EOT signal high in Cycle n + 1 (n is specified in the BLEN field of the WBURREG).
- **Cycles 3 to n + 1:** The host ASIC drives the DQ[67:0] with the data to be written to the next data array or mask array location (addressed by the auto-increment ADR field of the WBURREG register) of the selected device.
- **Cycle n + 2:** The M7020R drives the EOT signal low. At the termination of the Cycle n + 2, the M7020R floats the EOT signal to a 3-state, and a new instruction can begin.

Figure 17. Single Location WRITE Cycle Timing

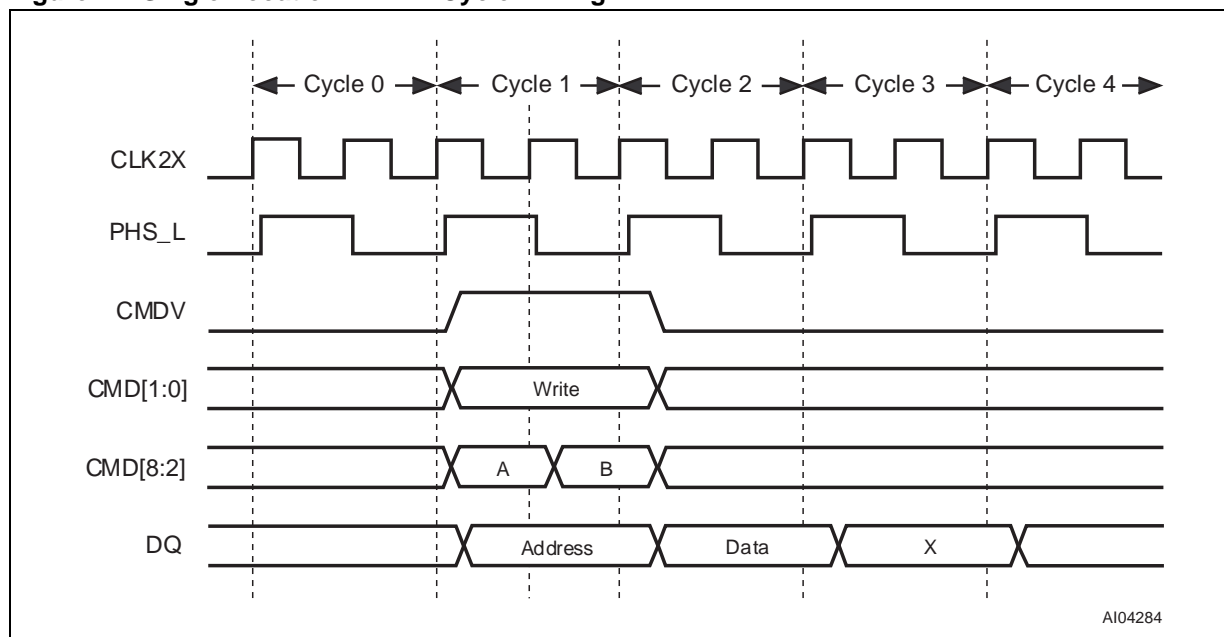


Figure 18. Burst WRITE of the Data and Mask Arrays (BLEN = 4)

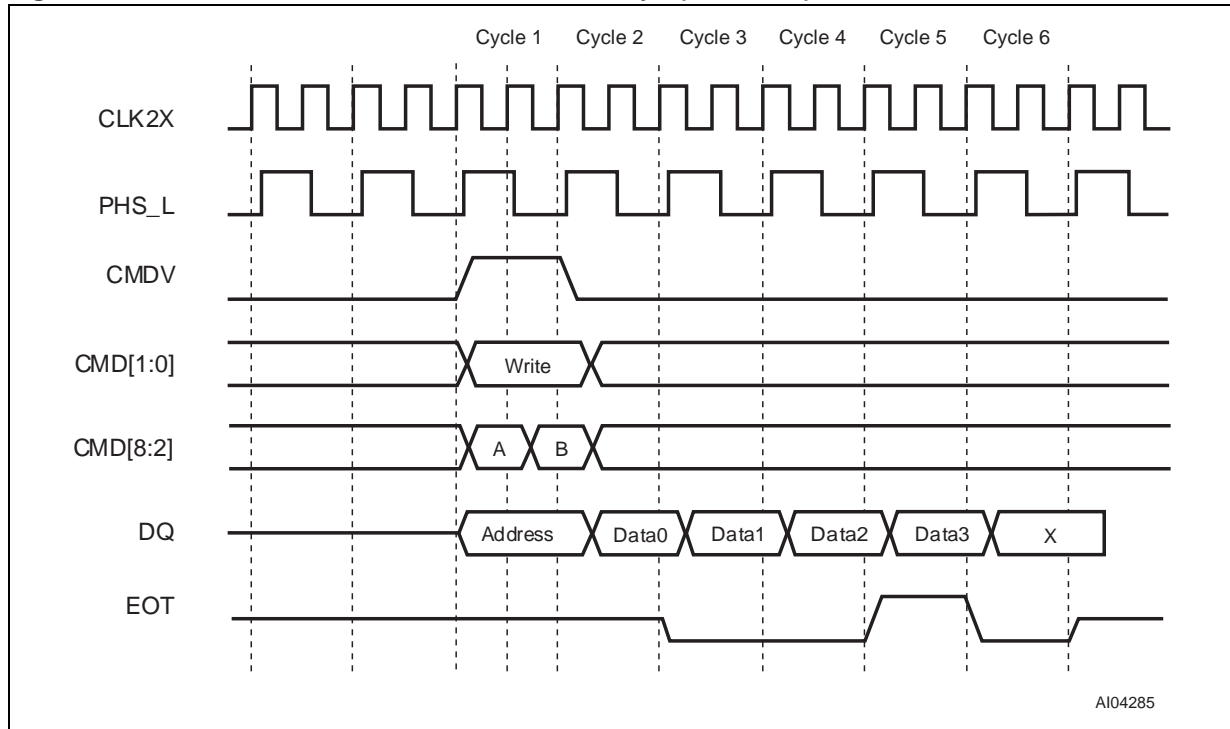


Table 22. (Single) WRITE Address Format for Data and Mask Arrays or SRAM

DQ [67:30]	DQ [29]	DQ [28:26]	DQ [25:21]	DQ [20:19]	DQ [18:15]	DQ [14:0]
Reserved	0: Direct 1: Indirect	Successful SEARCH Register Index (Applicable if DQ[29] is indirect)	ID	00: Data Array	Reserved	If DQ[29] is '0,' this field carries the address of the data array location. If DQ[29] is '1,' the successful search register specified by DQ[28:26] supplies the address of the data array location: {SSR[14:2], SSR[1] DQ[1], SSR[0] DQ[0]} ⁽¹⁾
Reserved	0: Direct 1: Indirect	Successful SEARCH Register Index (Applicable if DQ[29] is indirect)	ID	01: Mask Array	Reserved	If DQ[29] is '0,' this field carries address of the mask array location. If DQ[29] is '1,' the successful search register specified by DQ[28:26] supplies the address of the mask array location: {SSR[14:2], SSR[1] DQ[1], SSR[0] DQ[0]} ⁽¹⁾
Reserved	0: Direct 1: Indirect	Successful SEARCH Register Index (Applicable if DQ[29] is indirect)	ID	10: External SRAM	Reserved	If DQ[29] is '0,' this field carries address of the data SRAM location. If DQ[29] is '1,' the successful search register specified by DQ[28:26] supplies the address of the SRAM location: {SSR[14:2], SSR[1] DQ[1], SSR[0] DQ[0]} ⁽¹⁾

Note: 1. "||" stands for Logical OR operation. "{" stands for concatenation operator.

Table 23. WRITE Address Format for Internal Registers

DQ[67:26]	DQ[25:21]	DQ[20:19]	DQ[18:6]	DQ[5:0]
Reserved	ID	11: Register	Reserved	Register address

Table 24. WRITE Address Format for Data and Mask Array (Burst Write)

DQ [67:26]	DQ [25:21]	DQ [20:19]	DQ [18:15]	DQ [14:0]
Reserved	ID	00: Data array	Reserved	Don't care. These 15 bits come from the internal register (WBURADR), which increments with each access.
Reserved	ID	01: Mask array	Reserved	Don't care. These 15 bits come from the internal register (WBURADR), which increments with each access.

SEARCH COMMAND

The M7020R (Silicon) Search Engine can be configured in ten ways:

- 68-bit SEARCH on tables configured as x68 using one device
- 68-bit SEARCH on tables configured as x68 using up to 8 devices
- 68-bit SEARCH on tables configured as x68 using up to 31 devices
- 136-bit SEARCH on tables configured as x136 using one device
- 136-bit SEARCH on tables configured as x136 using up to 8 devices
- 136-bit SEARCH on tables configured as x136 using up to 31 devices
- 272-bit SEARCH on tables configured as x272 using one devices
- 272-bit SEARCH on tables configured as x272 using up to 8 devices
- 272-bit SEARCH on tables configured as x272 using up to 31 devices
- Mixed-sizes on tables configured with different widths using an M7020R

68-bit Configuration with Single Device

The hardware diagram of the search subsystem of a single device is shown in Figure 19. Figure 20, page 38 shows the timing diagram for a SEARCH operation in the 68-bit configuration (CFG = 00000000) for one set of parameters. This illustra-

tion assumes that the host ASIC has programmed TLSZ to '00,' HLAT to '000,' LRAM to '1,' and LDEV to '1' in the command register.

The following is the sequence of operations for a single 68-bit SEARCH command.

- **Cycle A:** The host ASIC drives CMDV high and applies the SEARCH command code ('10') on CMD[1:0] signals. CMD[5:3] must be driven with the index to the global mask register pair for use in the SEARCH operation. CMD[8:7] signals must be driven with the same bits that will be driven on SADR[21:20] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data to be compared. The CMD[2] signal must be driven to Logic '0.'
- **Cycle B:** The host ASIC continues to drive CMDV high and applies the SEARCH command ('10') on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ Bus during Cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the Hit Flag (see SEARCH-Successful Registers (SSR[0:7]), page 23). The DQ[67:0] continues to carry the 68-bit data to be compared.

Note: In the 68-bit configuration, the host ASIC must supply the same data on DQ[67:0] during both Cycles A and B. The even and odd pair of GMRs selected for the comparison must be programmed with the same value.

The logical 68-bit SEARCH operation is shown in Figure 21, page 39. The entire table consisting of 68-bit entries is compared to a 68-bit word K (presented on the DQ Bus in both Cycles A and B of the command) using the GMR and the local mask bits. The effective GMR is the 68-bit word specified by the identical value in both even and odd GMR pairs selected by the GMR Index in the command's Cycle A. The 68-bit word K (presented on the DQ Bus in both Cycles A and B of the command) is also stored in both even and odd comparand register pairs selected by the Comparand Register Index in the command's Cycle B. In a x68 configuration, only the even comparand register can be subsequently used by the LEARN command. The word K (presented on the DQ Bus in both Cycles A and B of the command) is compared with each entry in the table starting at location "0."

The first matching entry's location address, "L," is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see SRAM ADDRESSING, page 126).

The SEARCH command is a pipelined operation and executes a SEARCH at half the rate of the frequency of CLK2X for 68-bit searches in x68-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 68-bit SEARCH command cycle (two CLK2X cycles) is shown in Table 25, page 39.

The latency of a SEARCH from command to SRAM access cycle is 4 for a single device in the table and TLSZ = 00. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in Table 26, page 39.

Figure 19. Hardware Diagram for a Table with One Device

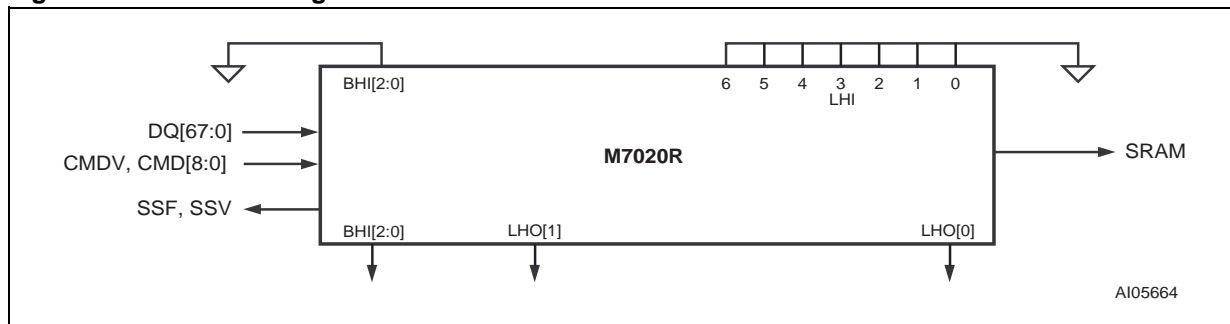


Figure 20. Timing Diagram for a 68-bit Configuration SEARCH for One Device

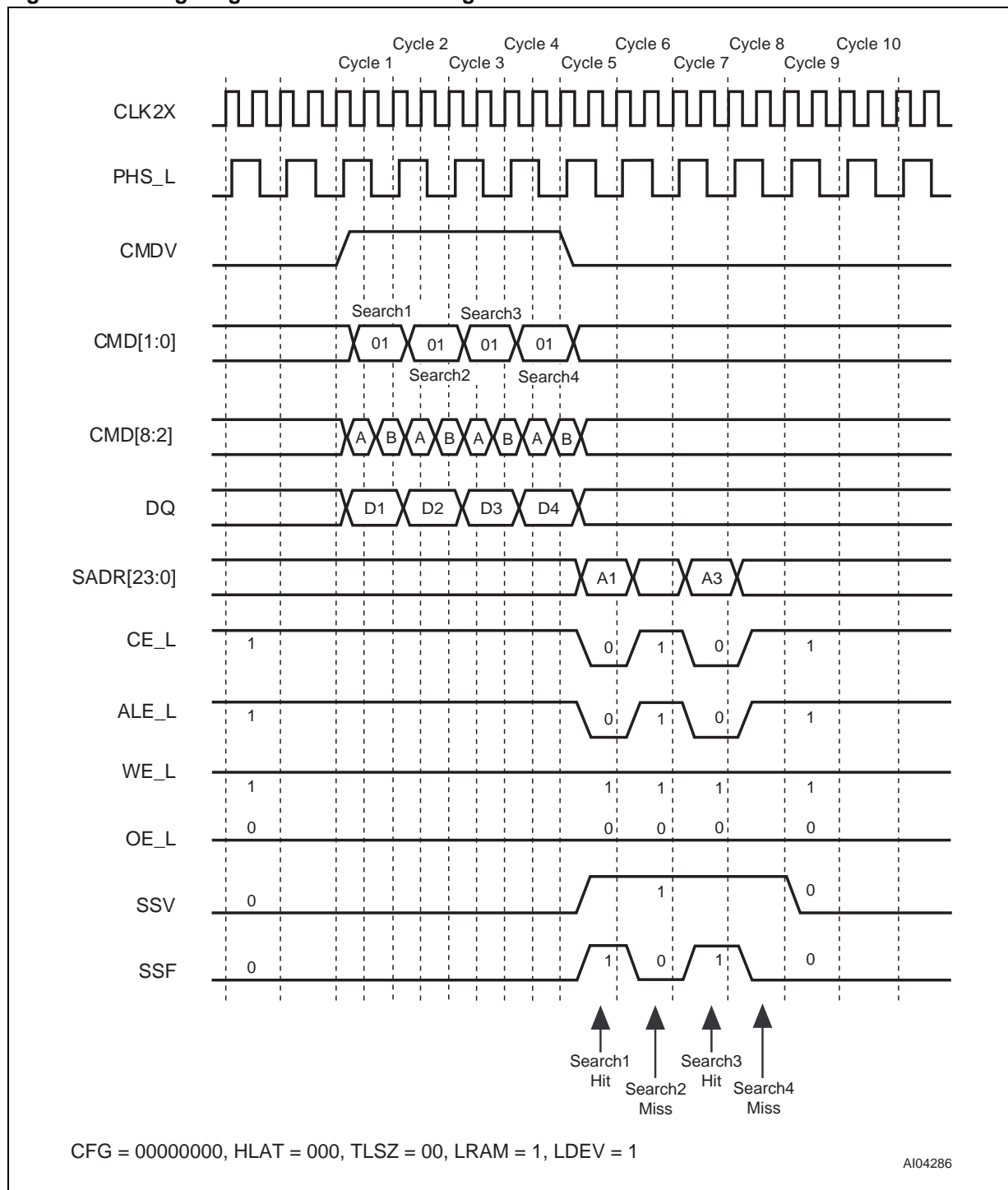


Figure 21. x68 Table with One Device

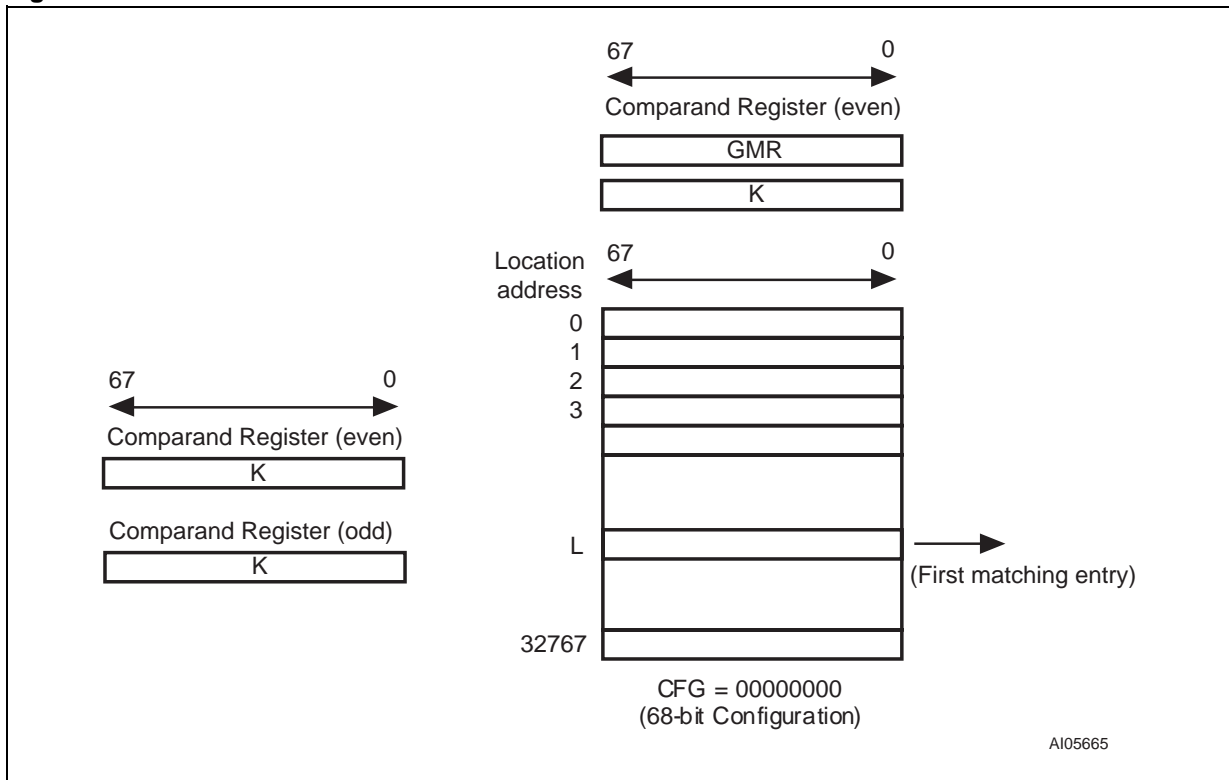


Table 25. Latency of SEARCH from Instruction to SRAM Access Cycle, 68-bit, 1 Device

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	32K x 68-bit	4
2-8 (TLSZ = 01)	256K x 68-bit	5
9-31 (TLSZ = 10)	992K x 68-bit	6

Table 26. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

68-bit SEARCH on Tables Configured as x68 Using up to Eight M7020R Devices

The hardware diagram of the search subsystem of eight devices is shown in Figure 22, page 41. The following are the parameters programmed into the eight devices:

- First seven devices (device 0–6):
CFG = 00000000, TLSZ = 01, HLAT = 010,
LRAM = 0, and LDEV = 0.
- Eighth device (device 7):
CFG = 00000000, TLSZ = 01, HLAT = 010,
LRAM = 1, and LDEV = 1.

Note: All eight devices must be programmed with the same values for TLSZ and HLAT. Only the last device in the table (Device 7 in this case) must be programmed with LRAM = 1 and LDEV = 1. All other upstream devices (Devices 0 through 6 in this case) must be programmed with LRAM = 0 and LDEV = 0.

Figure 24, page 43 shows the timing diagram for a SEARCH command in the 68-bit-configured table of eight devices for Device 0. Figure 25, page 44 shows the timing diagram for a SEARCH command in the 68-bit-configured table of eight devices for Device 1. Figure 26, page 45 shows the timing diagram for a SEARCH command in the 68-bit-configured table of eight devices for Device 7 (the last device in this specific table). For these timing diagrams four 68-bit searches are performed sequentially. HIT/MISS assumptions were made as shown below in Table 27.

The sequence of operation for a 68-bit SEARCH command is as follows:]

- **Cycle A:** The host ASIC drives CMDV high and applies the SEARCH command code ('10') on CMD[1:0] signals. CMD[5:3] must be driven with the index to the global mask register pair for use in the SEARCH operation. CMD[8:7] signals must be driven with the same bits that will be driven on SADR[23:21] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data to be compared. The CMD[2] signal must be driven to Logic '0.'
- **Cycle B:** The host ASIC continues to drive CMDV high and applies the SEARCH command ('10') on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ Bus during Cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the Hit Flag (see SEARCH-Successful

Registers (SSR[0:7]), page 23). The DQ[67:0] continues to carry the 68-bit data to be compared.

Note: For 68-bit searches, the host ASIC must supply the same data on DQ[67:0] during both Cycles A and B. The even and odd pair of GMRs selected for the comparison must be programmed with the same value.

The logical 68-bit SEARCH operation is shown in Figure 23, page 42. The entire table with eight devices of 68-bit entries is compared to a 68-bit word K (presented on the DQ Bus in both Cycles A and B of the command) using the GMR and the local mask bits. The effective GMR is the 68-bit word specified by the identical value in both even and odd GMR pairs in each of the eight devices and selected by the GMR Index in the command's Cycle A. The 68-bit word K (presented on the DQ Bus in both Cycles A and B of the command) is also stored in both even and odd comparand register pairs (selected by the Comparand Register Index in command Cycle B) in each of the eight devices. In the x68 configuration, only the even comparand register can subsequently be used by the LEARN command in one of the devices (only the first non-full device). The word K (presented on the DQ Bus in both Cycles A and B of the command) is compared with each entry in the table starting at location "0." The first matching entry's location address, "L," is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see SRAM ADDRESSING, page 126). The global winning device will drive the bus in a specific cycle. On a global miss cycle the device with LRAM = 1 (default driving device for the SRAM Bus) and LDEV = 1 (default driving device for SSF and SSV signals) will be the default driver for such missed cycles.

The SEARCH command is a pipelined operation and executes a search at half the rate of the frequency of CLK2X for 72-bit searches in x68-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 68-bit SEARCH command cycle (two CLK2X cycles) is shown in Table 28, page 46

The latency of the search from command to SRAM access cycle is 5 for up to eight devices in the table (TLSZ = 01). SSV and SSF also shift further to the right for different values of HLAT, as specified in Table 29, page 46.

Table 27. Hit/Miss Assumption

Search Number	1	2	3	4
Device 0	Hit	Miss	Hit	Miss
Device 1	Miss	Hit	Hit	Miss
Device 2-6	Miss	Miss	Miss	Miss
Device 7	Miss	Miss	Hit	Hit

Figure 22. Hardware Diagram for a Table with Eight Devices

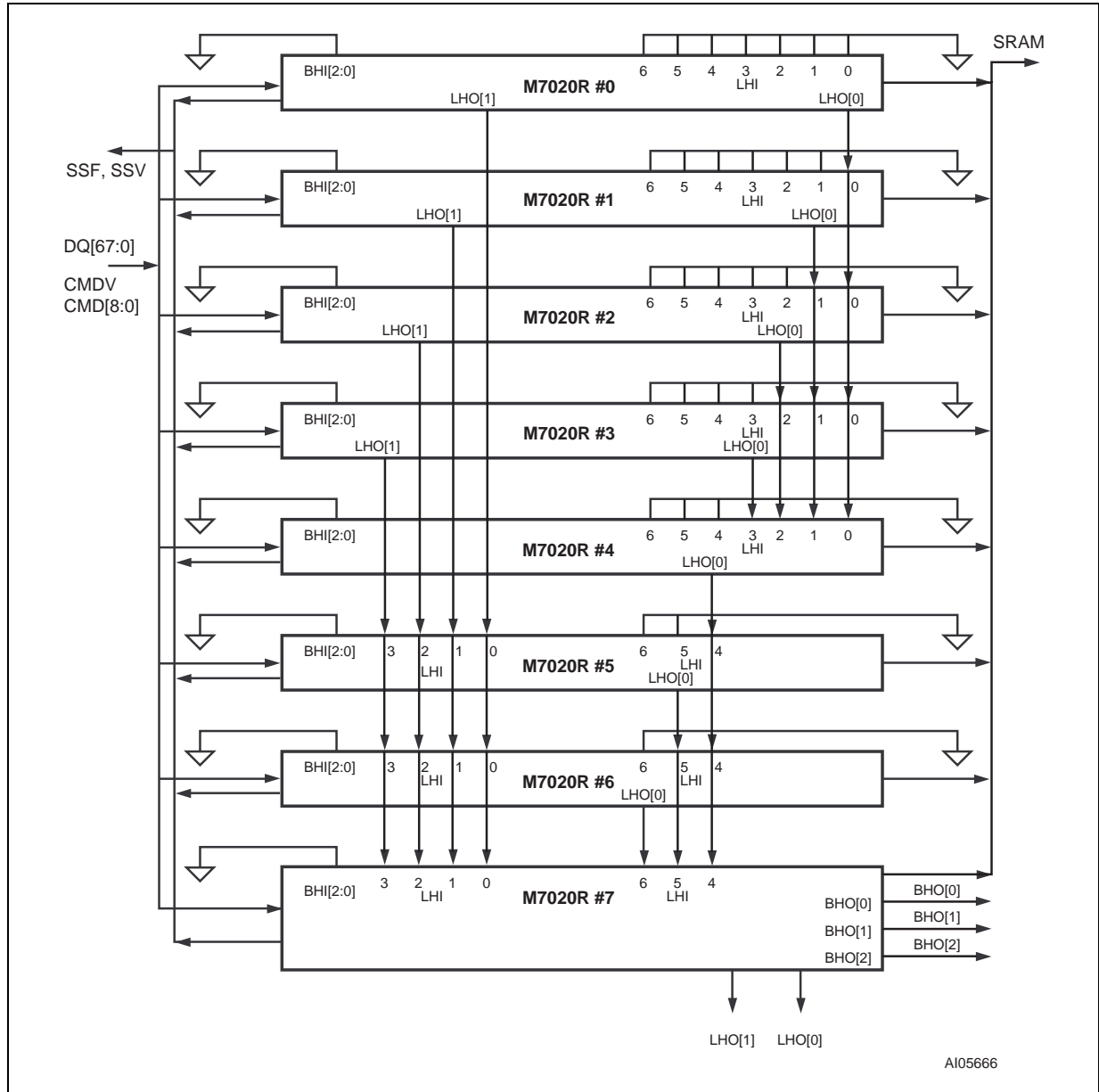
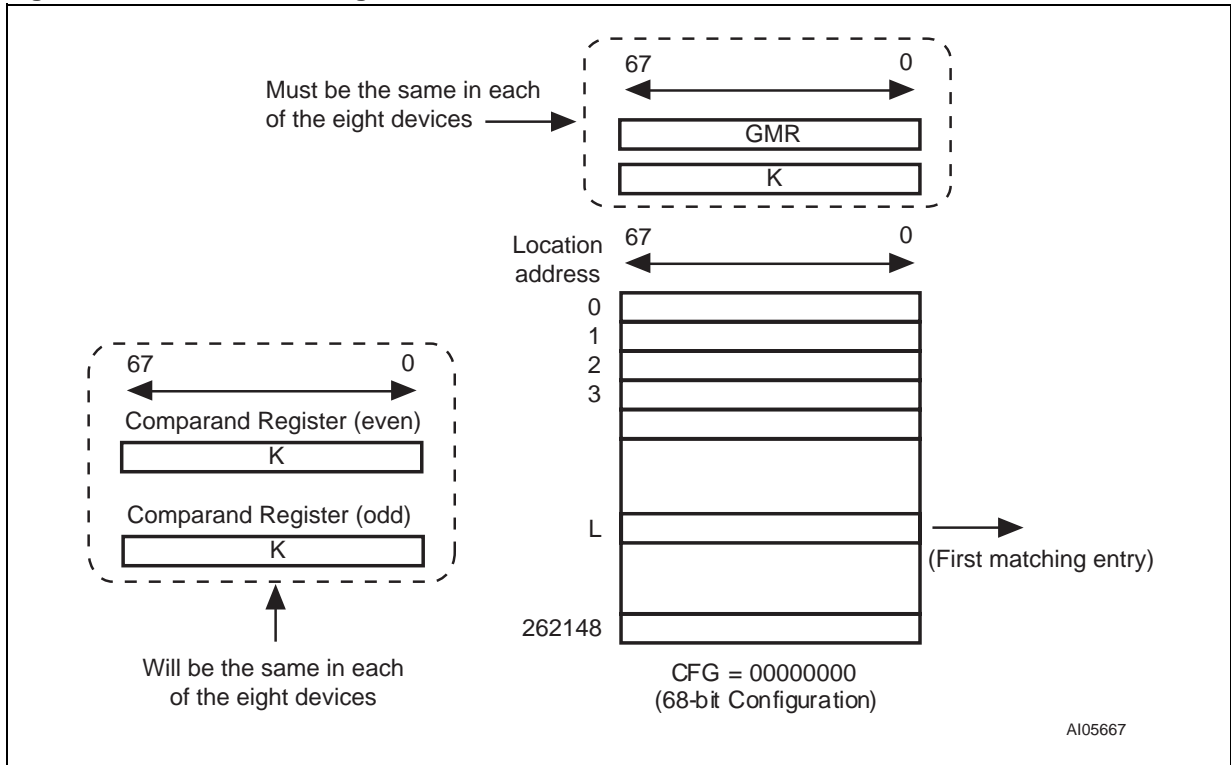


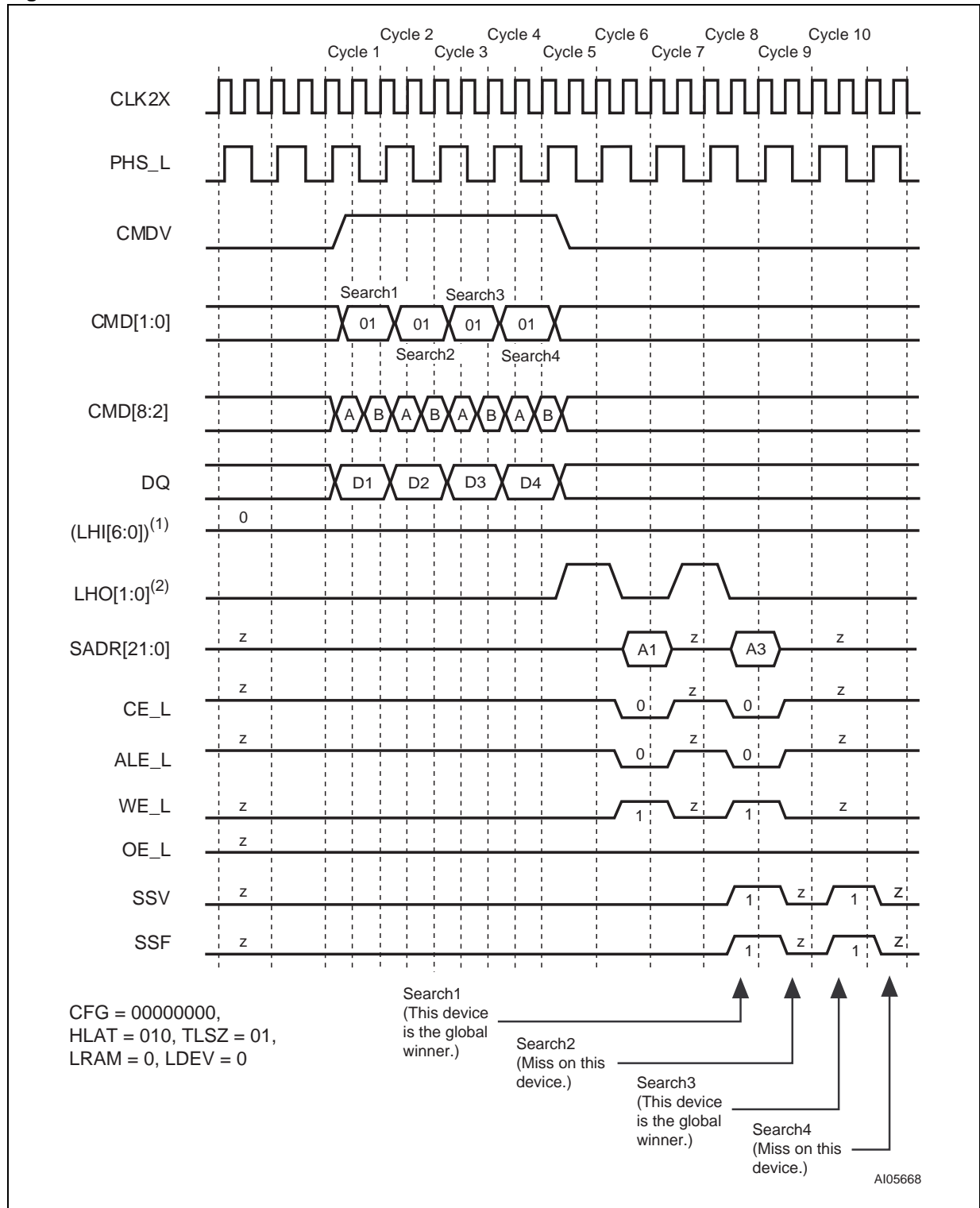
Figure 23. x68 Table with Eight Devices



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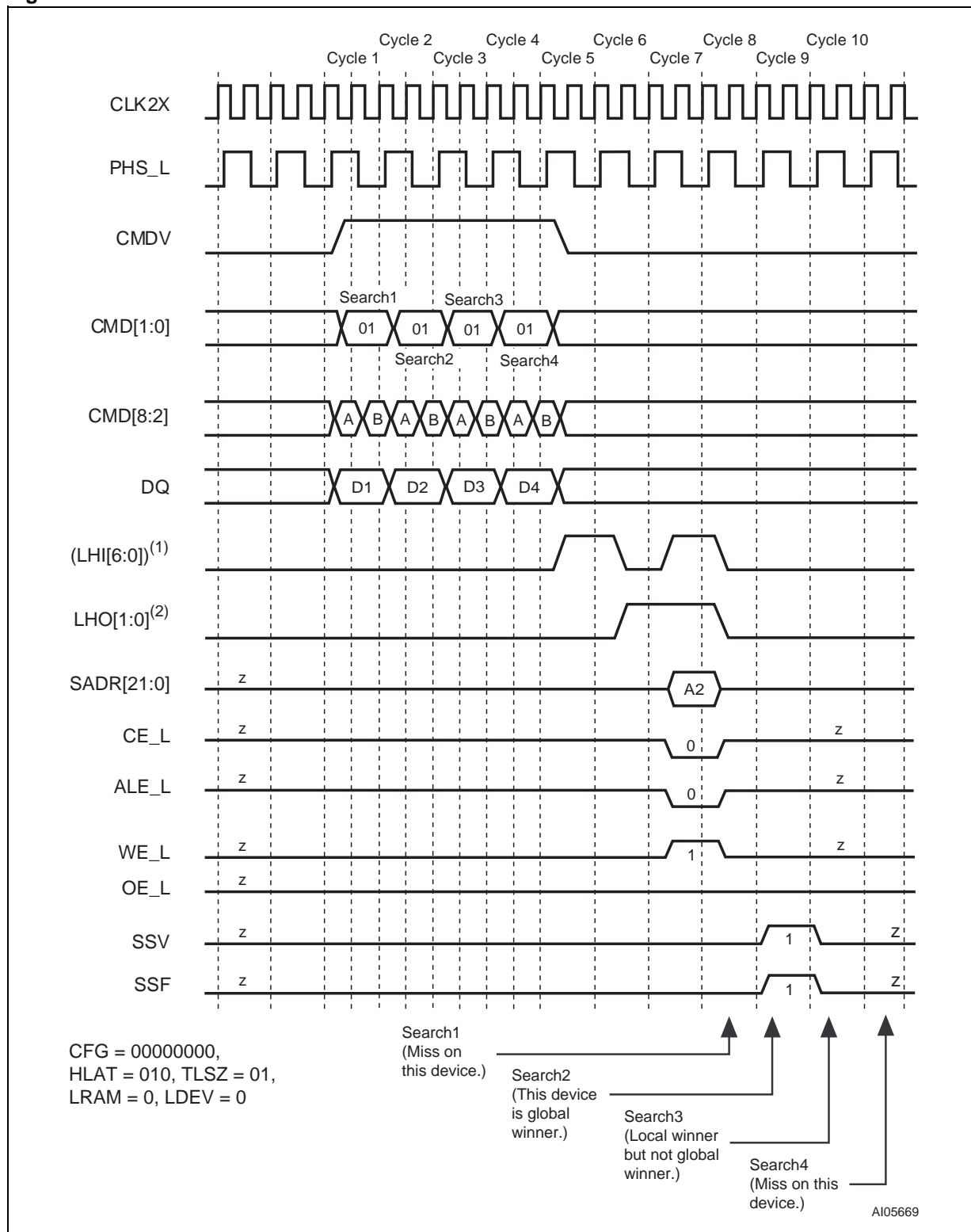
Timing Diagrams for x68 Using up to Eight M7020R Devices

Figure 24. 68-bit SEARCH For Device 0



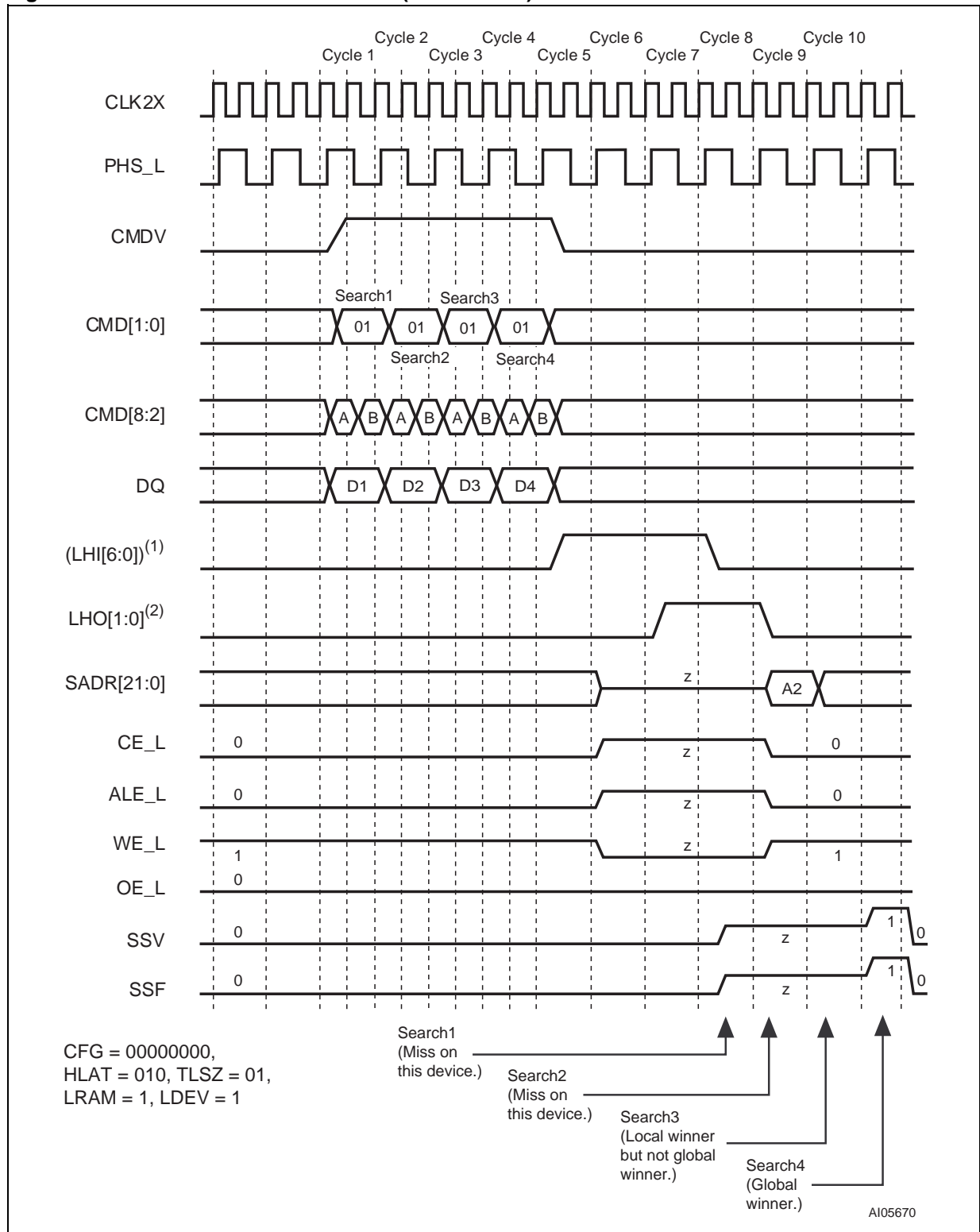
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.

Figure 25. 68-bit SEARCH For Device 1



Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.

Figure 26. 68-bit SEARCH For Device 7 (Last Device)



Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.

Table 28. Latency of SEARCH from Instruction to SRAM Access Cycle, 68-bit, Up to 8 Devices

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	32K x 68-bit	4
2–8 (TLSZ = 01)	256K x 68-bit	5
9–31 (TLSZ = 10)	992K x 68-bit	6

Table 29. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

68-bit SEARCH on Tables Configured as x68 Using Up To 31 M7020R Devices

The hardware diagram of the search subsystem of 31 devices is shown in Figure 27, page 48. Each of the four blocks in the diagram represents eight M7020R devices (except the last, which has seven devices). The diagram for a block of eight devices is shown in Figure 28, page 49. The following are the parameters programmed into the 31 devices:

- First thirty devices (devices 0–29):
CFG = 00000000, TLSZ = 10, HLAT = 001, LRAM = 0, and LDEV = 0.
- Thirty-first device (device 30):
CFG = 00000000, TLSZ = 10, HLAT = 001, LRAM = 1, and LDEV = 1.

Note: All 31 devices must be programmed with the same values for TLSZ and HLAT. Only the last device in the table must be programmed with LRAM = 1 and LDEV = 1 (Device 30 in this case). All other upstream devices must be programmed with LRAM = 0 and LDEV = 0 (Devices 0 through 29 in this case).

The timing diagrams referred to in this paragraph reference the HIT/MISS assumptions defined in Table 30, page 47. For the purpose of illustrating the timings, it is further assumed that there is only

one device with a matching entry in each of the blocks. Figure 30, page 51 shows the timing diagram for a SEARCH command in the 68-bit-configured table of 31 devices for each of the eight devices in Block Number 0. Figure 31, page 52 shows a timing diagram for a SEARCH command in the 68-bit-configured table of 31 devices for the all the devices in Block Number 1 (above the winning device in that block). Figure 32, page 53 shows the timing diagram for the globally winning device (defined as the final winner within its own and all blocks) in Block Number 1. Figure 33, page 54 shows the timing diagram for all the devices below the globally winning device in Block Number 1. Figure 34, page 55, Figure 35, page 56, and Figure 36, page 57 show the timing diagrams of the devices above the globally winning device, the globally winning device, and the devices below the globally winning device, respectively, for Block Number 2. Figure 37, page 58, Figure 38, page 59, Figure 39, page 60, and Figure 40, page 61 show the timing diagrams of the devices above globally winning device, the globally winning device, and the devices below the globally winning device except the last device (Device 30), respectively, for Block Number 3.

The following is the sequence of operation for a single 68-bit SEARCH command (also refer to Command Codes, page 29).

- **Cycle A:** The host ASIC drives the CMDV high and applies SEARCH command code ('10') on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair for use in this SEARCH operation. CMD[8:7] signals must be driven with the same bits that will be driven on SADR[21:20] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data to be compared. The CMD[2] signal must be driven to a logic '0.'
- **Cycle B:** The host ASIC continues to drive the CMDV high and applies SEARCH command ('10') on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ Bus during Cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the Hit Flag (see SEARCH-Successful Registers (SSR[0:7]), page 23). The DQ[67:0] continues to carry the 68-bit data to be compared.

Note: For 68-bit searches, the host ASIC must supply the same 68-bit data on DQ[67:0] during both Cycles A and B. The even and odd pair of GMRs selected for the comparison must be programmed with the same value.

The logical 68-bit SEARCH operation is shown in Figure 29, page 50. The entire table (31 devices of 68-bit entries) is compared to a 68-bit word K (presented on the DQ Bus in both Cycles A and B of the command) using the GMR and the local mask bits. The effective GMR is the 68-bit word specified by the identical value in both even and odd GMR pairs in each of the eight devices and selected by the GMR Index in the command's Cycle A. The 68-bit word K (presented on the DQ Bus in both Cycles A and B of the command) is also stored in both even and odd comparand register pairs in each of the eight devices and selected by the Comparand Register Index in command's Cy-

cle B. In the x68 configuration, the even comparand register can be subsequently used by the LEARN command only in the first non-full device. The word K (presented on the DQ Bus in both Cycles A and B of the command) is compared with each entry in the table starting at location "0." The first matching entry's location address, "L," is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see SRAM ADDRESSING, page 126). The global winning device will drive the bus in a specific cycle. On global miss cycles the device with LRAM = 1 and LDEV = 1 will be the default driver for such missed cycles.

The SEARCH command is a pipelined operation and executes a search at half the rate of the frequency of CLK2X for 68-bit searches in x68-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 68-bit SEARCH command cycle (two CLK2X cycles) is shown in Table 31, page 62.

For up to 31 devices in the table (TLSZ = 10), search latency from command to SRAM access cycle is 6. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in Table 32, page 62.

The 68-bit SEARCH operation is pipelined and executes as follows:

- Four cycles from the SEARCH command, each of the devices knows the outcome internal to it for that operation;
- In the fifth cycle after the SEARCH command, the devices in a block arbitrate for a winner amongst them (a "block" being defined as less than or equal to eight devices resolving the winner within them using the LHI[6:0] and LHO[1:0] signalling mechanism);
- In the sixth cycle after the SEARCH command, the blocks (of devices) resolve the winning block through the BHI[2:0] and BHO[2:0] signalling mechanism. The winning device within the winning block is the global winning device for a SEARCH operation.

Table 30. Hit/Miss Assumption

Search Number	1	2	3	4
Block 0	Miss	Miss	Miss	Miss
Block 1	Miss	Miss	Hit	Miss
Block 2	Miss	Hit	Hit	Miss
Block 3	Hit	Hit	Miss	Miss

Figure 27. Hardware Diagram for a Table with 31 Devices

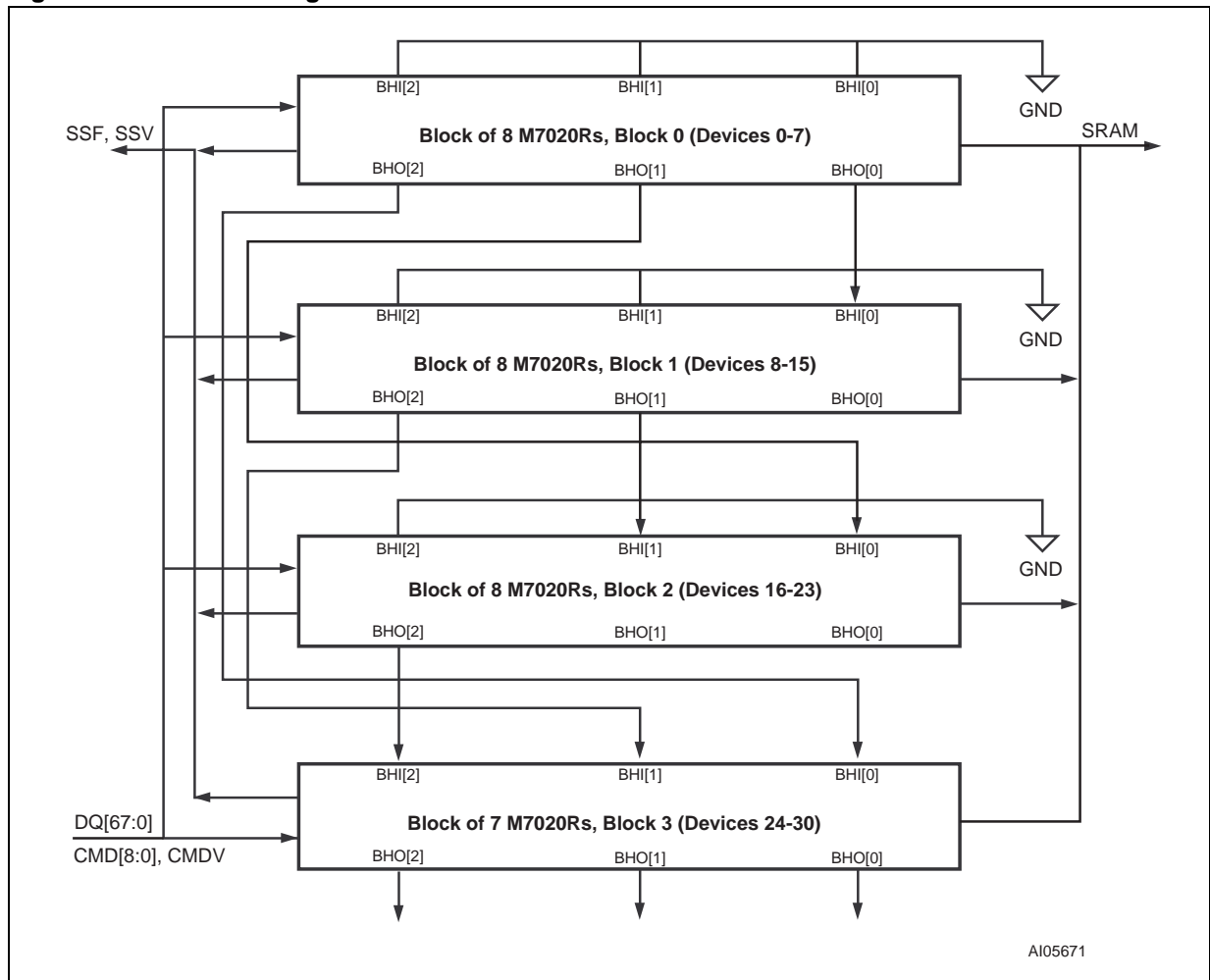


Figure 28. Hardware Diagram for a Block of Up To Eight Devices

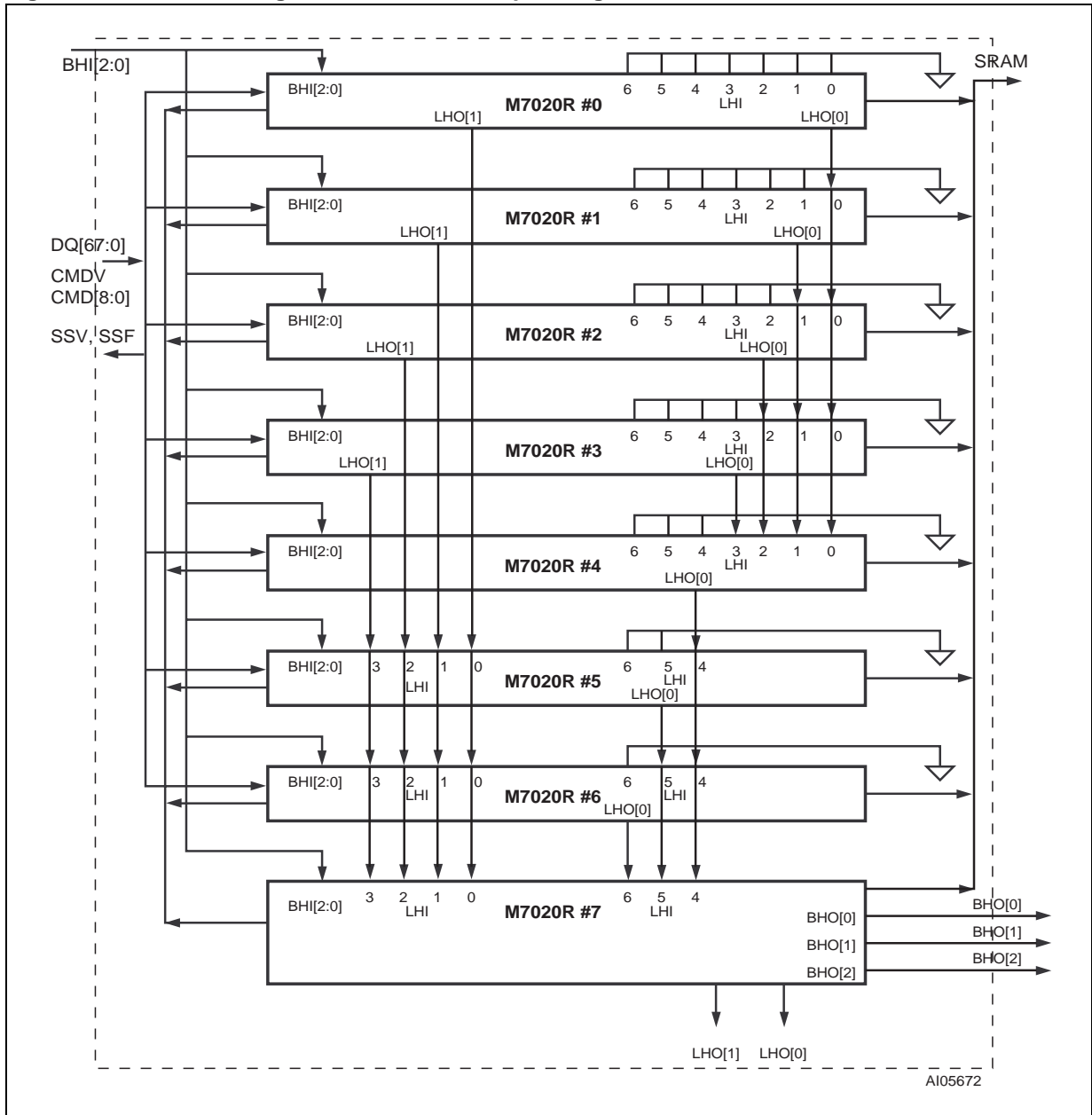
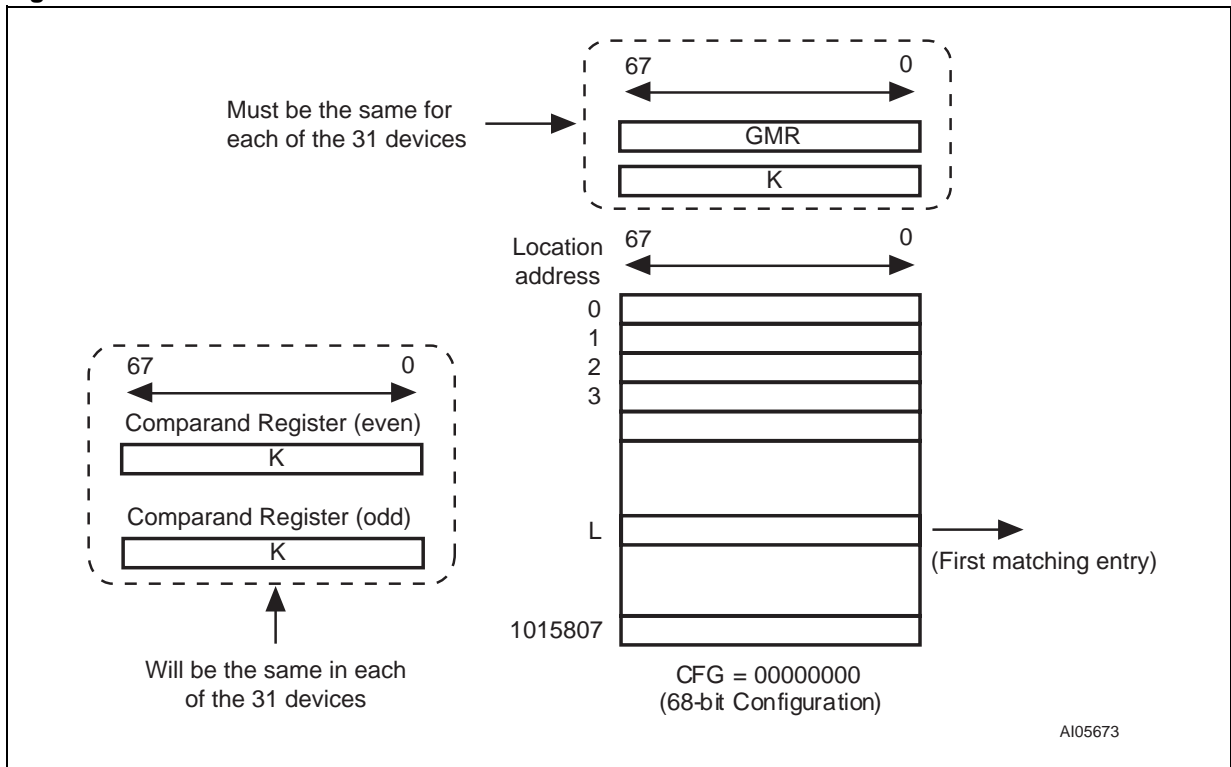


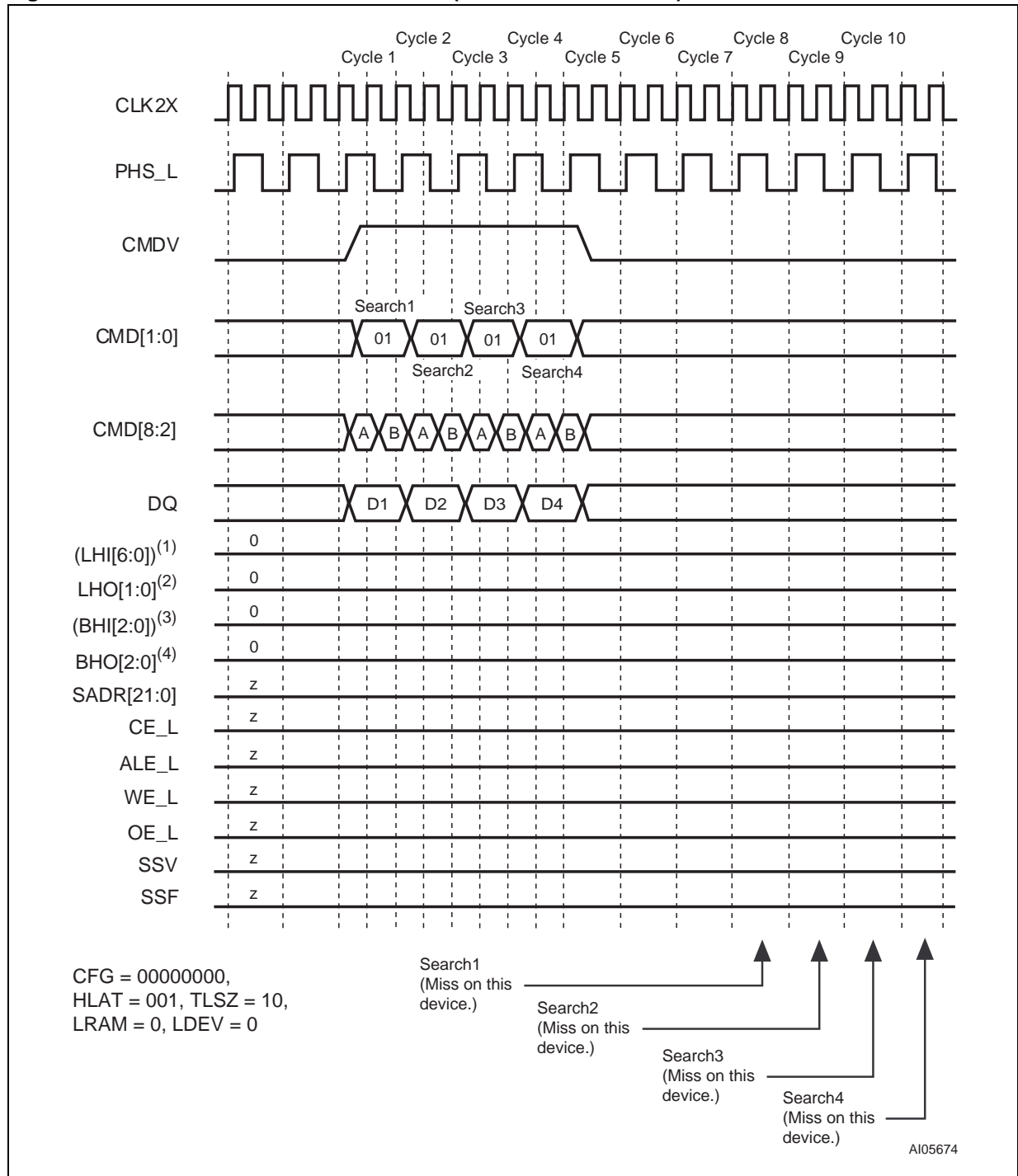
Figure 29. x68 Table with 31 Devices



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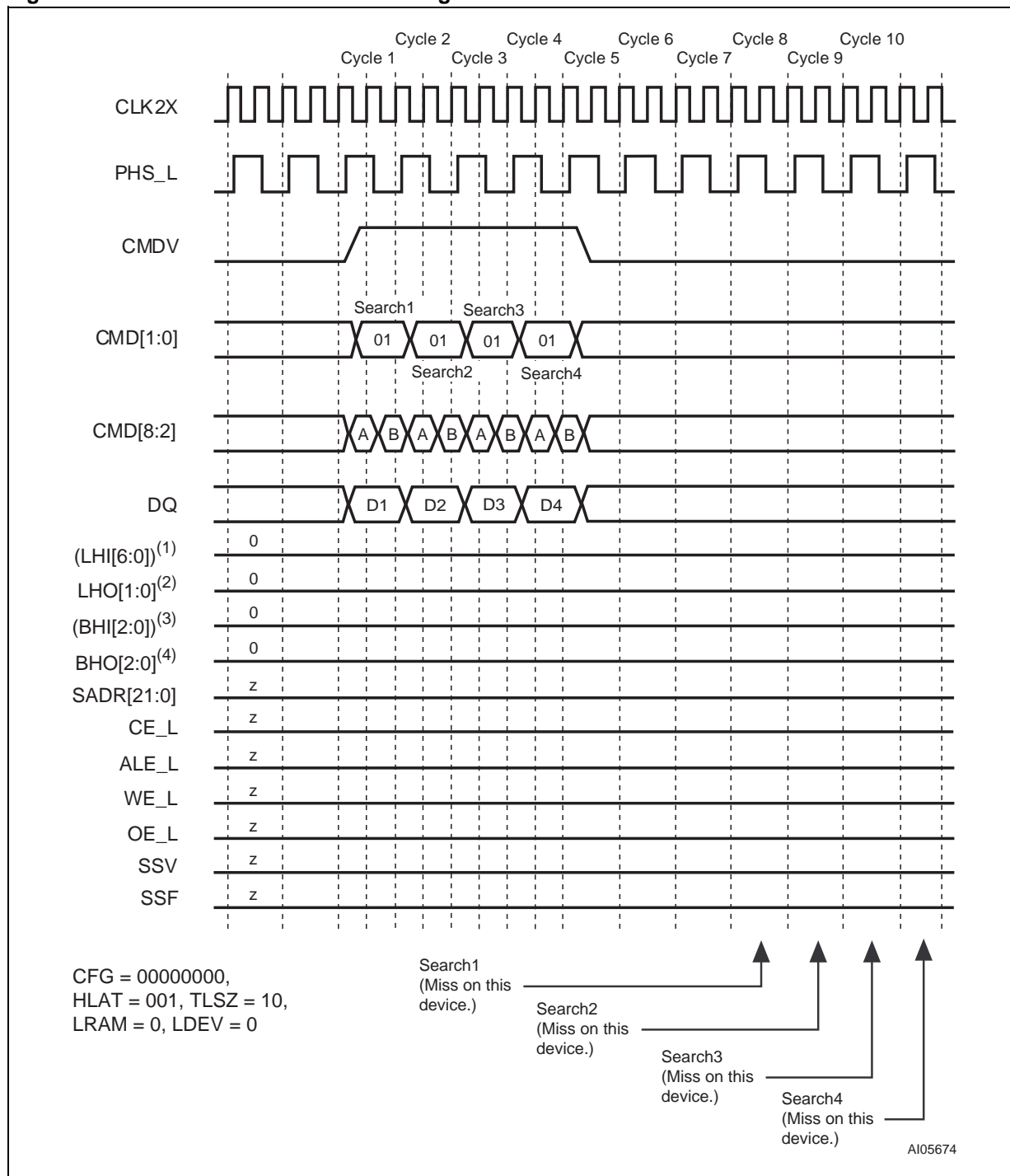
Timing Diagrams for x68 Using Up To 31 M7020R Devices

Figure 30. Each Device in Block Number 0 (Miss on Each Device)



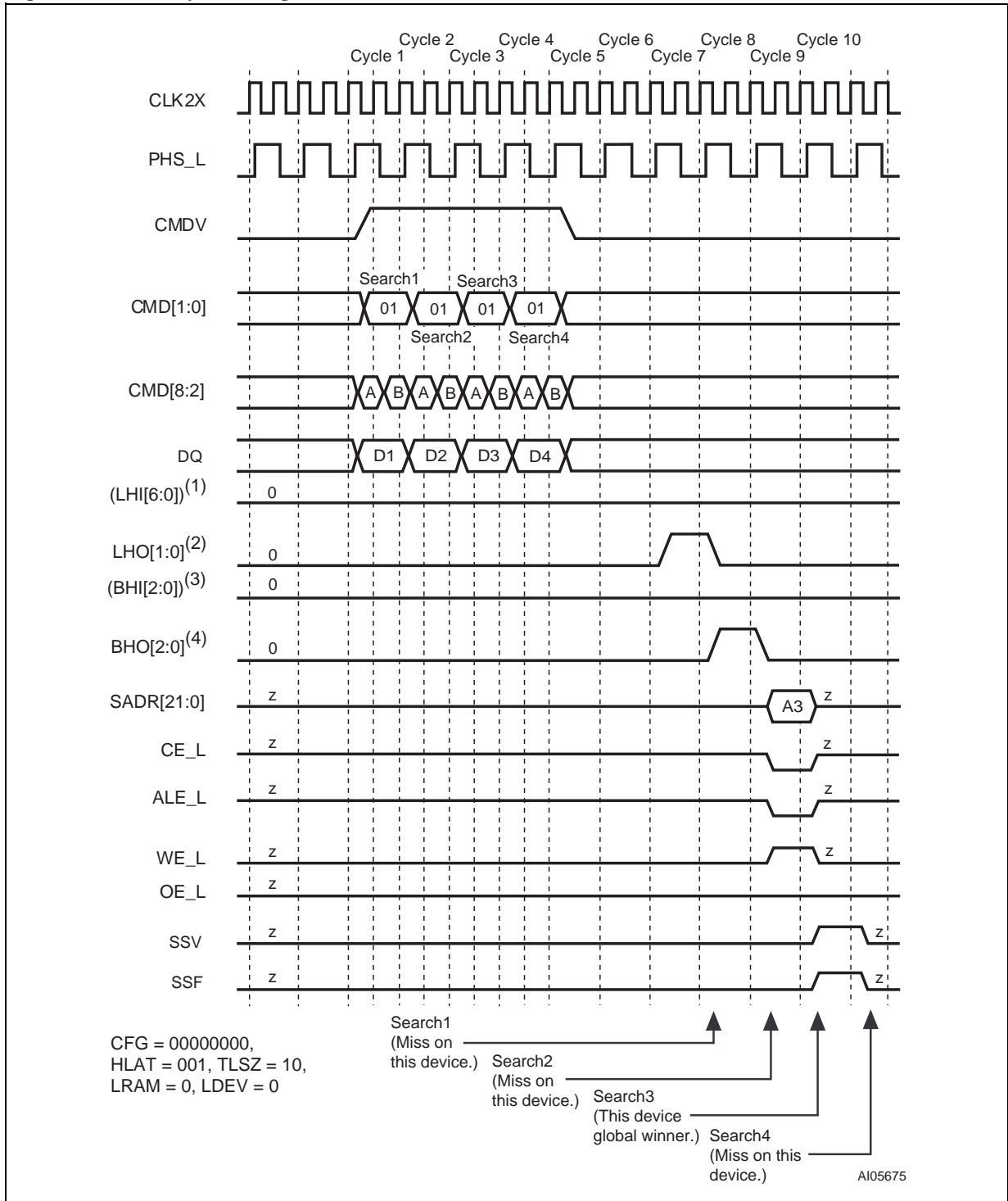
- Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 31. Each Device Above the Winning Device in Block Number 1



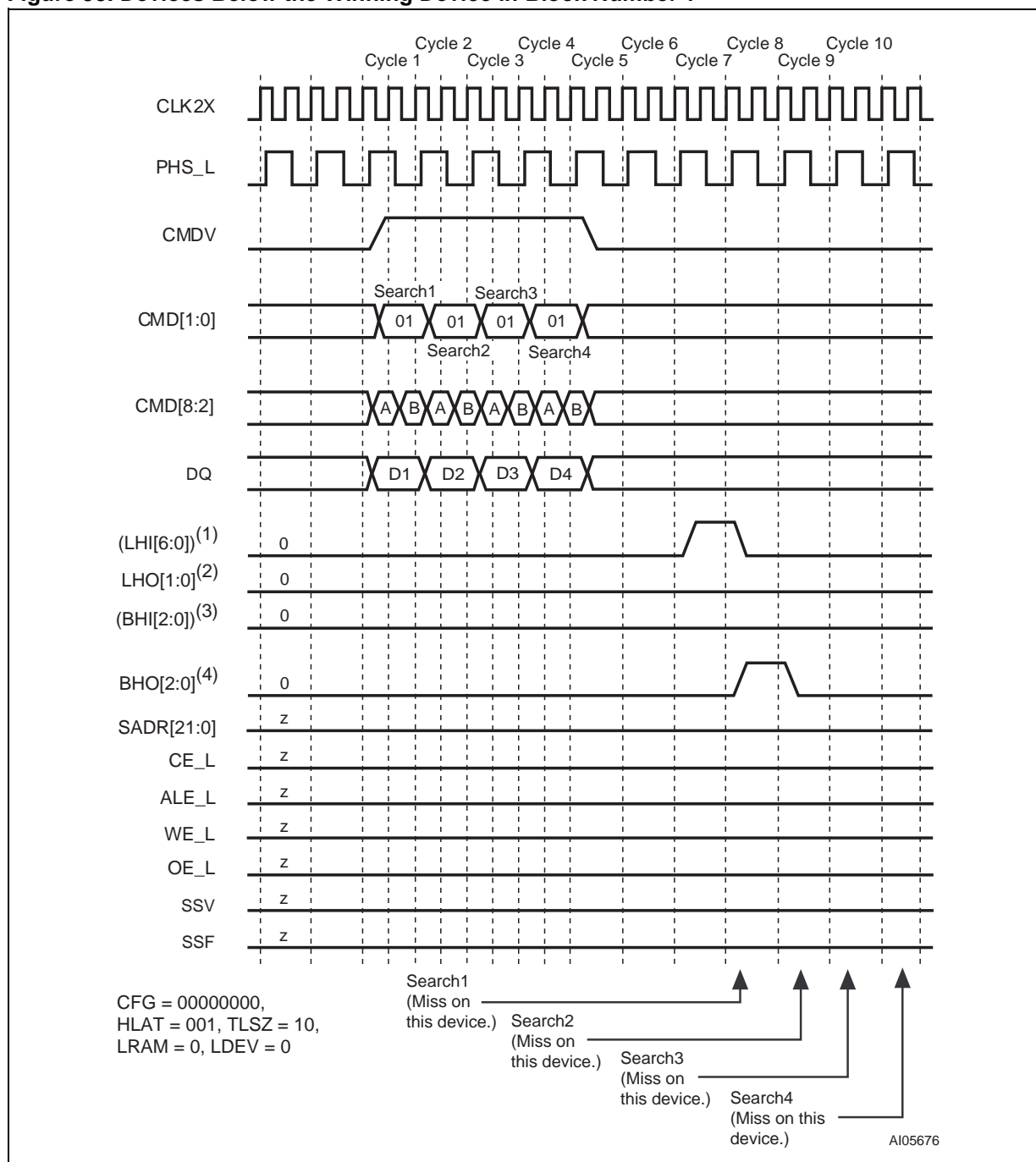
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 32. Globally Winning Device in Block Number 1



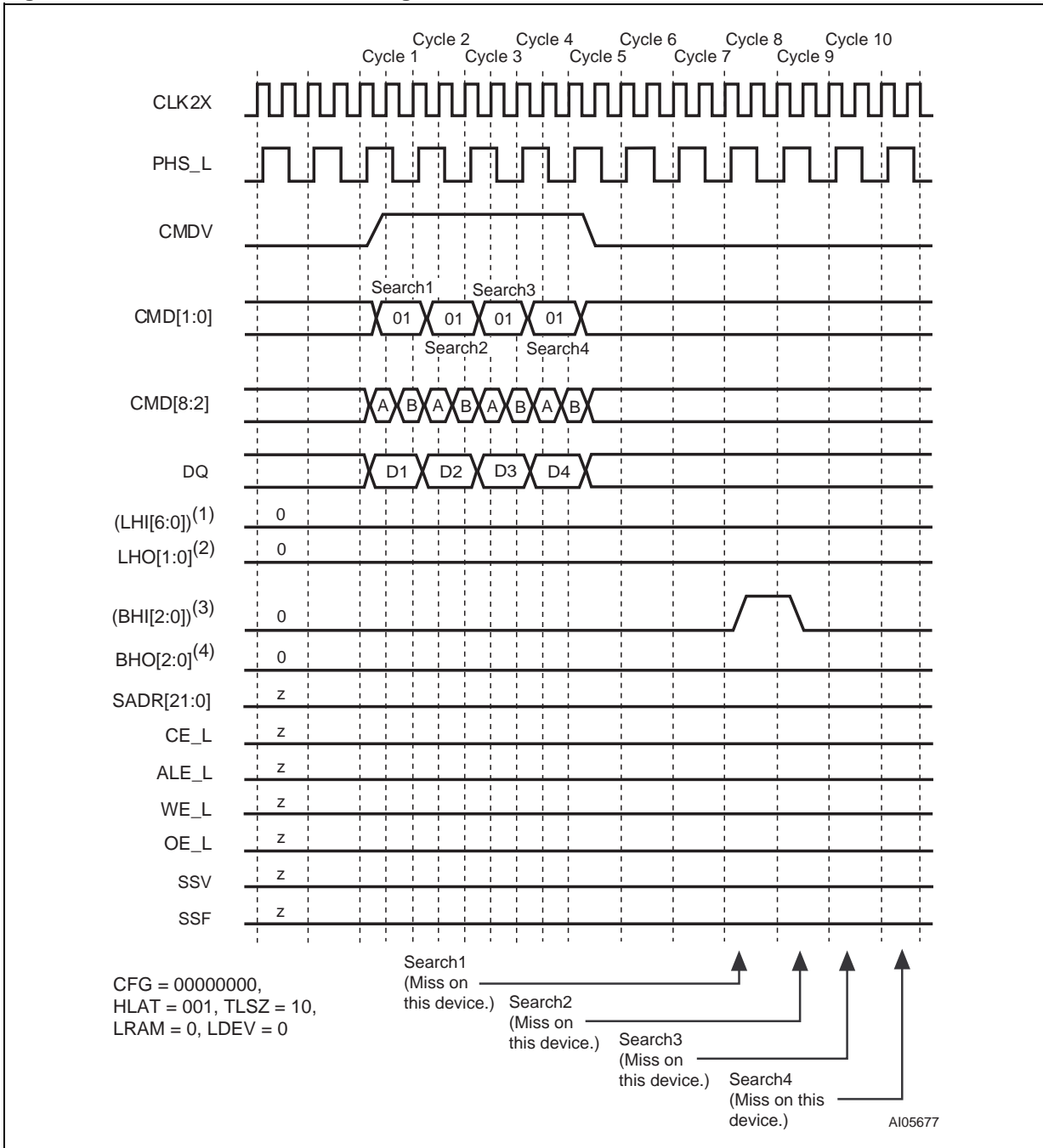
- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 33. Devices Below the Winning Device in Block Number 1



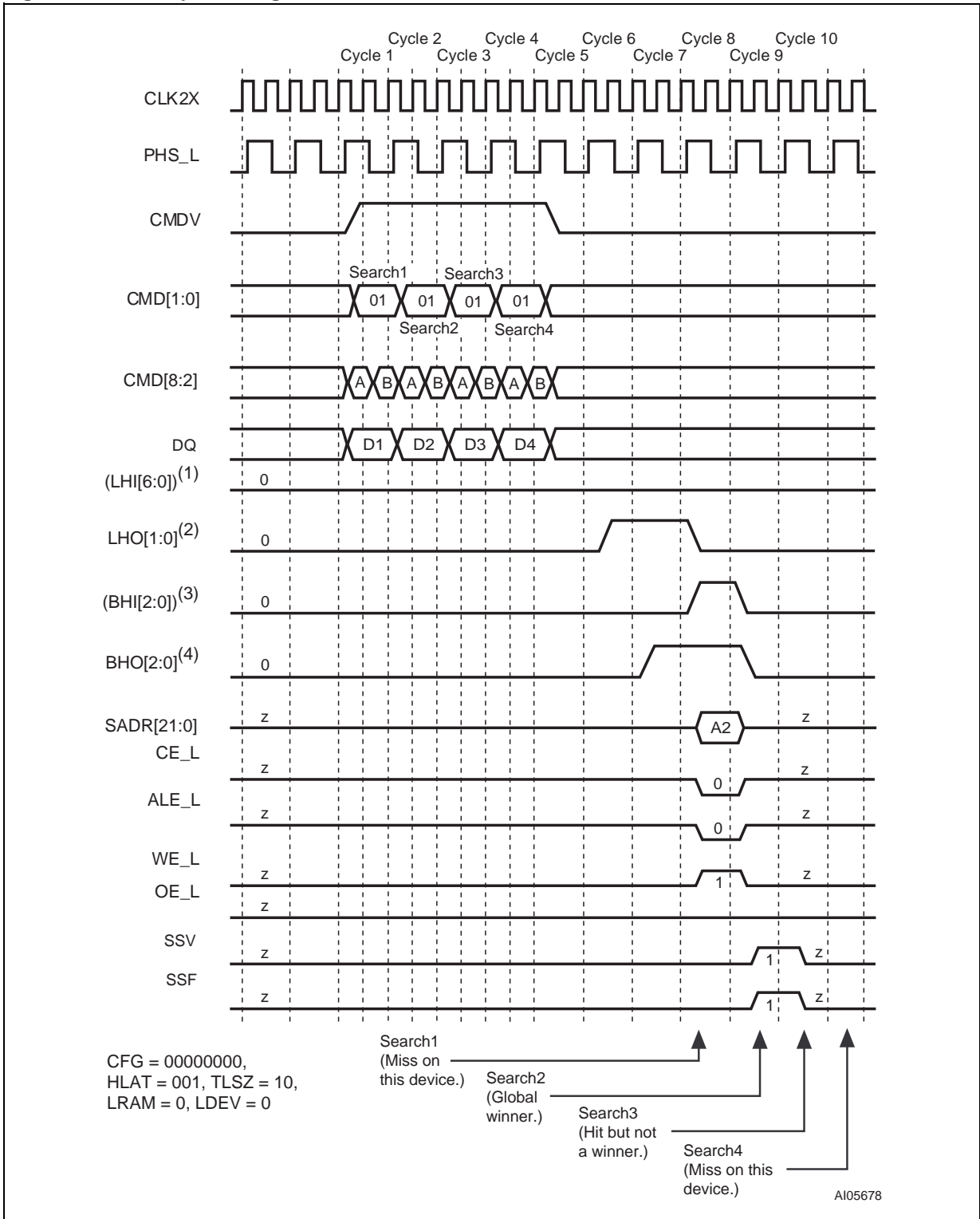
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 34. Devices Above the Winning Device in Block Number 2



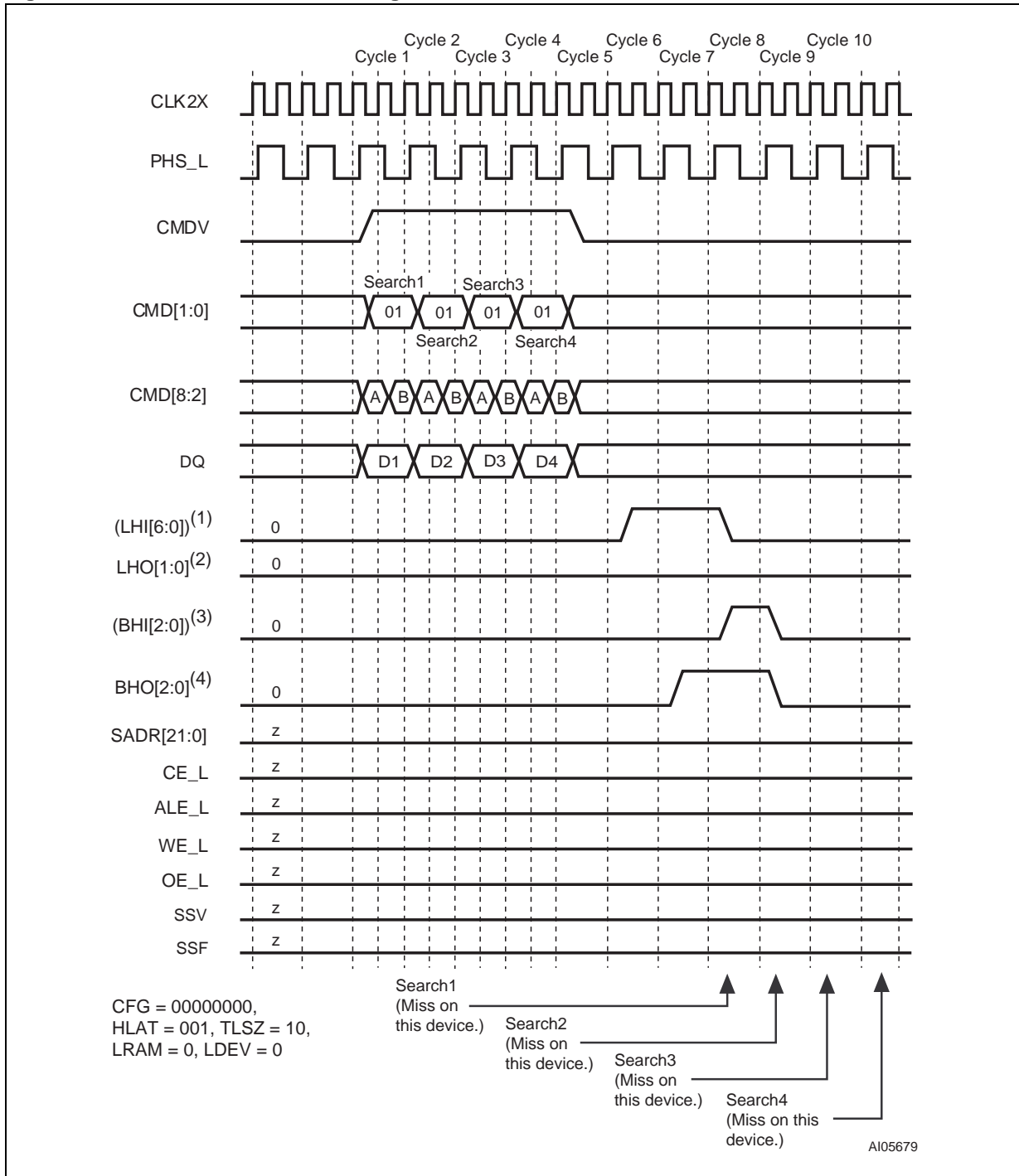
- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 35. Globally Winning Device in Block Number 2



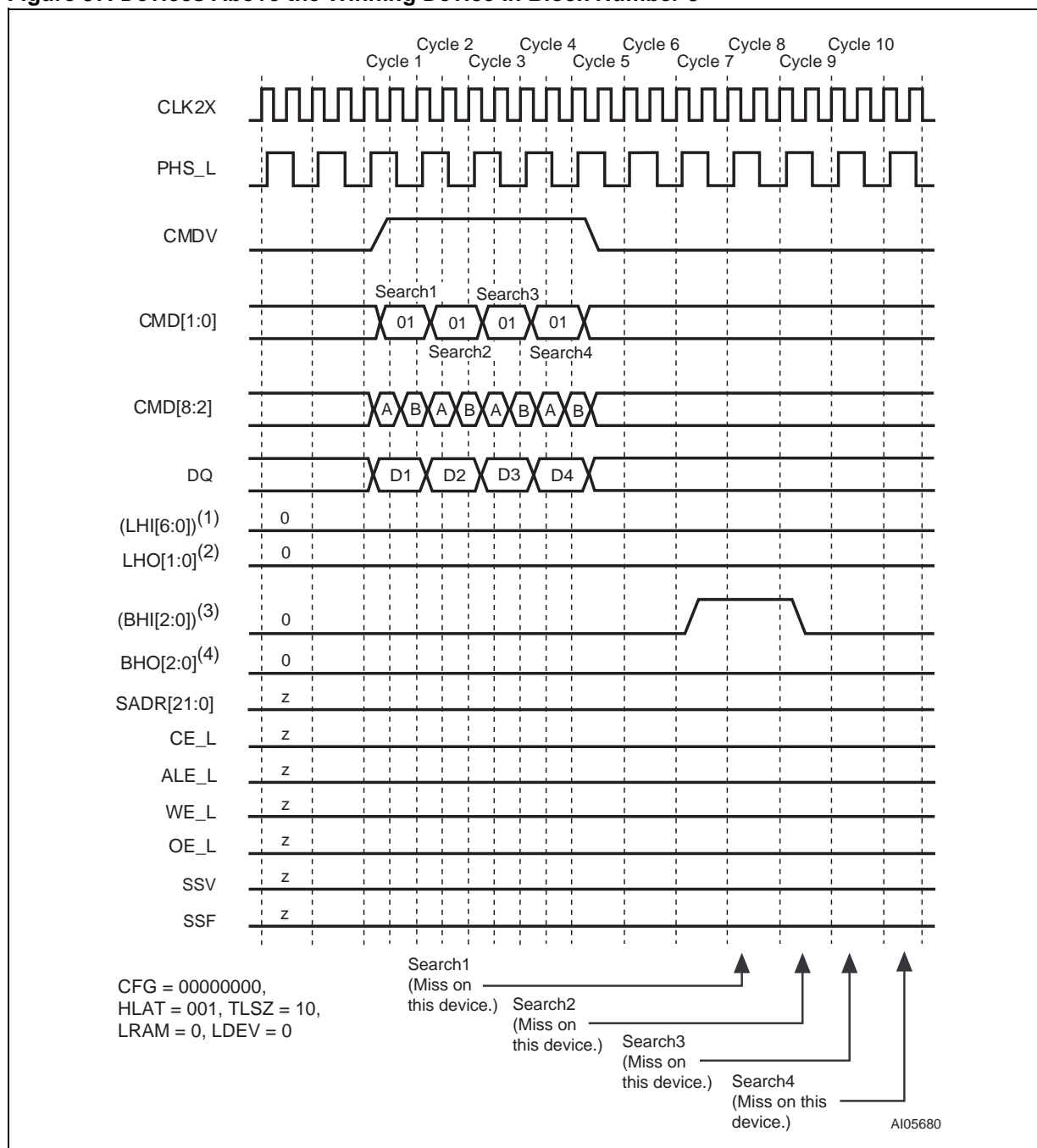
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 36. Devices Below the Winning Device in Block Number 2



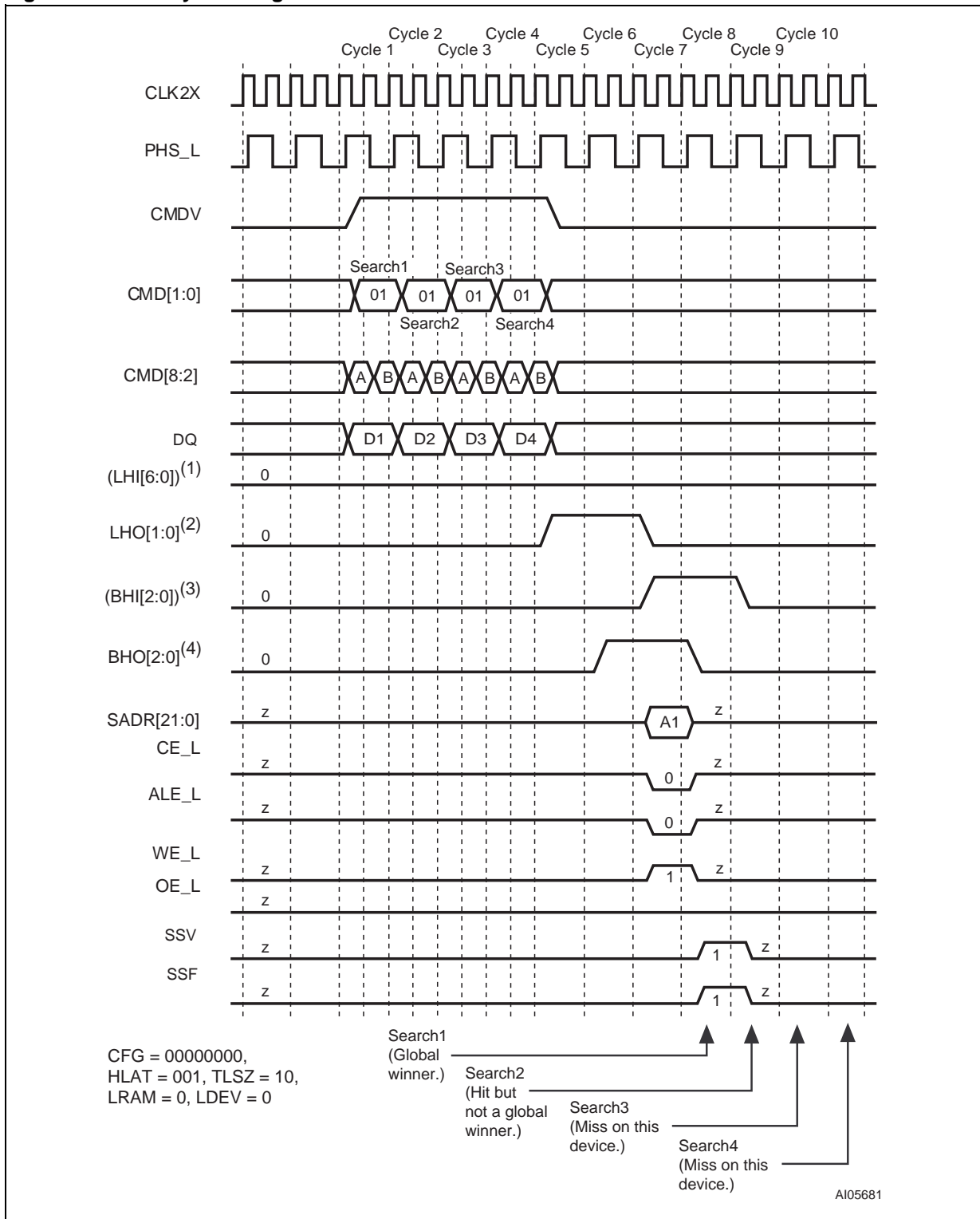
- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 37. Devices Above the Winning Device in Block Number 3



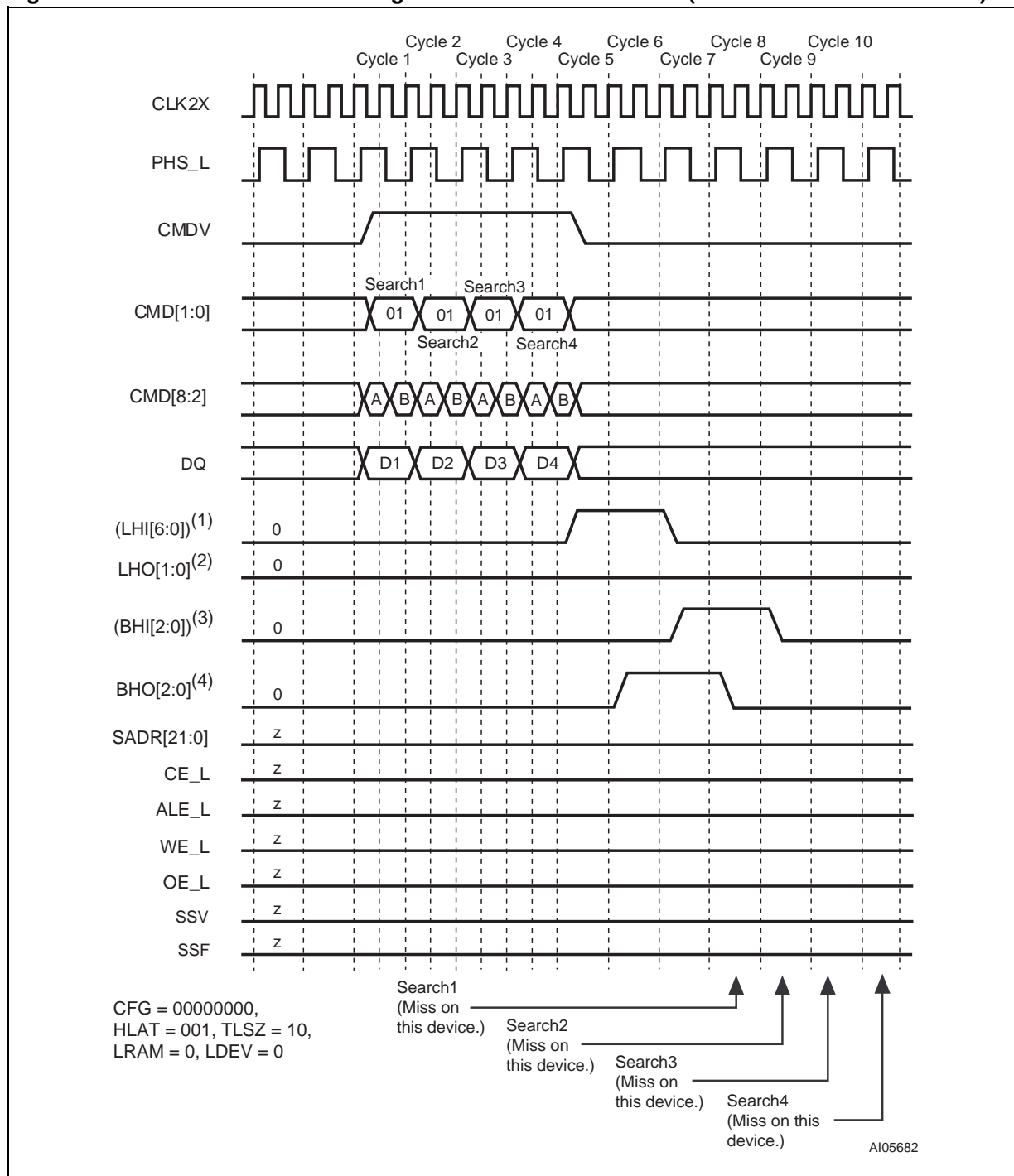
- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 38. Globally Winning Device in Block Number 3



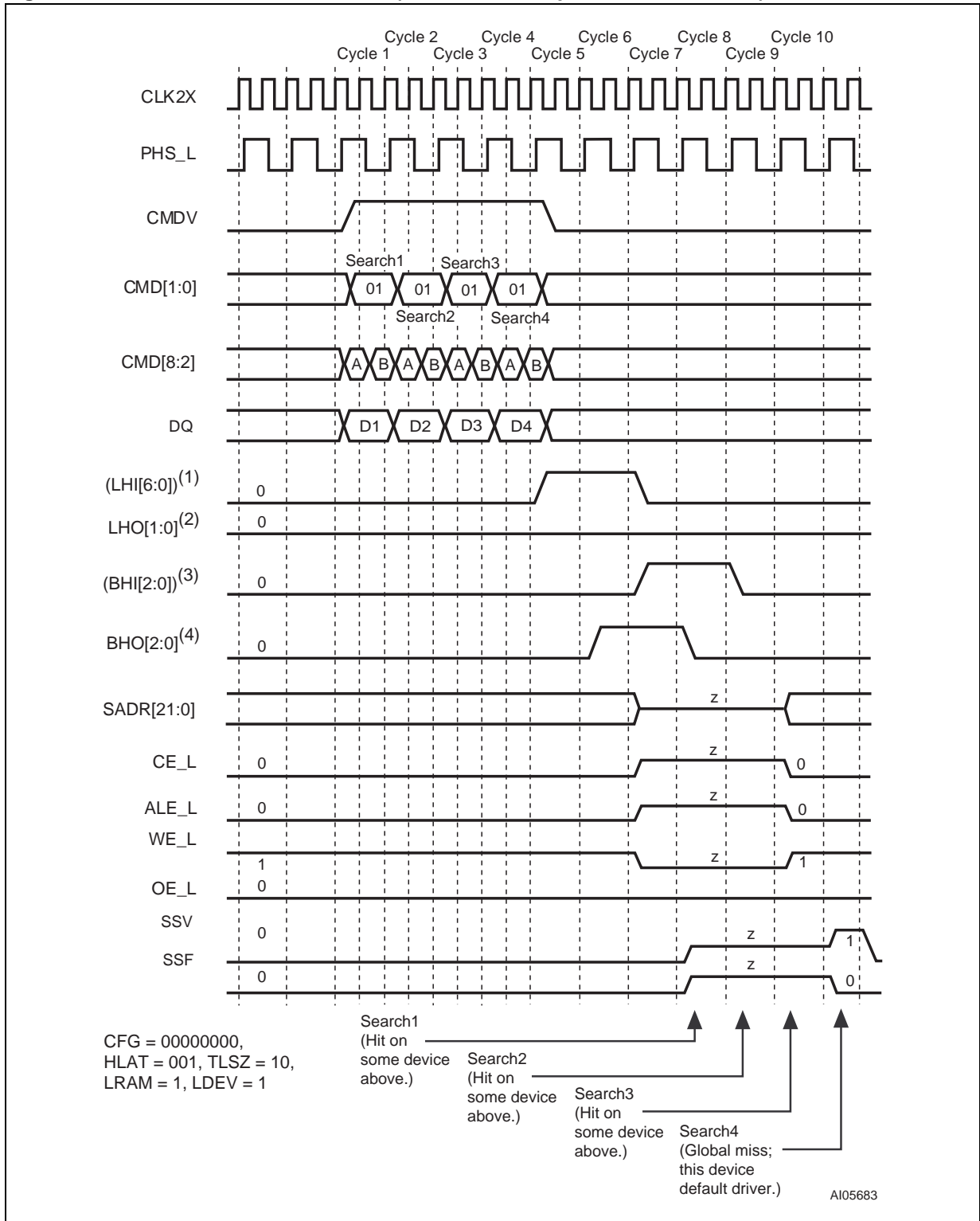
- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 39. Devices Below the Winning Device in Block Number 3 (not Device 30 - Last Device)



- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 40. Device 6 in Block Number 3 (Device 30 in Depth-Cascaded Table)



- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Table 31. Latency of SEARCH from Instruction to SRAM Access Cycle, 68-bit, Up to 31 Devices

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	32K x 68-bit	4
2–8 (TLSZ = 01)	256K x 68-bit	5
9–31 (TLSZ = 10)	992K x 68-bit	6

Table 32. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

136-bit Configuration with Single Device

The hardware diagram for this search subsystem is shown in Figure 41.

Figure 42, page 64 shows the timing diagram for a SEARCH command in the 136-bit-configured table (CFG = 01010101) consisting of a single device for one set of parameters. This illustration assumes that the host ASIC has programmed TLSZ to '00,' HLAT to '001,' LRAM to '1,' and LDEV to '1.'

The following is the operation sequence for a single 136-bit SEARCH command (refer to COMMAND CODES AND PARAMETERS, page 29).

- **Cycle A:** The host ASIC drives the CMDV high and applies SEARCH command code ('10') to CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair for use in this SEARCH operation. CMD[8:7] signals must be driven with the same bits that will be driven on SADR[21:20] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data ([135:68]) to be compared against all even loca-

tions. The CMD[2] signal must be driven to logic '0.'

- **Cycle B:** The host ASIC continues to drive the CMDV high and applies the command code of SEARCH command ('10') on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ Bus during Cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and Hit Flag (see SEARCH-Successful Registers (SSR[0:7]), page 23). The DQ[67:0] is driven with 68-bit data ([67:0]), compared to all odd locations.

Note: For 136-bit searches, the host ASIC must supply two distinct 68-bit data words on DQ[67:0] during Cycles A and B. The even-numbered GMR of the pair specified by the GMR Index is used for masking the word in Cycle A. The odd-numbered GMR of the pair specified by the GMR Index is used for masking the word in Cycle B.

The logical 136-bit search operation is shown in Figure 43, page 65. The entire table of 136-bit entries is compared to a 136-bit word K (presented on the DQ Bus in Cycles A and B of the command) using the GMR and the local mask bits. The GMR is the 136-bit word specified by the even and odd global mask pair selected by the GMR Index in the command's Cycle A. The 136-bit word K (presented on the DQ Bus in Cycles A and B of the command) is also stored in both even and odd comparand register pairs selected by the Comparand Register Index in the command's Cycle B. The two comparand registers can subsequently be used by the LEARN command with the even comparand register stored in an even location, and the odd comparand register stored in an adjacent odd location. The word K (presented on the DQ Bus in Cycles A and B of the command) is compared with each entry in the table starting at

location "0." The first matching entry's location address, "L," is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see SRAM ADDRESSING, page 126).

Note: The matching address is always going to an even address for a 136-bit SEARCH.

The SEARCH command is a pipelined operation that executes searches at half the rate of the frequency of CLK2X for 136-bit searches in x136-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 136-bit SEARCH command cycle (two CLK2X cycles) is shown in Table 33, page 65.

For a single device in the table with TLSZ = 00, the latency of the SEARCH from command to SRAM access cycle is 4. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in Table 34, page 65.

Figure 41. Hardware Diagram for a Table with 1 Device

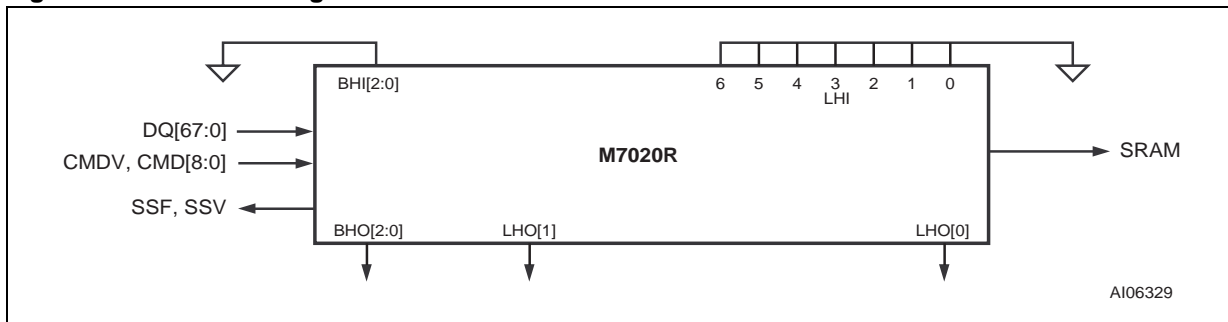


Figure 42. Timing Diagram for a 136-bit SEARCH for One Device

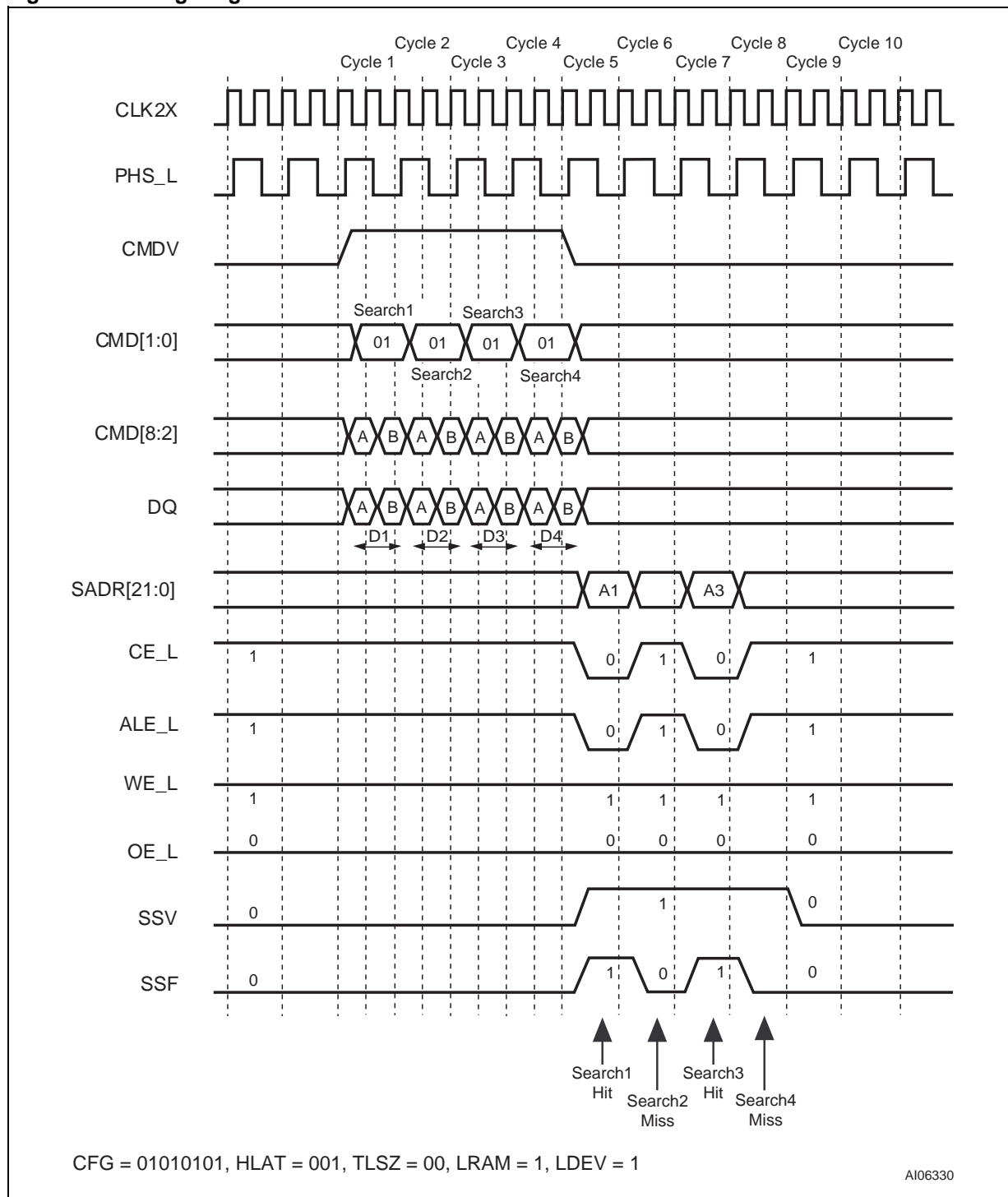


Figure 43. x136 Table with One Device

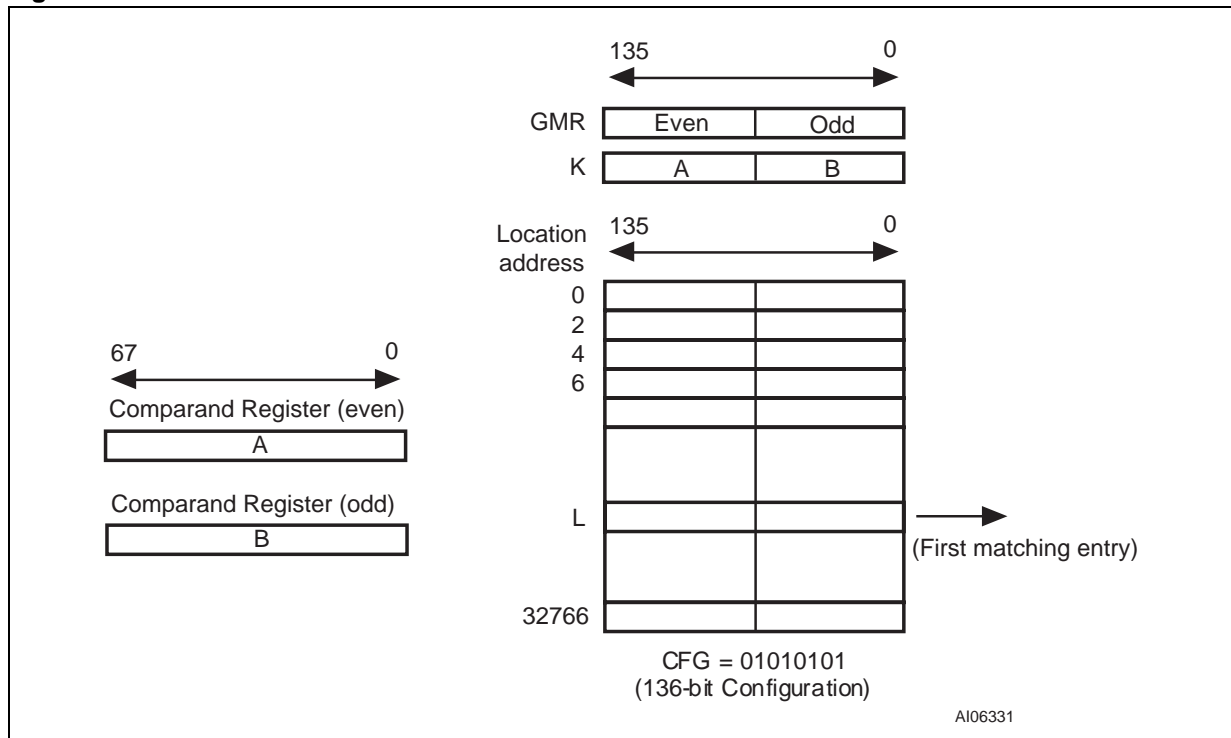


Table 33. Latency of SEARCH from Instruction to SRAM Access Cycle, 136-bit, 1 Device

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	16K x 136-bit	4
2–8 (TLSZ = 01)	128K x 136-bit	5
9–31 (TLSZ = 10)	496K x 136-bit	6

Table 34. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

136-bit Search on Tables Configured as x136 Using Up to Eight M7020R Devices

The hardware diagram of the search subsystem of eight devices is shown in Figure 44, page 67. The following are parameters programmed into the eight devices:

- First seven devices (devices 0–6):
CFG = 01010101, TLSZ = 01, HLAT = 010,
LRAM = 0, and LDEV = 0.
- Eighth device (device 7):
CFG = 01010101, TLSZ = 01, HLAT = 010,
LRAM = 1, and LDEV = 1.

Note: All eight devices must be programmed with the same value of TLSZ and HLAT. Only the last device in the table must be programmed with LRAM = 1 and LDEV = 1 (Device 7 in this case). All other upstream devices must be programmed with LRAM = 0 and LDEV = 0 (Devices 0 through 6 in this case).

Figure 46, page 69 shows the timing diagram for a SEARCH command in the 136-bit-configured table of eight devices for Device 0. Figure 47, page 70 shows the timing diagram for a SEARCH command in the 136-bit-configured table consisting of eight devices for Device 1. Figure 48, page 71 shows the timing diagram for a SEARCH command in the 136-bit configured table consisting of eight devices for Device 7 (the last device in this specific table). For these timing diagrams, four 136-bit searches are performed sequentially, and the following HIT/MISS assumptions were made (see Table 35)

The following is the sequence of operation for a single 136-bit SEARCH command (see COMMAND CODES AND PARAMETERS, page 29).

- **Cycle A:** The host ASIC drives CMDV high and applies SEARCH command code ('10') on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair for use in this SEARCH operation. CMD[8:7] signals must be driven with the same bits that will be driven by this device on SADR[21:20] if it has a hit. DQ[67:0] must be driven with the 68-bit data ([135:68]) in order to be compared against all even locations. The CMD[2] signal must be driven to a logic '0.'
- **Cycle B:** The host ASIC continues to drive CMDV high and to apply the command code for SEARCH command ('10') on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ Bus during Cycles A

and B. CMD[8:6] signals must be driven with the SSR Index that will be used for storing the address of the matching entry and the Hit Flag (see SEARCH-Successful Registers (SSR[0:7]), page 23). The DQ[67:0] is driven with 68-bit data ([67:0]) compared against all odd locations.

The logical 136-bit search operation is shown in Figure 45, page 68. The entire table (eight devices of 136-bit entries) is compared to a 136-bit word K (presented on the DQ Bus in Cycles A and B of the command) using the GMR and local mask bits. The GMR is the 136-bit word specified by the even and odd global mask pair selected by the GMR Index in the command's Cycle A.

The 136-bit word K (presented on the DQ Bus in Cycles A and B of the command) is also stored in the even and odd comparand registers specified by the Comparand Register Index in the command's Cycle B. In x136 configurations, the even and odd comparand registers can subsequently be used by the LEARN command in only one of the devices (the first non-full device). The word K (presented on the DQ Bus in Cycles A and B of the command) is compared to each entry in the table starting at location "0." The first matching entry's location, "L," is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see SRAM ADDRESSING, page 126). The global winning device will drive the bus in a specific cycle. On global miss cycles the device with LRAM = 1 (the default driving device for the SRAM Bus) and LDEV = 1 (the default driving device for SSF and SSV signals) will be the default driver for such missed cycles.

Note: During 136-bit searches of 136-bit-configured tables, the search hit will always be at an even address.

The SEARCH command is a pipelined operation and executes a search at half the rate of the frequency of CLK2X for 136-bit searches in x136-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 136-bit SEARCH command cycle (two CLK2X cycles) is shown in Table 36, page 72.

For one to eight devices in the table and TLSZ = 01, the latency of a SEARCH from command to SRAM access cycle is 5. In addition, SSV and SSF shift further to the right for different values of HLAT as specified in Table 37, page 72.

Table 35. Hit/Miss Assumption

Search Number	1	2	3	4
Device 0	Hit	Miss	Hit	Miss
Device 1	Miss	Hit	Hit	Miss
Device 2-6	Miss	Miss	Miss	Miss
Device 7	Miss	Miss	Hit	Hit

Figure 44. Hardware Diagram for a Table with Eight Devices

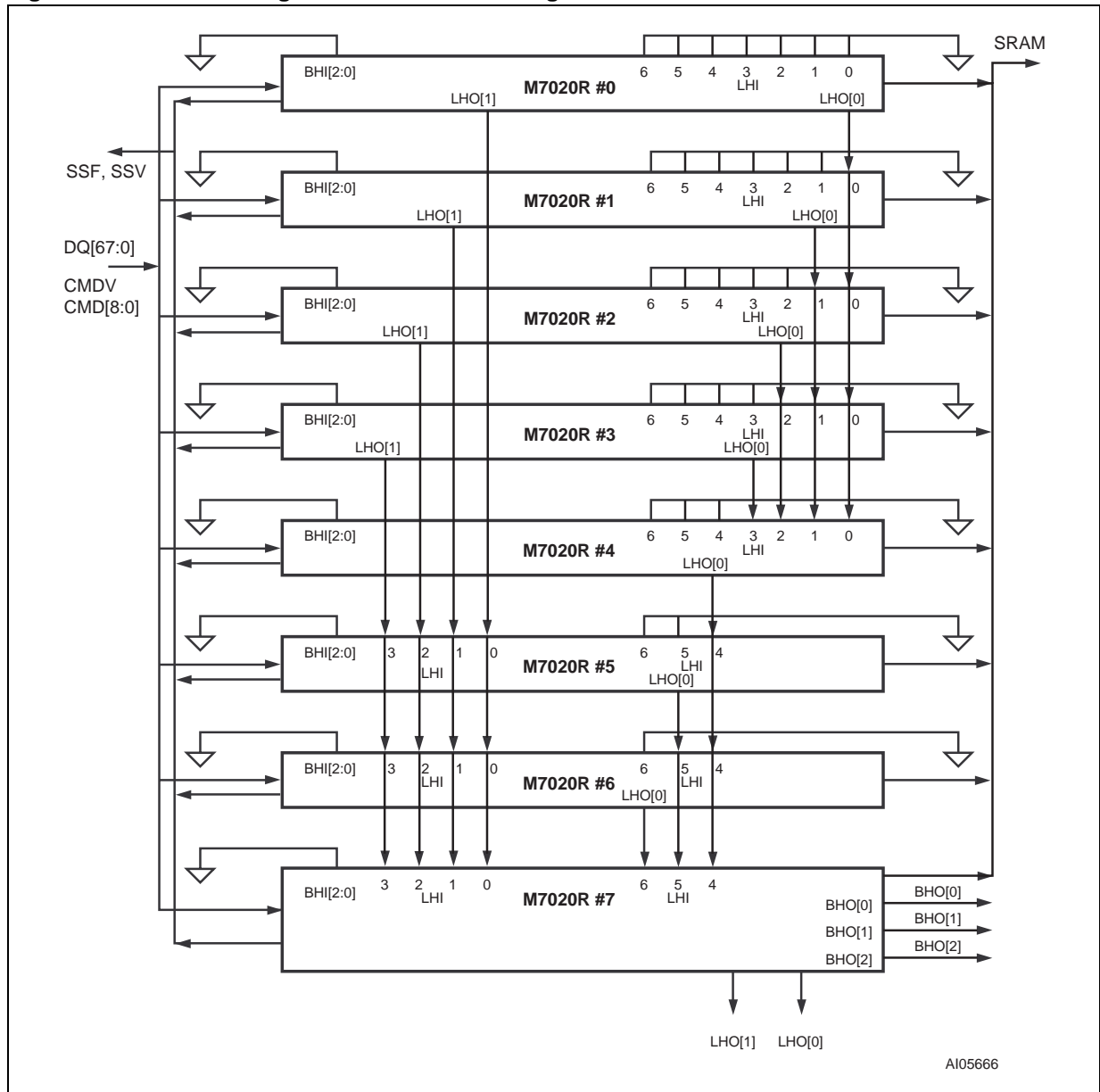
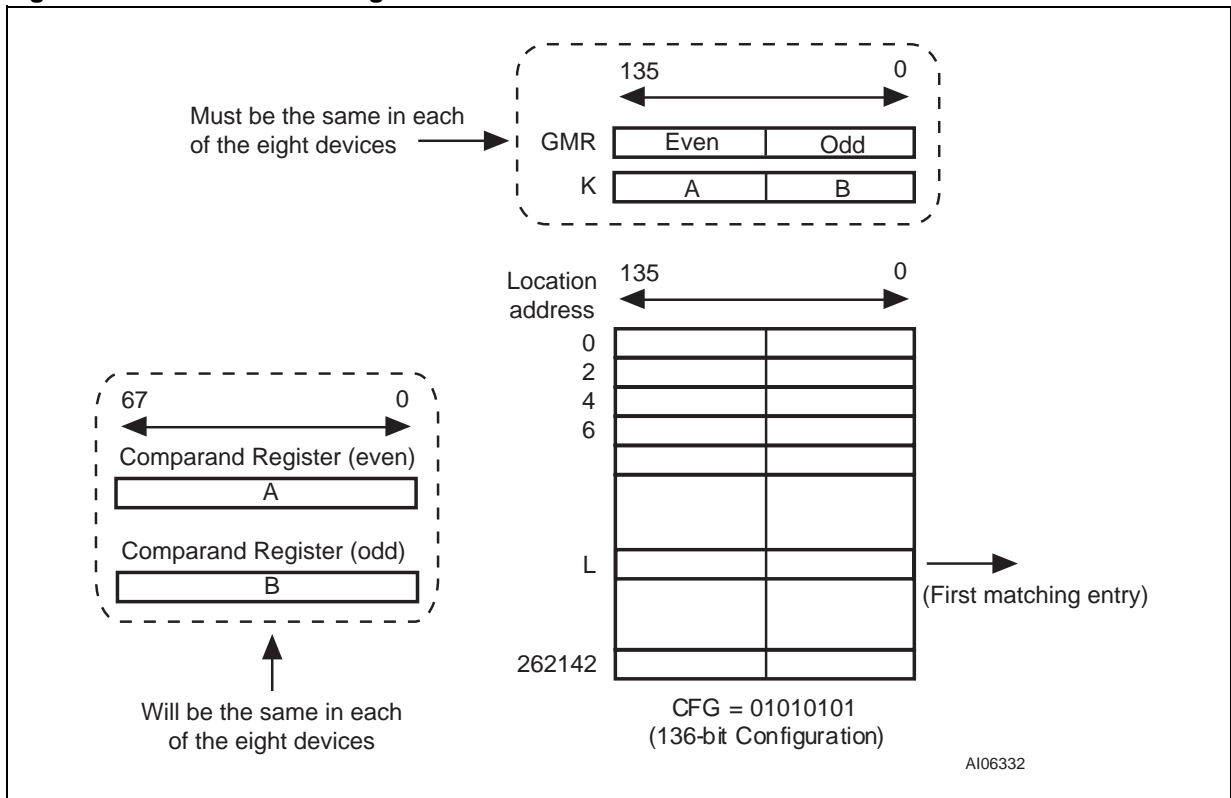
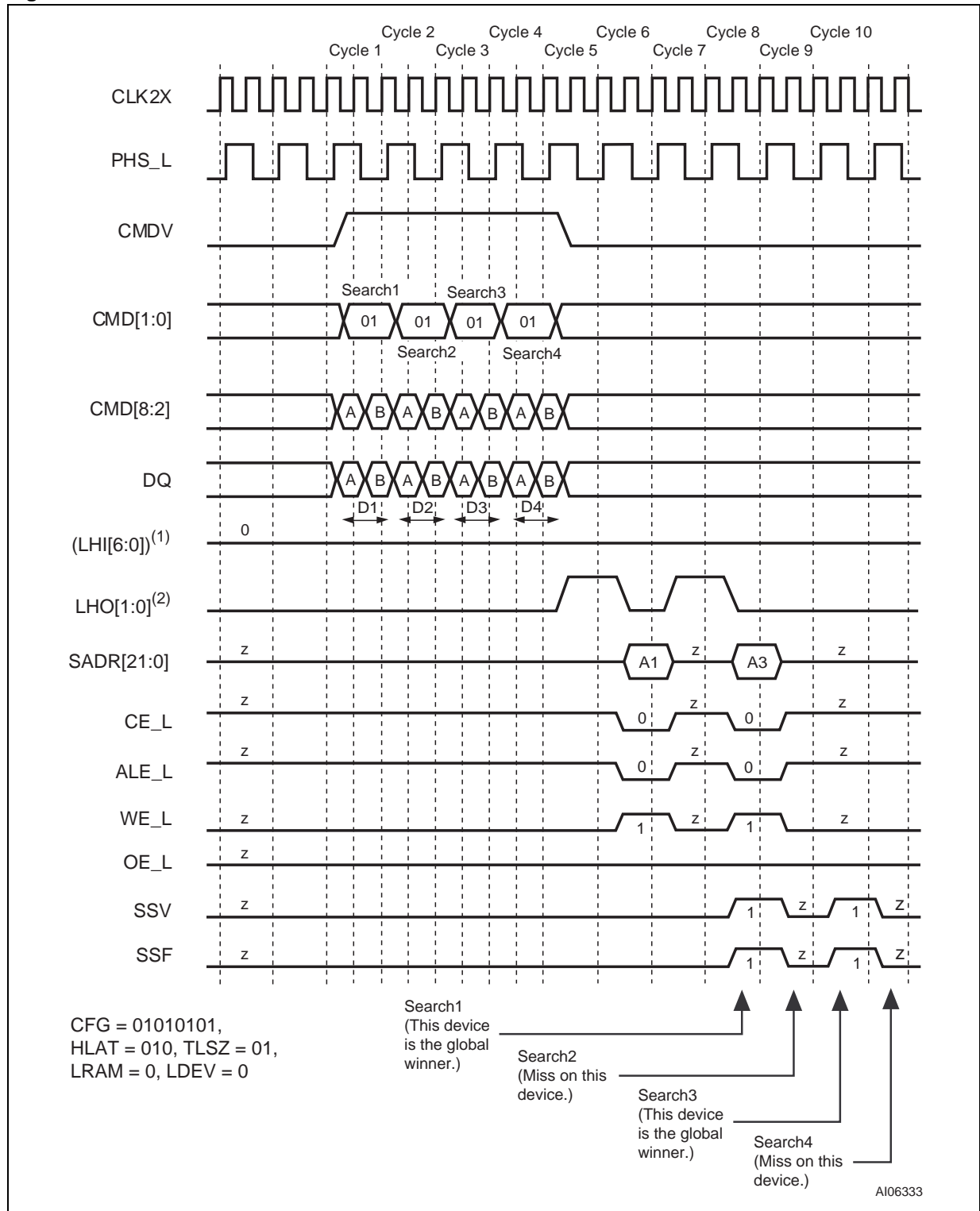


Figure 45. x136 Table with Eight Devices



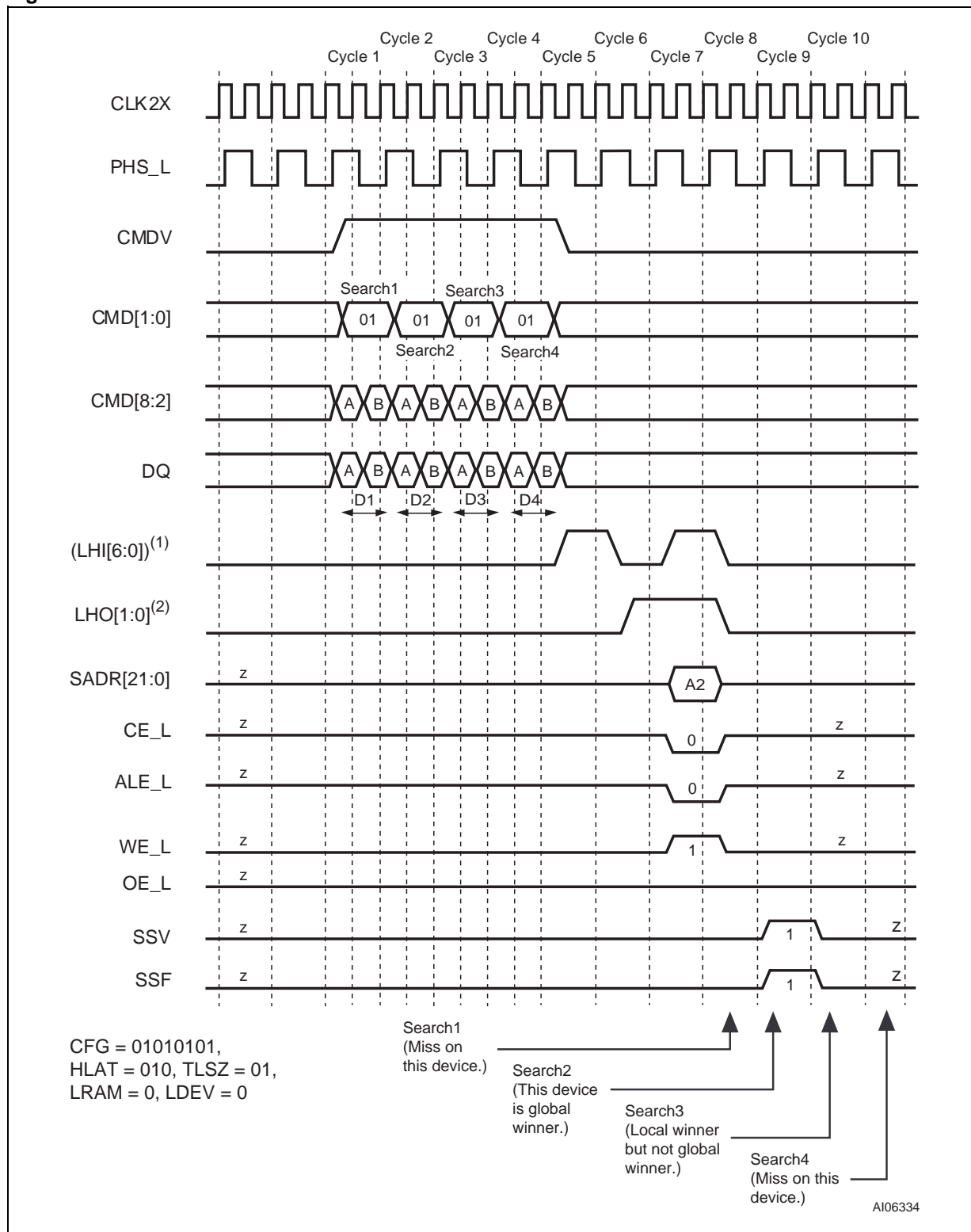
Timing Diagrams for x136 Using Up to Eight M7020R Devices

Figure 46. 136-bit SEARCH for Device Number 0



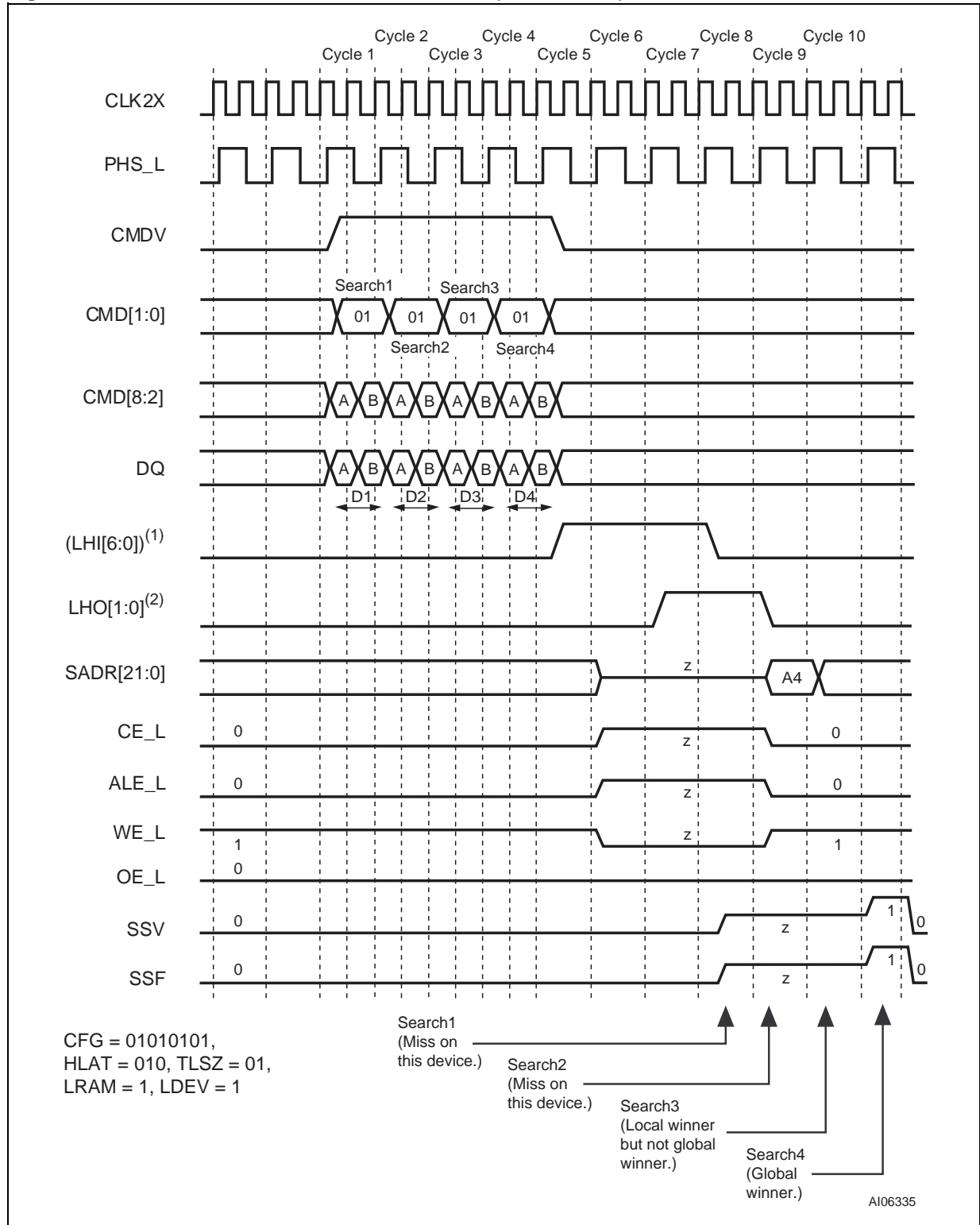
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.

Figure 47. 136-bit SEARCH for Device Number 1



Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.

Figure 48. 136-bit SEARCH for Device Number 7 (Last Device)



Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.

Table 36. Latency of SEARCH from Instruction to SRAM Access Cycle, 136-bit, Up to 8 Devices

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	16K x 136-bit	4
2–8 (TLSZ = 01)	128K x 136-bit	5
9–31 (TLSZ = 10)	496K x 136-bit	6

Table 37. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

136-bit Search on Tables Configured as x136 Using Up to 31 M7020R Devices

The hardware diagram of the search subsystem of 31 devices is shown in Figure 49, page 74. Each of the four blocks in the diagram represents a block of eight M7020R devices (except the last, which has seven devices). The diagram for a block of eight devices is shown in Figure 50, page 75. Following are the parameters programmed into the 31 devices.

First thirty devices (devices 0–29):
CFG = 01010101, TLSZ = 10, HLAT = 001,
LRAM = 0, and LDEV = 0.

Thirty-first device (device 30):
CFG = 01010101, TLSZ = 10, HLAT = 001,
LRAM = 1, and LDEV = 1.

Note: All 31 devices must be programmed with the same value of TLSZ and HLAT. Only the last device in the table must be programmed with LRAM = 1 and LDEV = 1 (Device 30 in this case). All other upstream devices must be programmed with LRAM = 0 and LDEV = 0 (Devices 0 through 29 in this case).

The timing diagrams referred to in this paragraph reference the HIT/MISS assumptions defined in Table 38, page 73. For the purpose of illustrating timings, it is further assumed that there is only

one device with a matching entry in each of the blocks. Figure 52, page 77 shows the timing diagram for a SEARCH command in the 136-bit-configured table (31 devices) for each of the eight devices in Block 0. Figure 53, page 78 shows the timing diagram for SEARCH command in the 68-bit-configured table (31 devices) for all the devices in Block 1 above the winning device in that block. Figure 54, page 79 shows the timing diagram for the globally winning device (the final winner within its own block and all blocks) in Block 1. Figure 55, page 80 shows the timing diagram for all the devices below the globally winning device in Block 1. Figure 56, page 81, Figure 57, page 82, and Figure 58, page 83 respectively show the timing diagrams of the devices above globally winning device, the globally winning device and devices below the globally winning device for Block 2. Figure 59, page 84, Figure 60, page 85, Figure 61, page 86, and Figure 62, page 87 respectively show the timing diagrams of the devices above the globally winning device, the globally winning device, and devices below the globally winning device except the last device (Device 30), and the last device (Device 30) for Block 3.

The following is the sequence of operation for a single 136-bit SEARCH command (see COMMAND CODES AND PARAMETERS, page 29).

- **Cycle A:** The host ASIC drives the CMDV high and applies SEARCH command code ('10') on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair for use in this SEARCH operation. CMD[8:7] signals must be driven with the bits that will be driven on SADR[21:20] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data ([135:68]) in order to be compared against all even locations. The CMD[2] signal must be driven to logic '0.'
- **Cycle B:** The host ASIC continues to drive the CMDV high and to apply SEARCH command code ('10') on CMD[1:0]. CMD[5:2] must be driven by the index of the comparand register pair for storing the 136-bit word presented on the DQ Bus during Cycles A and B. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the Hit Flag (see SEARCH-Successful Registers (SSR[0:7]), page 23). The DQ[67:0] is driven with 68-bit data ([67:0]) to be compared against all odd locations.

The logical 136-bit SEARCH operation is as shown in Figure 51, page 76. The entire table of 31 devices (consisting of 136-bit entries) is compared against a 136-bit word K that is presented on the DQ Bus in Cycles A and B of the command using the GMR and local mask bits. The GMR is the 136-bit word specified by the even and odd global mask pair selected by the GMR Index in the command's Cycle A.

The 136-bit word K that is presented on the DQ Bus in Cycles A and B of the command is also stored in the even and odd comparand registers specified by the Comparand Register Index in the command's Cycle B. In x136 configurations, the even and odd comparand registers can subsequently be used by the LEARN command in only the first non-full device.

Note: The LEARN command is supported for only one of the blocks consisting of up to eight devices in a depth-cascaded table of more than one block.

The word K that is presented on the DQ Bus in Cycles A and B of the command is compared with each entry in the table starting at location "0." The first matching entry's location address, "L," is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see SRAM ADDRESSING, page 126). The global winning device will drive the bus in a specific cycle. On global miss cycles the device with LRAM = 1 (the default driving device for the SRAM bus) and LDEV = 1 (the default driving device for SSF and SSV signals) will be the default driver for such missed cycles.

Note: During 136-bit searches of 136-bit-configured tables, the search hit will always be at an even address.

The SEARCH command is a pipelined operation. It executes a search at half the rate of the frequency of CLK2X for 136-bit searches in x136-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 136-bit SEARCH command cycle (two CLK2X cycles) is shown in Table 39, page 88.

The latency of a search from command to the SRAM access cycle is 6 for 1–31 devices in the table and where TLSZ = 10. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in Table 40, page 88.

The 136-bit SEARCH operation is pipelined and executes as follows:

- Four cycles from the SEARCH command, each of the devices knows the outcome internal to it for that operation.
- In the fifth cycle after the SEARCH command, the devices in a block (being less than or equal to eight devices resolving the winner within them using the LHI[6:0] and LHO[1:0] signalling mechanism) arbitrate for a winner amongst them.
- In the sixth cycle after the SEARCH command, the blocks (of devices) resolve the winning block through the BHI[2:0] and BHO[2:0] signalling mechanism. The winning device in the winning block is the global winning device for a SEARCH operation.

Table 38. Hit/Miss Assumption

Search Number	1	2	3	4
Block 0	Miss	Miss	Miss	Miss
Block 1	Miss	Miss	Hit	Miss
Block 2	Miss	Hit	Hit	Miss
Block 3	Hit	Hit	Miss	Miss

Figure 49. Hardware Diagram for a Table with 31 Devices

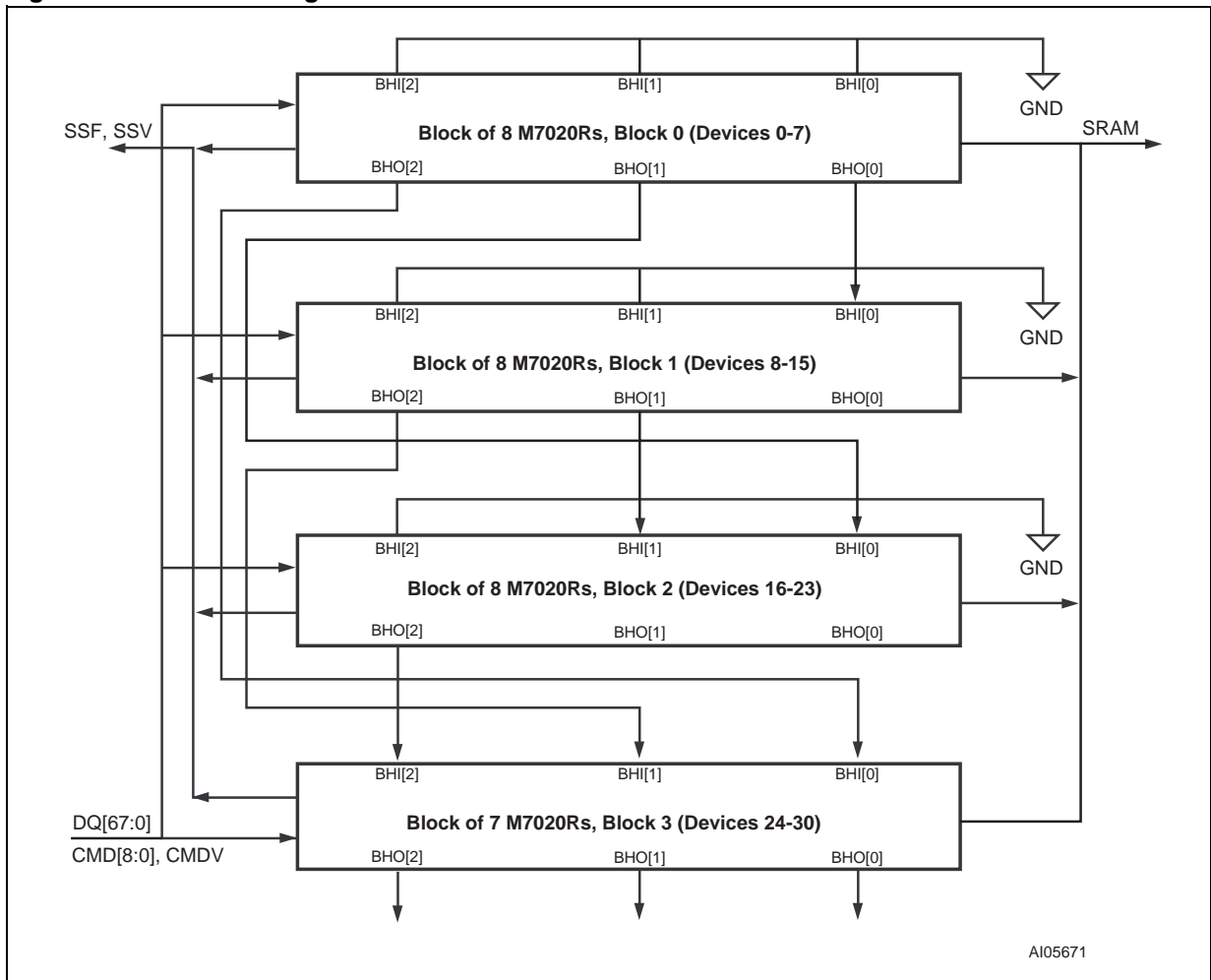


Figure 50. Hardware Diagram for a Block of Up to Eight Devices

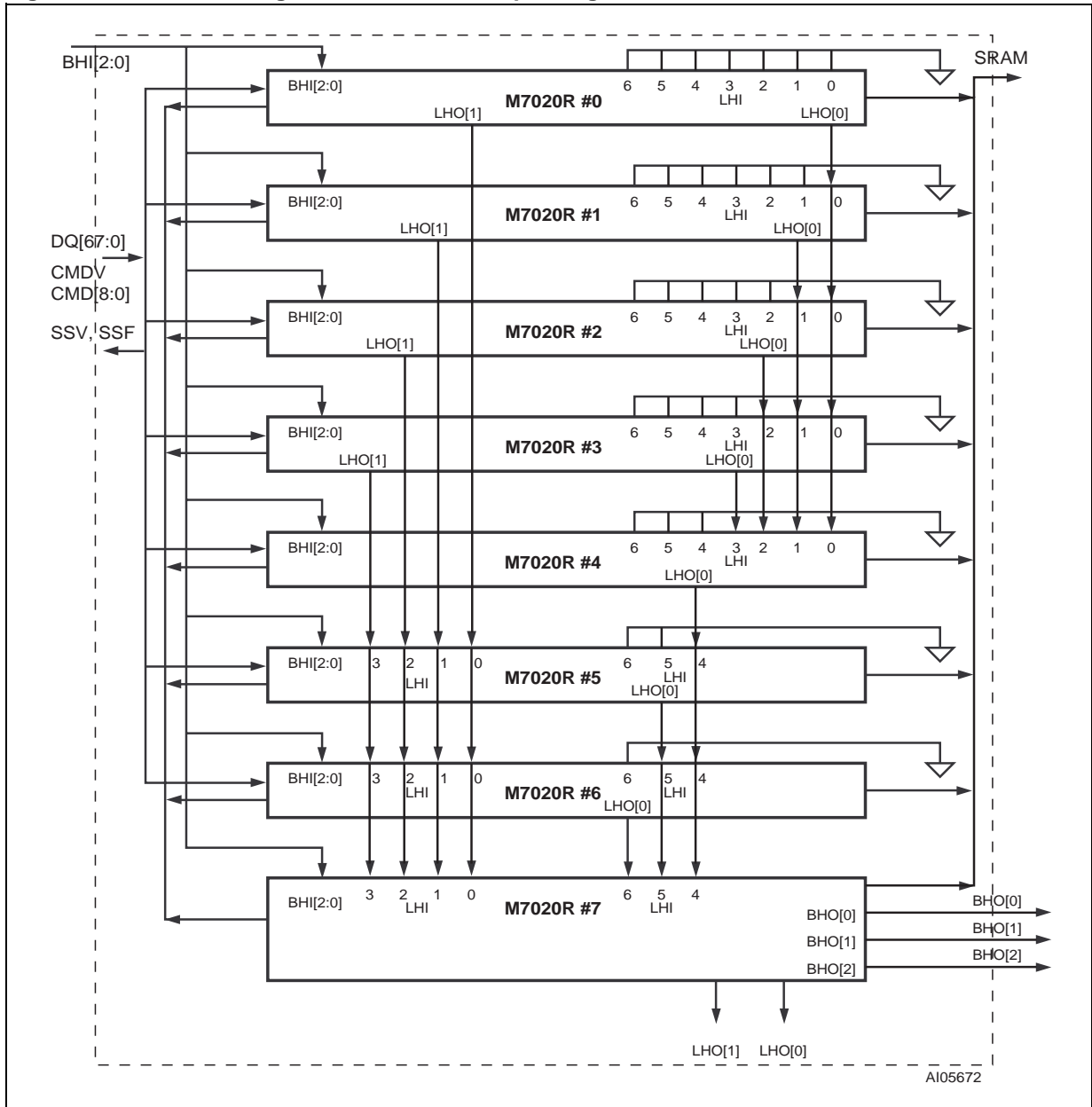
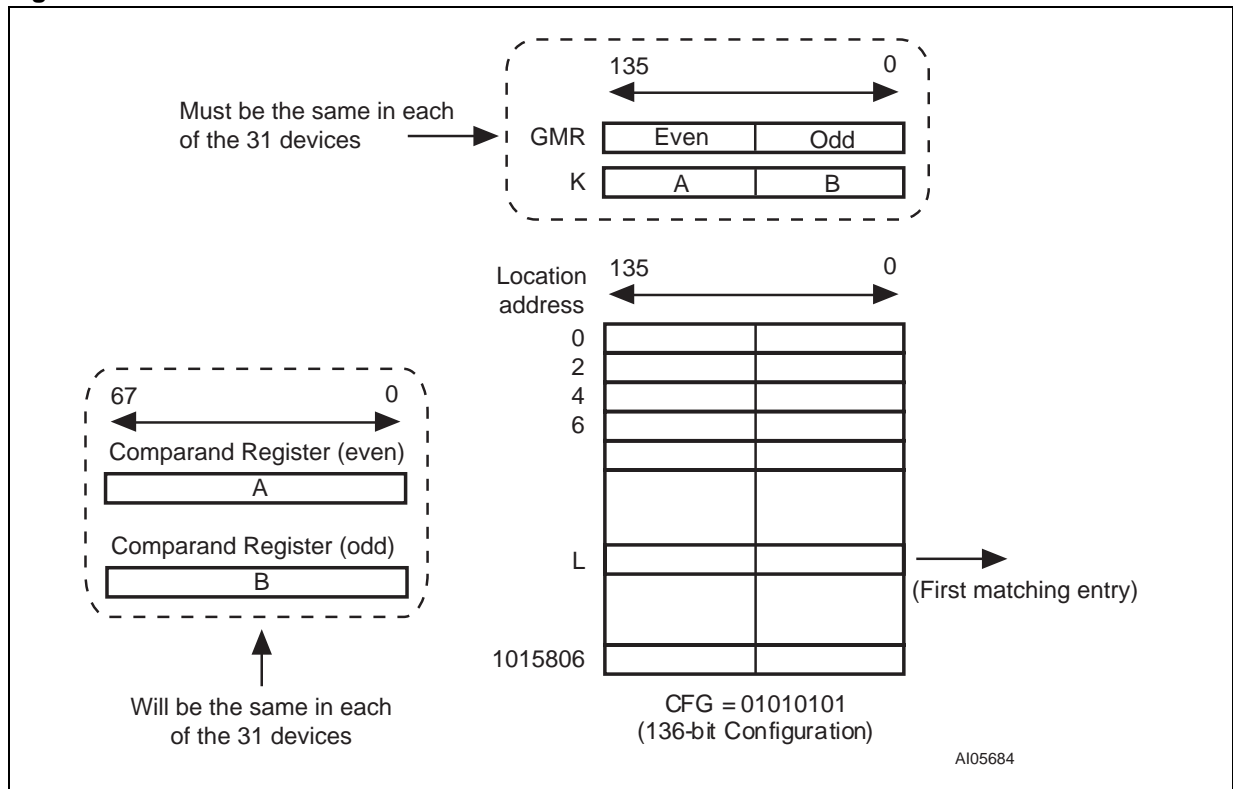
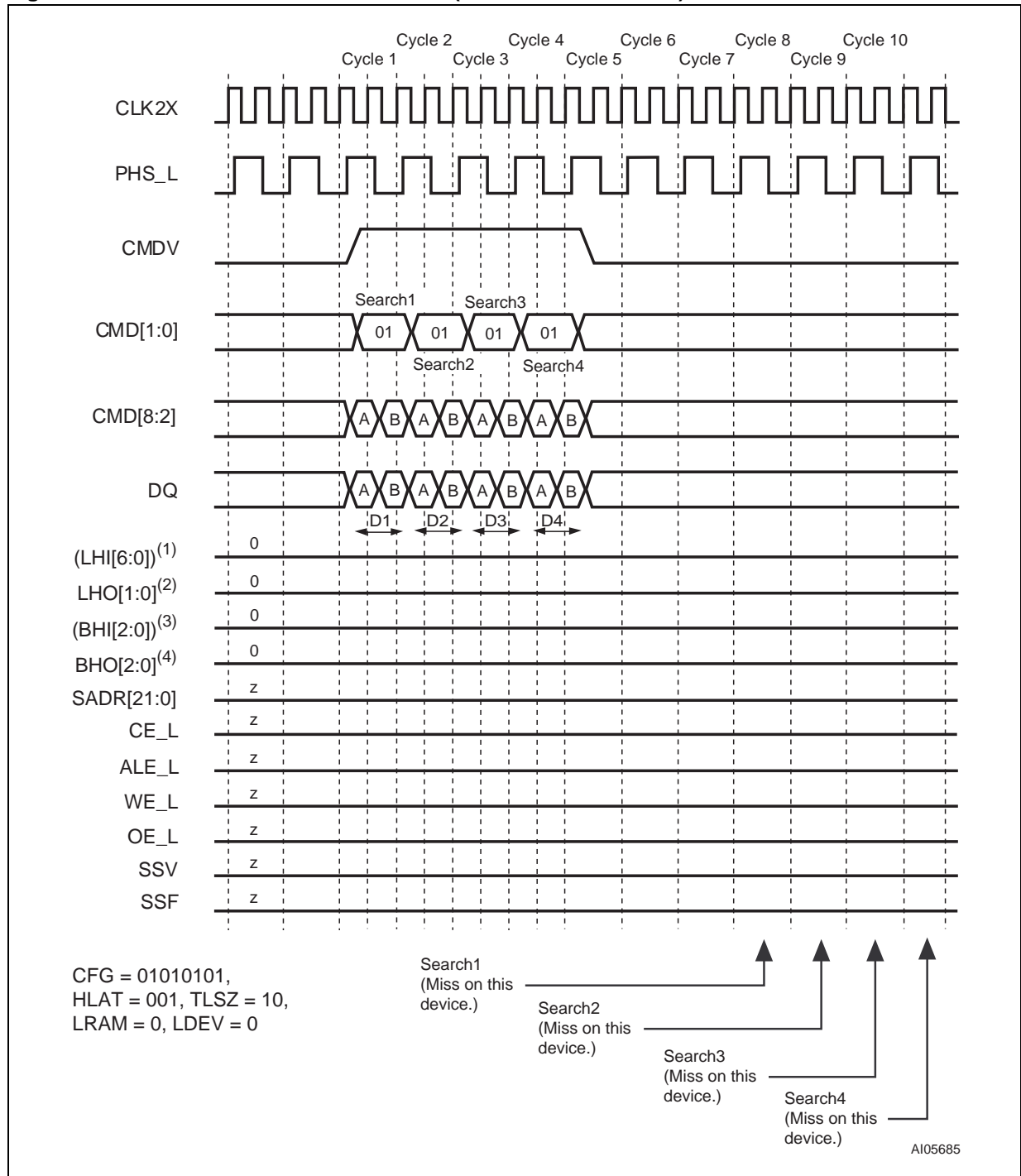


Figure 51. x136 Table with 31 Devices



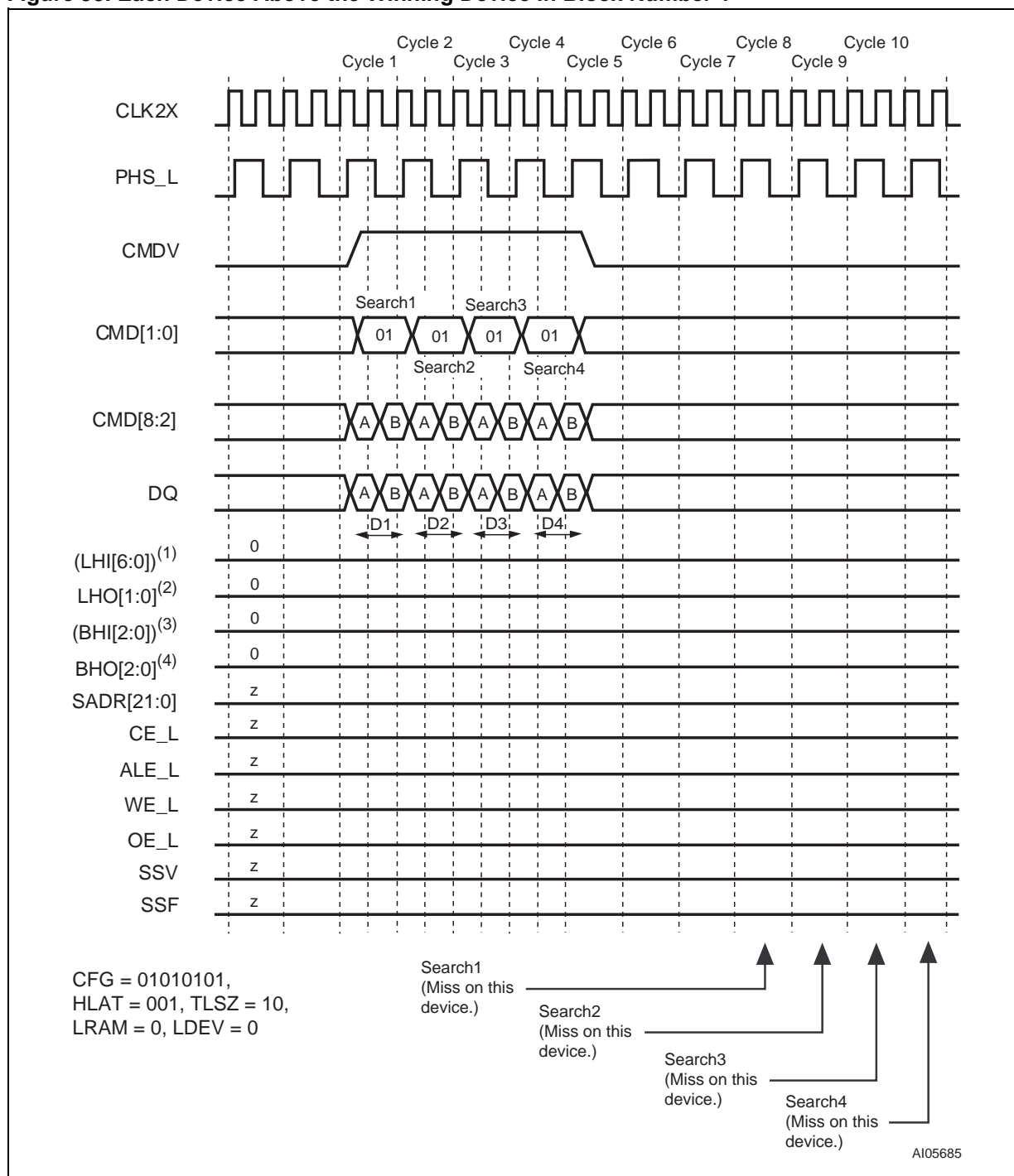
Timing Diagrams for x136 Using Up to 31 M7020R Devices

Figure 52. Each Device in Block Number 0 (Miss on Each Device)



- Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

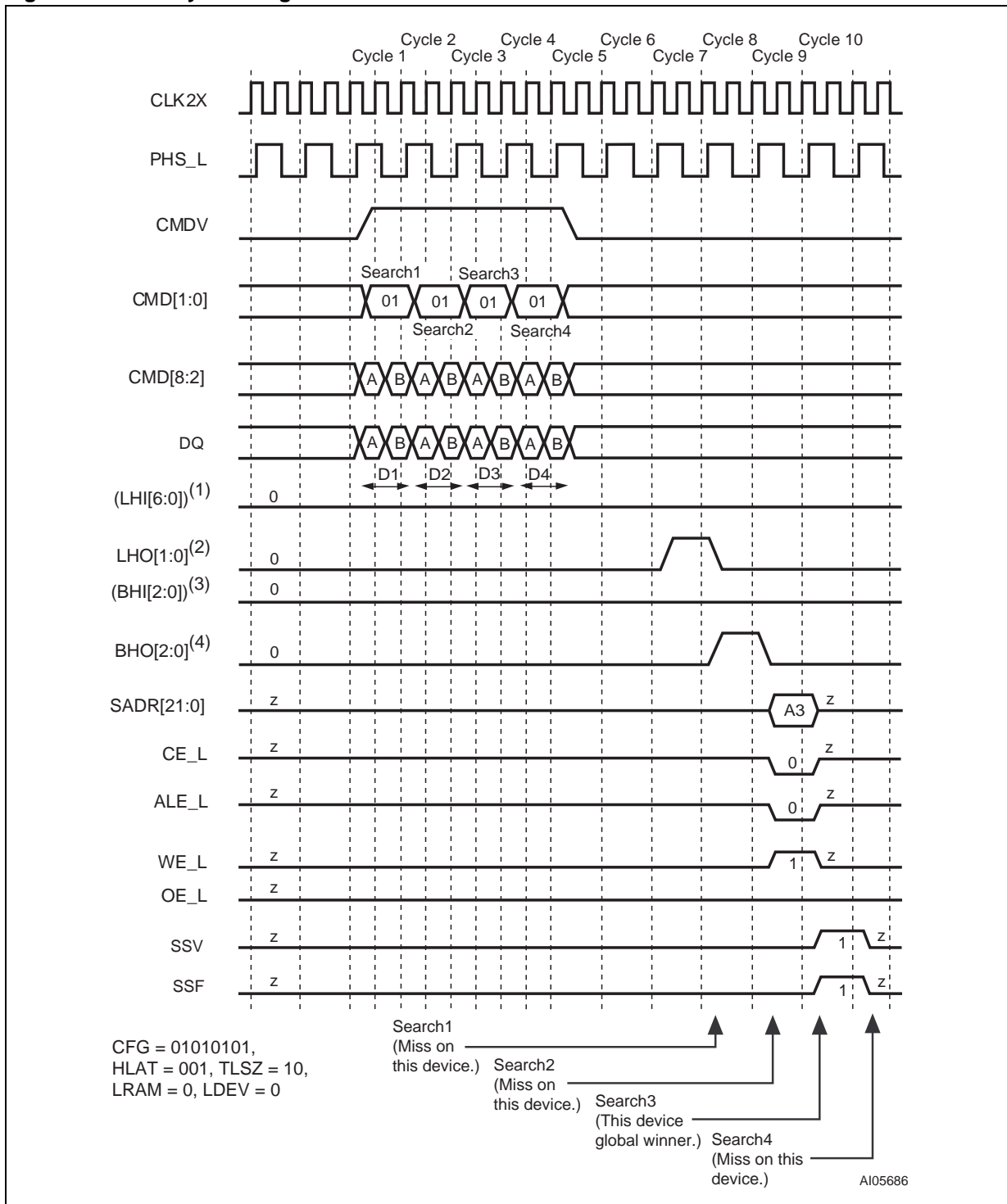
Figure 53. Each Device Above the Winning Device in Block Number 1



- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

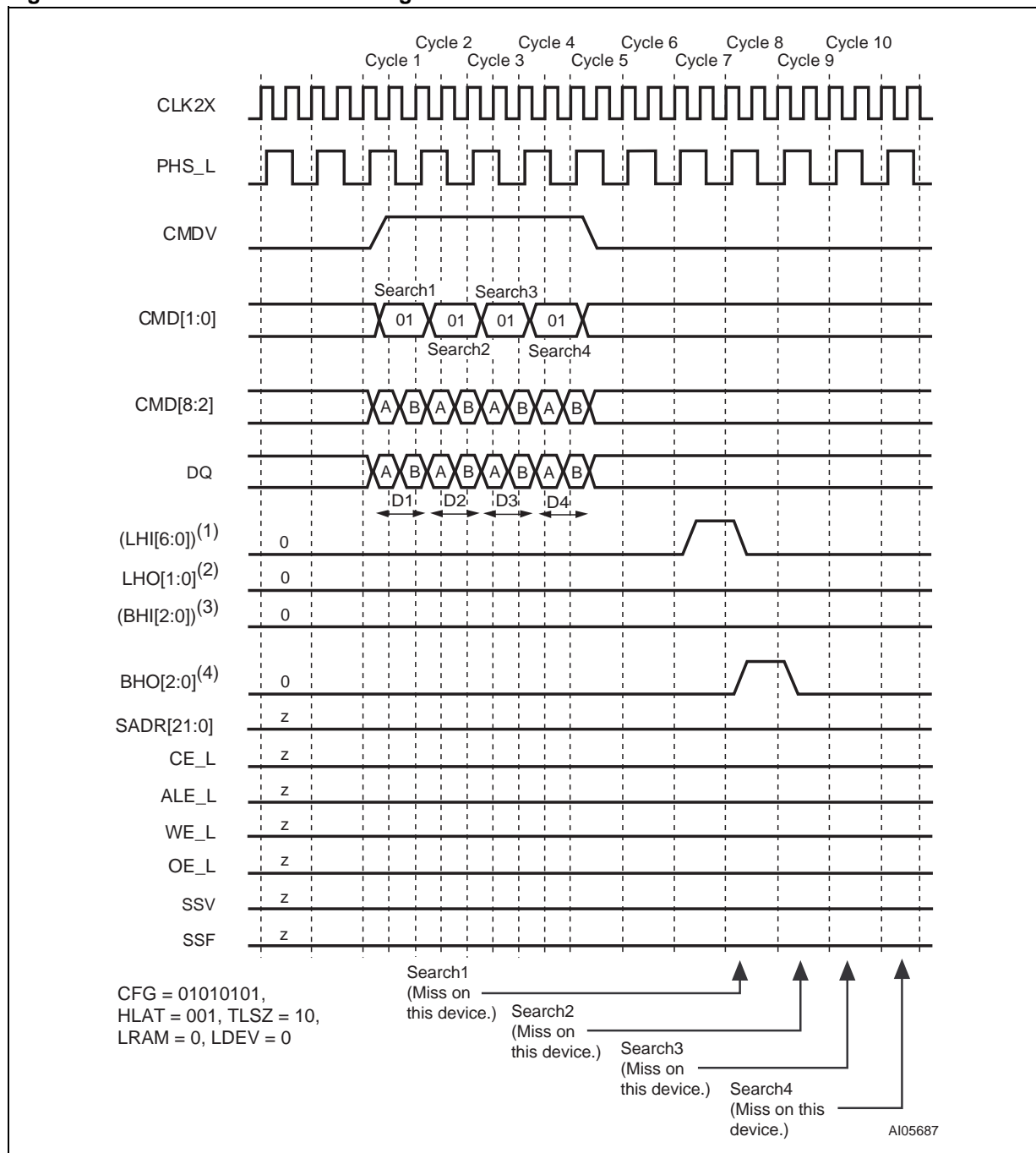


Figure 54. Globally Winning Device in Block Number 1



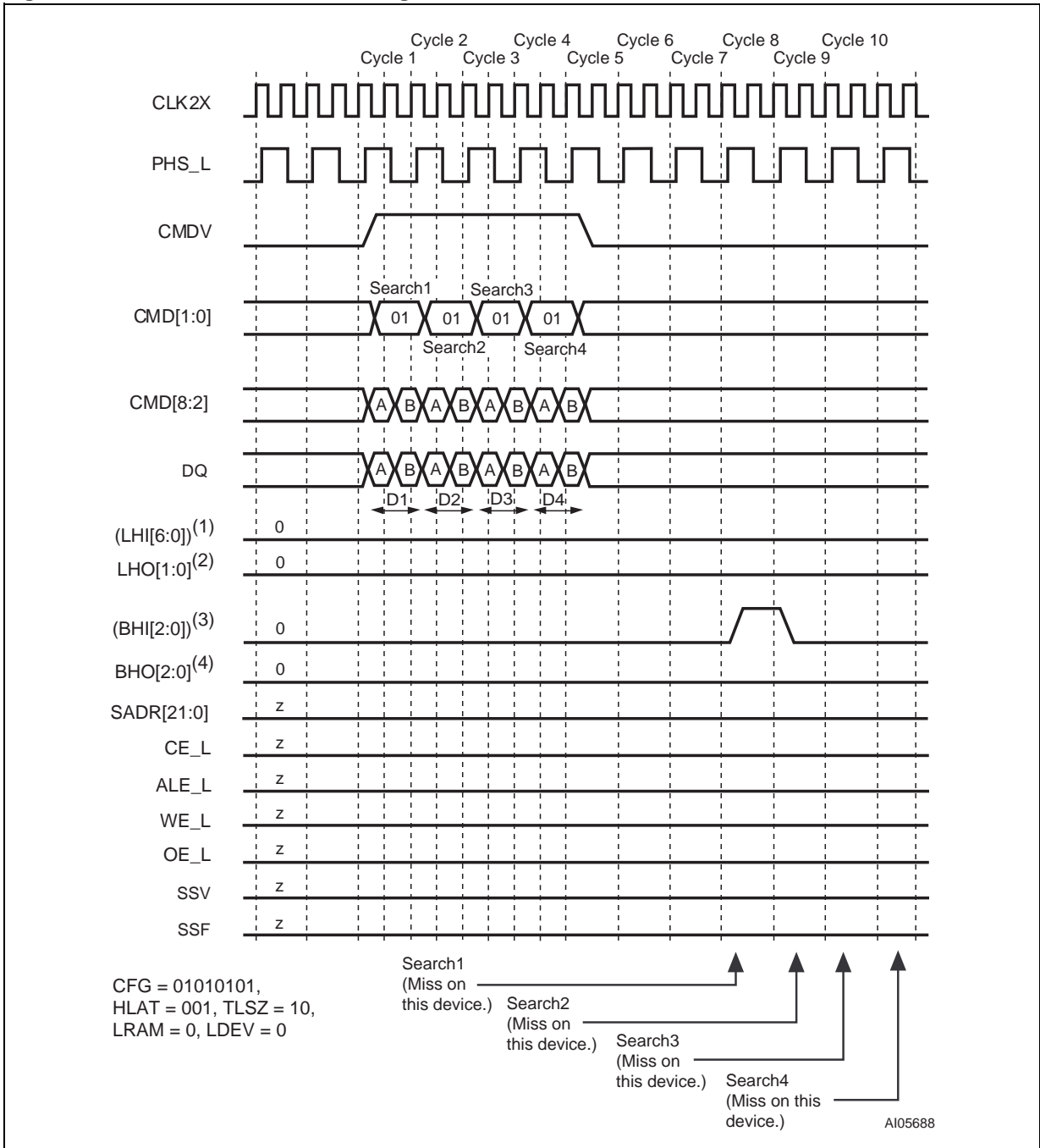
- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 55. Devices Below the Winning Device in Block Number 1



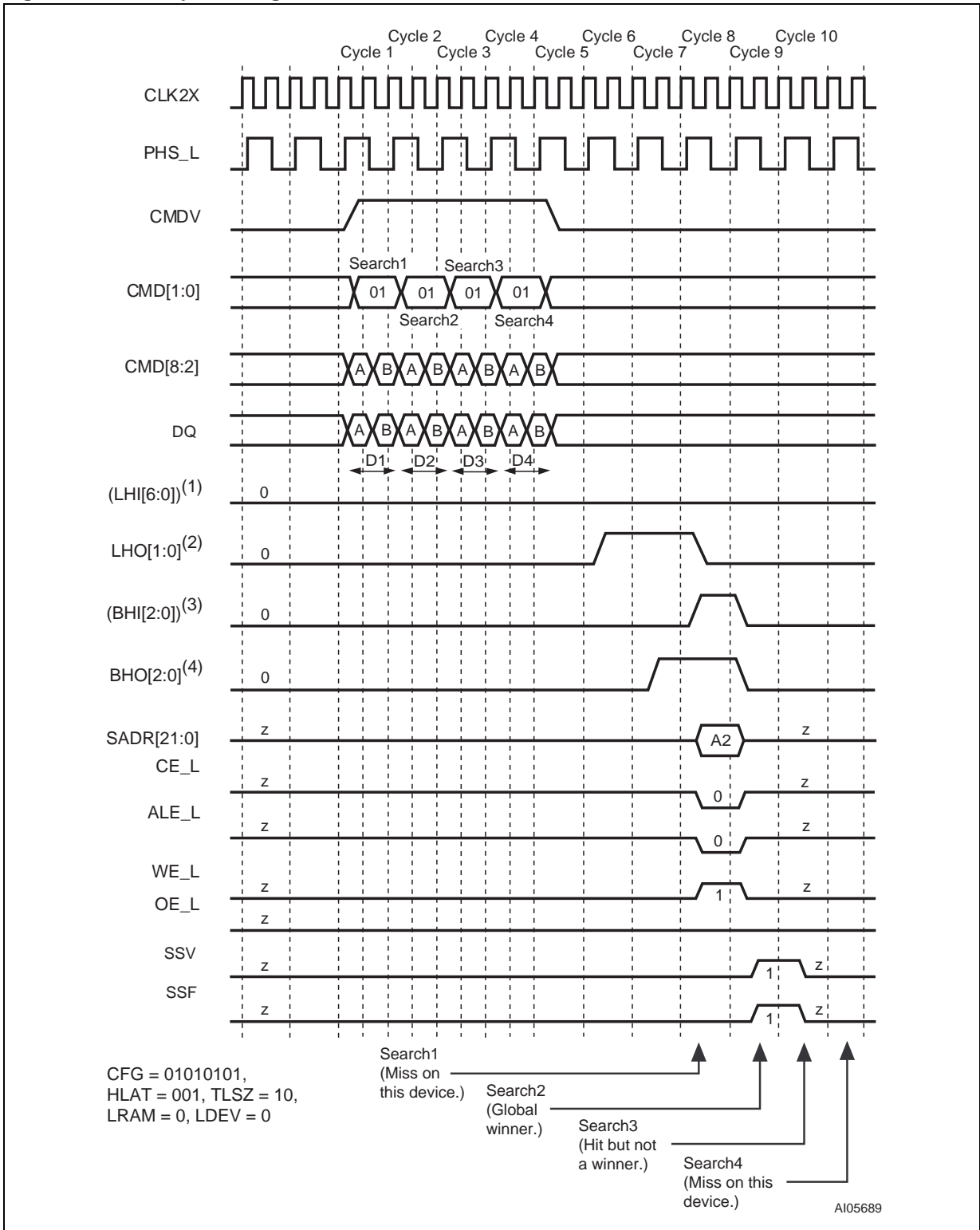
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 56. Devices Above the Winning Device in Block Number 2



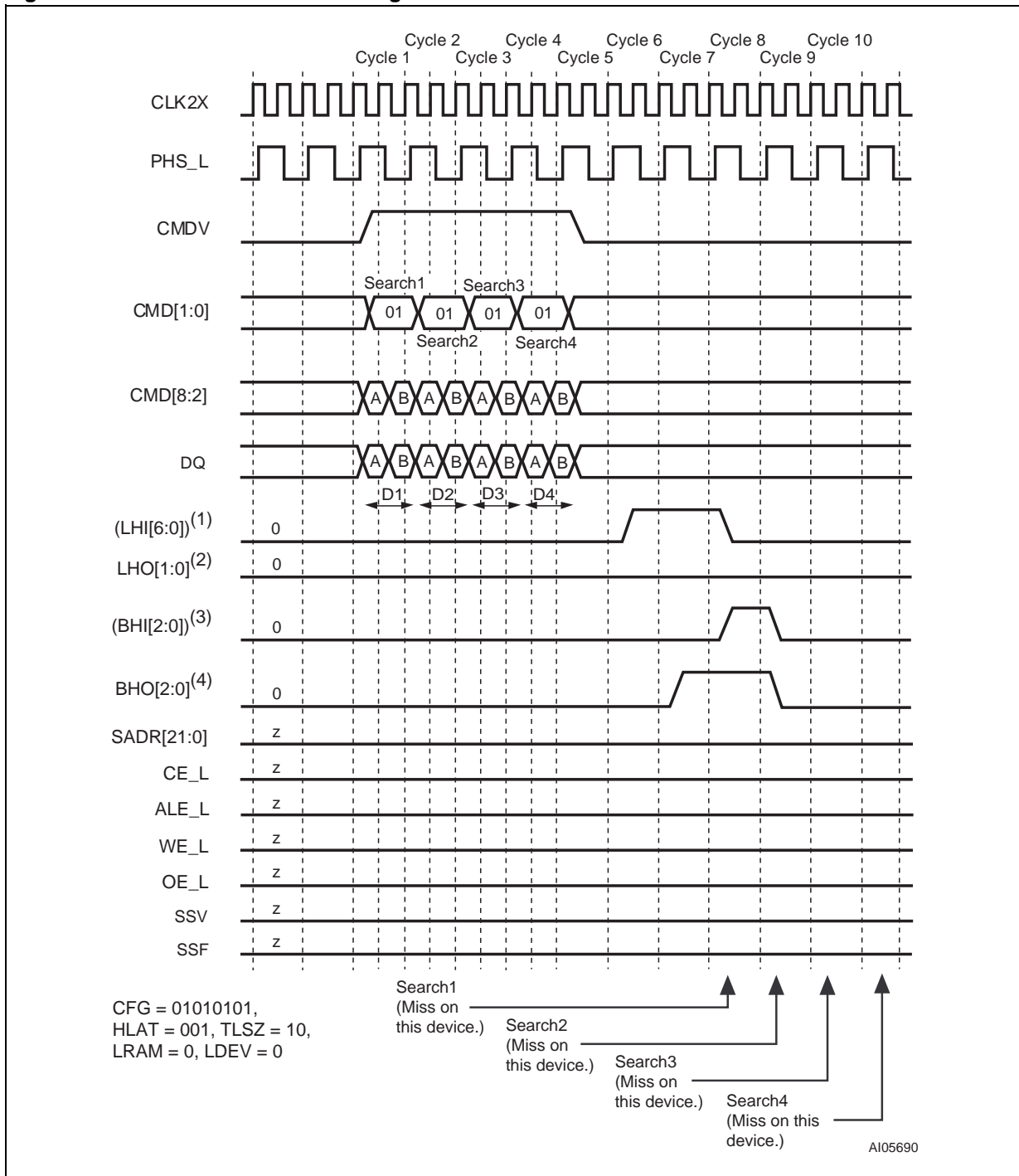
- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 57. Globally Winning Device in Block Number 2



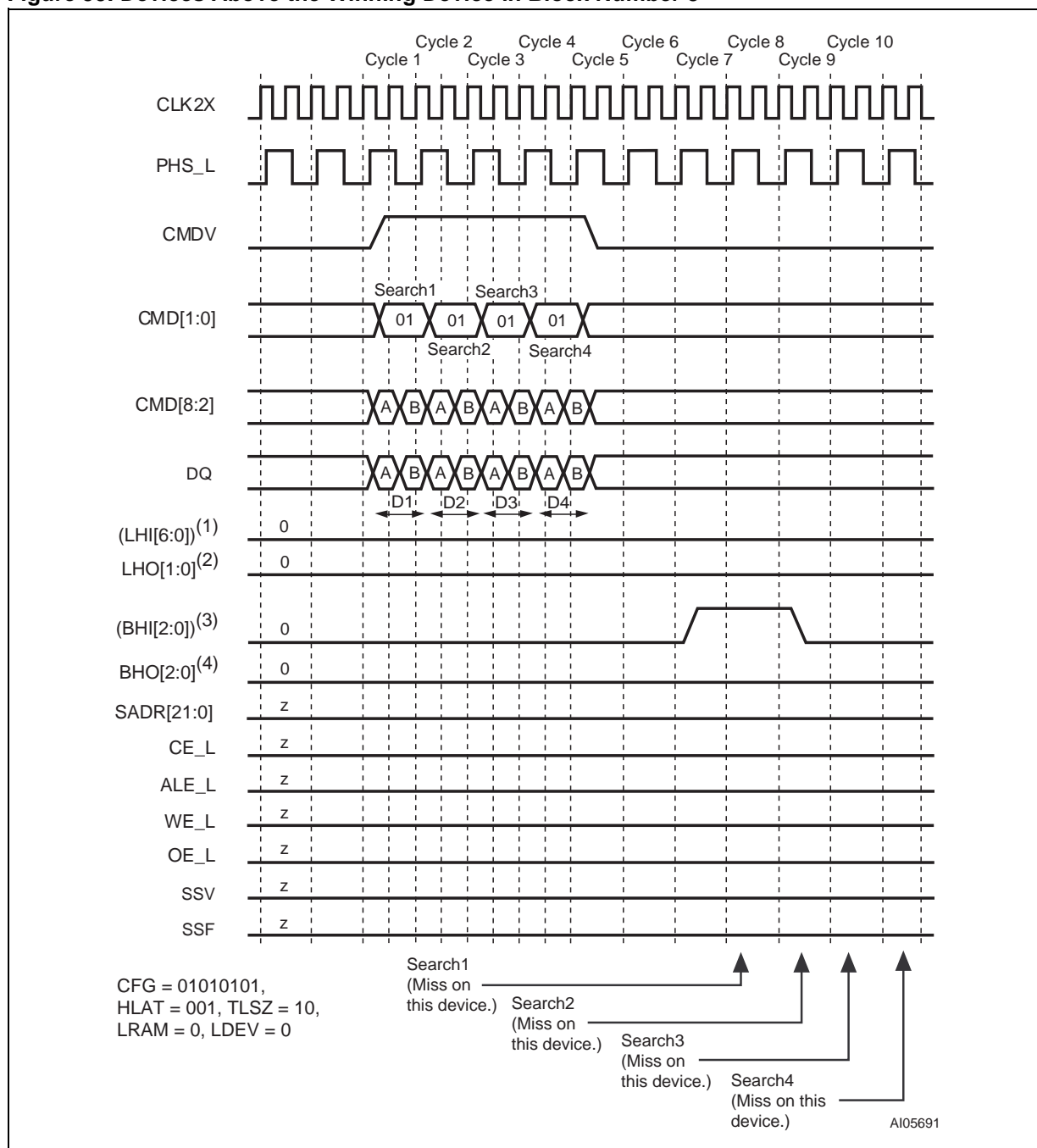
- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 58. Devices Below the Winning Device in Block Number 2



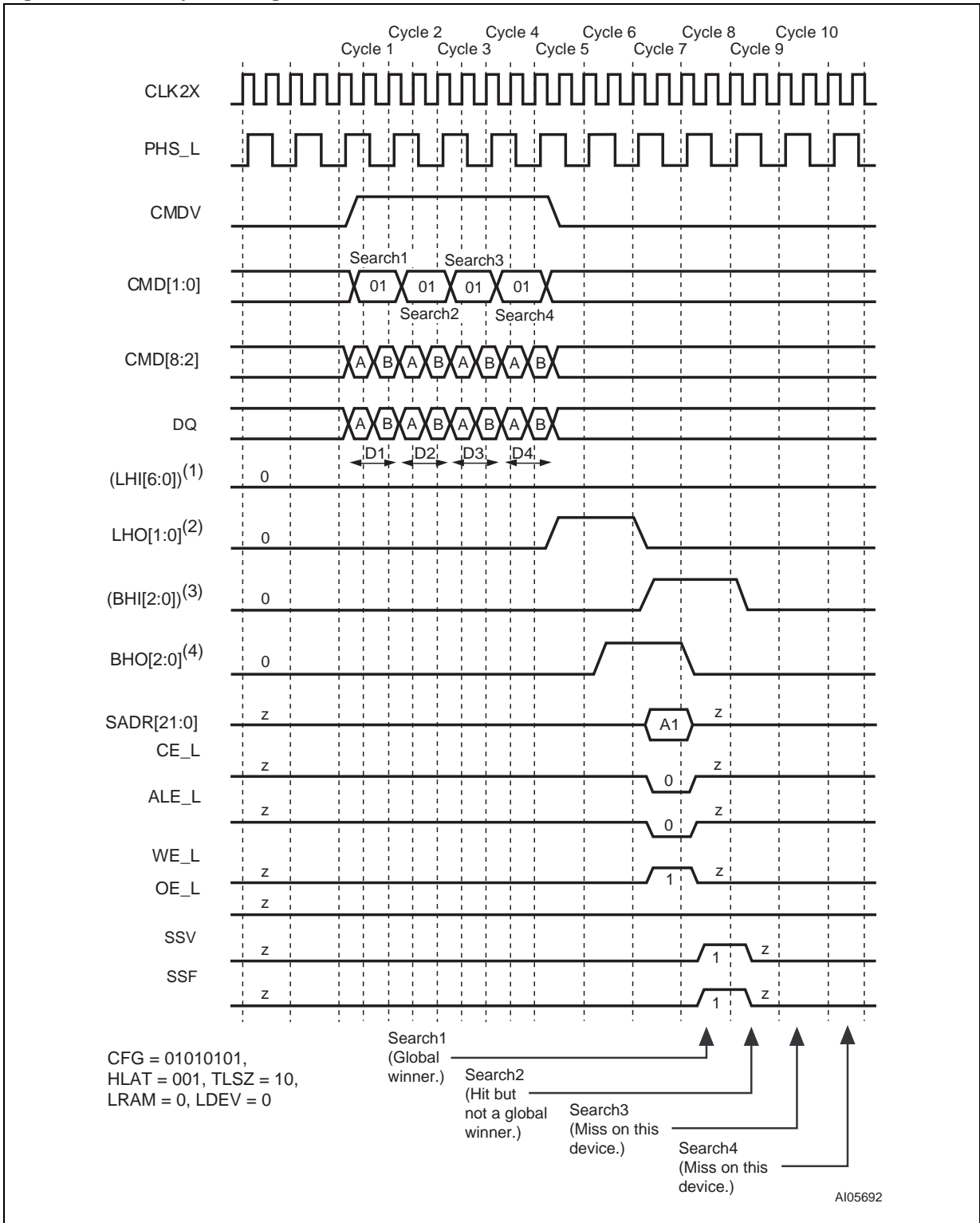
- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 59. Devices Above the Winning Device in Block Number 3



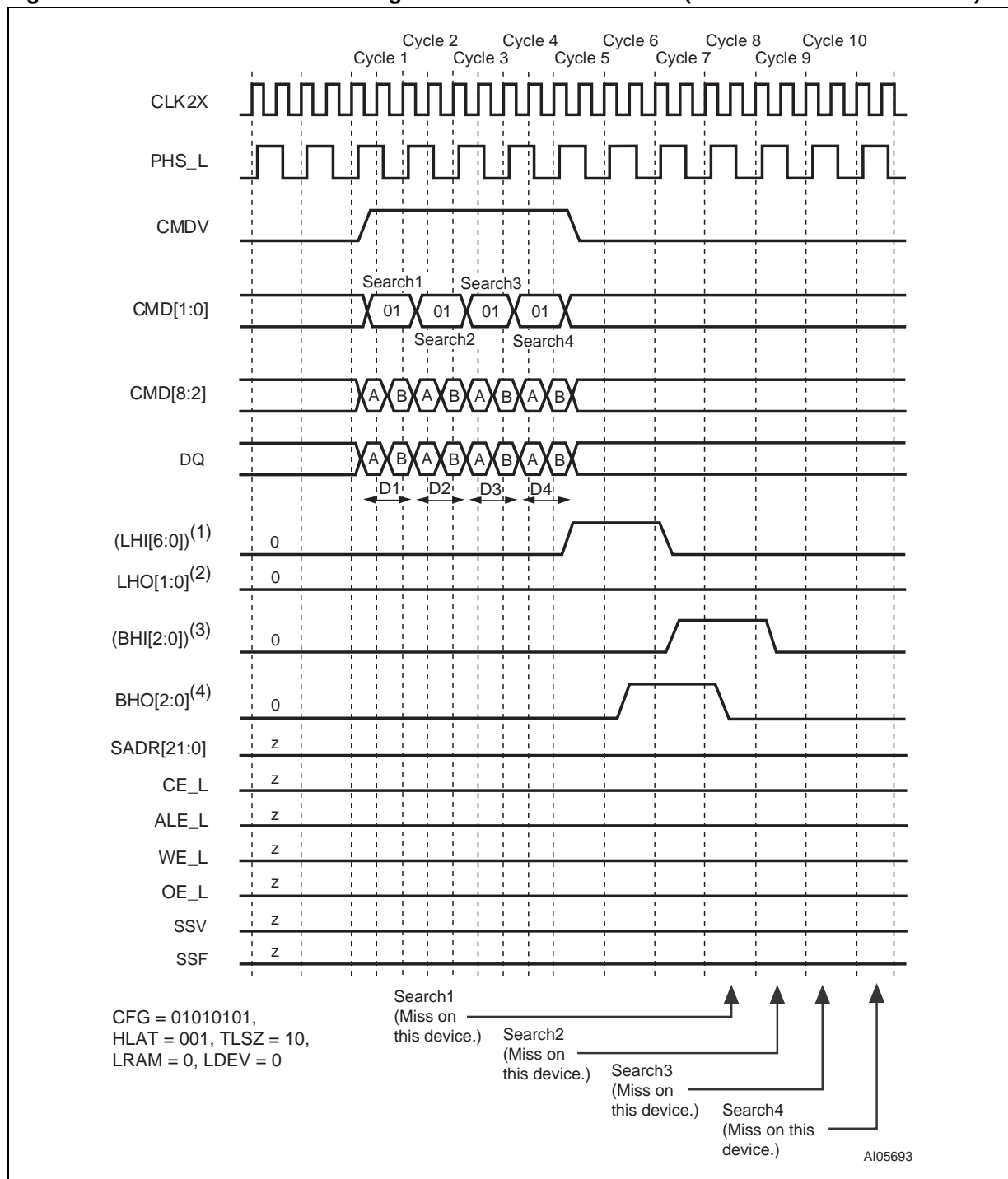
- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 60. Globally Winning Device in Block Number 3



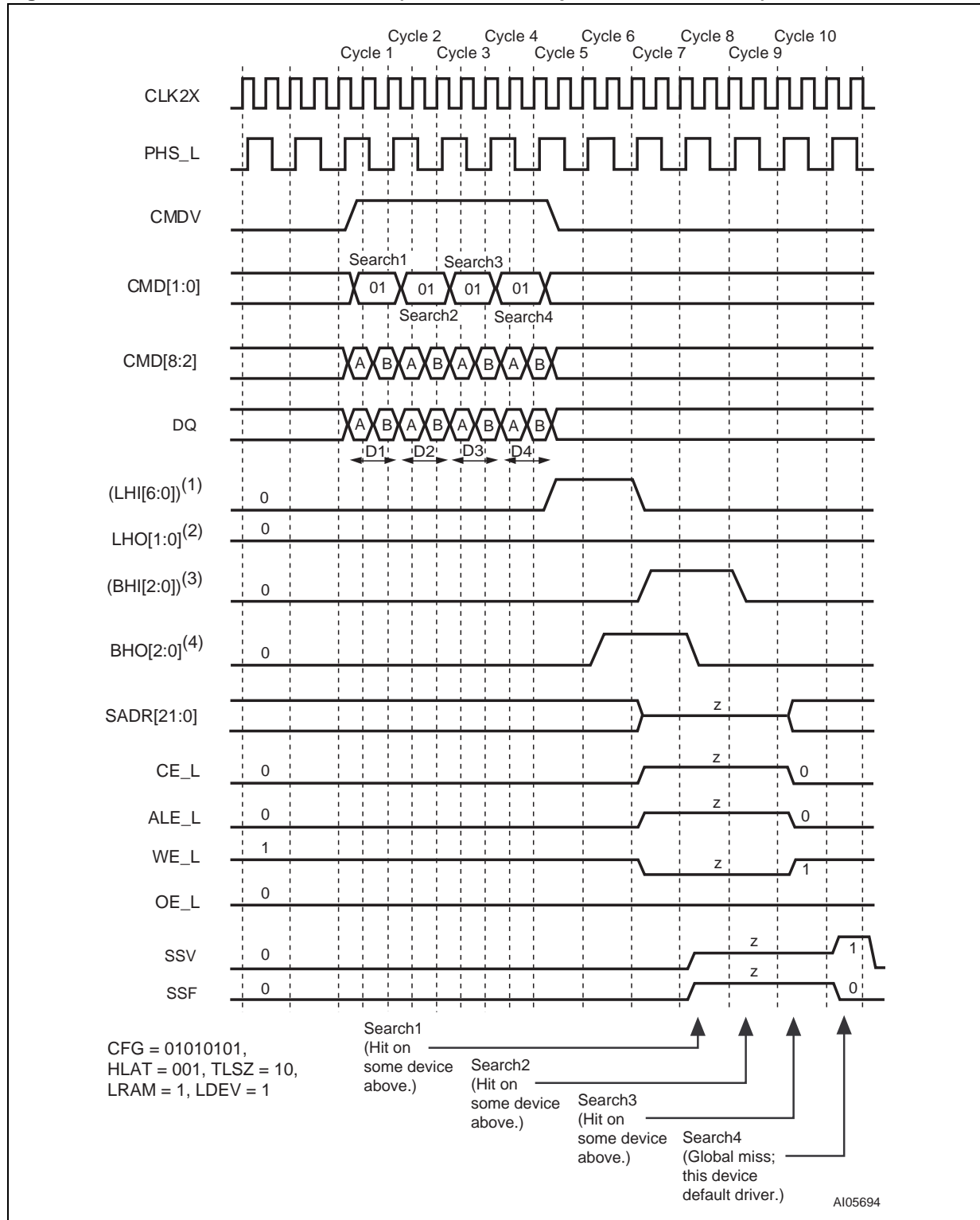
- Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.
3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
4. Each bit in BHO[2:0] is the same logical signal.

Figure 61. Devices Below the Winning Device in Block Number 3 (not Device 30 - Last Device)



Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 62. Device 6 in Block Number 3 (Device 30 in Depth-Cascaded Table)



- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Table 39. Latency of SEARCH from Instruction to SRAM Access Cycle, 136-bit, Up to 31 Devices

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	16K x 136-bit	4
2–8 (TLSZ = 01)	128K x 136-bit	5
9–31 (TLSZ = 10)	496K x 136-bit	6

Table 40. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

272-bit SEARCH on Tables Configured as x272 Using a Single M7020R Device

The hardware diagram for this search subsystem is shown in Figure 63, page 89. Figure 64, page 90 shows the timing diagram for a SEARCH command in the 272-bit-configured table (CFG = 10101010) consisting of a single device for one set of parameters: TLSZ = '00,' HLAT = '001,' LRAM = '1,' and LDEV = '1.'

The following is the sequence of operation for a single 136-bit SEARCH command (also refer to COMMAND CODES AND PARAMETERS, page 29).

- **Cycle A:** The host ASIC drives the CMDV high and applies SEARCH command code ('10') on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair used for bits [271:136] of the data being searched. DQ[67:0] must be driven with the 68-bit data ([271:204]) to be compared to all locations "0" in the four 68-bits-word page. The CMD[2] signal must be driven to logic '1.'
- Note:** CMD[2] = 1 signals that the search is a x272-bit search. CMD[8:3] in this cycle is ignored.
- **Cycle B:** The host ASIC continues to drive the CMDV high and continues to apply the command code of SEARCH command ('10') on CMD[1:0]. The DQ[67:0] is driven with the 68-bit data ([204:136]) to be compared to all locations "1" in the four 68-bits-word page.

- **Cycle C:** The host ASIC drives the CMDV high and applies SEARCH command code ('10') on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair used for bits [135:0] of the data being searched. CMD[8:7] signals must be driven with the bits that will be driven on SADR[21:20] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data ([135:68]) to be compared to all locations "2" in the four 68-bits-word page. The CMD[2] signal must be driven to logic '0.'
- **Cycle D:** The host ASIC continues to drive the CMDV high and applies SEARCH command code ('10') on CMD[1:0]. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the Hit Flag (see SEARCH-Successful Registers (SSR[0:7]), page 23). The DQ[67:0] is driven with the 68-bit data ([67:0]) to be compared to all locations "3" in the four 68-bits-word page. CMD[5:2] is ignored because the LEARN Instruction is not supported for x272 tables.
- Note:** For 272-bit searches, the host ASIC must supply four distinct 68-bit data words on DQ[67:0] during Cycles A, B, C, and D. The GMR Index in Cycle A selects a pair of GMRs that apply to DQ data in Cycles A and B. The GMR Index in Cycle C selects a pair of GMRs that apply to DQ data in Cycles C and D.

The logical 272-bit SEARCH operation is shown in Figure 65, page 91. The entire table of 272-bit entries is compared to a 272-bit word K that is presented on the DQ Bus in Cycles A, B, C, and D of the command using the GMR and local mask bits. The GMR is the 272-bit word specified by the two pairs of GMRs selected by the GMR Indexes in the command's Cycles A and C. The 272-bit word K that is presented on the DQ Bus in Cycles A, B, C, and D of the command is compared with each entry in the table starting at location "0." The first matching entry's location address, "L," is the winning address that is driven as part of the SRAM address on SADR[21:0] lines (see SRAM ADDRESSING, page 126).

Note: The matching address is always going to be location "0" in a four-entry page for a 272-bit

SEARCH (two LSBs of the matching index will be '00').

The SEARCH command is a pipelined operation and executes at one-fourth the rate of the frequency of CLK2X for 272-bit searches in x272-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 272-bit SEARCH command (measured in CLK cycles) from the CLK2X cycle that contains the C and D Cycles is shown in Table 41, page 91.

The latency of a SEARCH from command to SRAM access cycle is 4 for only a single device in the table and TLSZ = 00. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in Table 42, page 91.

Figure 63. Hardware Diagram for a Table with One Device

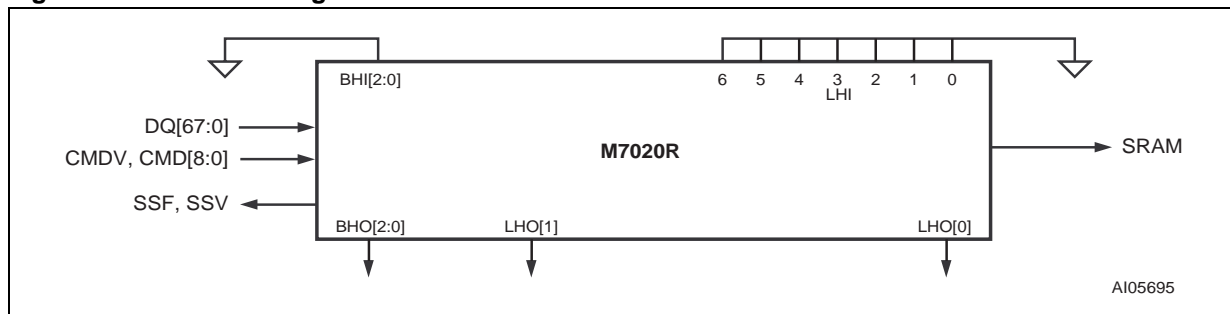


Figure 64. Timing Diagram for a 272-bit SEARCH for One Device

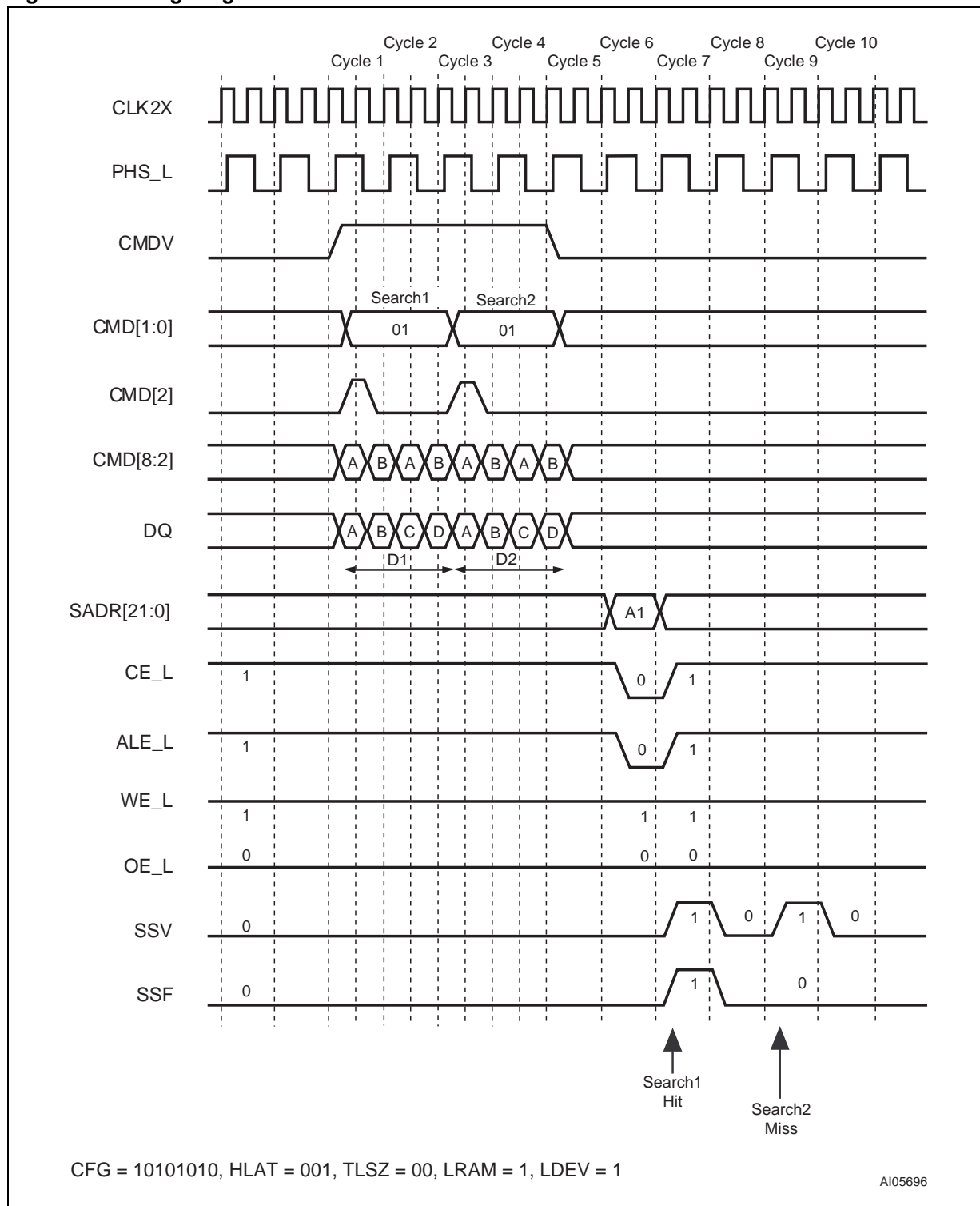


Figure 65. x272 Table with One Device

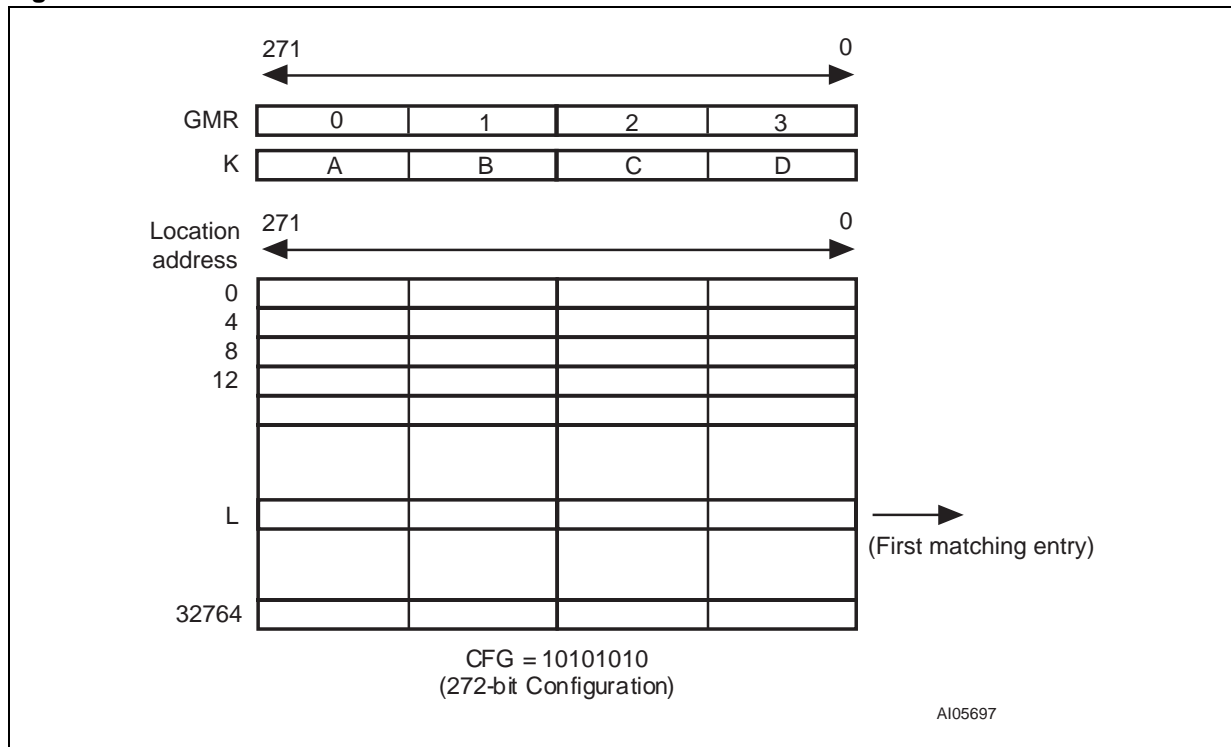


Table 41. Latency of SEARCH from Cycles C and D to SRAM Access Cycle, 272-bit, 1 Device

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	8K x 272-bit	4
2-8 (TLSZ = 01)	64K x 272-bit	5
9-31 (TLSZ = 10)	248K x 272-bit	6

Table 42. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

272-bit SEARCH on Tables x272-configured Using Up to Eight M7020R Devices

The hardware diagram of the search subsystem of eight devices is shown in Figure 66, page 94. The following are the parameters programmed in the eight devices.

- First seven devices (devices 0–6):
CFG = 10101010, TLSZ = 01, HLAT = 000,
LRAM = 0, and LDEV = 0.
- Eighth device (device 7):
CFG = 10101010, TLSZ = 01, HLAT = 000,
LRAM = 1, and LDEV = 1.

Note: All eight devices must be programmed with the same value of TLSZ and HLAT. Only the last device in the table must be programmed with LRAM = 1 and LDEV = 1 (Device 7 in this case). All other upstream devices must be programmed with LRAM = 0 and LDEV = 0 (Devices 0 through 6 in this case).

Figure 68, page 96 shows the timing diagram for a SEARCH command in the 272-bit-configured table of eight devices for Device 0. Figure 69, page 97 shows the timing diagram for a SEARCH command in the 272-bit-configured table of eight devices for Device 1. Figure 70, page 98 shows the timing diagram for a SEARCH command in the 272-bit-configured table of eight devices for Device 7 (the last device in this specific table). For these timing diagrams three 272-bit searches are performed sequentially. The following HIT/MISS assumptions were made as shown in Table 43, page 93.

The following is the sequence of operation for a single 272-bit SEARCH command (also COMMAND CODES AND PARAMETERS, page 29).

- **Cycle A:** The host ASIC drives the CMDV high and applies SEARCH command code ('10') on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair used for bits [271:136] of the data being searched in this operation. DQ[67:0] must be driven with the 68-bit data ([271:204]) to be compared against all locations "0" in the four-word, 68-bit page. The CMD[2] signal must be driven to logic '1.'
- Note:** CMD[2] = 1 signals that the search is a 272-bit search. CMD[8:3] in this cycle is ignored.
- **Cycle B:** The host ASIC continues to drive the CMDV high and applies SEARCH command code ('10') on CMD[1:0]. The DQ[67:0] is driven with the 68-bit data ([203:136]) to be compared against all locations "1" in the four 68-bit-word page.

- **Cycle C:** The host ASIC drives the CMDV high and applies SEARCH command code ('10') on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair used for bits [135:0] of the data being searched. CMD[8:7] signals must be driven with the bits that will be driven on SADR[21:20] by this device if it has a hit. DQ[67:0] must be driven with the 68-bit data ([135:68]) to be compared against all locations "2" in the four 68-bit-word page. The CMD[2] signal must be driven to logic '0.'
- **Cycle D:** The host ASIC continues to drive the CMDV high and applies SEARCH command code ('10') on CMD[1:0]. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the Hit Flag (see SEARCH-Successful Registers (SSR[0:7]), page 23). The DQ[67:0] is driven with the 68-bit data ([67:0]) to be compared to all locations "3" in the four 68-bit-word page. CMD[5:2] is ignored because the LEARN Instruction is not supported for x272 tables.

Note: For 272-bit searches, the host ASIC must supply four distinct 68-bit data words on DQ[67:0] during Cycles A, B, C, and D. The GMR Index in Cycle A selects a pair of GMRs in each of the eight devices that apply to DQ data in Cycles A and B. The GMR Index in Cycle C selects a pair of GMRs in each of the eight devices that apply to DQ data in Cycles C and D.

The logical 272-bit SEARCH operation is shown in Figure 67, page 95. The entire table of 272-bit entries is compared to a 272-bit word K that is presented on the DQ Bus in Cycles A, B, C, and D of the command using the GMR and the local mask bits. The GMR is the 272-bit word specified by the two pairs of GMRs selected by the GMR Indexes in the command's Cycles A and C in each of the eight devices. The 272-bit word K that is presented on the DQ Bus in Cycles A, B, C, and D of the command is compared to each entry in the table starting at location "0." The first matching entry's location address, "L," is the winning address that is driven as part of the SRAM address on the SADR[23:0] lines (see SRAM ADDRESSING, page 126).

Note: The matching address is always going to be a location "0" in a four-entry page for 272-bit SEARCH (two LSBs of the matching index will be '00').

The SEARCH command is a pipelined operation and executes search at one-fourth the rate of the frequency of CLK2X for 272-bit searches in x272-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 272-bit SEARCH command (measured in CLK cycles)

from the CLK2X cycle that contains the C and D Cycles is shown in Table 44, page 99.

The latency of search from command to SRAM access cycle is 5 for only a single device in the table and TLSZ = 01. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in Table 45, page 99.

Table 43. Hit/Miss Assumption

Search Number	1	2	3
Device 0	Hit	Miss	Miss
Device 1	Miss	Hit	Miss
Device 2-6	Miss	Miss	Miss
Device 7	Miss	Miss	Miss

Figure 66. Hardware Diagram for a Table with Eight Devices

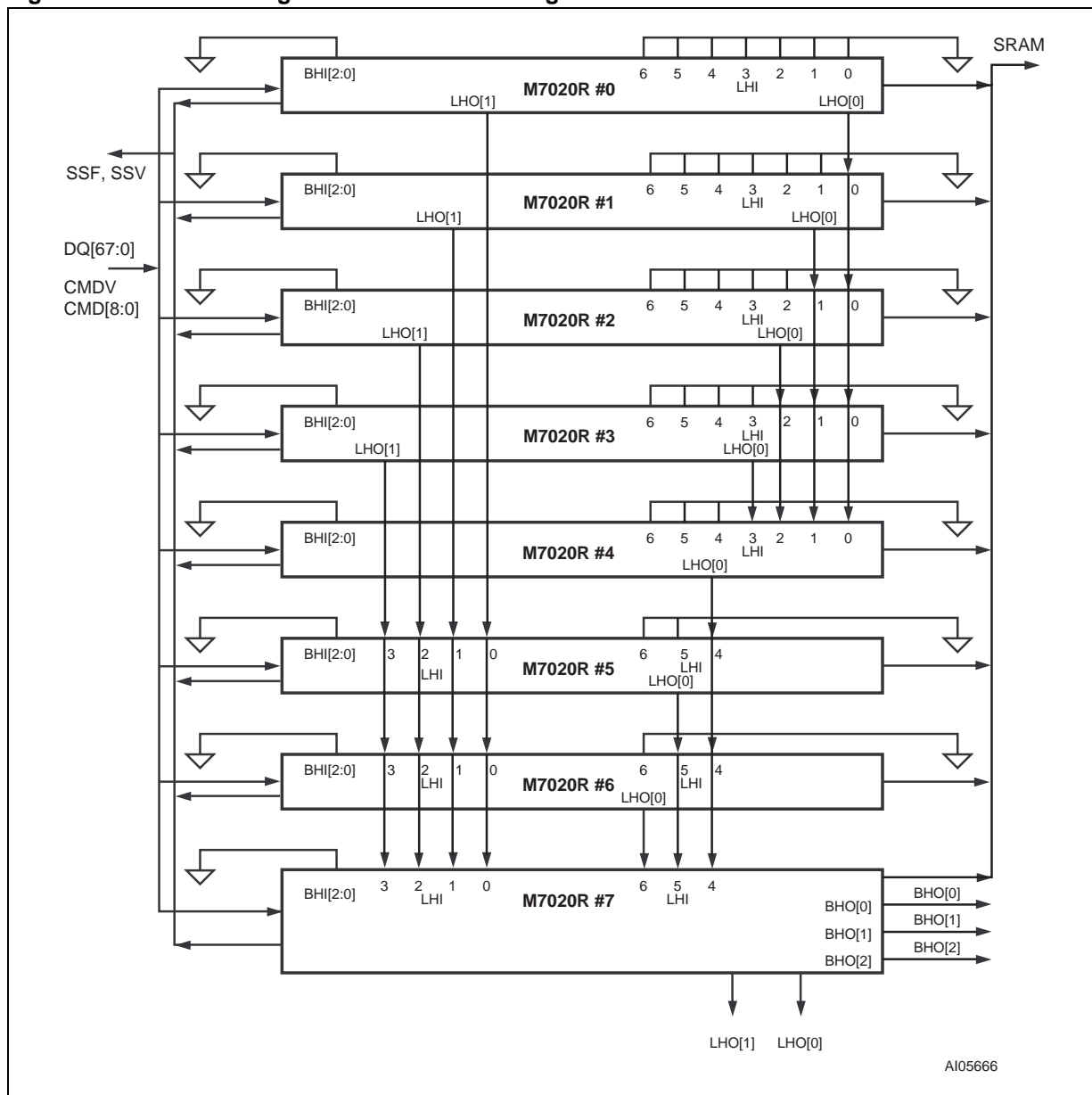
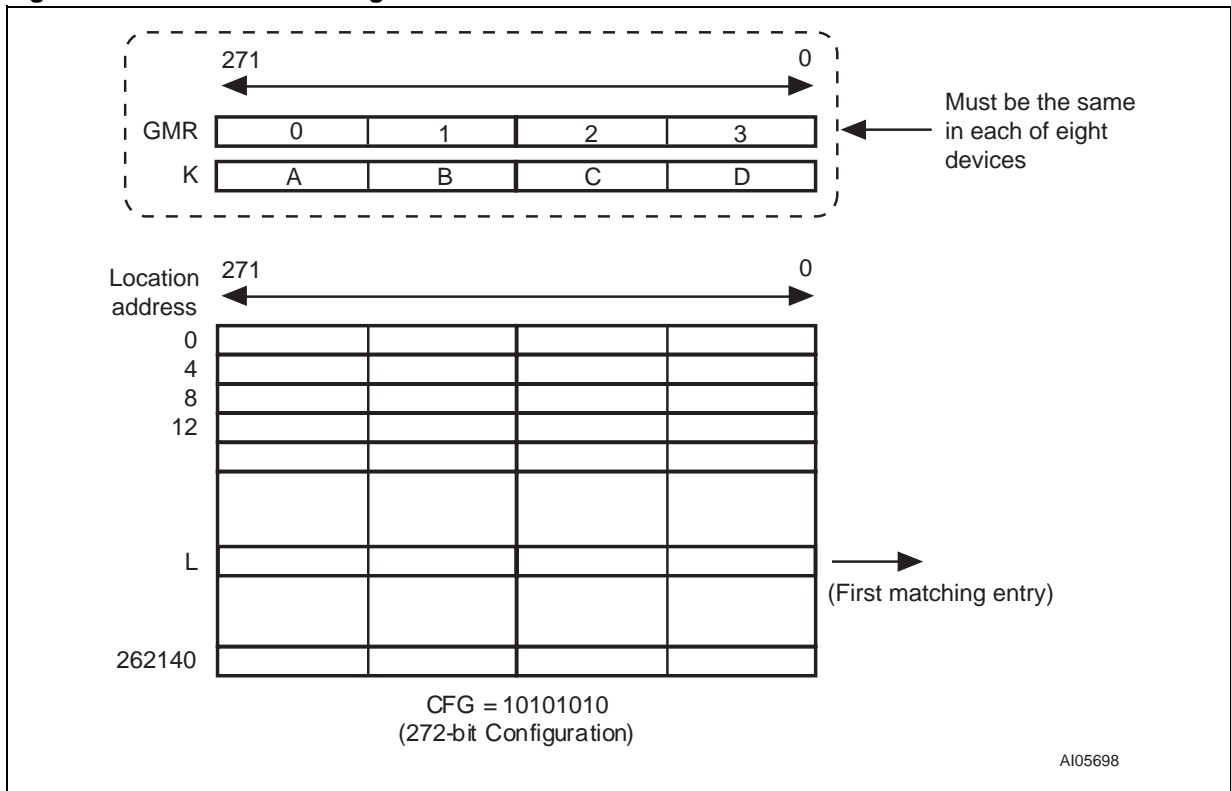
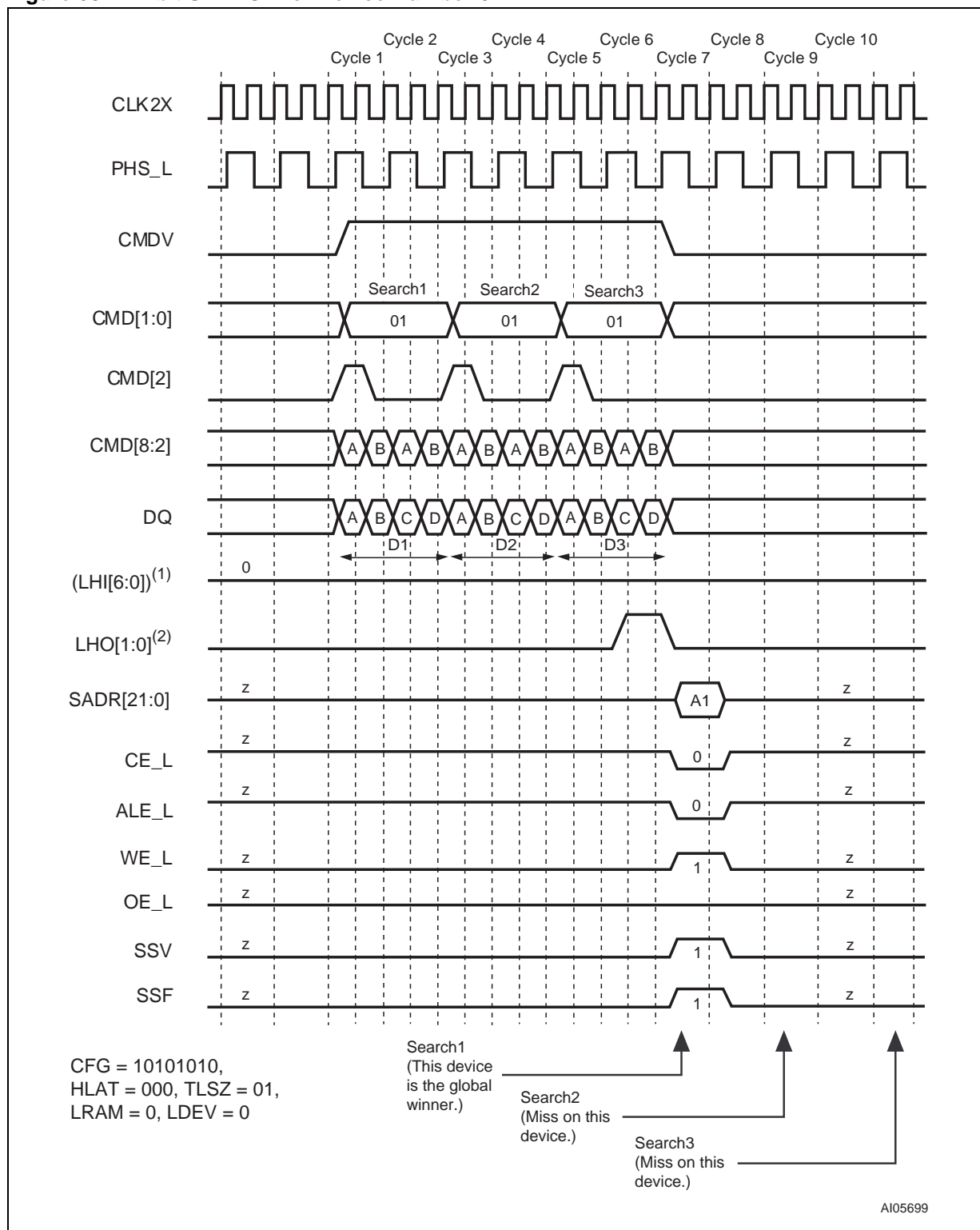


Figure 67. x272 Table with Eight Devices



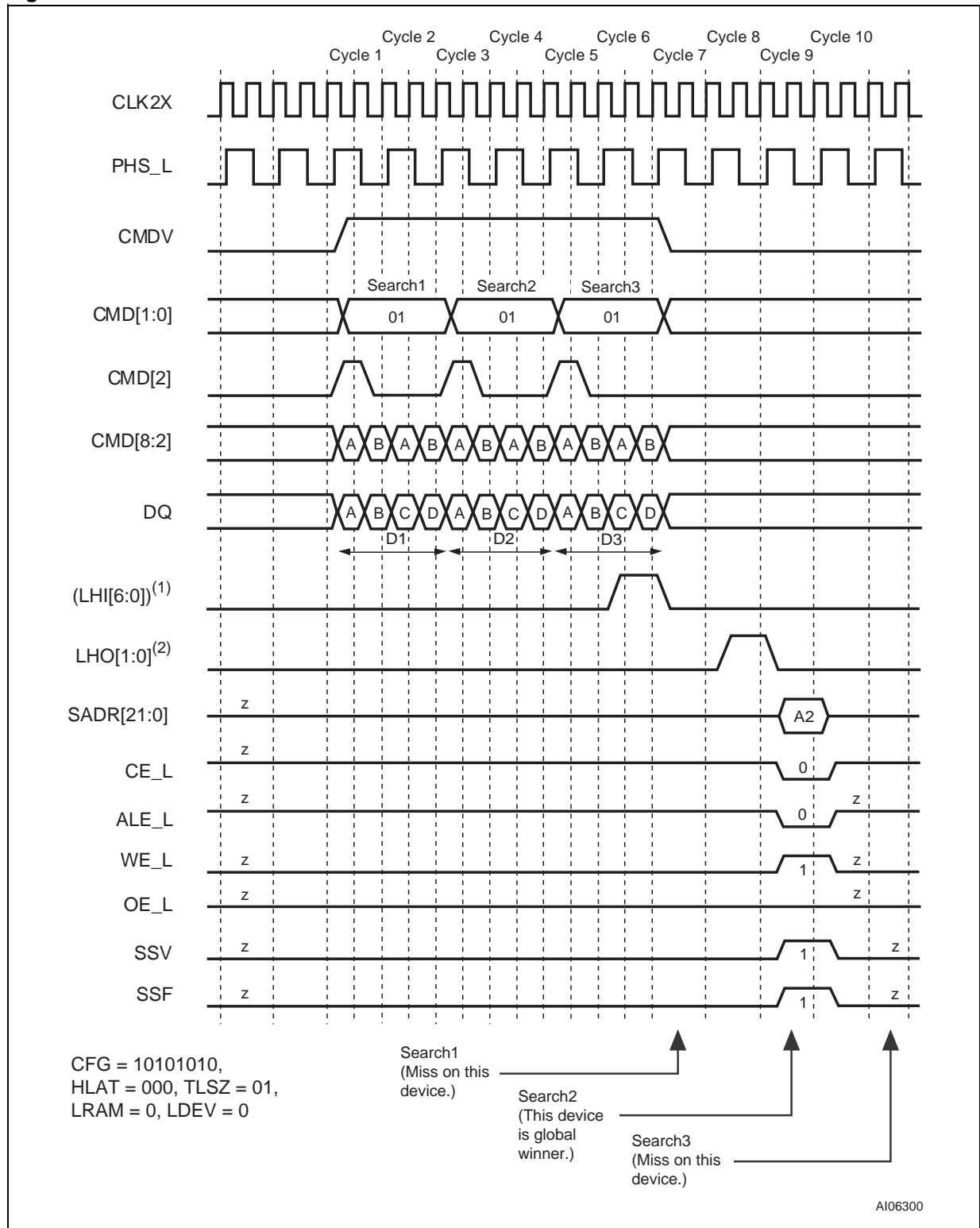
Timing Diagrams for x272-configured Using Up to Eight M7020R Devices

Figure 68. 272-bit SEARCH for Device Number 0



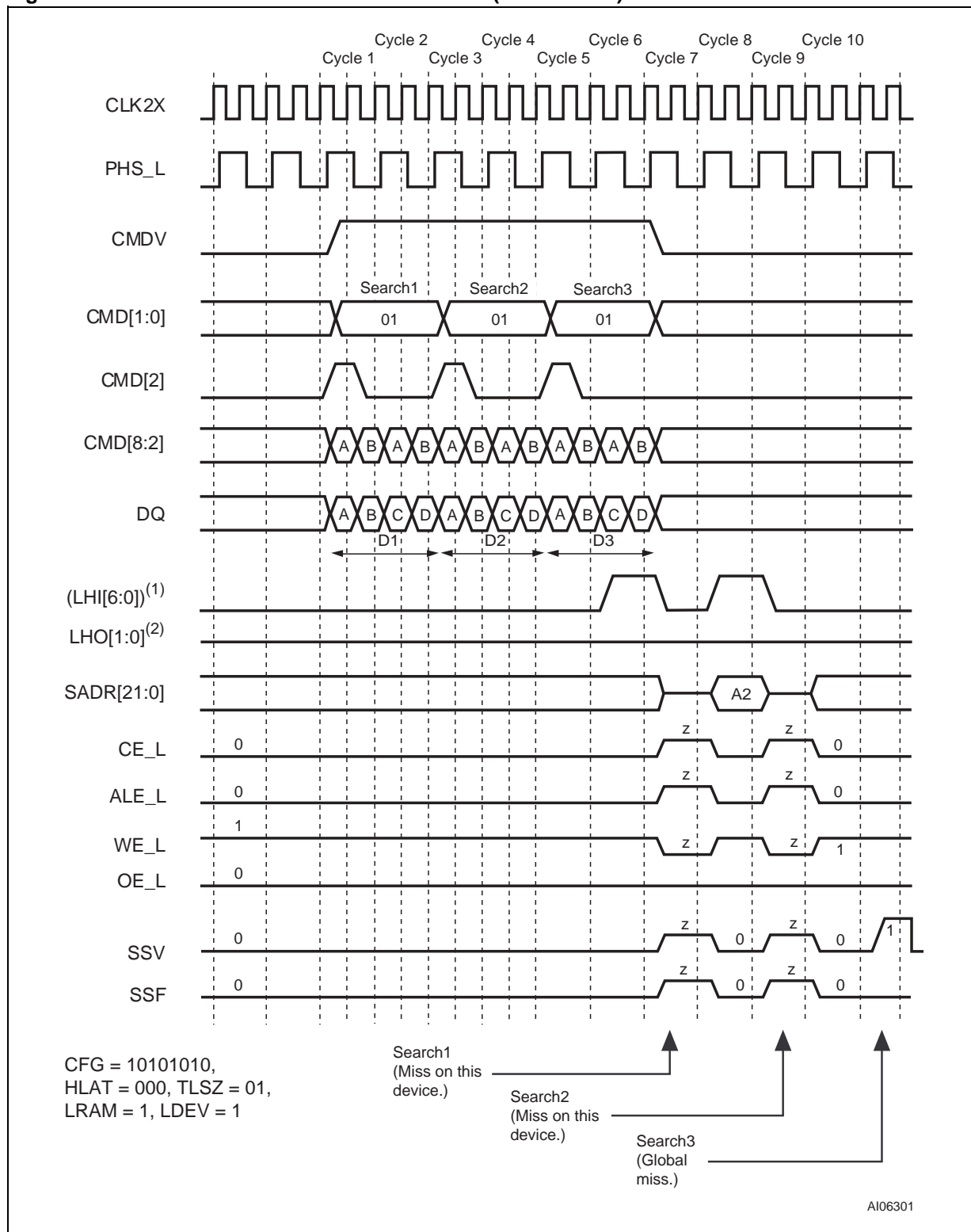
Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.

Figure 69. 272-bit SEARCH for Device Number 1



Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.

Figure 70. 272-bit SEARCH for Device Number 7 (Last Device)



Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
2. Each bit in LHO[1:0] is the same logical signal.

Table 44. Latency of SEARCH from Cycles C and D to SRAM Access Cycle, 272-bit, Up to 8 Devices

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	8K x 272-bit	4
2–8 (TLSZ = 01)	64K x 272-bit	5
9–31 (TLSZ = 10)	248K x 272-bit	6

Table 45. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

272-bit Search on Tables Configured as x272 Using Up to 31 M7020R Devices

The hardware diagram of the search subsystem of 31 devices is shown in Figure 71, page 101. Each of the four blocks in the diagram represents a block of eight M7020R devices, except the last which has seven devices. The diagram for a block of eight devices is shown in Figure 72, page 102. The following are the parameters programmed into the 31 devices.

- First thirty devices (devices 0–29):
CFG = 10101010, TLSZ = 10, HLAT = 000, LRAM = 0, and LDEV = 0.
- Thirty-first device (device 30):
CFG = 10101010, TLSZ = 10, HLAT = 000, LRAM = 1, and LDEV = 1.

Note: All 31 devices must be programmed with the same value of TLSZ and HLAT. Only the last device in the table must be programmed with LRAM = 1 and LDEV = 1 (Device 30 in this case). All other upstream devices must be programmed with LRAM = 0 and LDEV = 0 (Devices 0 through 29 in this case).

The timing diagrams referred to in this paragraph reference the HIT/MISS assumptions defined in Table 46, page 101. For the purpose of illustrating

the timings, it is further assumed that there is only one device with the matching entry in each block. Figure 74, page 104 shows the timing diagram for a SEARCH command in the 272-bit-configured table consisting of 31 devices for each of the eight devices in Block 0. Figure 75, page 105 shows the timing diagram for a SEARCH command in the 272-bit-configured table of 31 devices for all devices above the winning device in Block 1. Figure 76, page 106 shows the timing diagram for the globally winning device (the final winner within its own and all blocks) in Block 1. Figure 77, page 107 shows the timing diagram for all the devices below the globally winning device in Block 1. Figure 78, page 108, Figure 79, page 109, and Figure 80, page 110, respectively, show the timing diagrams of the devices above the globally winning device, the globally winning device, and the devices below the globally winning device for Block 2. Figure 81, page 111, Figure 82, page 112, Figure 83, page 113, and Figure 84, page 114, respectively, show the timing diagrams of the device above the globally winning device, the globally winning device, the devices below the globally winning device (except Device 30), and last device (Device 30) for Block 3.

The following is the sequence of operation for a single 272-bit SEARCH command (see COMMAND CODES AND PARAMETERS, page 29).

- **Cycle A:** The host ASIC drives the CMDV high and applies SEARCH command code ('10') on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair used for bits [271:136] of the data being searched. DQ[67:0] must be driven with the 68-bit data ([271:204]) to be compared to all locations "0" in the four 68-bit-word page. The CMD[2] signal must be driven to logic '1.'

Note: CMD[2] = 1 signals that the search is a x272-bit search. CMD[8:7] is ignored in this cycle.

- **Cycle B:** The host ASIC continues to drive the CMDV high and applies SEARCH command ('10') on CMD[1:0]. The DQ[67:0] is driven with the 68-bit data ([203:136]) to be compared to all locations '1' in the four 68-bit-word page.
- **Cycle C:** The host ASIC drives the CMDV high and applies SEARCH command code ('10') on CMD[1:0] signals. CMD[5:3] signals must be driven with the index to the GMR pair used for the bits [135:0] of the data being searched. CMD[8:7] signals must be driven with the bits that will be driven by this device on SADR[21:20] if it has a hit. DQ[67:0] must be driven with the 68-bit data ([135:68]) to be compared to all locations "2" in the four 68-bit-word page. The CMD[2] signal must be driven to logic '0.'
- **Cycle D:** The host ASIC continues to drive the CMDV high and continues to apply SEARCH command code ('10') on CMD[1:0]. CMD[8:6] signals must be driven with the index of the SSR that will be used for storing the address of the matching entry and the Hit Flag (see SEARCH-Successful Registers (SSR[0:7]), page 23). The DQ[67:0] is driven with the 68-bit data ([67:0]) to be compared to all locations "3" in the four 68-bit-word page. CMD[5:2] is ignored because the LEARN Instruction is not supported for x272 tables.

Note: For 272-bit searches, the host ASIC must supply four distinct 68-bit data words on DQ[67:0] during Cycles A, B, C, and D. The GMR Index in Cycle A selects a pair of GMRs in each of the 31 devices that apply to DQ data in Cycles A and B. The GMR Index in Cycle C se-

lects a pair of GMRs in each of the 31 devices that apply to DQ data in Cycles C and D.

The logical 272-bit SEARCH operation is as shown in Figure 73, page 103. The entire table of 272-bit entries is compared to a 272-bit word K that is presented on the DQ Bus in Cycles A, B, C, and D of the command using the GMR and local mask bits. The GMR is the 272-bit word specified by the two pairs of GMRs selected by the GMR Indexes in the command's Cycles A and C in each of the 31 devices. The 272-bit word K that is presented on the DQ Bus in Cycles A, B, C, and D of the command is compared to each entry in the table starting at location "0." The first matching entry's location address, "L," is the winning address that is driven as part of the SRAM address on the SADR[21:0] lines (see SRAM ADDRESSING, page 126).

Note: The matching address is always going to be location "0" in a four-entry page for 272-bit search (two LSBs of the matching index will be '00').

The SEARCH command is a pipelined operation and executes a search at one-fourth the rate of the frequency of CLK2X for 272-bit searches in x272-configured tables. The latency of SADR, CE_L, ALE_L, WE_L, SSV, and SSF from the 272-bit SEARCH command (measured in CLK cycles) from the CLK2X cycle that contains Cycles C and D shown in Table 47, page 115.

The latency of a SEARCH from command to SRAM access cycle is 6 for only a single device in the table and TLSZ = 10. In addition, SSV and SSF shift further to the right for different values of HLAT, as specified in Table 48, page 115

The 272-bit SEARCH operation is pipelined and executes as follows:

- Four cycles from the last cycle of the SEARCH command each of the devices knows the outcome internal to it for that operation.
- In the fifth cycle from the SEARCH command, the devices in a block (which is less than or equal to eight devices resolving the winner within them using an LHI[6:0] and LHO[1:0] signalling mechanism) arbitrate for a winner.
- In the sixth cycle after the SEARCH command, the blocks of devices resolve the winning block through a BHI[2:0] and BHO[2:0] signalling mechanism. The winning device within the winning block is the global winning device for the SEARCH operation.

Table 46. Hit/Miss Assumption

Search Number	1	2	3
Block 0	Miss	Miss	Miss
Block 1	Miss	Miss	Hit
Block 2	Miss	Hit	Hit
Block 3	Hit	Hit	Miss

Figure 71. Hardware Diagram for a Table with 31 Devices

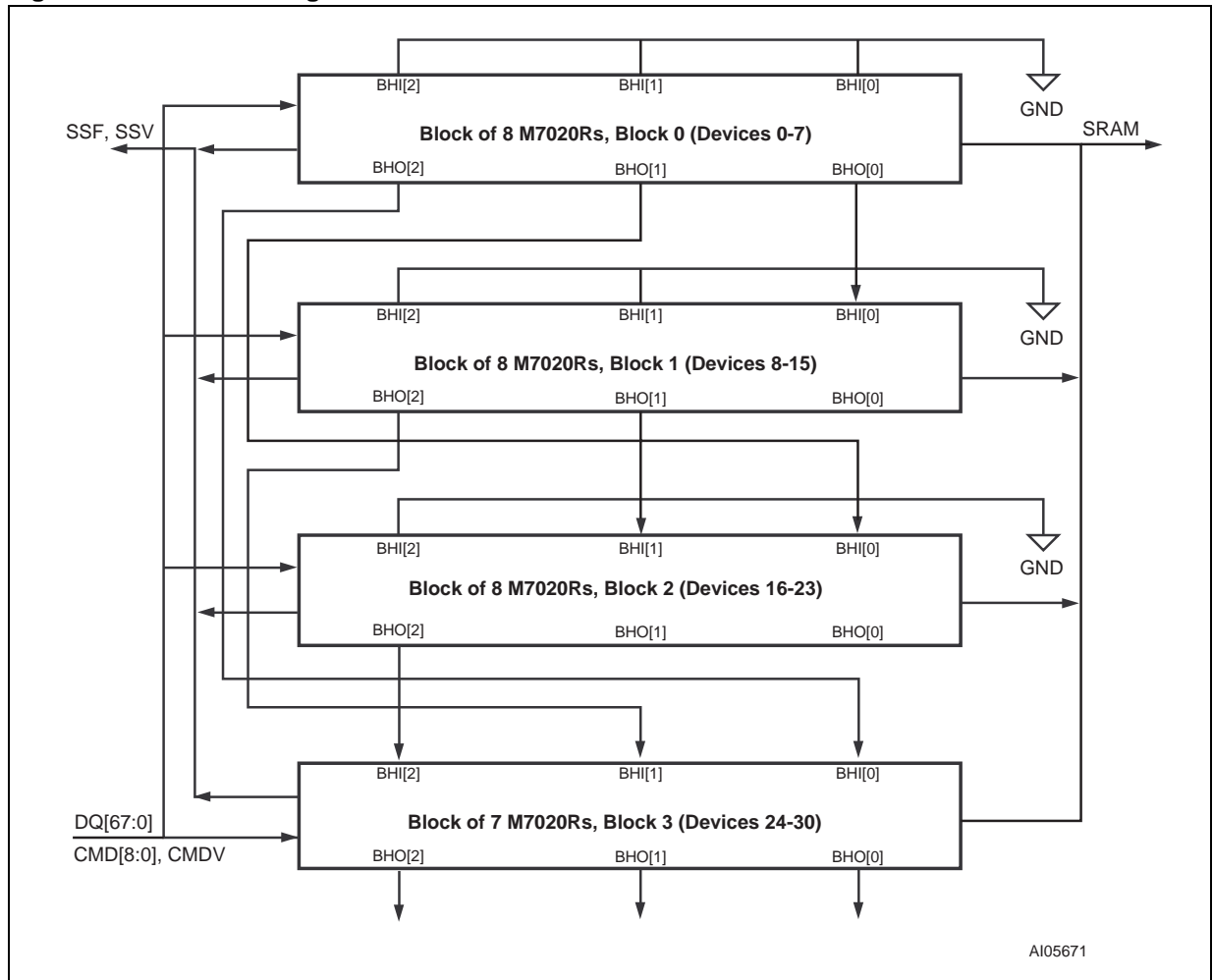


Figure 72. Hardware Diagram for a Block of Up to Eight Devices

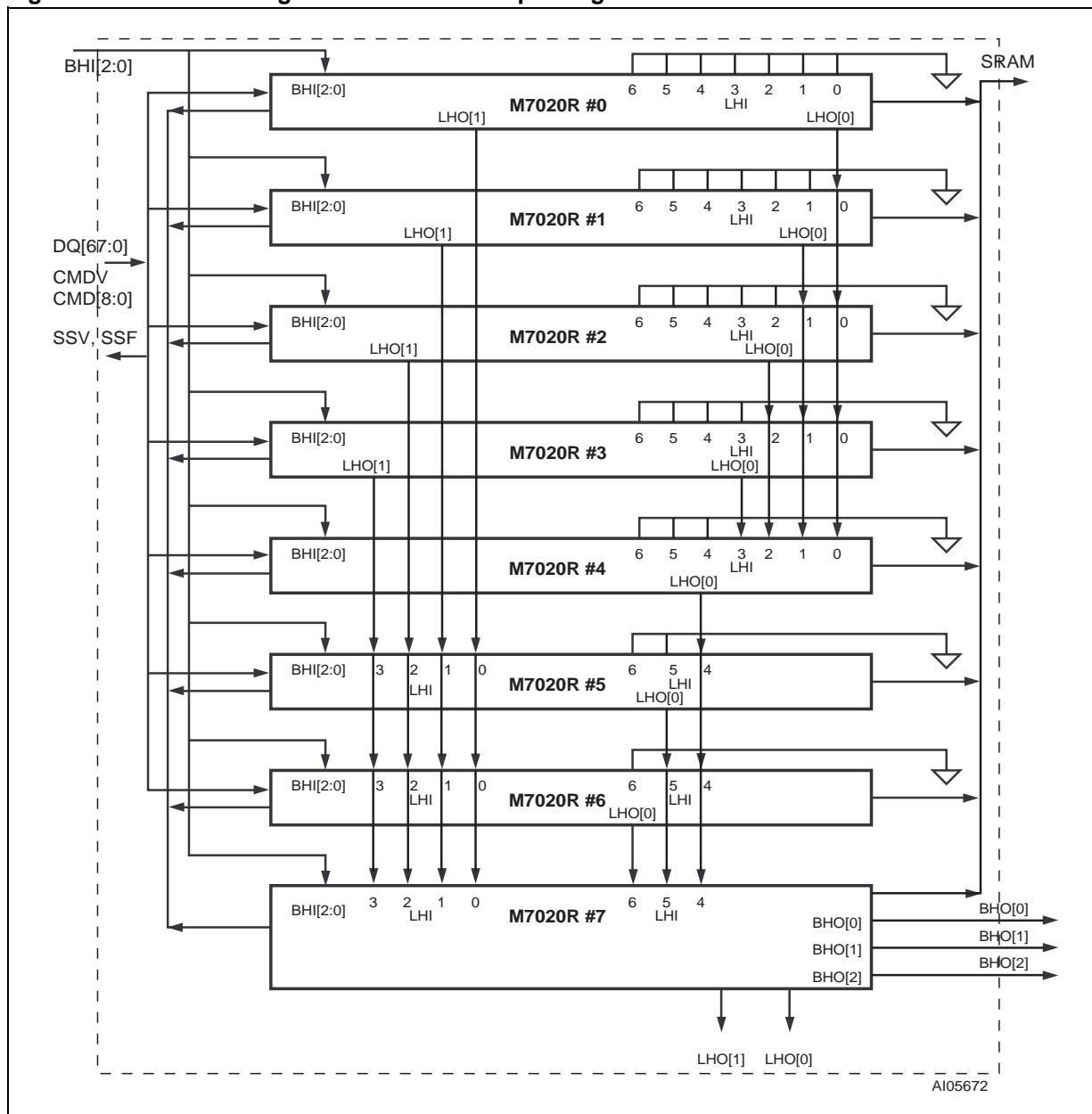
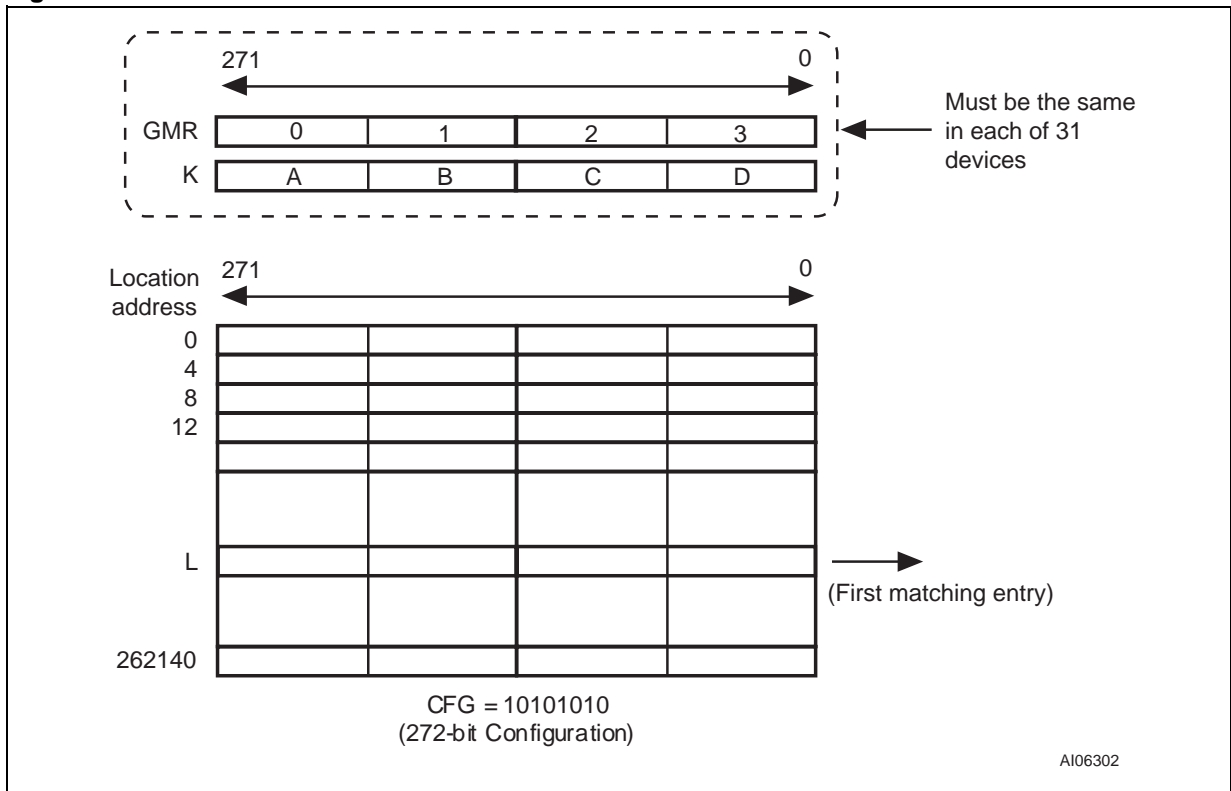
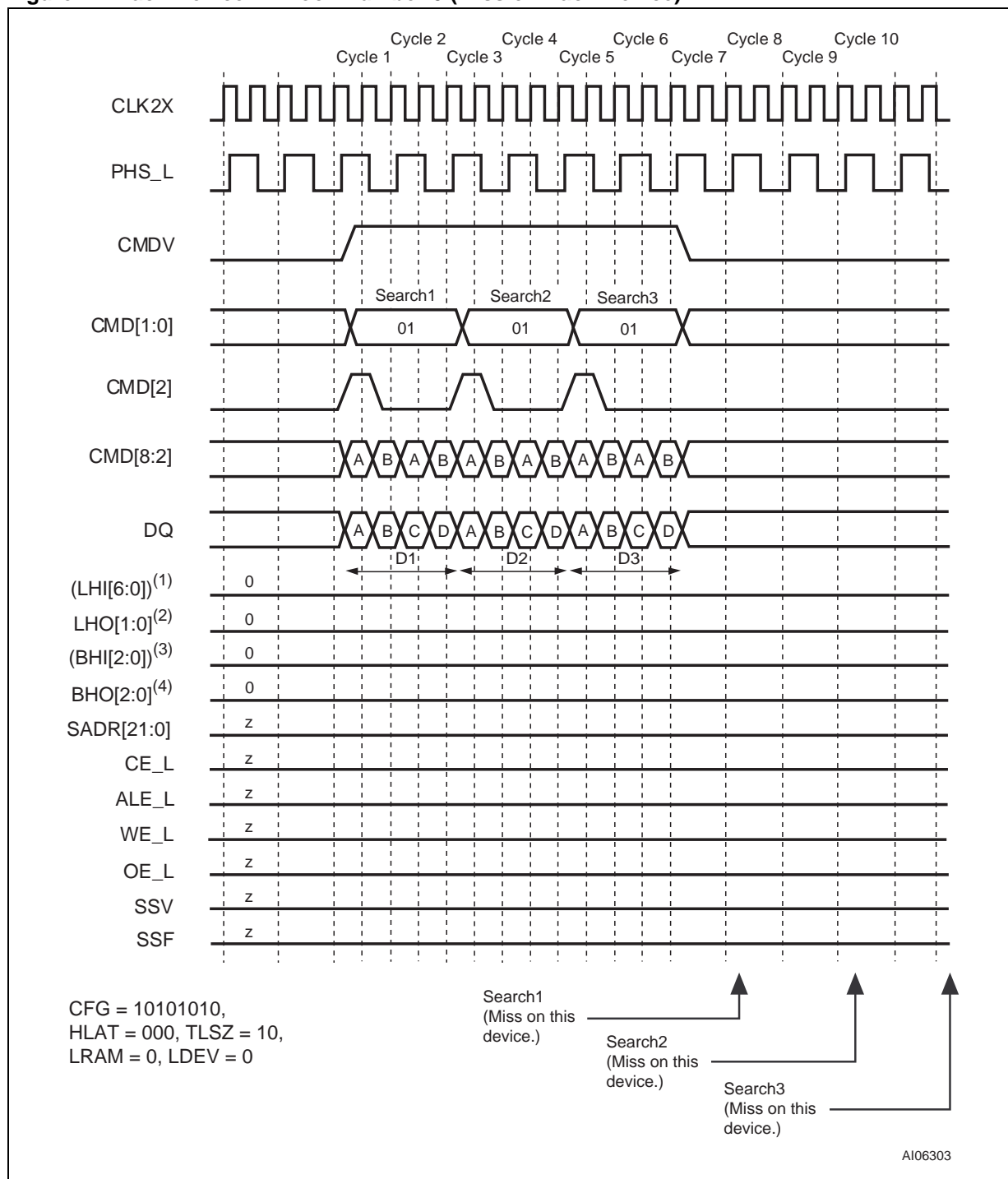


Figure 73. x272 Table with 31 Devices



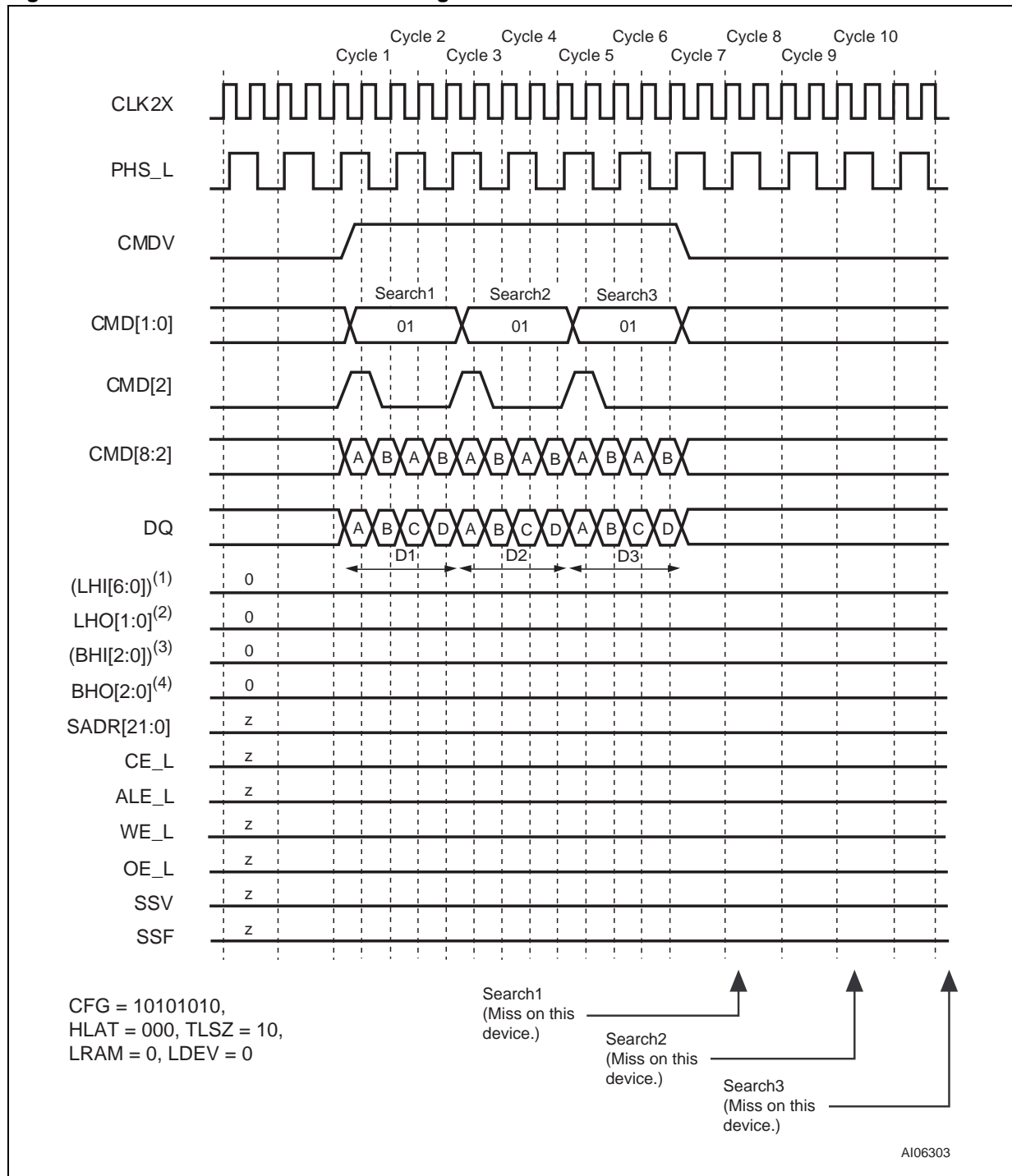
Timing Diagrams for x272 Using Up to 31 M7020R Devices

Figure 74. Each Device in Block Number 0 (Miss on Each Device)



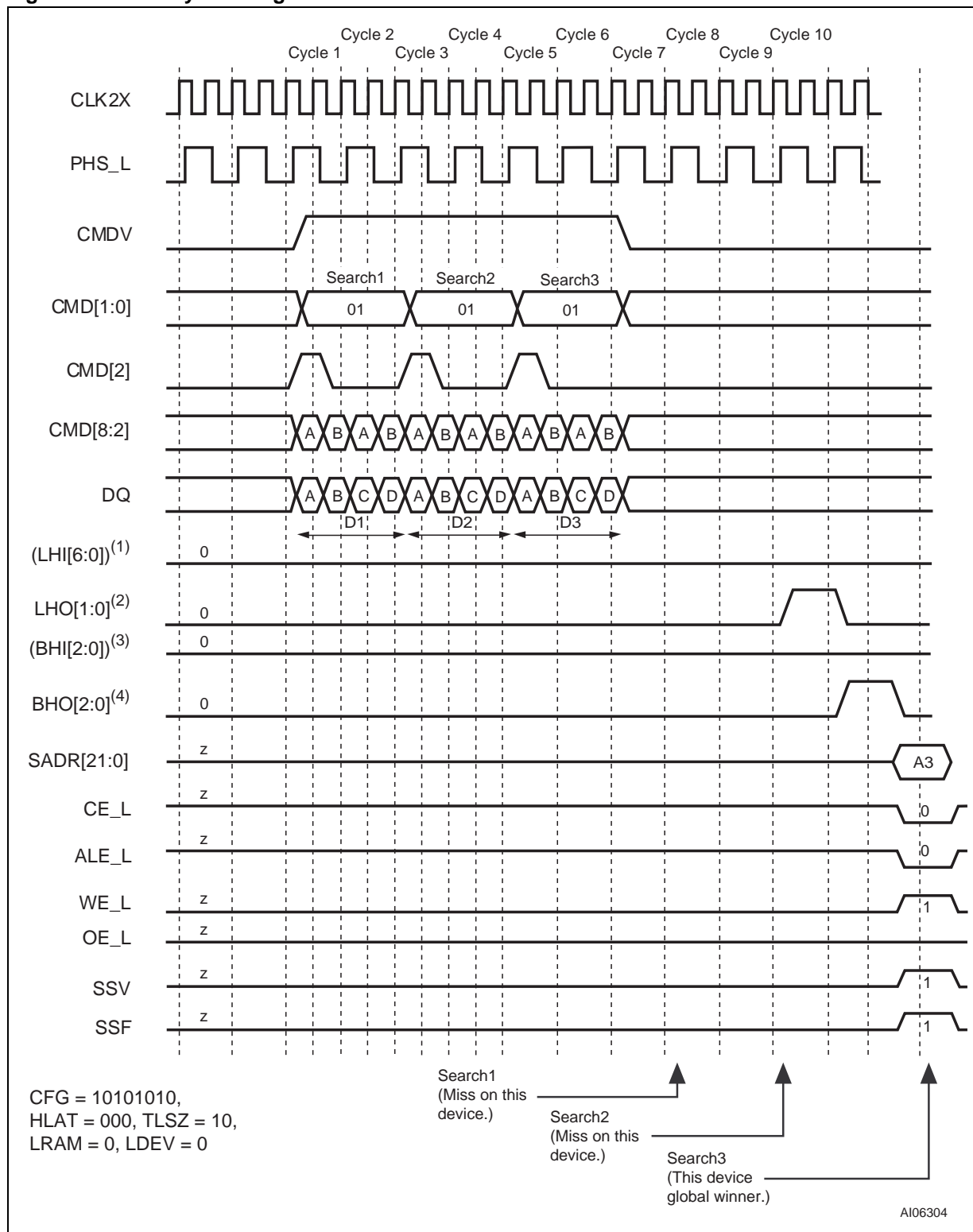
- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 75. Each Device Above the Winning Device in Block Number 1



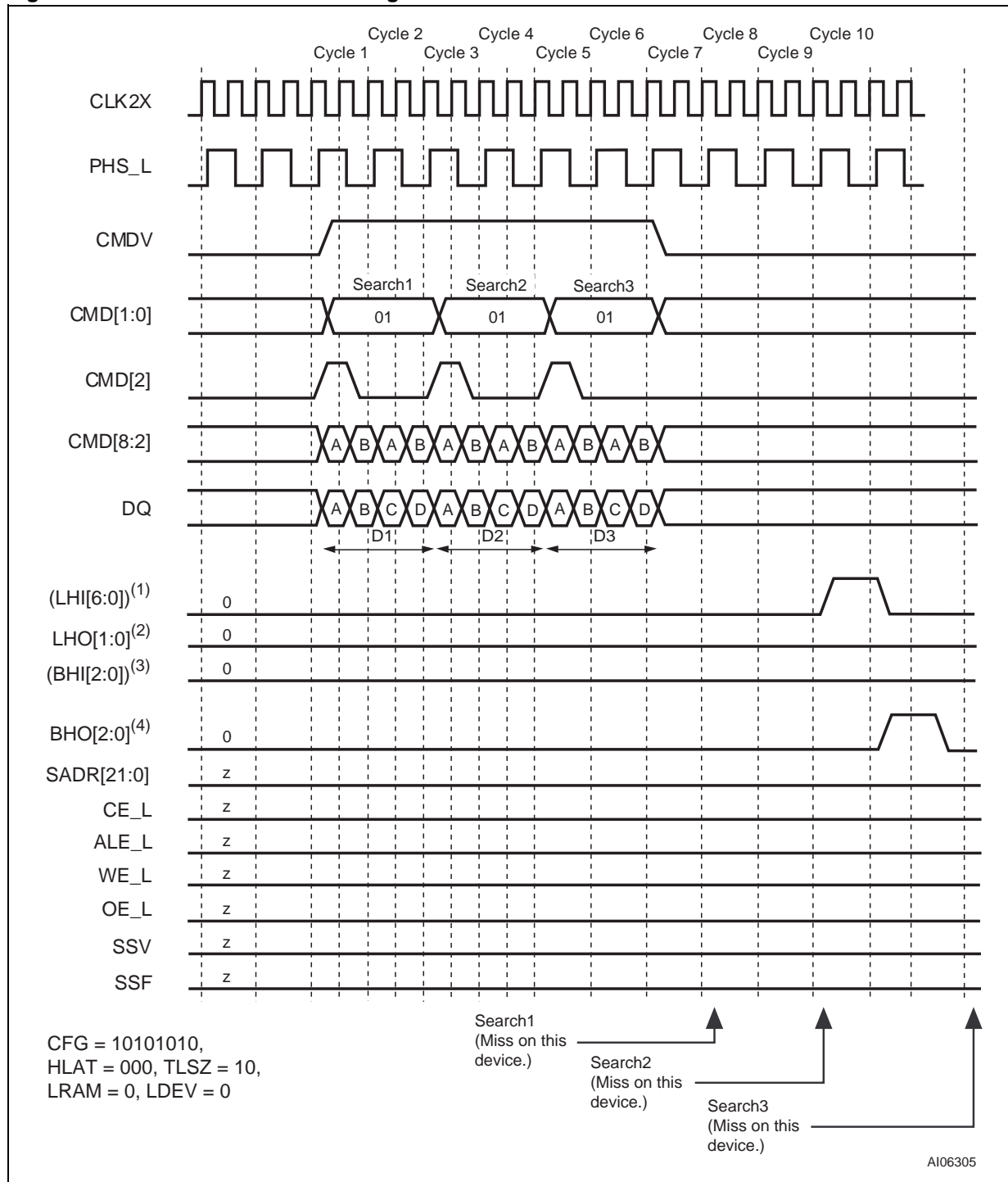
- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 76. Globally Winning Device in Block Number 1



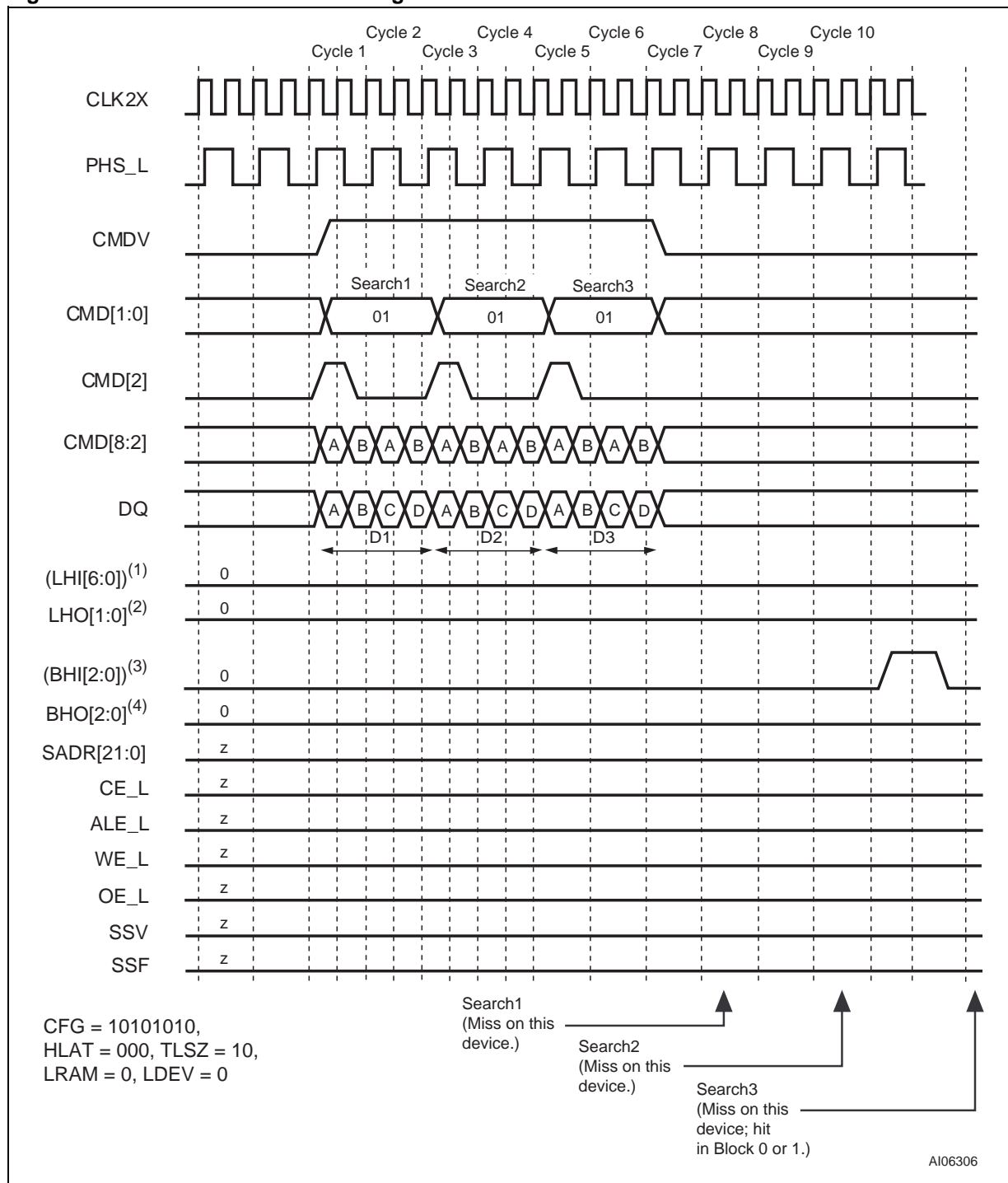
- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 77. Devices Below the Winning Device in Block Number 1



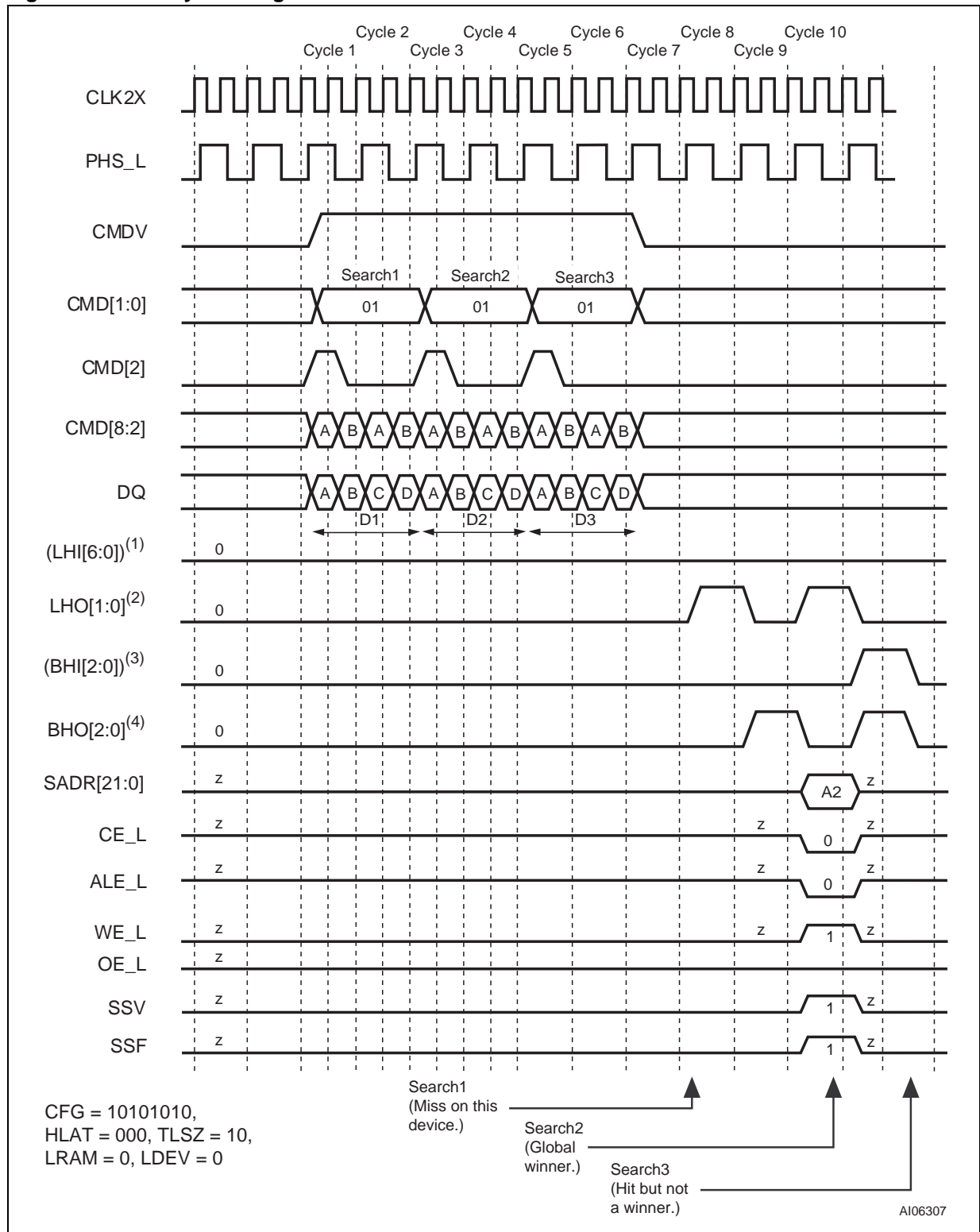
- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 78. Devices Above the Winning Device in Block Number 2



- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

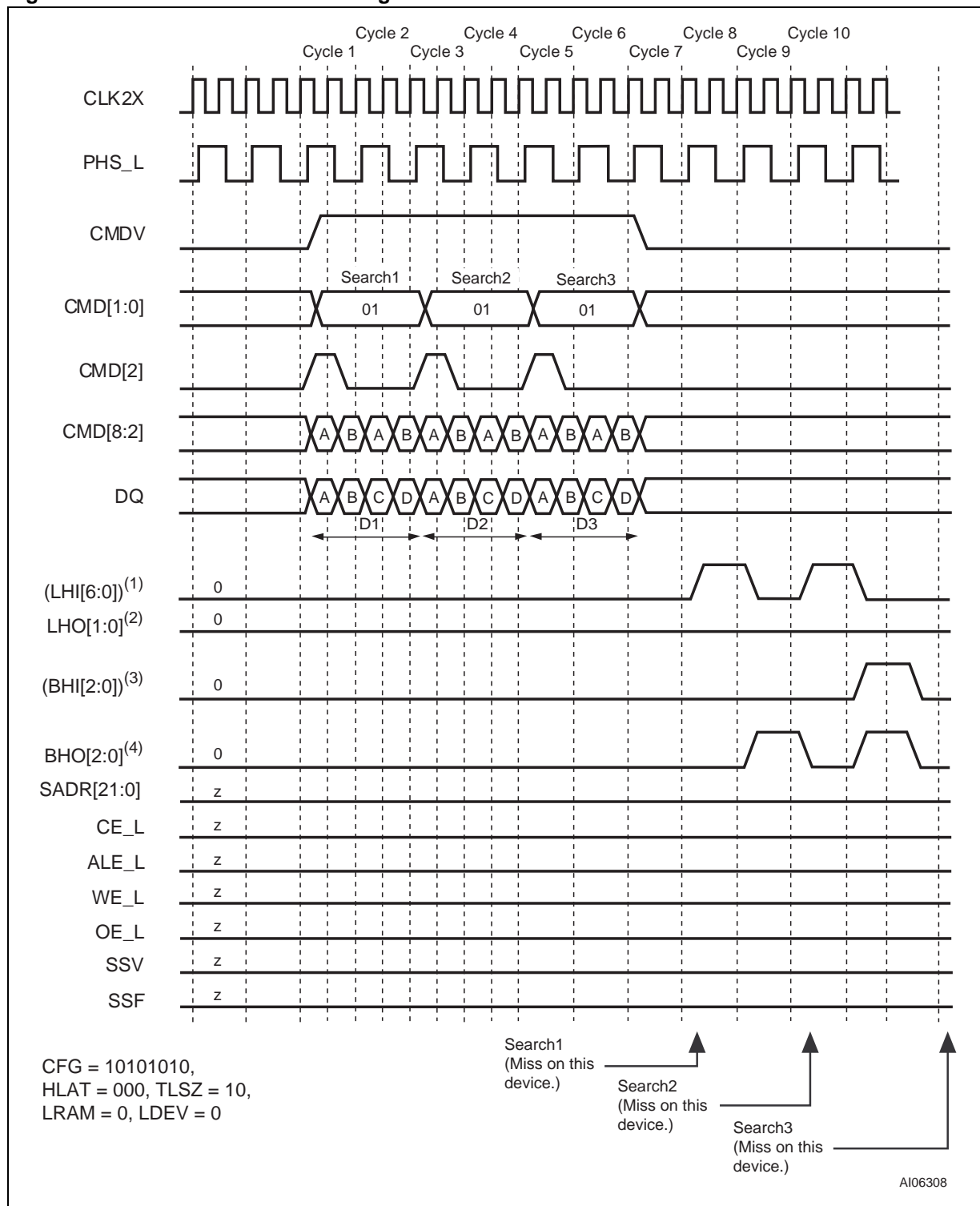
Figure 79. Globally Winning Device in Block Number 2



- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

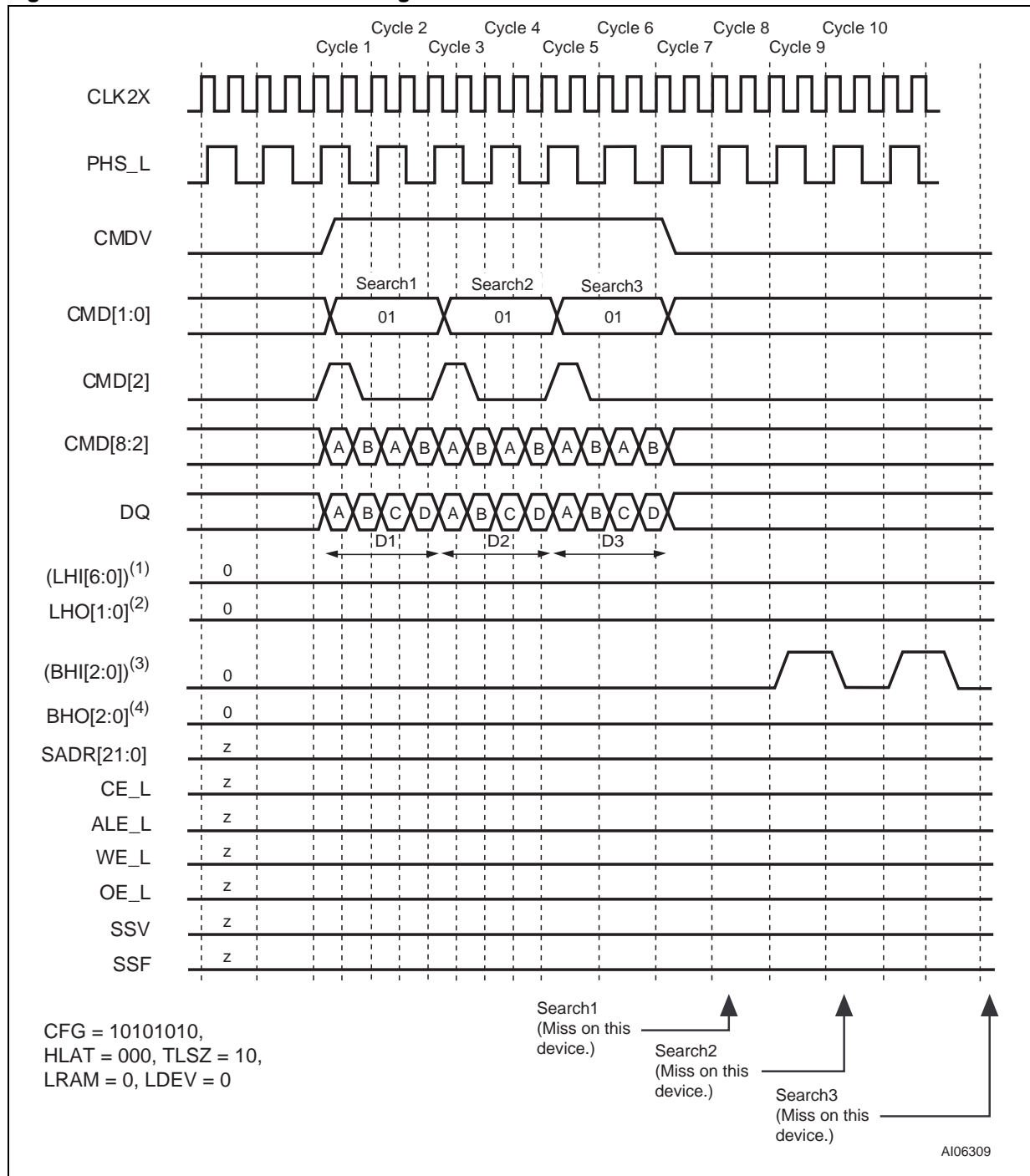


Figure 80. Devices Below the Winning Device in Block Number 2



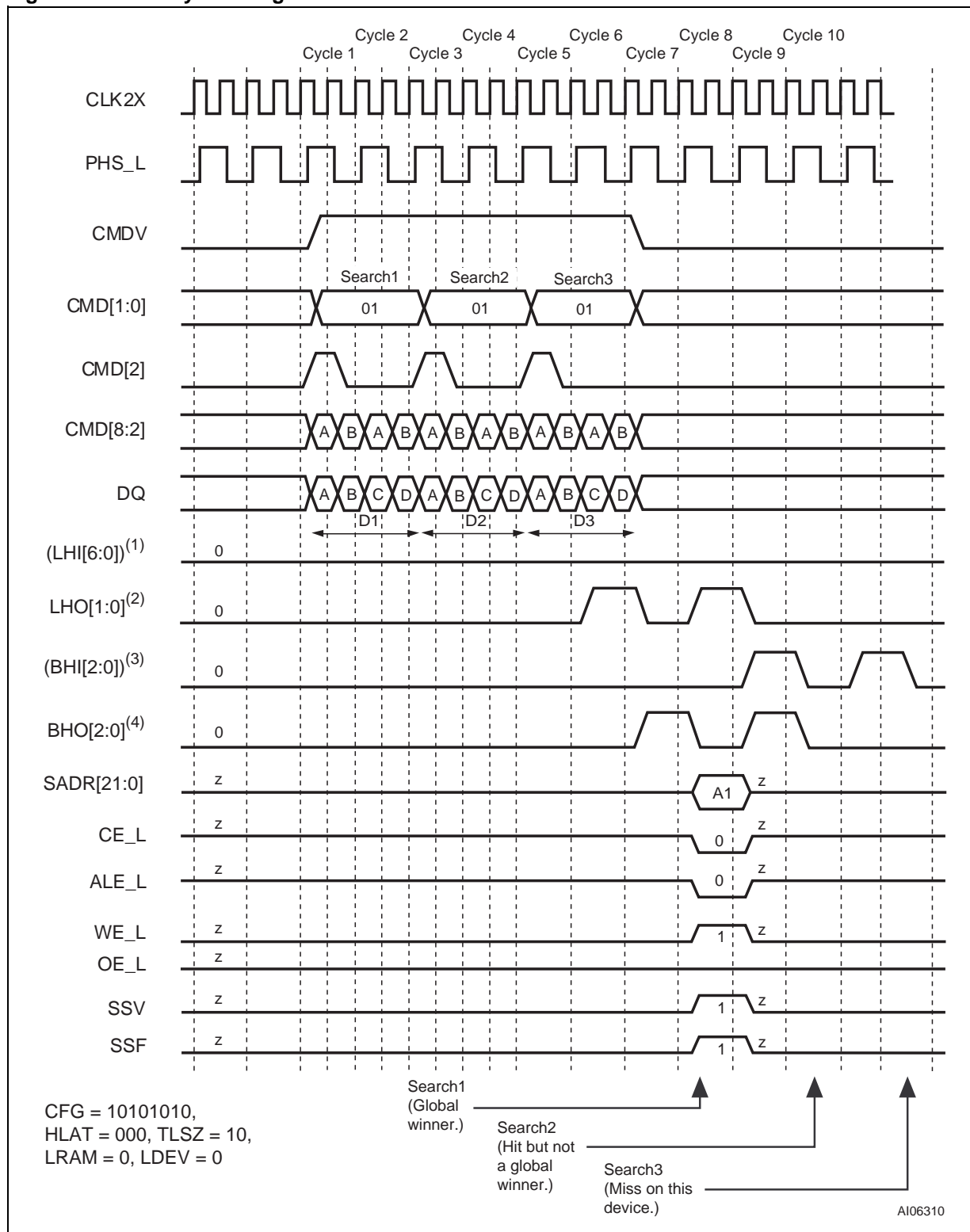
- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 81. Devices Above the Winning Device in Block Number 3



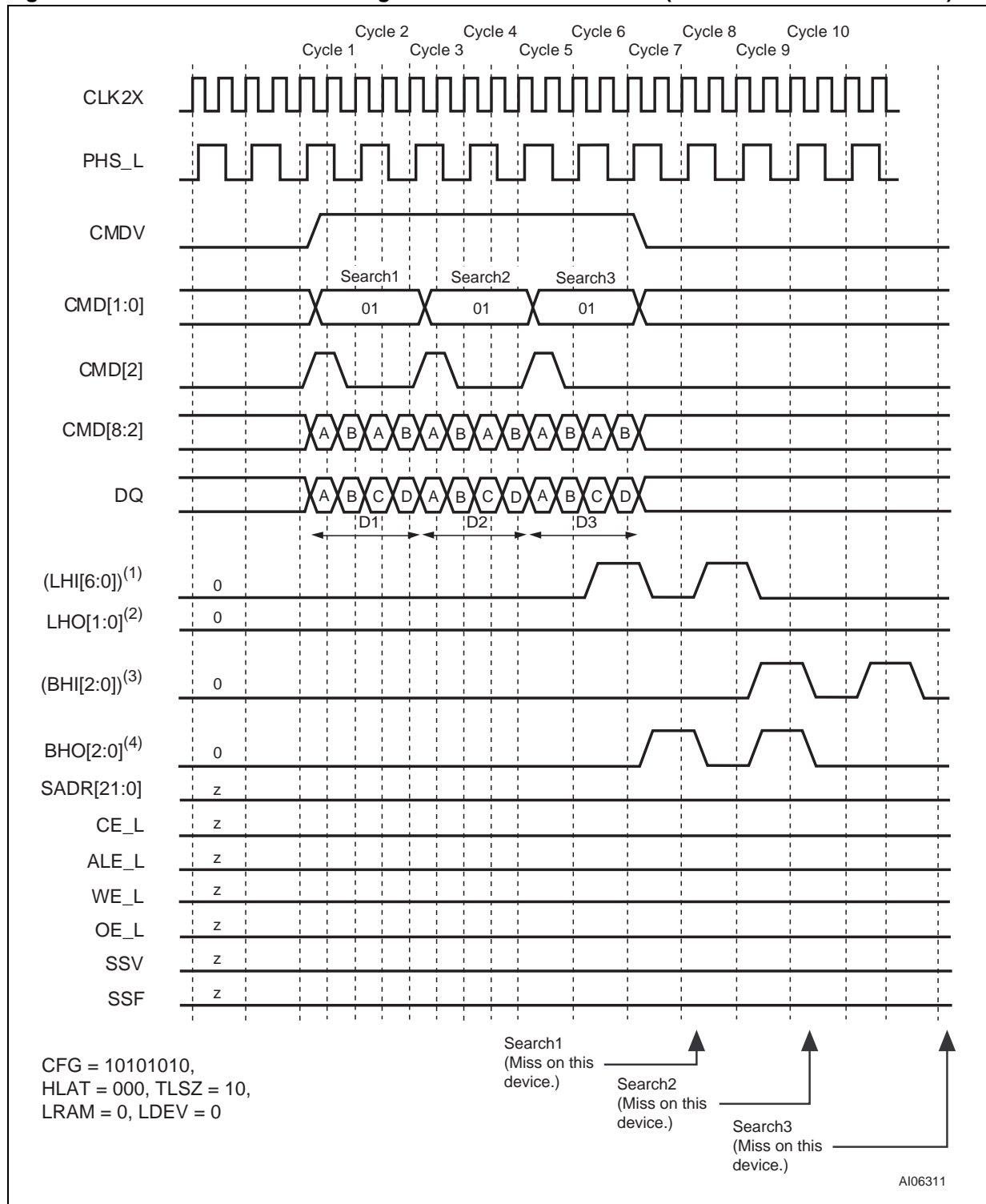
- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 82. Globally Winning Device in Block Number 3



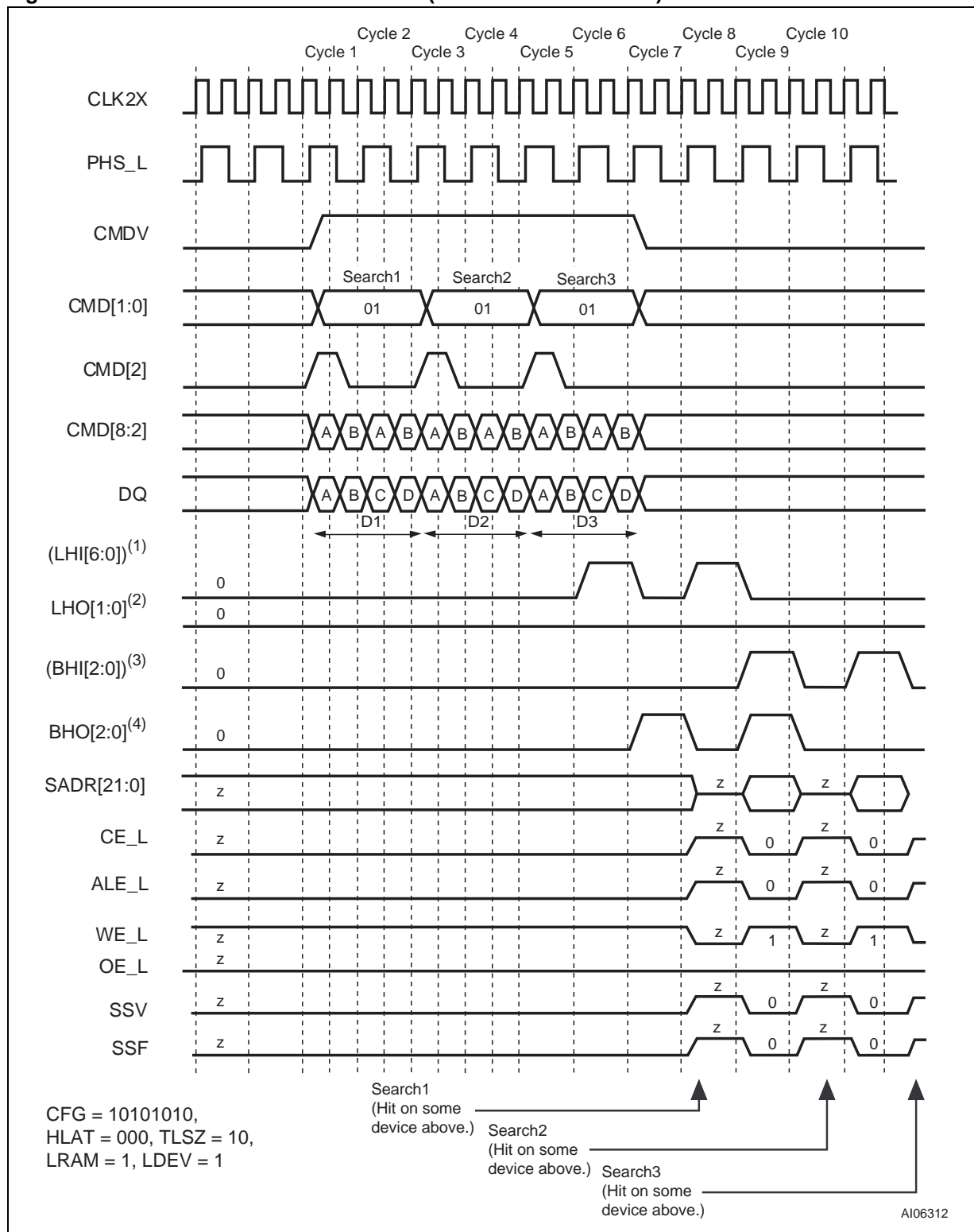
- Note: 1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 83. Devices Below the Winning Device in Block Number 3 (not Device 30 - Last Device)



- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Figure 84. Last Device in Block Number 3 (Device 30 in the Table)



- Note:
1. (LHI[6:0]) stands for the boolean 'OR' of the entire bus LHI[6:0].
 2. Each bit in LHO[1:0] is the same logical signal.
 3. (BHI[2:0]) stands for the boolean 'OR' of the entire bus BHI[2:0].
 4. Each bit in BHO[2:0] is the same logical signal.

Table 47. Latency of SEARCH from Cycles C and D to SRAM Access Cycle, 272-bit, Up to 31 Devices

# of devices	Max Table Size	Latency in CLK Cycles
1 (TLSZ = 00)	8K x 272-bit	4
2–8 (TLSZ = 01)	64K x 272-bit	5
9–31 (TLSZ = 10)	248K x 272-bit	6

Table 48. Shift of SSF and SSV from SADR

HLAT	Number of CLK Cycles
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

MIXED SEARCHES

Tables Configured with Different Widths Using an M7020R

The sample operation shown is for a single device with CFG = 1001000. It contains three tables of x68, x136, and x272 widths. The operation may be generalized to a block of 8–31 devices using four blocks; the timing and the pipeline operation is the same as described previously for fixed searches on a table of one-width-size.

Figure 85, page 116 shows three sequential searches:

- a 68-bit search on the table configured as x68;
- a 136-bit search on a table configured as x136; and
- a 272-bit search on the table configured as x272 bits that each results in a hit.

Note: The DQ[67:66] will be '00' in both of the Cycles A and B of the x68-bit search (Search1). DQ[67:66] is '01' in both of the Cycles A and B of the x136-bit search (Search2). DQ[67:66] is '10' in all of the Cycles A, B, C, and D of the x272-bit search (Search 3). By having table designation bits, the M7020R enables the creation of many tables in a bank of search engines of different widths.

Figure 86, page 117 shows the sample table. Two bits in each 68-bit entry will need to be designated as the Table Number Bits. One example choice can be the '00' values for the table configured as x68, '01' values for tables configured as x136, and '10' values for tables configured as x272. For the above explanation, it is further assumed that bits [67:66] for each entry will be designated as these Table Designation Bits.

Figure 85. Timing Diagram for Mixed SEARCH for One Device

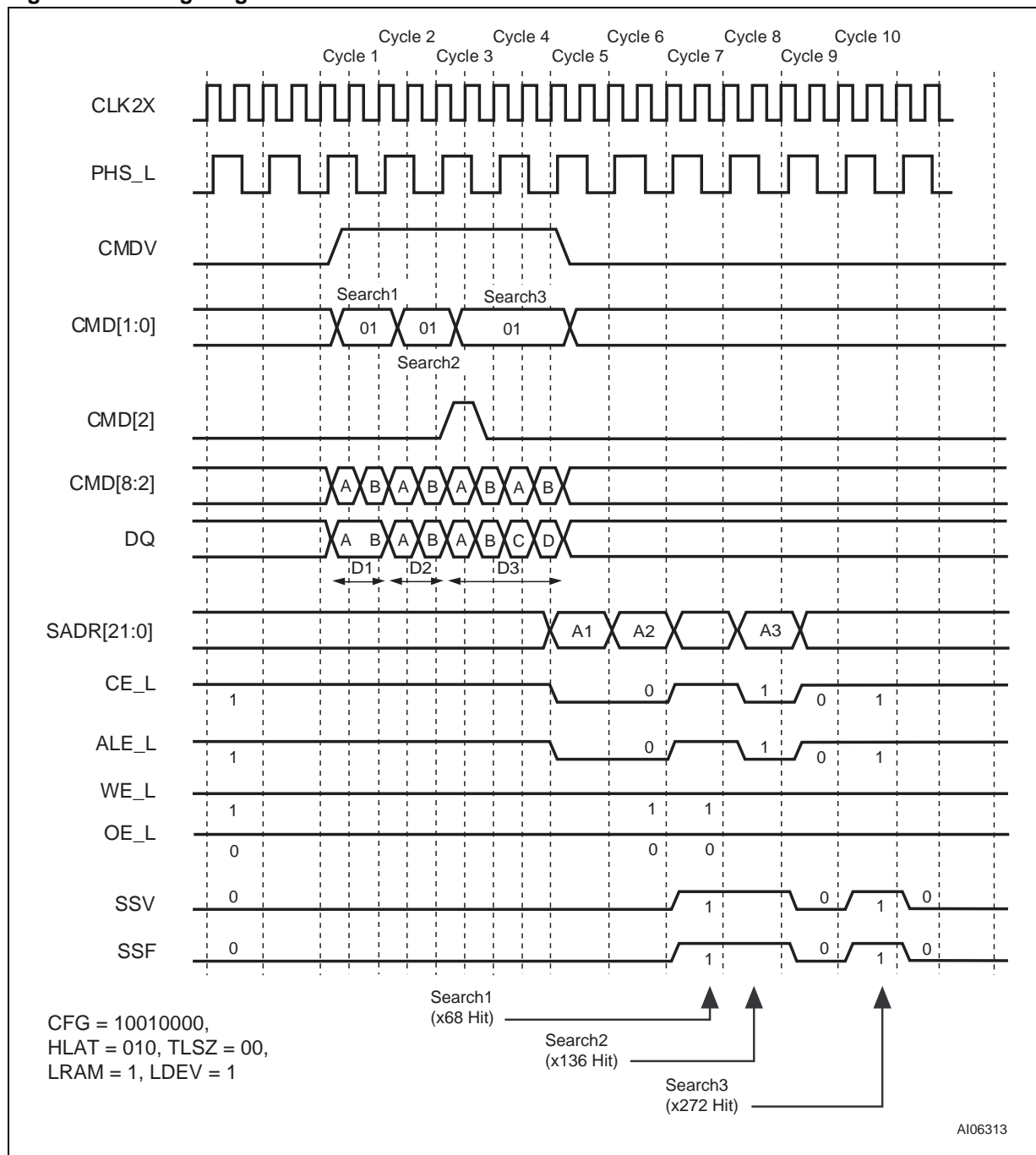
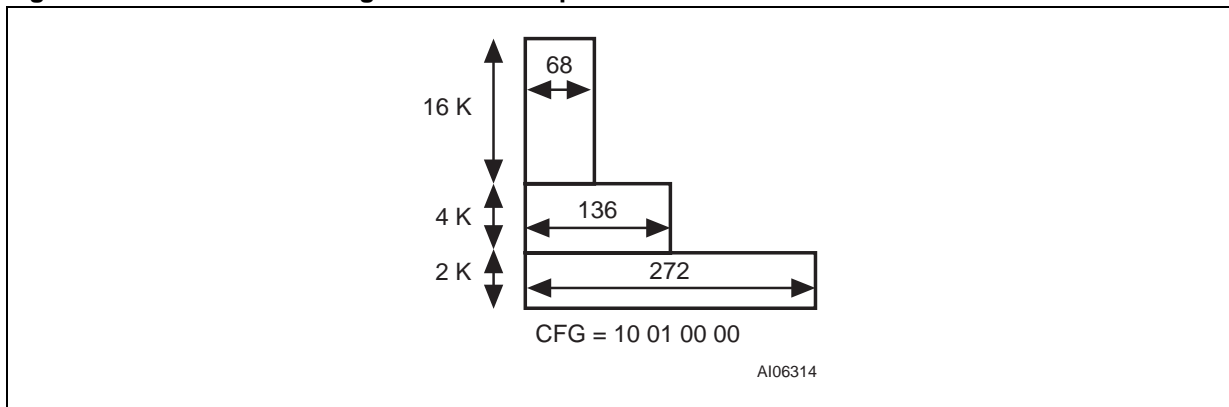


Figure 86. Multi-Width Configurations Example



LRAM AND LDEV DESCRIPTION

When search engines are cascaded using multiple M7020Rs, the SADR, CE_L, and WE_L (3-state signals) are all tied together. In order to eliminate external pull-up and pull-downs, one device in a bank is designated as the default driver. For non-SEARCH or non-LEARN cycles (see LEARN COMMAND in the section below) or search cycles with a global miss, the SADR, CE_L, and WE_L signals are driven by the device with the LRAM Bit set.

Note: It is important that only one device in a bank of search engines that are cascaded have this bit set. Failure to do so will cause contention on SADR, CE_L, WE_L, and can potentially cause damage to the device(s).

Similarly, when search engines using multiple M7020Rs are cascaded, SSF and SSV (also 3-state signals) are tied together. In order to eliminate external pull-up and pull-downs, one device in a bank is designated as the default driver. For non-SEARCH cycles or SEARCH cycles with a global miss the SSF and SSV signals are driven by the device with the LDEV Bit set.

Note: It is important that only one device in a bank of search engines that are cascaded together have this bit set. Failure to do so will cause contention on SSV and SSF and can potentially cause damage to the device(s).

LEARN COMMAND

Bit [0] of each 68-bit data location specifies whether an entry in the database is occupied. If all the entries in a device are occupied, the device asserts FULO signal to inform the downstream devices that it is full.

The result of this communication between depth-cascaded devices determines the global FULL signal for the entire table. The FULL signal in the last device determines the fullness of the depth-cascaded table.

In a depth-cascaded table, only a single device will learn the entry through the application of a LEARN Instruction. The determination of which device is going to learn is based on the FULL and FULO signalling between the devices. The first non-full device learns the entry by storing the contents of the specified comparand registers to the location(s) pointed to by NFA.

In a x68-configured table the LEARN command writes a single 68-bit location. In a x136-configured table the LEARN command writes the next even and odd 68-bit locations. In 136-bit mode, Bit[0] of the even and odd 68-bit locations is '0,' which indicates they are cascaded empty, or '1,' which indicates they are occupied.

The global FULL signal indicates to the Table Controller (the host ASIC) that all entries within a block are occupied and that no more entries can be learned. The M7020R updates the signal after each WRITE or LEARN command to a data array. The LEARN command generates a WRITE cycle to the external SRAM, also using the NFA register as part of the SRAM address (see SRAM ADDRESSING, page 126).

The LEARN command is supported on a single block containing up to eight devices if the table is configured either as a x68 or a x136. The LEARN command is not supported for x272-configured tables.

LEARN is a pipelined operation and lasts for two CLK cycles, as shown in Figure 87, page 119 where TLSZ = 00, and Figure 88, page 120 and Figure 89, page 121 where TLSZ = 01 (which assume the device performing the LEARN operation is not the last device in the table and has its LRAM Bit set to '0.')

Note: The OE_L for the device with the LRAM Bit set goes high for two cycles for each LEARN (one during the SRAM WRITE cycle, and one the cycle before). The latency of the SRAM WRITE cycle from the second cycle of the Instruction is shown in Table 49, page 121.

The sequence of operation is as follows:

- **Cycle 1A:** The host ASIC applies the LEARN Instruction on the CMD[1:0], using CMDV = 1. The CMD[5:2] field specifies the index of the comparand register pair that will be written in the data array in the 136-bit-configured table. For a LEARN in a 68-bit-configured table, the even-numbered comparands specified by this index will be written. CMD[8:7] carries the bits that will be driven on SADR[21:20] in the SRAM WRITE cycle.
- **Cycle 1B:** The host ASIC continues to drive CMDV to '1,' CMD[1:0] to '11,' and CMD[5:2] with the comparand pair index. CMD[6] must be set to '0' if the LEARN is being performed on a 68-bit-configured table, and to '1' if the LEARN is being performed on a 136-bit-configured table.
- **Cycle 2:** The host ASIC drives the CMDV to '0.' At the end of Cycle 2, a new instruction can begin. The latency of the SRAM WRITE is the same as the search to the SRAM READ Cycle. It is measured from the second cycle of the LEARN Instruction.

Figure 87. Timing Diagram of LEARN: TLSZ = 00

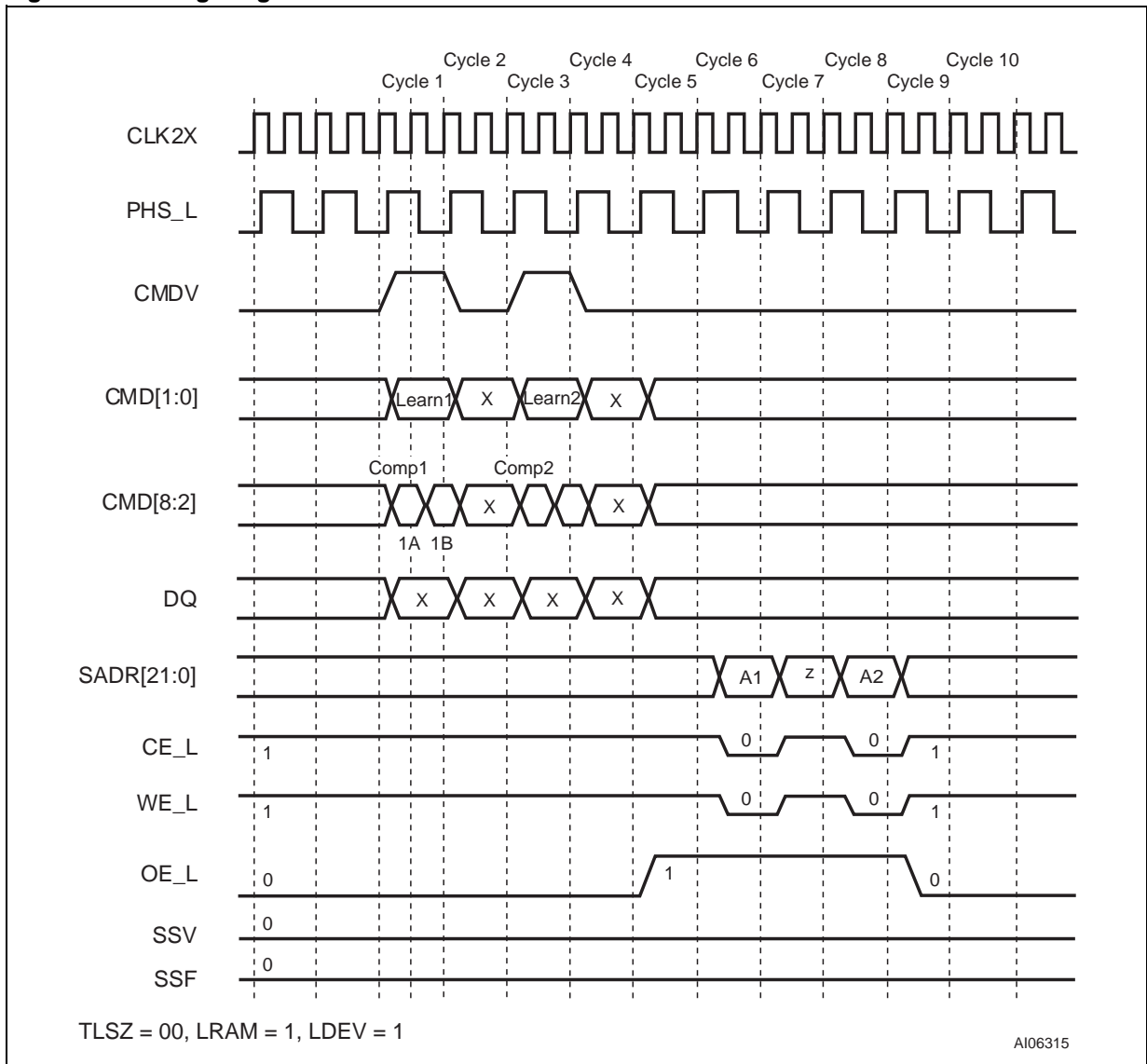


Figure 88. Timing Diagram of LEARN: TLSZ = 01 (Except on the Last Device)

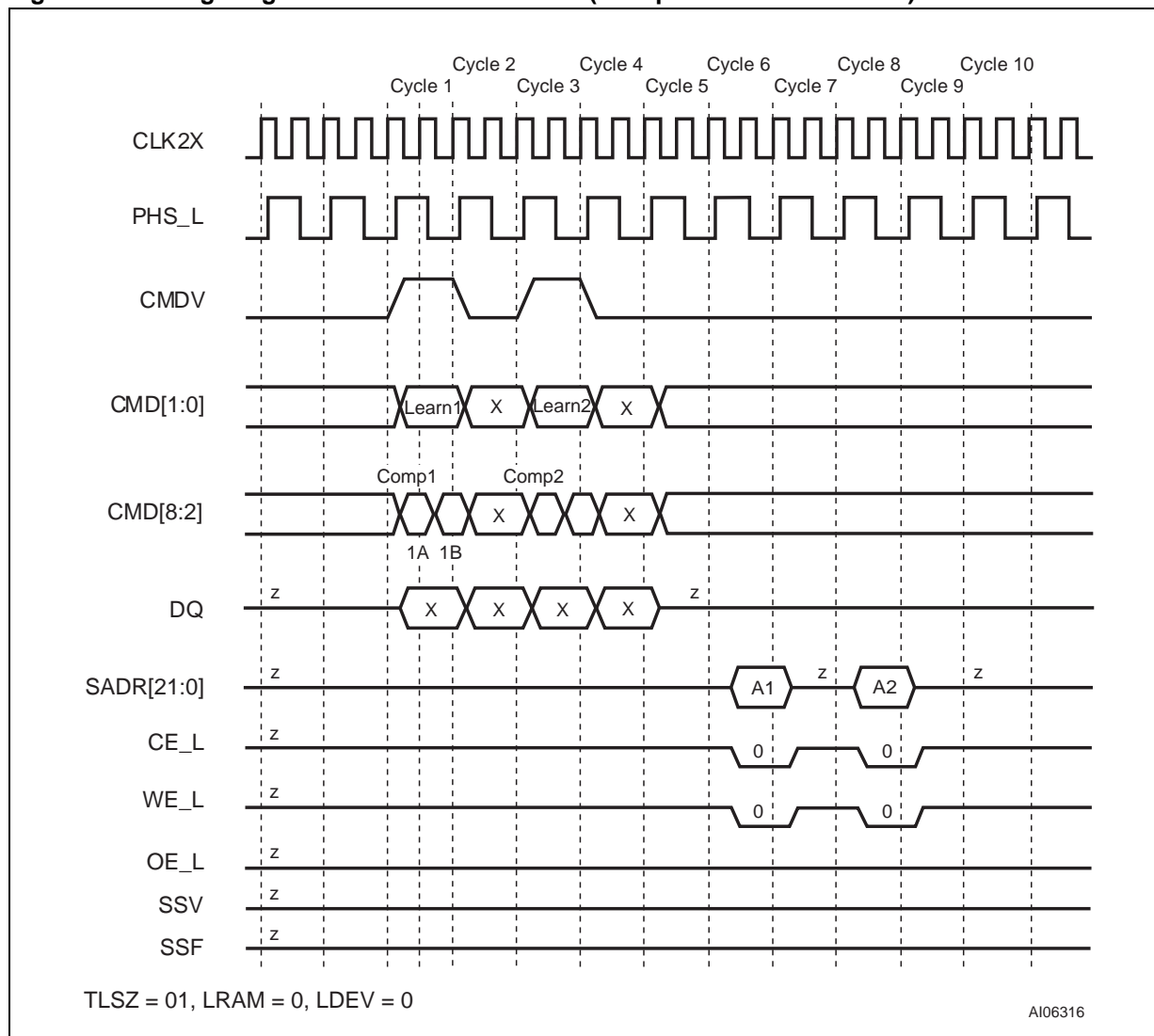


Figure 89. Timing Diagram of LEARN on Device 7: TLSZ = 01

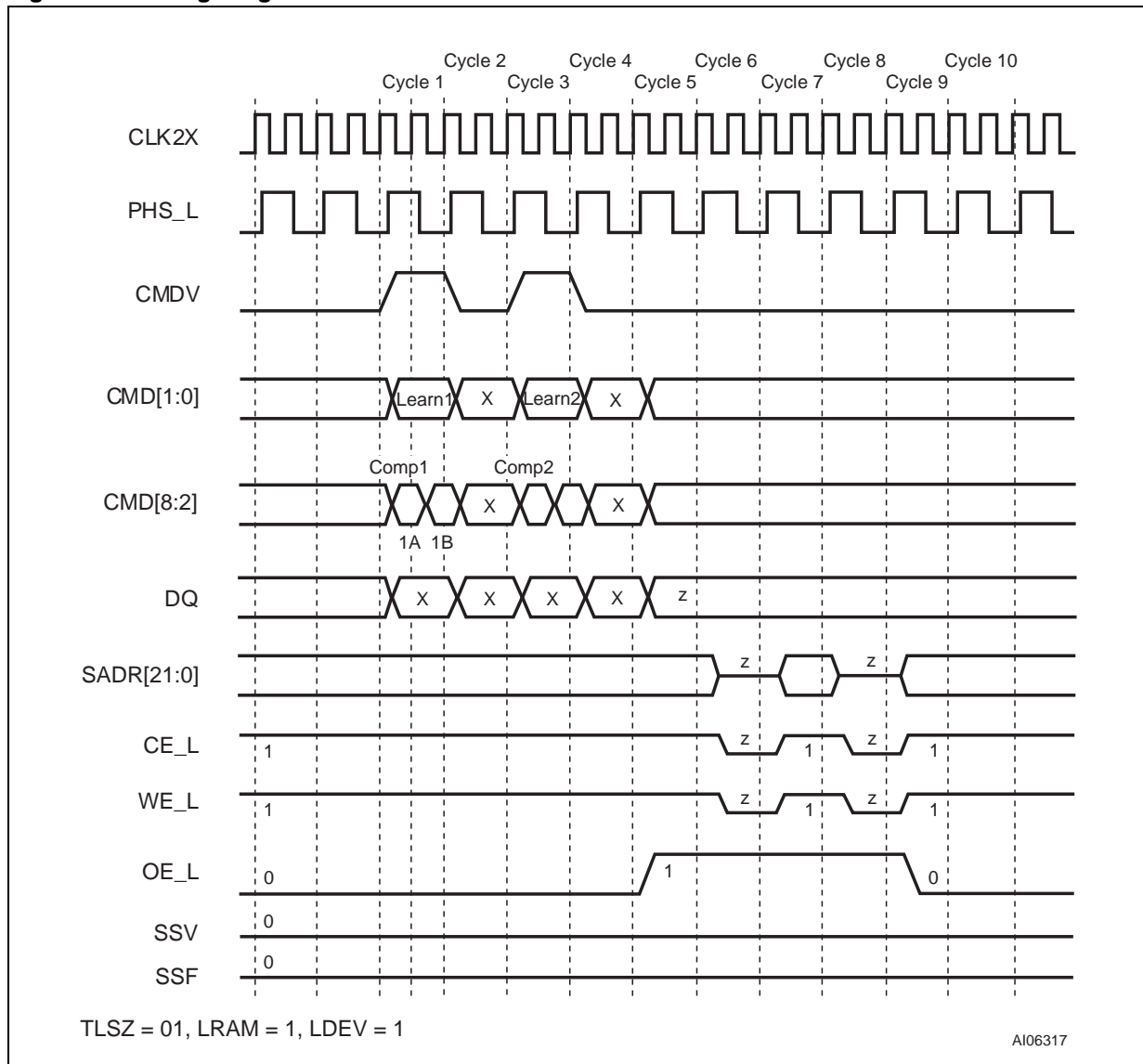


Table 49. Latency of SRAM WRITE Cycle from Second Cycle of LEARN Instruction

# of devices	Latency in CLK Cycles
1 (TLSZ = 00)	4
2-8 (TLSZ = 01)	5
9-31 (TLSZ = 10)	6

DEPTH-CASCADING

The search engine application can depth-cascade the device to various table sizes of different widths (e.g., 68-bit, 136-bit, and 272-bit configurations). The devices perform all the necessary arbitration to decide which device drives the SRAM Bus. The latency of the searches increases as the table size increases while the search rate remains constant.

Depth-Cascading Up to Eight Devices (One Block)

Figure 90, page 123 shows how up to eight devices can cascade to form a 256K x68, 128K x136, or 64K x272 bit table. It also shows the interconnection between the devices for depth-cascading. Each Search Engine asserts the LHO[1] and LHO[0] signals to inform downstream devices of its result. The LHI[6:0] signals for a device are connected to LHO signals of the upstream devices. The host ASIC must program the TLSZ to '01' for each of up to eight devices in a block. Only a single device drives the SRAM Bus in any single cycle.

Depth-Cascading Up to 31 Devices (4 Blocks)

Figure 91, page 124 shows how to cascade up to four blocks. Each block contains up to eight M7020Rs (except the last block) and the interconnection within each is shown in Figure 90, page 123.

Note: The interconnection between blocks for depth-cascading is important. For each SEARCH, a block asserts BHO[2], BHO[1], and BHO[0]. The BHO[2:0] signals for a block are the signals taken only from the last device in the block. For all other

devices within that block, these signals stay open and floating. The host ASIC must program the table size (TLSZ) field to '10' in each of the devices for cascading up to 31 devices (in up to four blocks).

Depth-Cascading to Generate a "FULL" Signal

Bit[0] of each of the 68-bit entries is designated as a special bit (1 = occupied; 0 = empty). For each LEARN or PIO WRITE to the data array, each device asserts FULO[1] and FULO[0] if it does not have any empty locations (see Figure 92, page 125).

Each device combines the FULO signals from the devices above it with its own "full" status to generate a FULL signal that gives the "full" status of the table up to the device asserting the FULL signal. Figure 92, page 125 shows the hardware connection diagram for generating the FULL signal that goes back to the ASIC. In a depth-cascaded block of up to eight devices, the FULL signal from the last device should be fed back to the ASIC controller to indicate the fullness of the table. The FULL signal of the other devices should be left open.

Note: The LEARN instruction is supported for only up to eight devices, whereas FULL cascading is allowed only for one block in tables containing more than eight devices. In tables for which a LEARN Instruction is not going to be used, the Bit[0] of each 68-bit entry should always be set to '1.'

Figure 90. Depth-Cascading to Form a Single Block

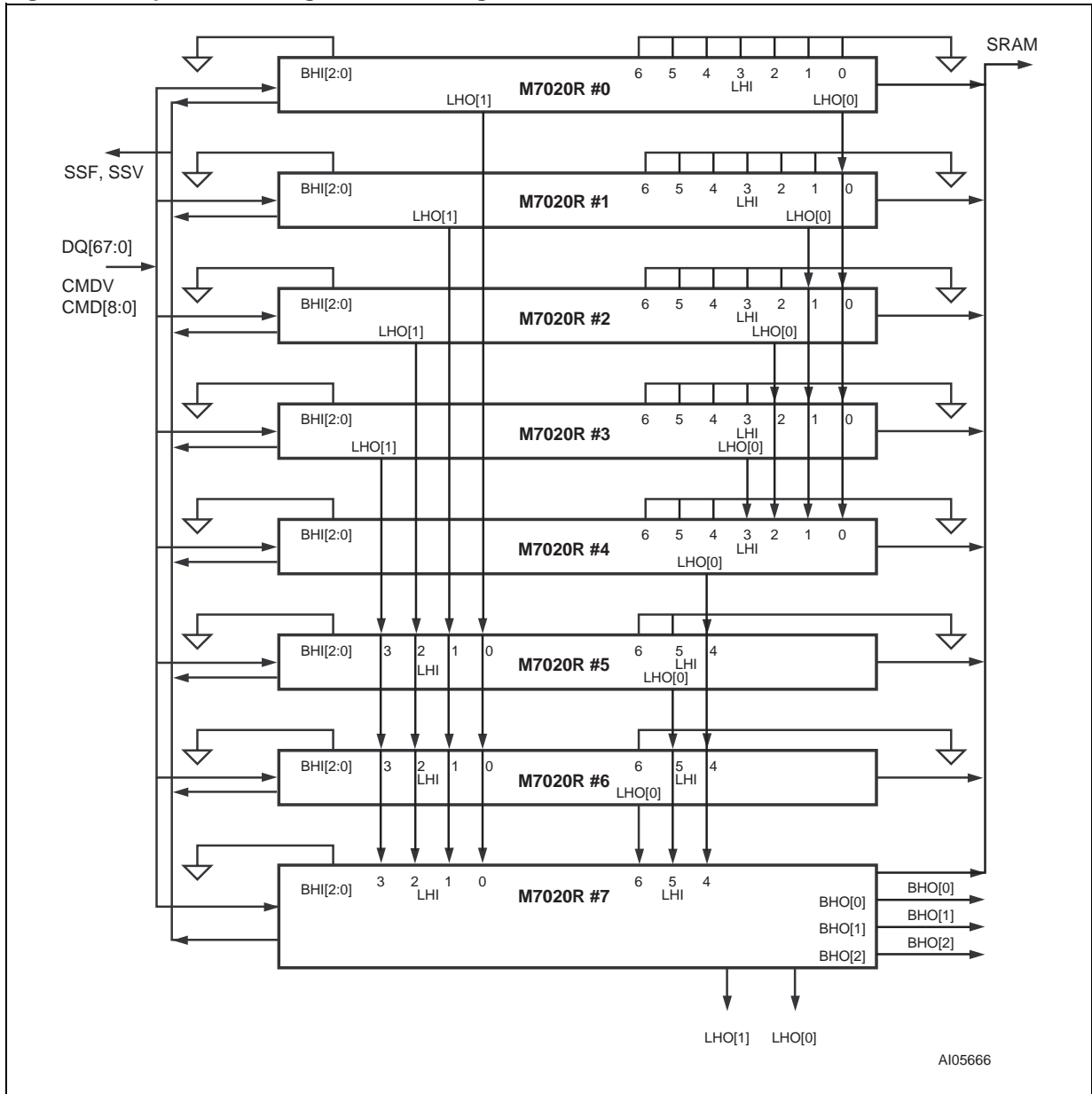


Figure 91. Depth-Cascading Four Blocks

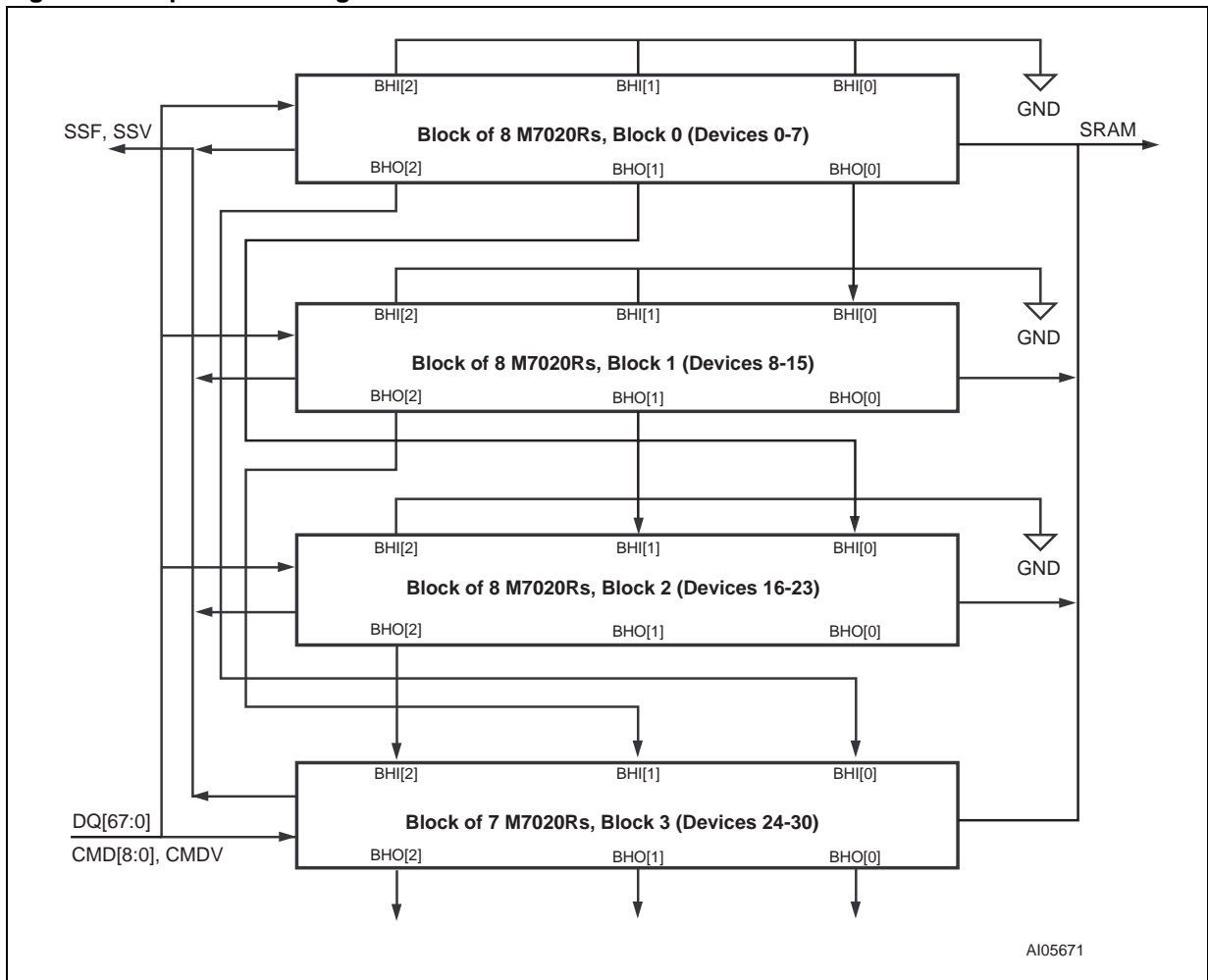
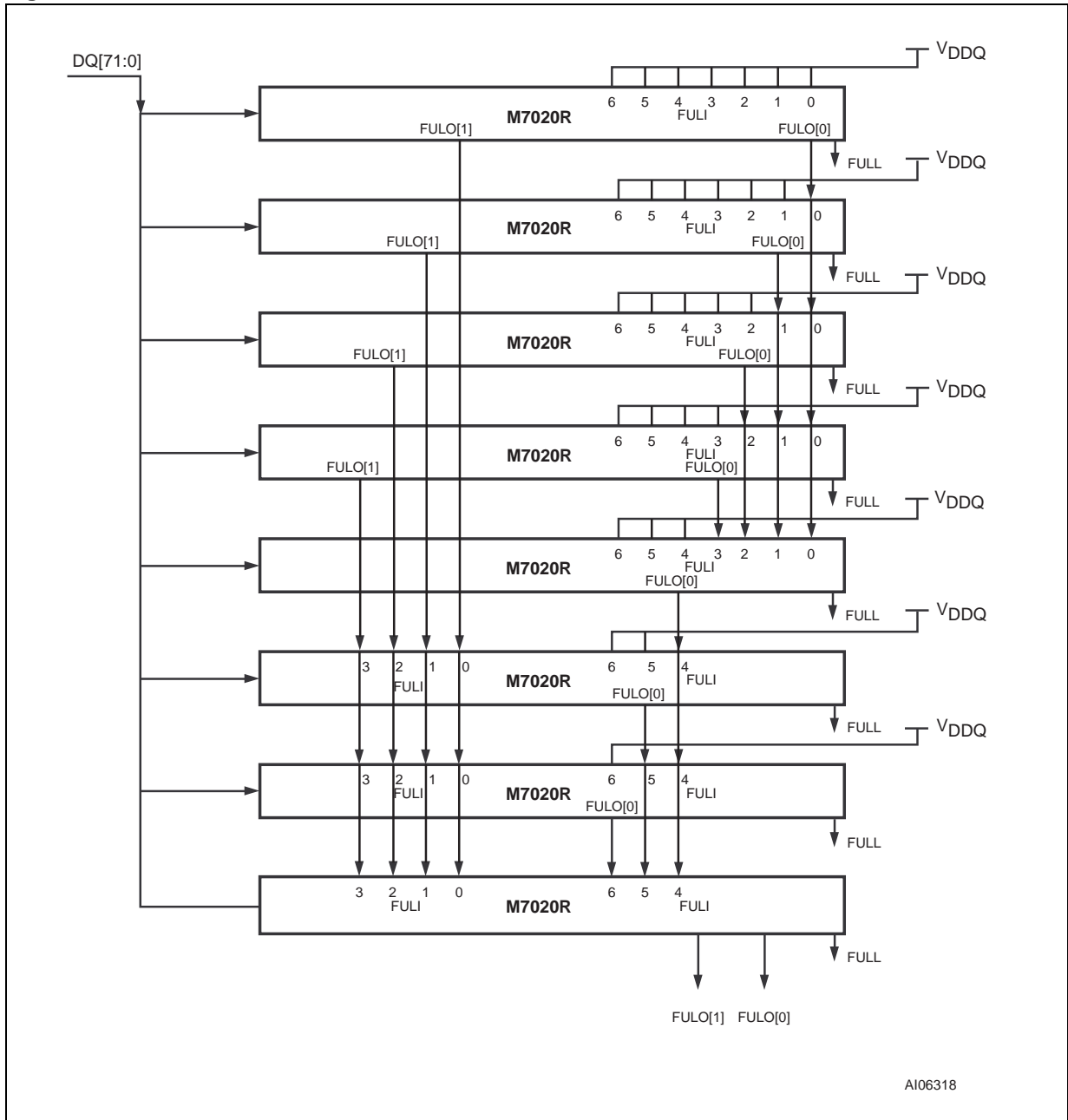


Figure 92. "FULL" Generation in a Cascaded Table



SRAM ADDRESSING

Table 50, page 127 describes the commands used to generate addresses on the SRAM Address Bus. The index [14:0] field contains the address of a 68-bit entry that results in a hit in 68-bit-configured quadrant. It is the address of the 68-bit entry that lies at the 136-bit page, and the 272-bit page boundaries in 136-bit- and 272-bit-configured quadrants, respectively.

REGISTERS, page 21 of this specification, describes the NFA and SSR Registers. ADR[14:0] contains the address supplied on the DQ Bus during PIO access to the M7020R. Command Bits 8 and 7 {CMD[8:7]} are passed from the command to the SRAM Address Bus (see COMMAND CODES AND PARAMETERS, page 29 for more information). ID[4:0] is the ID of the device driving the SRAM Bus (see Figure 3, page 10 and Table 2, page 9 for more information).

SRAM PIO Access

SRAM READ enables READ access to off-chip SRAM that contains associative data. The latency from the issuance of the READ Instruction to the address appearing on the SRAM Bus is the same as the latency of the SEARCH Instruction and will depend on the TLSZ value parameter programmed in the device Configuration Register. The latency of the ACK from the READ Instruction is the same as the latency of the SEARCH Instruction to the SRAM address plus the HLAT programmed in the Configuration Register.

Note: SRAM READ is a blocking operation – no new instruction can begin until the ACK is returned by the selected device performing the access.

SRAM WRITE enables WRITE access to the off-chip SRAM containing associative data. The latency from the second cycle of the WRITE Instruction to the address appearing on the SRAM Bus is the same as the latency of the SEARCH Instruction and will depend on the TLSZ value parameter programmed in the device Configuration Register.

Note: SRAM WRITE is a pipelined operation – new instruction can begin right after the previous command has ended.

SRAM READ with a Table of One Device

SRAM READ enables READ access to the off-chip SRAM containing associative data. The latency from the issuance of the READ Instruction to

the address appearing on the SRAM Bus is the same as the latency of the SEARCH Instruction and will depend on the TLSZ value parameter programmed in the device configuration register. The latency of the ACK from the READ Instruction is the same as the latency of the SEARCH Instruction to the SRAM address plus the HLAT programmed in the configuration register.

The following explains the SRAM READ operation in a table with only one device that has the following parameters: TLSZ = 00, HLAT = 000, LRAM = 1, and LDEV = 1. Figure 93, page 127 shows the associated timing diagram.

For the following description, the selected device refers to the only device in the table because it is the only device to be accessed.

The sequence of the operation is as follows:

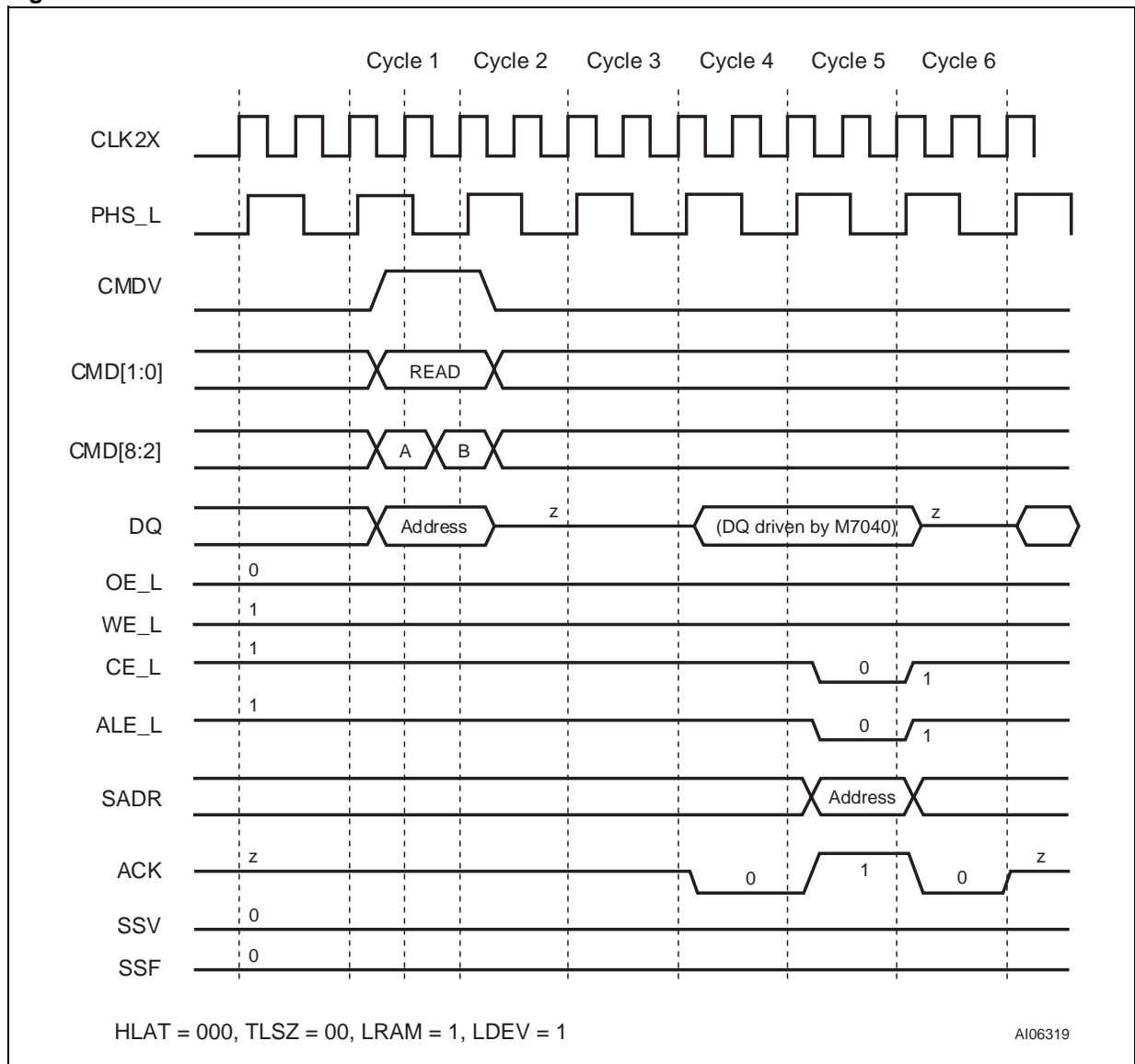
- **Cycle 1A:** The host ASIC applies the READ Instruction on the CMD[1:0], using CMDV = 1. The DQ Bus supplies the address with DQ[20:19] set to '10' to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. During this cycle, the host ASIC also supplies SADR[21:20] on CMD[8:7] in this cycle.
- **Cycle 1B:** The host ASIC continues to apply the READ Instruction on the CMD[1:0] using CMDV = 1. The DQ Bus supplies the address with DQ[20:19] set to '10' to select the SRAM address.
- **Cycle 2:** The host ASIC floats DQ[67:0] to a 3-state condition.
- **Cycle 3:** The host ASIC keeps DQ[67:0] in a 3-state condition.
- **Cycle 4:** The selected device starts to drive DQ[67:0] and drives ACK from High-Z to low.
- **Cycle 5:** The selected device drives the READ address on SADR[21:0]; it also drives ACK high, CE_L low, and ALE_L low.
- **Cycle 6:** The selected device drives CE_L high, ALE_L high, the SADR Bus, and the DQ Bus in a 3-state condition; it drives ACK low.

At the end of Cycle 6, the selected device floats ACK in a 3-state condition, and a new command can begin.

Table 50. Generating an SRAM Bus Address

Command	SRAM Operation	21	20	[19:15]	[14:0]
SEARCH	READ	C8	C7	ID[4:0]	Index[14:0]
LEARN	WRITE	C8	C7	ID[4:0]	NFA[14:0]
PIO READ	READ	C8	C7	ID[4:0]	ADR[14:0]
PIO WRITE	WRITE	C8	C7	ID[4:0]	ADR[14:0]
Indirect Access	WRITE/READ	C8	C7	ID[4:0]	SSR[14:0]

Figure 93. SRAM READ Access for One Device



SRAM READ with a Table of Up to Eight Devices

The following explains the SRAM READ operation completed through a table of up to eight devices using the following parameters: TLSZ = 01. Figure 94, page 129 diagrams a block of eight devices.

The following assumes that SRAM access is successfully achieved through M7020R Device 0. Figure 95, page 130 and Figure 96, page 131 show timing diagrams for Device 0 and Device 7, respectively.

- **Cycle 1A:** The host ASIC applies the READ Instruction on the CMD[1:0] using CMDV = 1. The DQ Bus supplies the address, with DQ[20:19] set to '10' to select the SRAM address. The host ASIC selects the device for which ID[4:0] matches the DQ[25:21] lines. During this cycle the host ASIC also supplies SADR[21:20] on CMD[8:7].
- **Cycle 1B:** The host ASIC continues to apply the READ Instruction on the CMD[1:0] using CMDV = 1. The DQ Bus supplies the address

with DQ[20:19] set to '10' to select the SRAM address.

- **Cycle 2:** The host ASIC floats DQ[67:0] to a 3-state condition.
- **Cycle 3:** The host ASIC keeps DQ[67:0] in a 3-state condition.
- **Cycle 4:** The selected device starts to drive DQ[67:0].
- **Cycle 5:** The selected device continues to drive DQ[67:0] and drives ACK from high-Z to low
- **Cycle 6:** The selected device drives the READ address on SADR[21:0]. It also drives ACK high, CE_L low, WE_L high, and ALE_L low.
- **Cycle 7:** The selected device drives CE_L, ALE_L, WE_L, and the DQ Bus in a 3-state condition. It continues to drive ACK low.

At the end of Cycle 7, the selected device floats ACK in 3-state condition and a new command can begin.

Figure 94. Table with Eight Devices

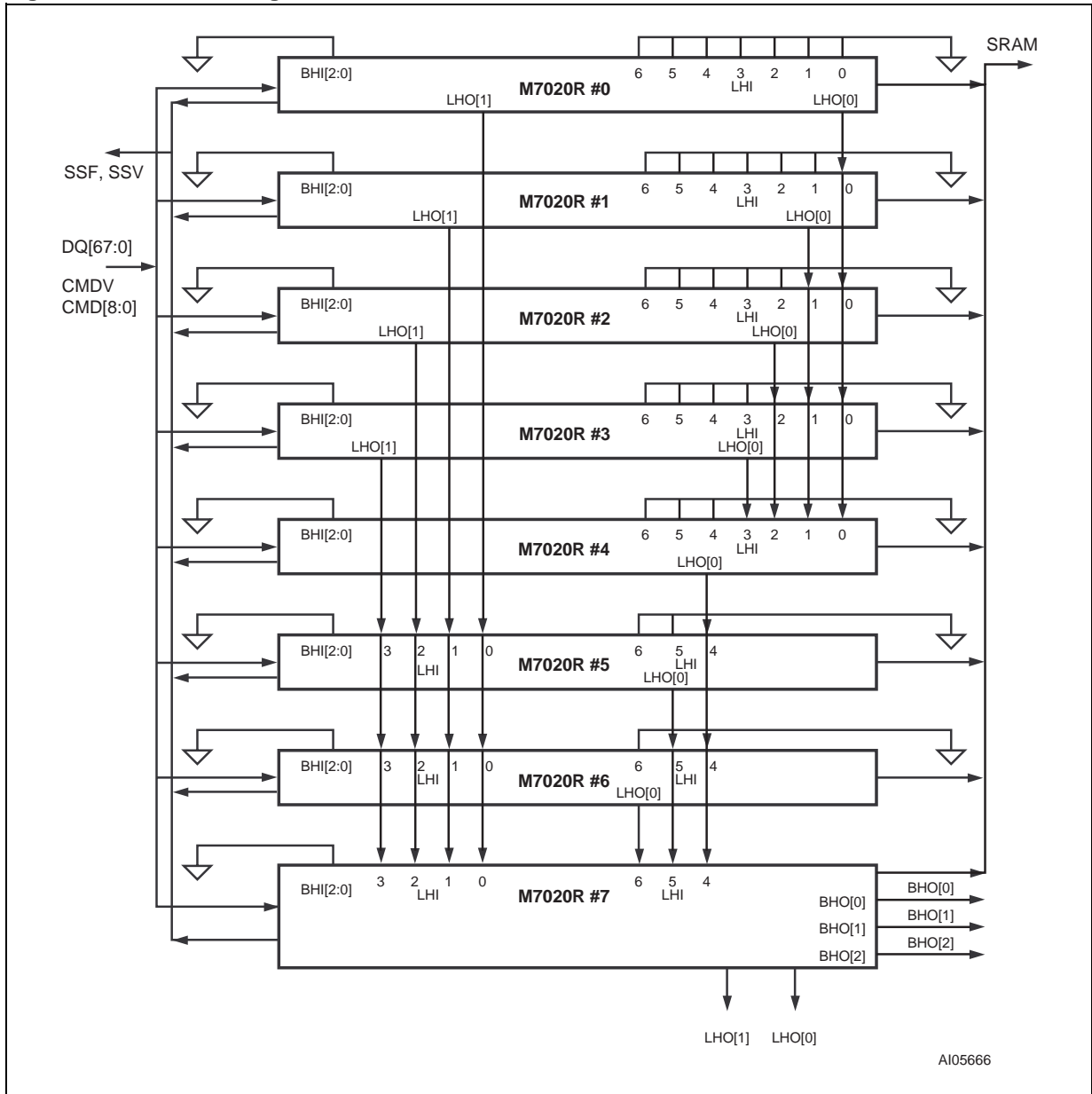


Figure 95. SRAM READ Through Device 0 in a Block of Eight Devices

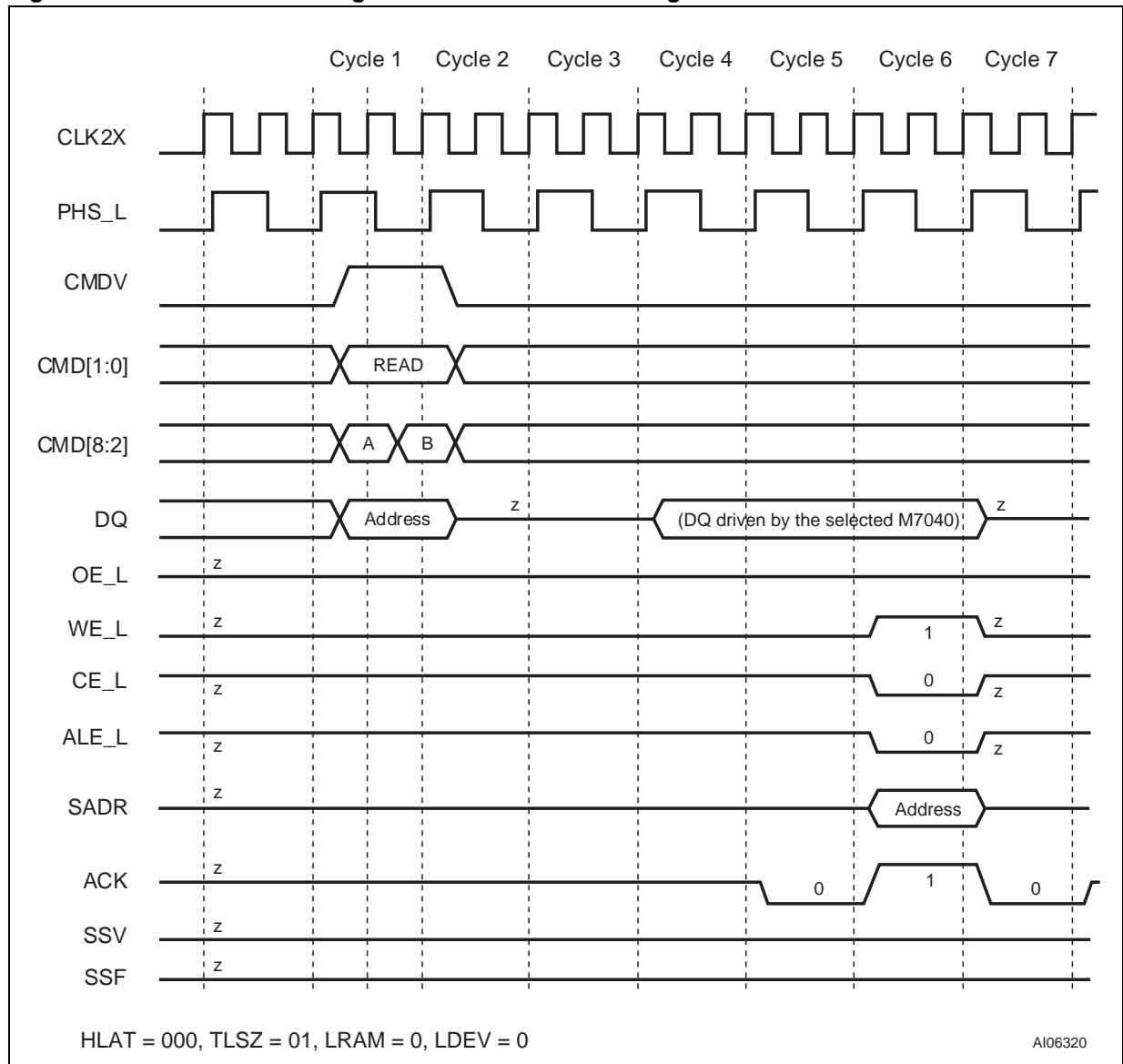
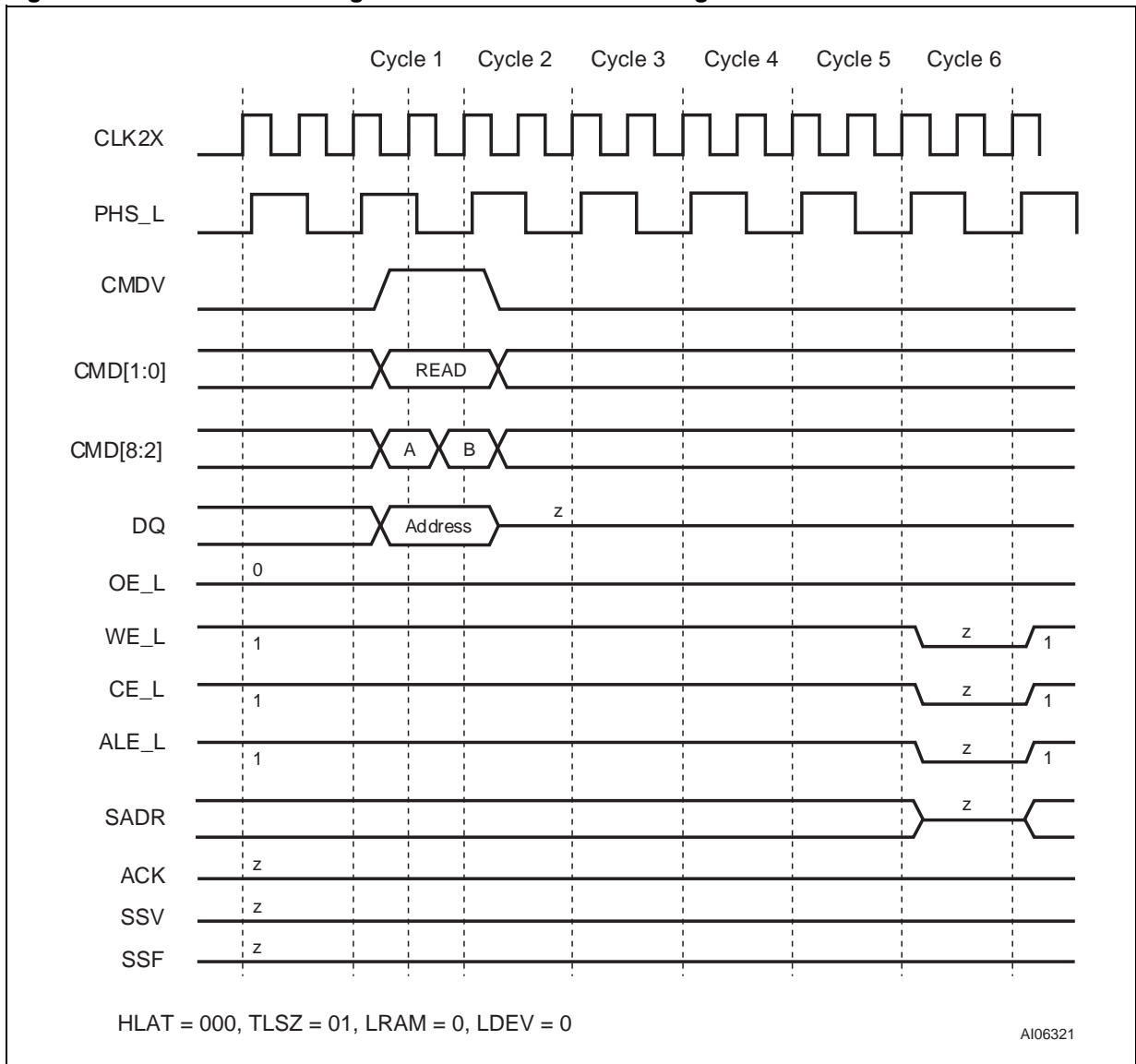


Figure 96. SRAM READ Timing for Device 7 in a Block of Eight Devices



SRAM READ with a Table of Up to 31 Devices

The following explains the SRAM READ operation accomplished through a table of up to 31 devices, using the following parameters: TLSZ = 10. The diagram of such a table is shown in Figure 97, page 133.

The following assumes that SRAM access is being accomplished through M7020R Device 0 and that Device 0 is the selected device. Figure 98, page 134 and Figure 99, page 135 show the timing diagrams for Device 0 and Device 30, respectively.

- **Cycle 1A:** The host ASIC applies the READ Instruction to CMD[1:0] using CMDV = 1. The DQ Bus supplies the address, with DQ[20:19] set to '10,' to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. During this cycle, the host ASIC also supplies SADR[21:20] on CMD[8:7].
- **Cycle 1B:** The host ASIC continues to apply the READ Instruction to CMD[1:0] using CMDV = 1. The DQ Bus supplies the address, with

DQ[20:19] set to '10,' to select the SRAM address.

- **Cycle 2:** The host ASIC floats DQ[67:0] to a 3-state condition.
- **Cycle 3:** The host ASIC keeps DQ[67:0] in a 3-state condition.
- **Cycle 4:** The selected device starts to drive DQ[67:0].
- **Cycles 5 to 6:** The selected device continues to drive DQ[67:0].
- **Cycle 7:** The selected device continues to drive DQ[67:0] and drives an SRAM READ cycle.
- **Cycle 8:** The selected device drives ACL from Z to low.
- **Cycle 9:** The selected device drives ACK to high.
- **Cycle 10:** The selected device drives ACK from high to low.

At the end of Cycle 10, the selected device floats ACL in a 3-state condition.

Figure 97. Table of 31 Devices Made of Four Blocks

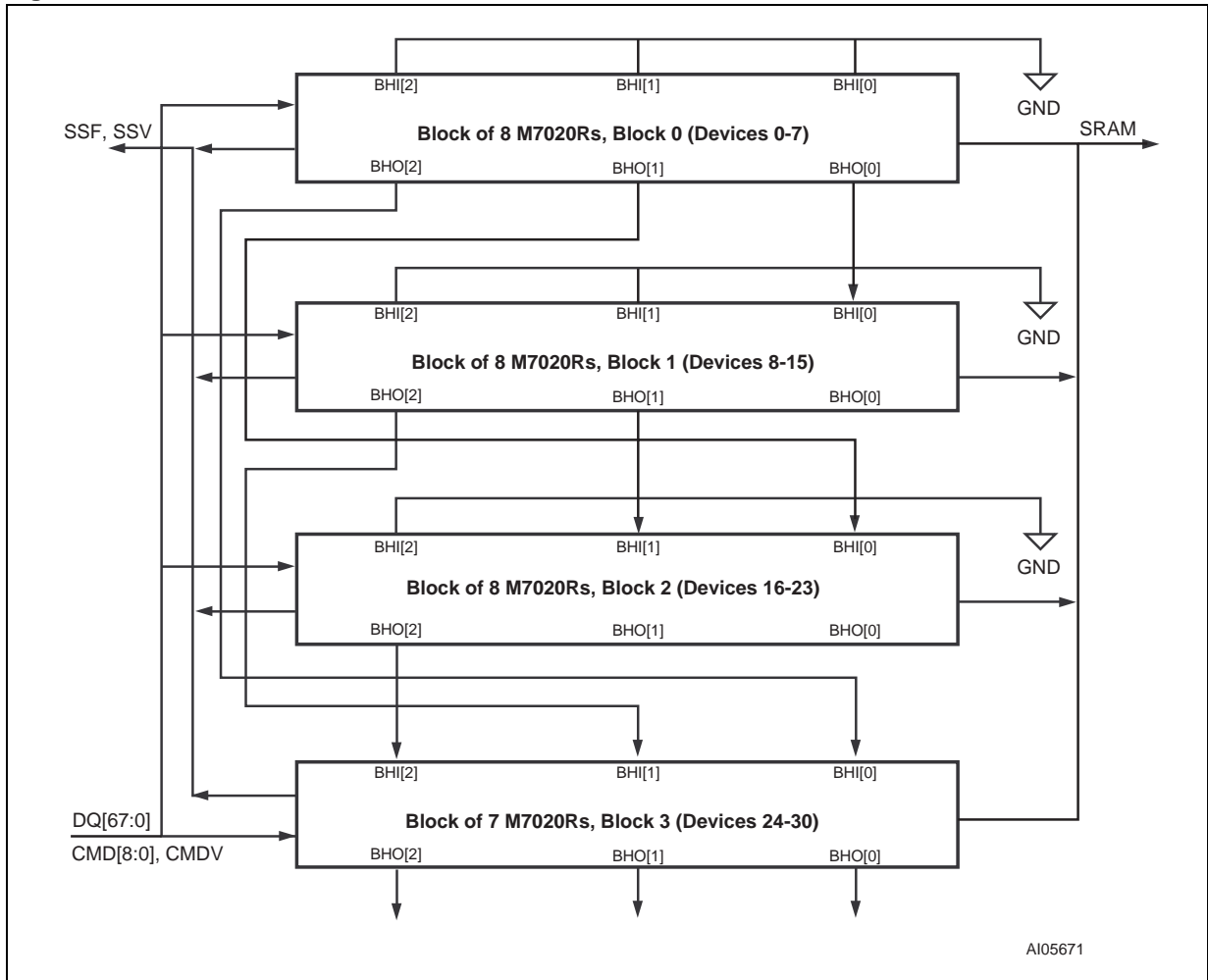


Figure 98. SRAM READ Through Device 0 in a Bank of 31 Devices (Device 0 Timing)

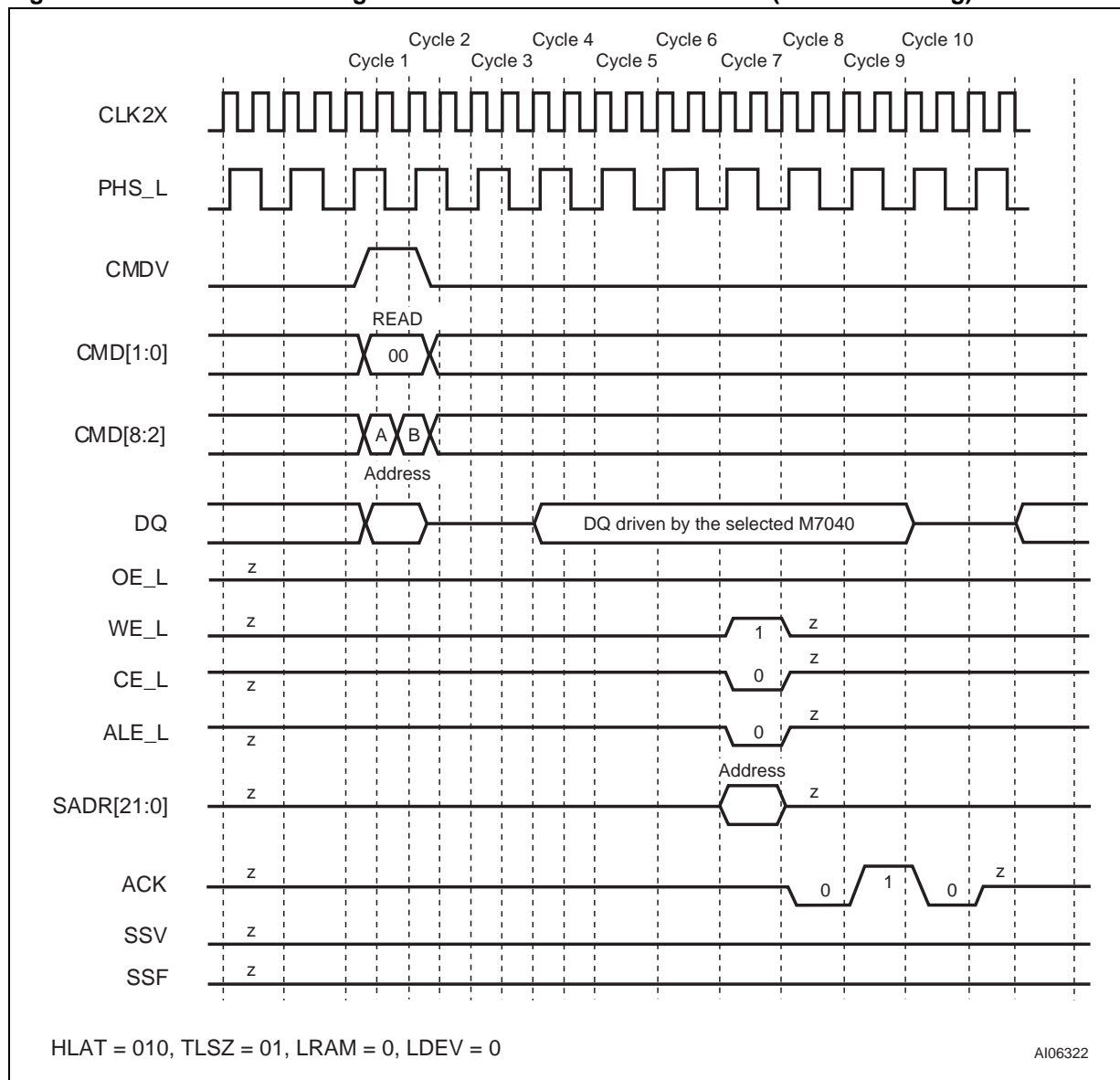
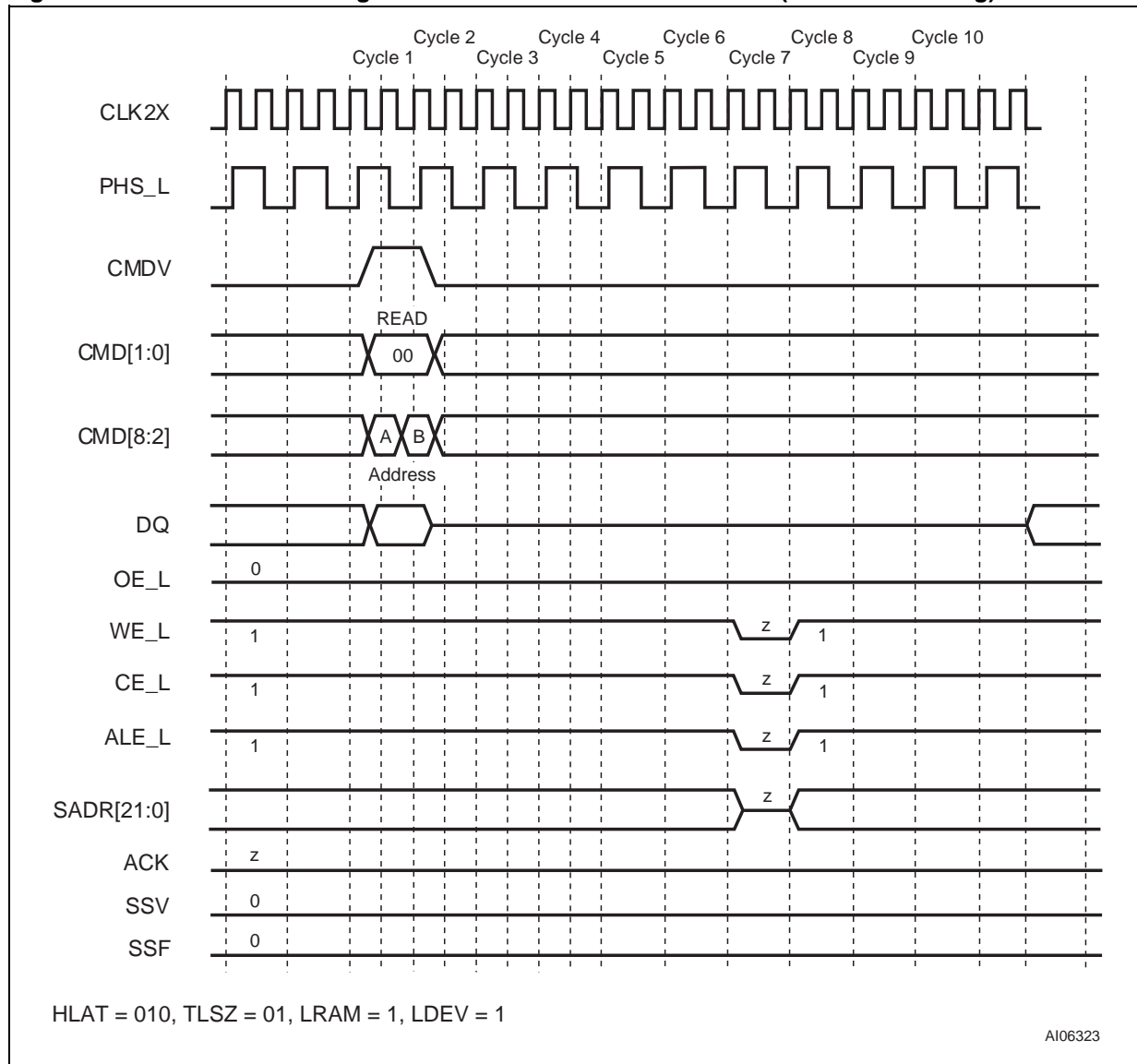


Figure 99. SRAM READ Through Device 0 in a Bank of 31 Devices (Device 30 Timing)



SRAM WRITE with a Table of One Device

SRAM WRITE enables WRITE access to the off-chip SRAM that contains associative data. The latency from the second cycle of the WRITE Instruction to the address appearing on the SRAM Bus is the same as the latency of the SEARCH Instruction, and will depend on the TLSZ value parameter programmed in the device configuration register. The following explains the SRAM WRITE operation accomplished with a table of only one device of the following parameters: TLSZ = 00, HLAT = 000, LRAM = 1, and LDEV = 1. Figure 100, page 137 shows the timing diagram.

For the following description the selected device refers to the only device in the table as it is the only device that will be accessed.

- **Cycle 1A:** The host ASIC applies the WRITE Instruction on CMD[1:0] using CMDV = 1. The DQ Bus supplies the address with DQ[20:19] set to '10' to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. The host ASIC also supplies SADR[21:20] on CMD[8:7] in this cycle.

Note: CMD[2] must be set to '0' for SRAM WRITE because Burst WRITES into the SRAM are not supported.

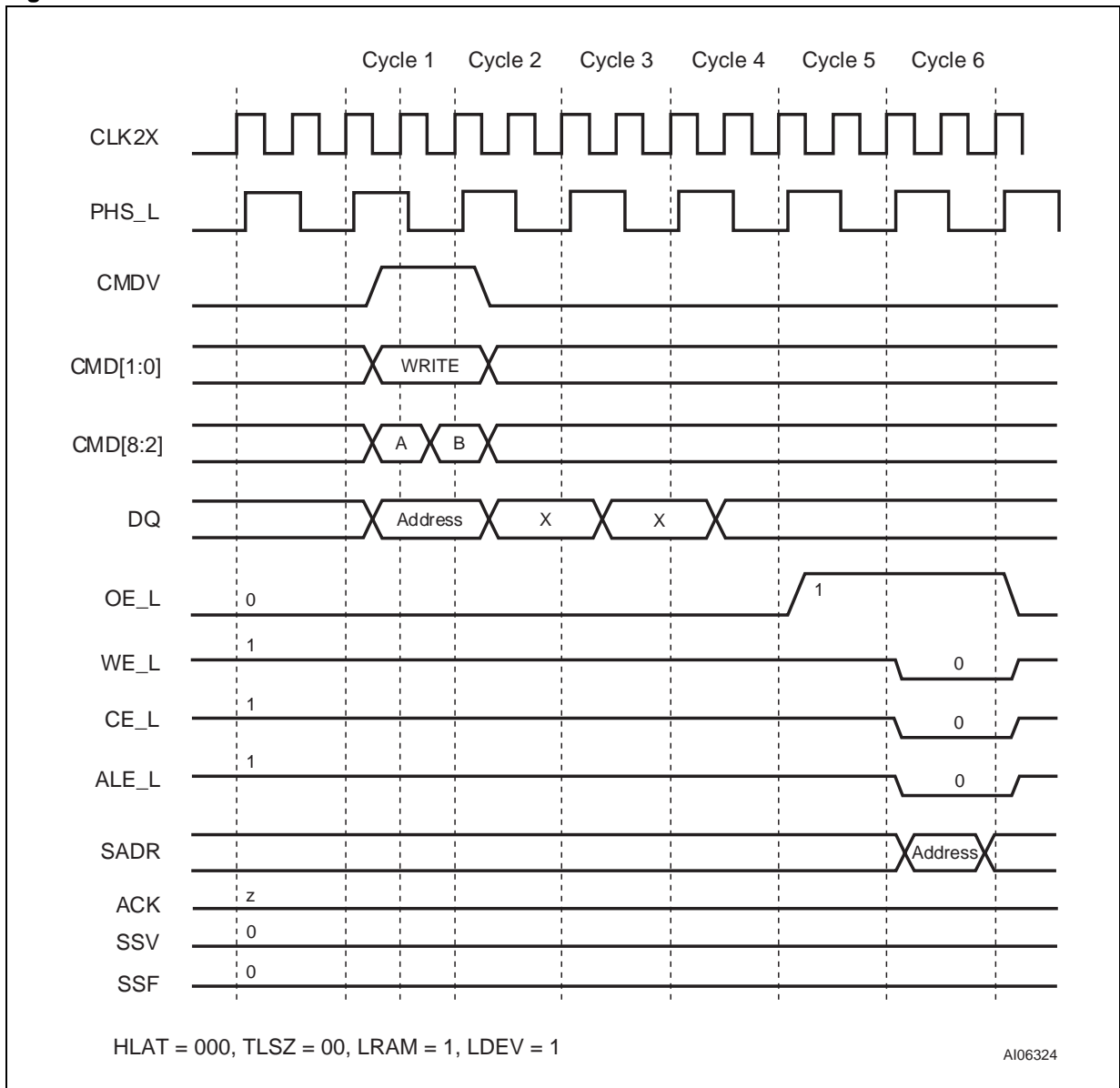
- **Cycle 1B:** The host ASIC continues to apply the WRITE Instruction on CMD[1:0], using CMDV = 1. The DQ Bus supplies the address with DQ[20:19] set to '10' to select the SRAM address.

Note: CMD[2] must be set to '0' for SRAM WRITE because Burst WRITES into the SRAM are not supported.

- **Cycle 2:** The host ASIC continues to drive DQ[67:0]. The data in this cycle is not used by the M7020R device.
- **Cycle 3:** The host ASIC continues to drive DQ[67:0]. The data in this cycle is not used by the M7020R device.

At the end of Cycle 3, a new command can begin. The WRITE is a pipelined operation. The WRITE Cycle appears at the SRAM Bus, however, with the same latency as that of a SEARCH Instruction, as measured from the second cycle of the WRITE command.

Figure 100. SRAM WRITE Access for One Device



SRAM WRITE with a Table of Up to Eight Devices

The following explains the SRAM WRITE operation done through a table(s) of up to eight devices with the following parameters (TLSZ = 01). The diagram of such a table is shown in Figure 101, page 139.

The following assumes that SRAM access is done through M7020R Device 0. Figure 102, page 140 and Figure 103, page 141 show the timing diagram for Device 0 and Device 7, respectively.

- **Cycle 1A:** The host ASIC applies the WRITE Instruction on CMD[1:0] using CMDV = 1. The DQ Bus supplies the address with DQ[20:19] set to '10' to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. The host ASIC also supplies SADR[23:21] on CMD[8:6] in this cycle.

Note: CMD[2] must be set to '0' for SRAM WRITE because Burst WRITES into the SRAM are not supported.

- **Cycle 1B:** The host ASIC continues to apply the WRITE Instruction on CMD[1:0] using CMDV = 1. The DQ Bus supplies the address with DQ[20:19] set to '10' to select the SRAM address.

Note: CMD[2] must be set to '0' for SRAM WRITE because Burst WRITES into the SRAM are not supported.

- **Cycle 2:** The host ASIC continues to drive DQ[67:0]. The data in this cycle is not used by the M7020R device.
- **Cycle 3:** The host ASIC continues to drive DQ[67:0]. The data in this cycle is not used by the M7020R device.

At the end of cycle 3, a new command can begin. The WRITE is a pipelined operation. The WRITE Cycle appears at the SRAM Bus, however, with the same latency as that of a SEARCH Instruction, as measured from the second cycle of the WRITE command.

Figure 101. Table with Eight Devices

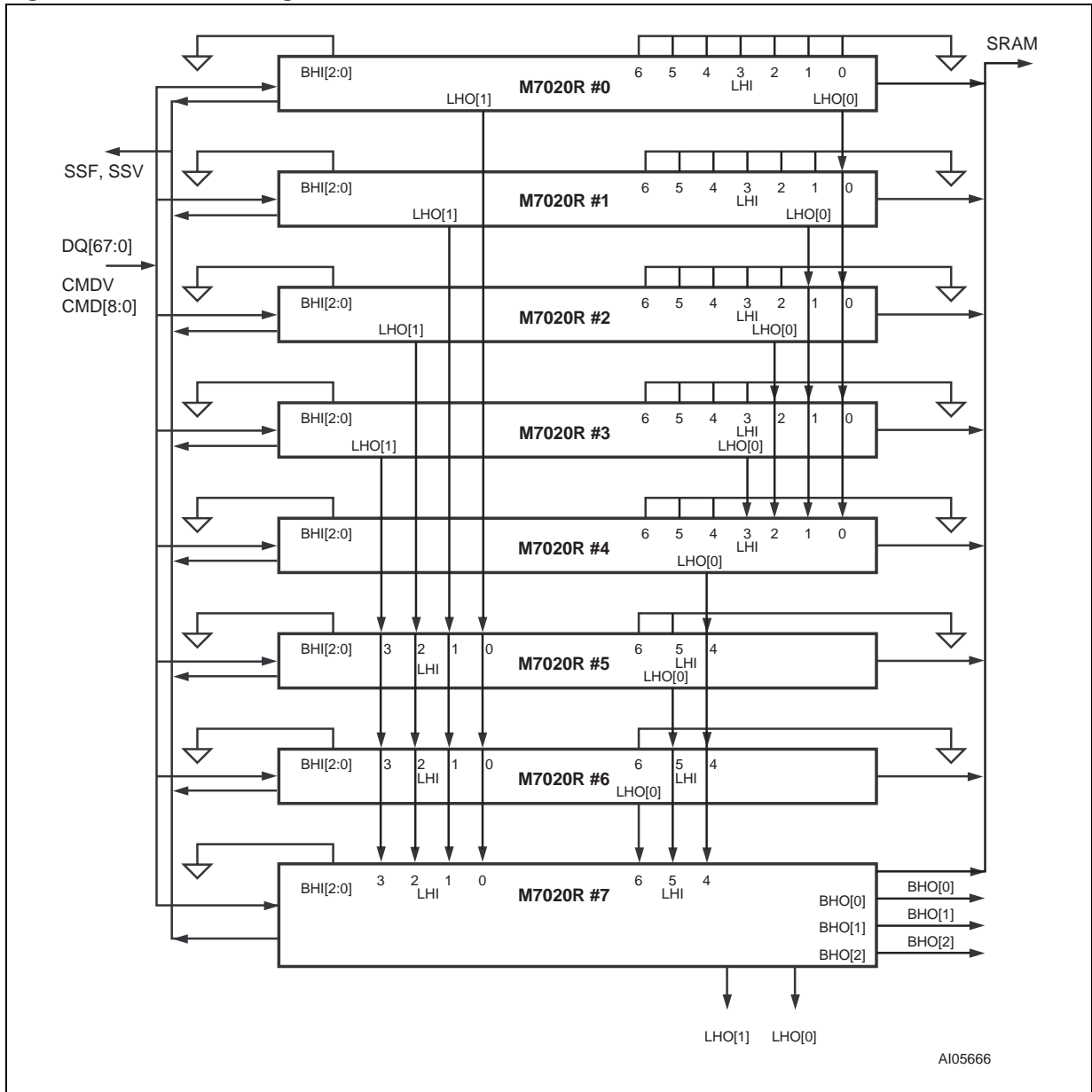


Figure 102. SRAM WRITE Through Device 0 in a Block of Eight Devices

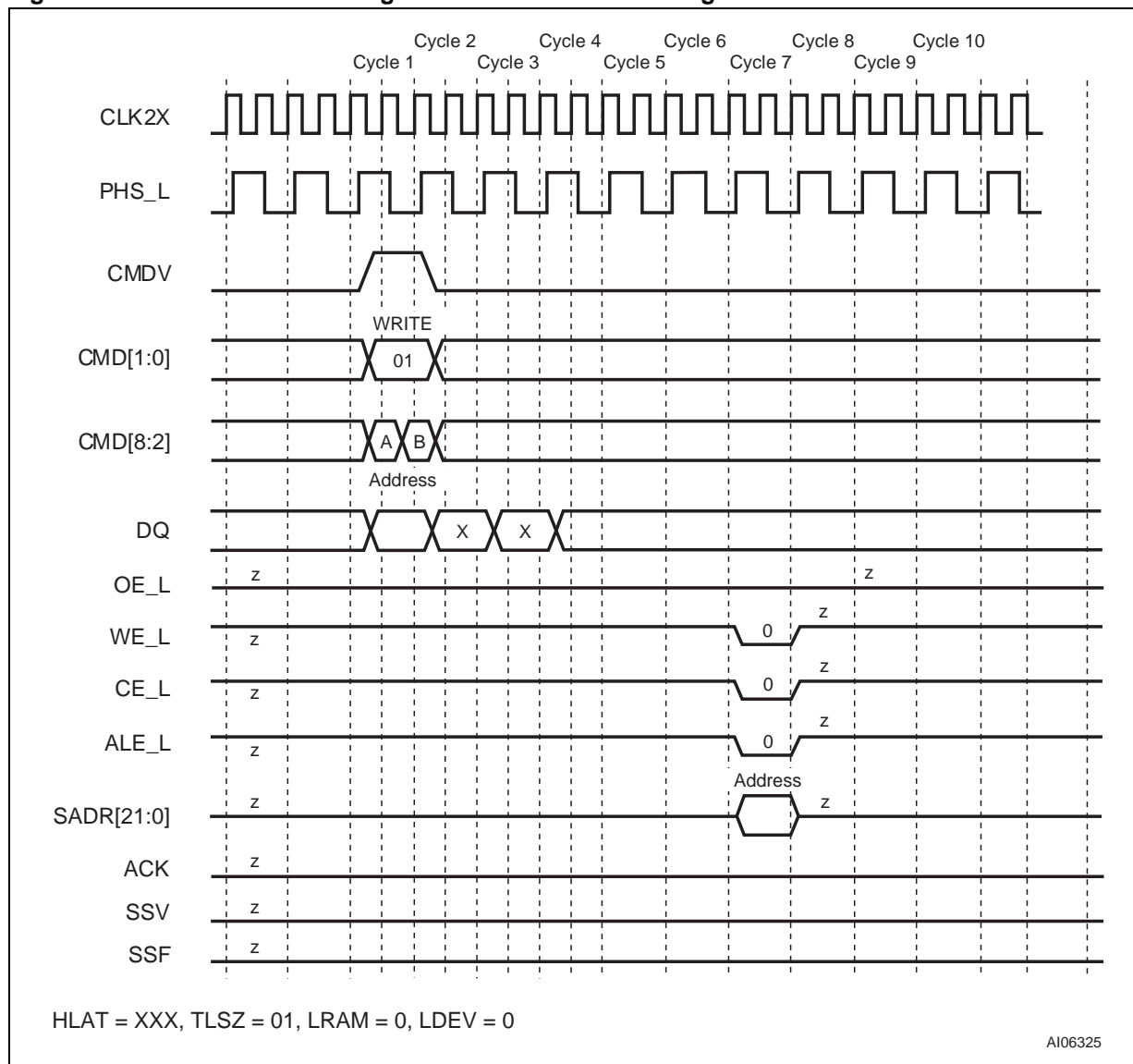
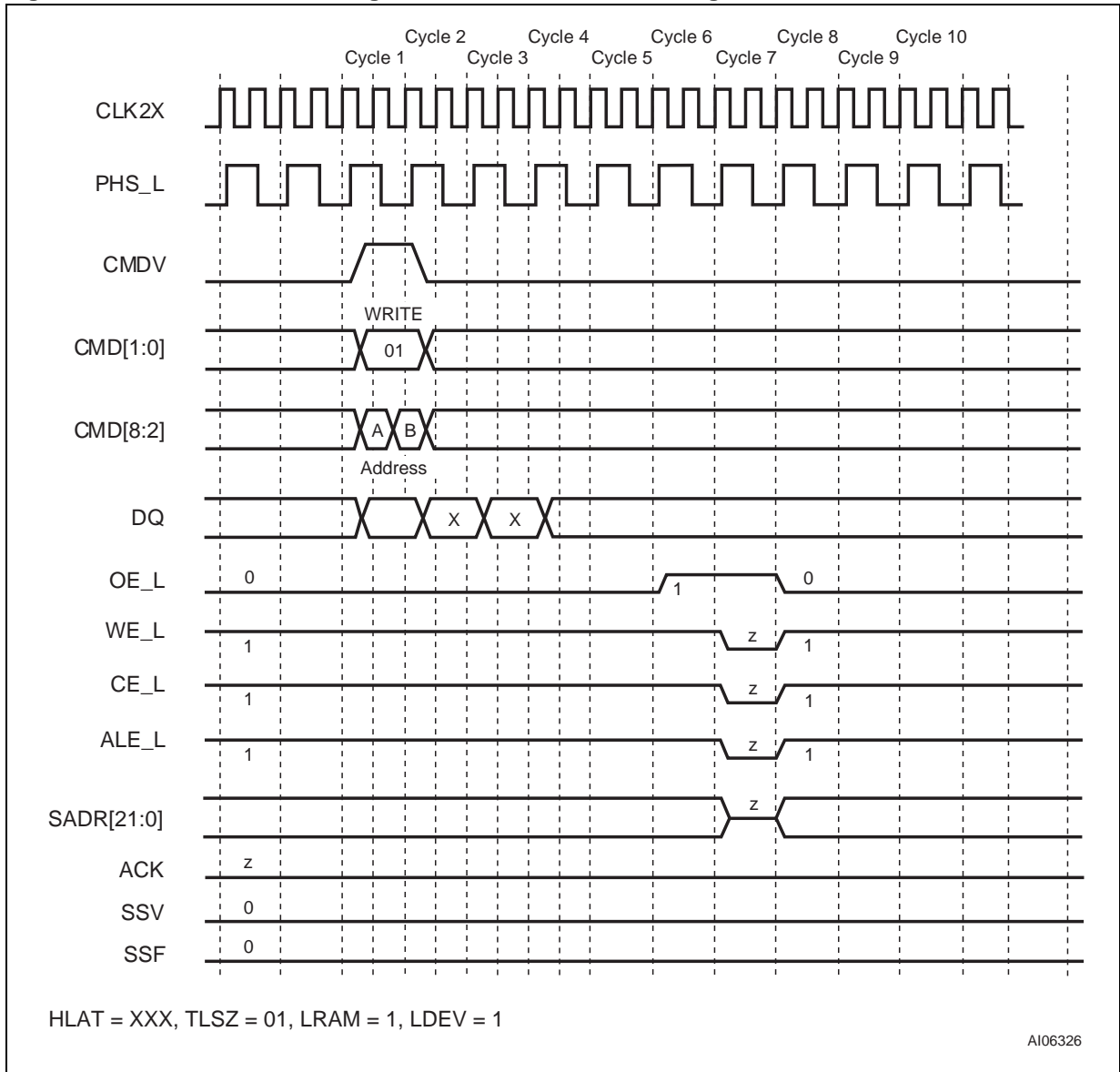


Figure 103. SRAM WRITE Timing for Device 7 in a Block of Eight Devices



SRAM WRITE with Table(s) of Up to 31 Devices

The following explains the SRAM WRITE operation done through a table(s) of up to 31 devices with the following parameters (TLSZ = 10). The diagram of such table(s) is shown in Figure 104, page 143. The following assumes that SRAM access is done through M7020R Device 0 – Device 0 is the selected device. Figure 105, page 144 and Figure 106, page 145 show the timing diagram for Device 0 and Device 30, respectively.

- **Cycle 1A:** The host ASIC applies the WRITE Instruction on CMD[1:0] using CMDV = 1. The DQ Bus supplies the address with DQ[20:19] set to '10' to select the SRAM address. The host ASIC selects the device for which the ID[4:0] matches the DQ[25:21] lines. The host ASIC also supplies SADR[21:20] on CMD[8:7] in this cycle.

Note: CMD[2] must be set to '0' for SRAM WRITE because Burst WRITES into the SRAM are not supported.

- **Cycle 1B:** The host ASIC continues to apply the WRITE Instruction on CMD[1:0] using CMDV = 1. The DQ Bus supplies the address with DQ[20:19] set to '10' to select the SRAM address.

Note: CMD[2] must be set to '0' for SRAM WRITE because Burst WRITES into the SRAM are not supported.

- **Cycle 2:** The host ASIC continues to drive DQ[67:0]. The data in this cycle is not used by the M7020R device.
- **Cycle 3:** The host ASIC continues to drive DQ[67:0]. The data in this cycle is not used by the M7020R device.

At the end of Cycle 3, a new command can begin. The WRITE is a pipelined operation. The WRITE Cycle appears at the SRAM Bus, however, with the same latency as that of a SEARCH Instruction, as measured from the second cycle of the WRITE command

Figure 104. Table of 31 Devices (Four Blocks)

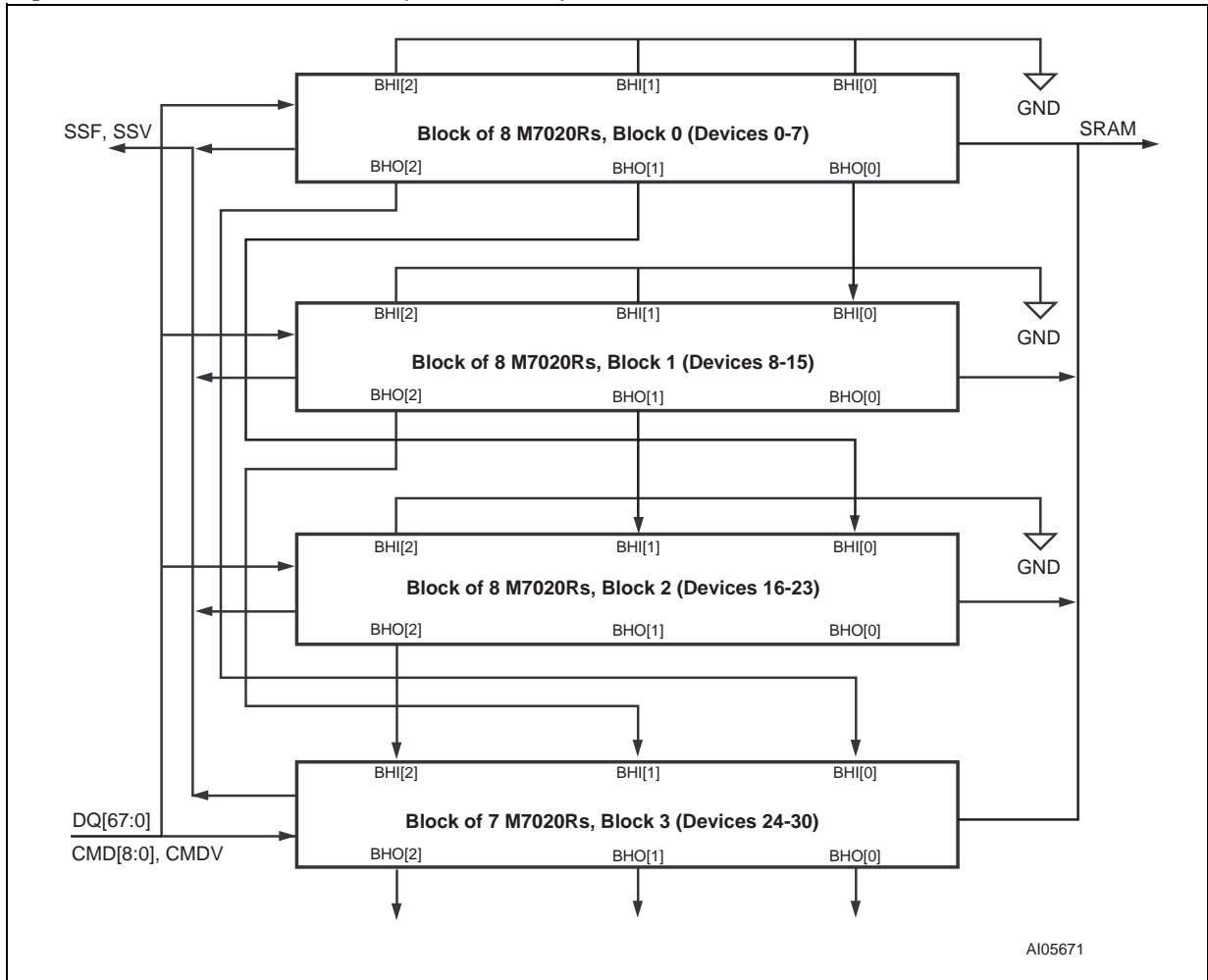


Figure 105. SRAM WRITE Through Device 0 in a Bank of 31 Devices (Device 0 Timing)

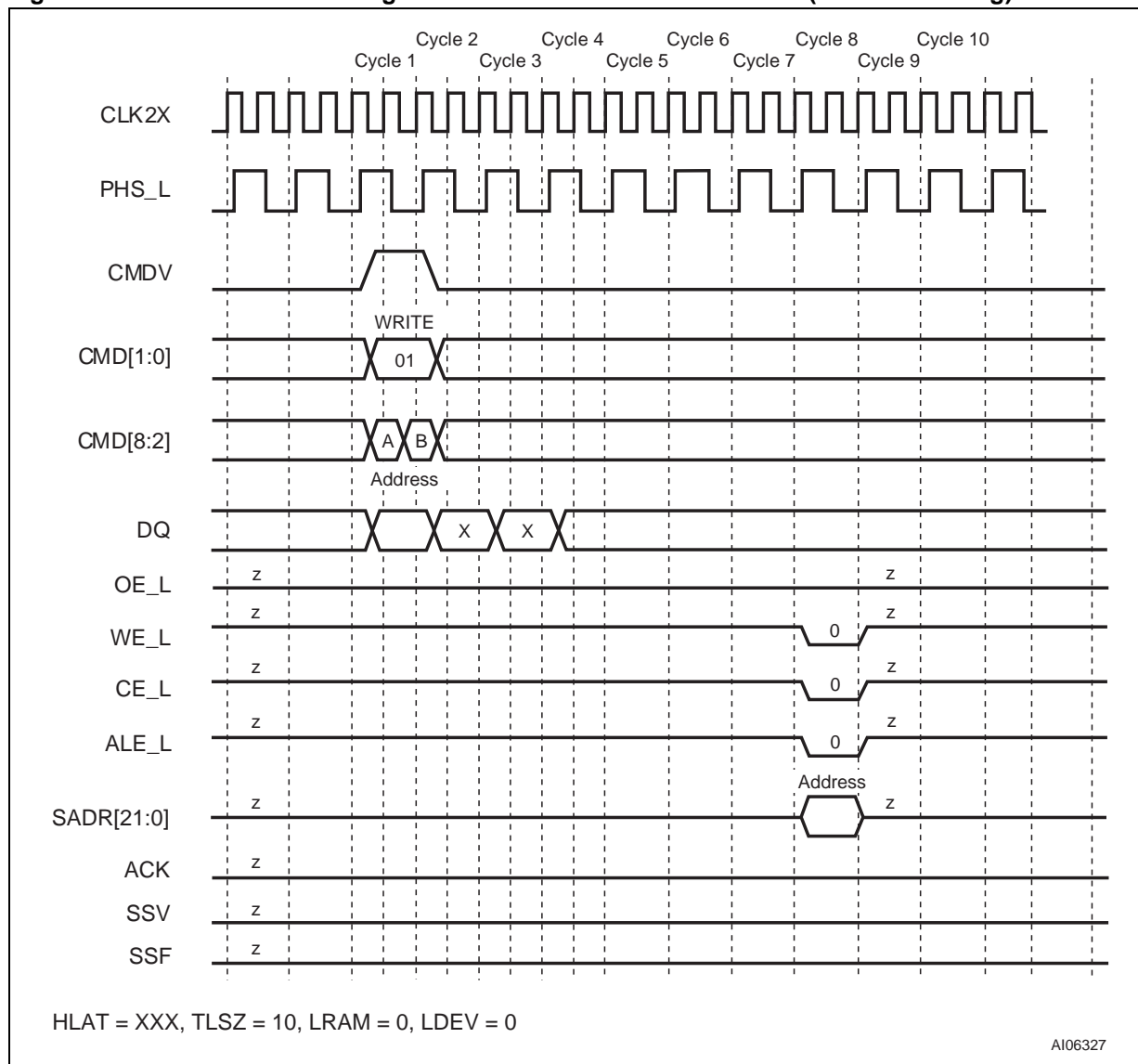
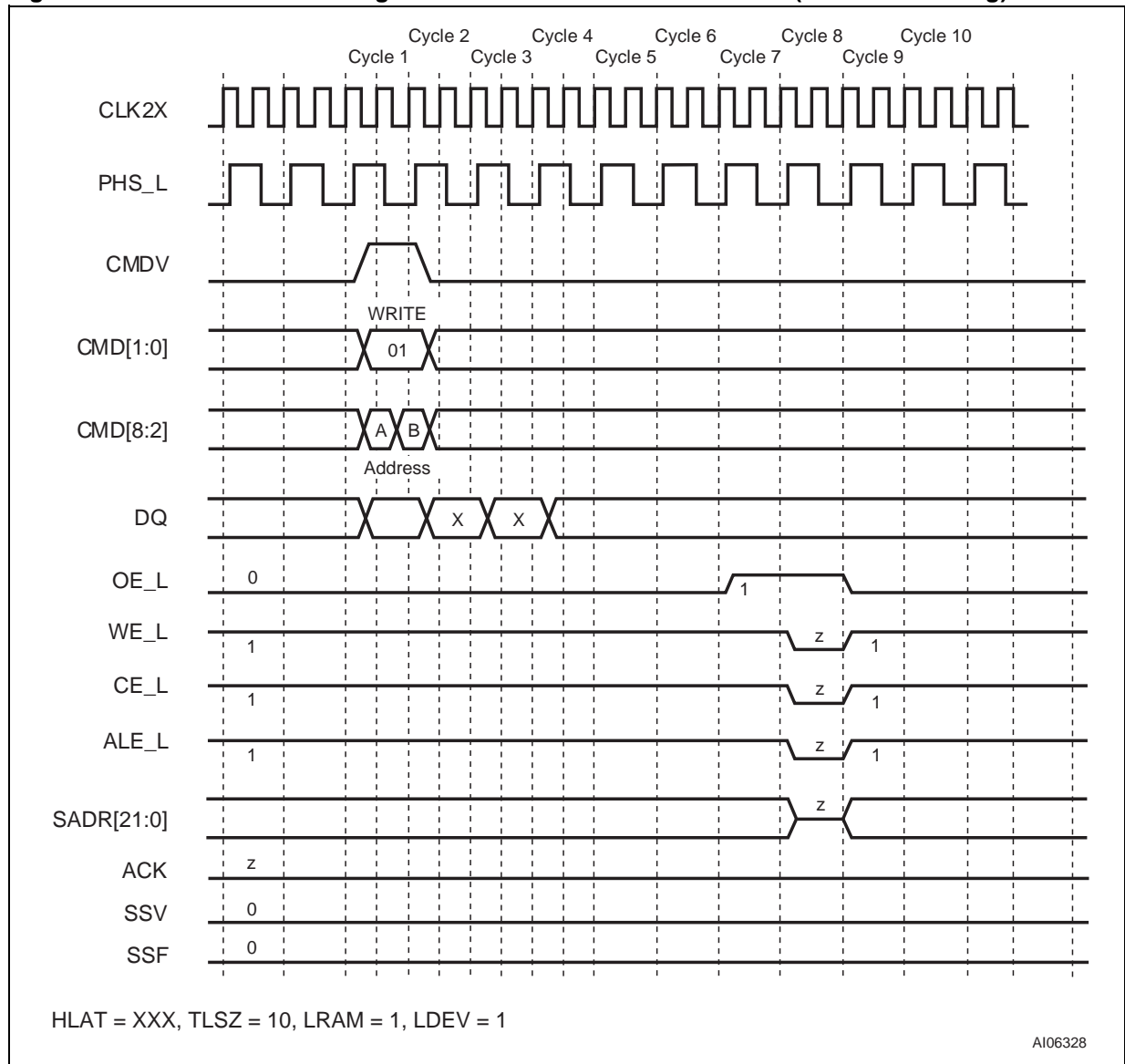


Figure 106. SRAM WRITE Through Device 0 in a Bank of 31 Devices (Device 30 Timing)



JTAG (1149.1) TESTING

The M7020R supports the Test Access Port and Boundary Scan Architecture as specified in the IEEE JTAG standard 1149.1. The pin interface to the chip consists of five signals with the standard definitions: TCK, TMS, TDI, TDO, and TRST_L. Table 51 describes the operations that the test ac-

cess port controller supports and Table 52 describes the TAP Device ID Register.

Note: To disable JTAG functionality, connect the TCK, TMS, and TDI pins to Ground, and TRST_L to VDD.

Table 51. Supported Operations

Instruction	Type	Description
SAMPLE/PRELOAD	Mandatory	Sample/Preload. Loads the values of signals going to and from IO pins into the boundary scan shift register to provide a snapshot of the normal functional operation.
EXTEST	Mandatory	External Test. Uses boundary scan values shifted in from TAP to test connectivity external to the device.
INTEST	Optional	Internal Test. Allows slow-speed, functional testing of the device using the boundary scan register to provide the I/O values.

Table 52. TAP Device ID Register

Field	Range	Initial Value	Description
Revision	[31:28]	0001	Revision Number. This is the current device revision number. Numbers start from one and increment by one for each revision of the device.
Part #	[27:12]	0000 0000 0000 0001	This is the part number for this device.
MFID	[11:1]	000_1101_1100	Manufacturer ID. This field is the same as the manufacturer ID used in the TAP controller.
LSB	[0]	1	Least Significant Bit

PART NUMBERING

Table 53. Ordering Information Scheme

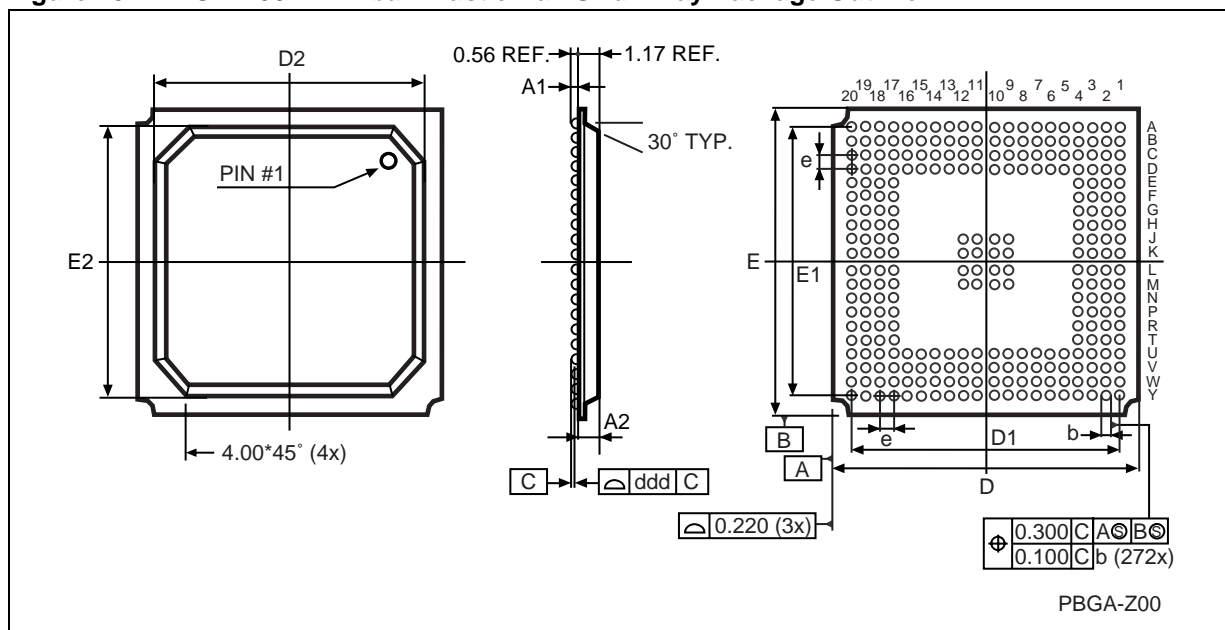
Example:	M70	20	R	-083	ZA	1	T
Device Type							
M70 Search Engine							
Density							
20 = 2Mb (32K x 68-bit Table Entries)							
Operating Supply Voltage							
R = $V_{DD} = 1.8V$							
Speed							
-083 = 83 Million Searches per Second							
-066 = 66 Million Searches per Second							
-050 = 50 Million Searches per Second							
Package							
PBGA = 272-ball count, 27mm x 27mm ⁽¹⁾ , 1.27mm ball pitch							
Temperature Range							
1 = 0 to 70°C							
Shipping Option							
Tape & Reel Packing = T							

Note: 1. Where "Z" is the symbol for BGA packages and "A" denotes 1.27mm ball pitch

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

PACKAGE MECHANICAL INFORMATION

Figure 107. PBGA-Z00 – 272-ball Plastic Ball Grid Array Package Outline



Note: Drawing is not to scale.

Table 54. PBGA-Z00 – 272-ball Plastic Ball Grid Array Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A ⁽⁴⁾	27.00	26.80	27.20 ⁽¹⁾	1.102	1.094	1.110 ⁽¹⁾
A1 ^(2,3)	0.60	0.50	0.70	0.024	0.020	0.029
A2		1.63	1.90		0.067	0.078
B ⁽⁴⁾	27.00	26.80	27.20	1.102	1.094	1.110
b	0.75	0.60	0.90	0.031	0.024	0.037
D	27.00	26.80	27.20	1.102	1.094	1.110
D1	24.13			0.985		
D2	24.00			0.980		
e	1.27			0.052		
E	27.00	26.80	27.20	1.102	1.094	1.110
E1	24.13			0.985		
E2	24.00			0.980		
n	272			272		
ddd			0.20			0.008
eee			0.30			0.012

- Note: 1. Maximum mounted height is 2.45mm based on a 0.65mm ball pad diameter. Solder paste is 0.15mm thickness and 0.65mm in diameter.
 2. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink, or metallized markings, or other feature of package body or integral heatslug.
 3. A distinguished feature is allowable on the bottom surface of the package to identify the terminal A1 corner.
 4. Exact shape of each corner is optional.

REVISION HISTORY**Table 55. Document Revision History**

Date	Revision Details
February 2001	First Issue
03/23/01	Document re-organization, change in Power Distribution text
04/02/01	Updated mechanical drawing and table (Figure 107, Table 54)
07/23/01	Routine maintenance (based on recent data sheet review findings)
10/02/01	Change references to "Lara" and "ST" to Cypress in "Description" section; added 83MHz speed grade to document; values, references, and footnotes changed (Table 3, 4, 5, 6, 7, 54); labels changed (Figures 5, 8); basic formatting changes based on recent reviews
11/14/01	Rework document (add graphics, change text) after Cypress purchase

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