M-927 DTMF Receiver

The Teltone® M-927 is a high-quality Dual-Tone Multi-frequency (DTMF) digital receiver and/or rotary dial pulse counter. The M-927 is contained in a 40-pin package and requires no external components except a single 3.579 MHz television color burst crystal.

As shown in Figure 2, the M-927 is typically connected in parallel with the voice pair (Tip and Ring) of a telephone line. It receives signals from a DTMF generator or pulsing mechanism and translates them into logic level outputs for use by other devices, permitting applications such as data entry via telephone or instrument and control system access and activation. For applications such as DTMF-to-rotary conversion, additional outputs provide early indications of signal presence. Logic inputs to the M-927 enable or disable the receiver, inhibit or enable the reception of DTMF or rotary signals, and select from the output formats listed in Table 1.

The M-927 is manufactured under U.S. Patent 4,145,576.

Features

- Meets CEPT overall performance requirement of less than one false operation per 10,000 digits dialed
- Meets CCITT recommendations for tone receivers
- Decodes all 16 DTMF digits
- Time-guarded rotary dial pulse counting
- Selectable output formats: binary, 2 of 8 (2 of 7), 1 of 12, or blank
- Accepts differential or single-ended input with no additional components
- Provides superior signal-to-noise characteristics and speech immunity
- Three different chip enable/disable inputs
- Separate outputs indicating dial pulse or early DTMF tone presence
- Valid data output strobe
- Stable, free-running clock outputs: 447 kHz, 881 Hz, and 20 Hz

Telephone Switching Applications

- Central office products
- PBX and intercom systems
- Consumer-oriented special feature phones and services
- Radio equipment interface to telephone network

Access and Control Applications

- Answering and recording devices
- Radio communication remote switching

- Remote control of machinery or microprocessors
- Monitoring equipment

Data Entry Applications

- Remote computer and peripheral systems interface
- Consumer credit and shopping systems
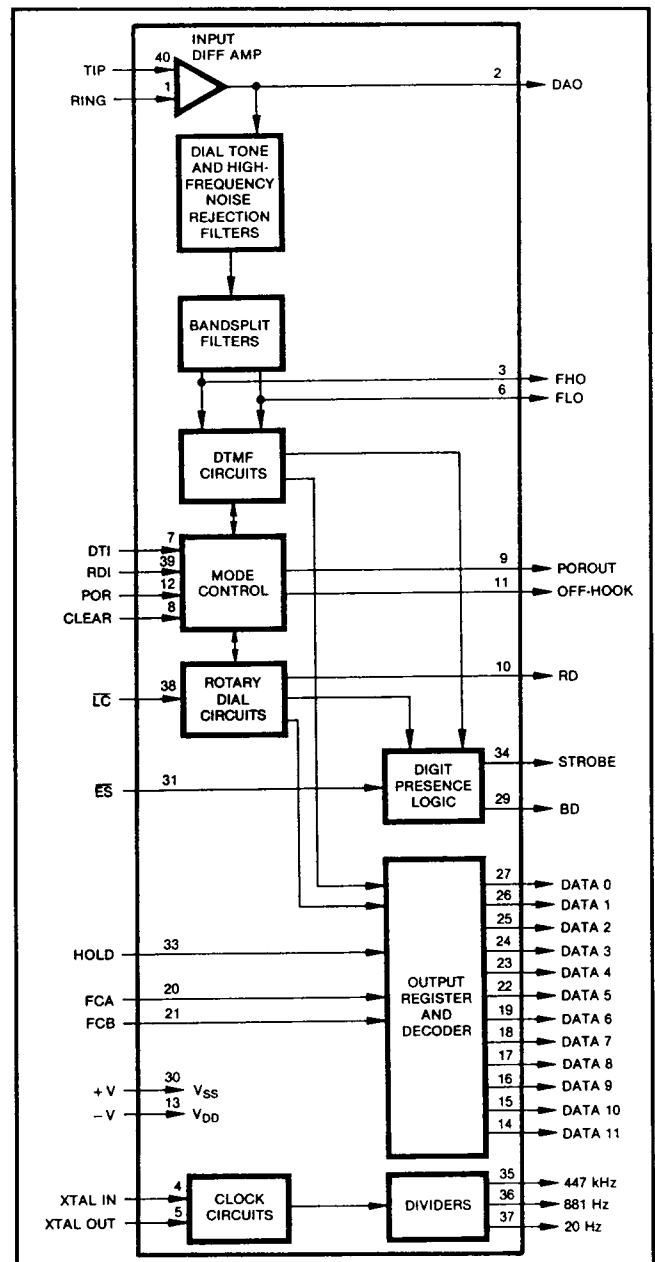- Telephone banking, credit, and bill-paying systems
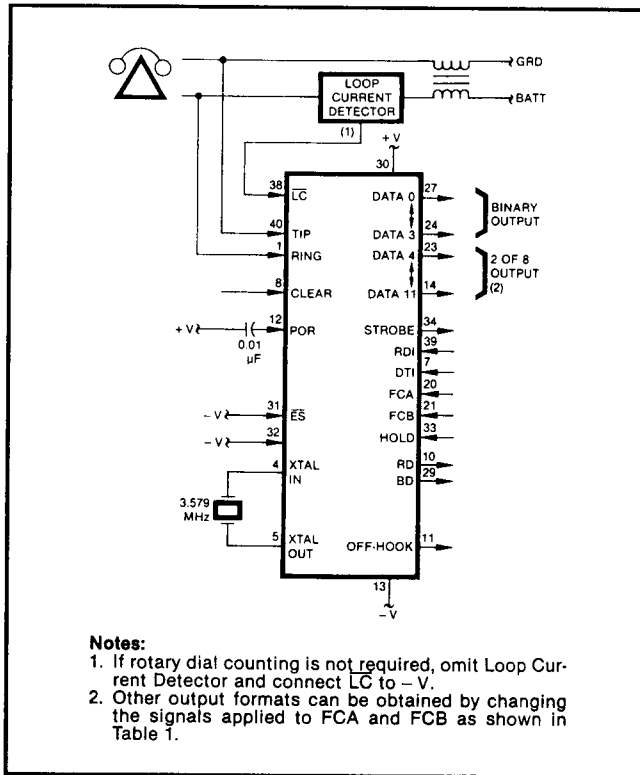

Figure 1 Block Diagram

Notes:
1. If rotary dial counting is not required, omit Loop Current Detector and connect LC to −V.
2. Other output formats can be obtained by changing the signals applied to FCA and FCB as shown in Table 1.

Figure 2 Typical Application

Table 1 Output Formats

1 OF 12 OUTPUT FORMAT
FCA 0   FCB 0

BINARY AND 2 OF 8 OR 2 OF 7
OUTPUT FORMATS
FCA 1   FCB 0

BINARY OUTPUT FORMAT
FCA 0   FCB 1

BLANK OUTPUT FORMAT
FCA 1   FCB 1

1. TO TTL OR CMOS AT A LOWER SUPPLY VOLTAGE

2. TO LOW POWER SCHOTTKY TTL

3. TO RELAYS OR DISPLAYS (NEGATIVE SUPPLY)

4. TO TRANSISTOR DRIVERS

5. (NOT SHOWN) TO CMOS AT THE SAME SUPPLY VOLTAGE—INTERFACE DIRECTLY (ALL OUTPUTS)
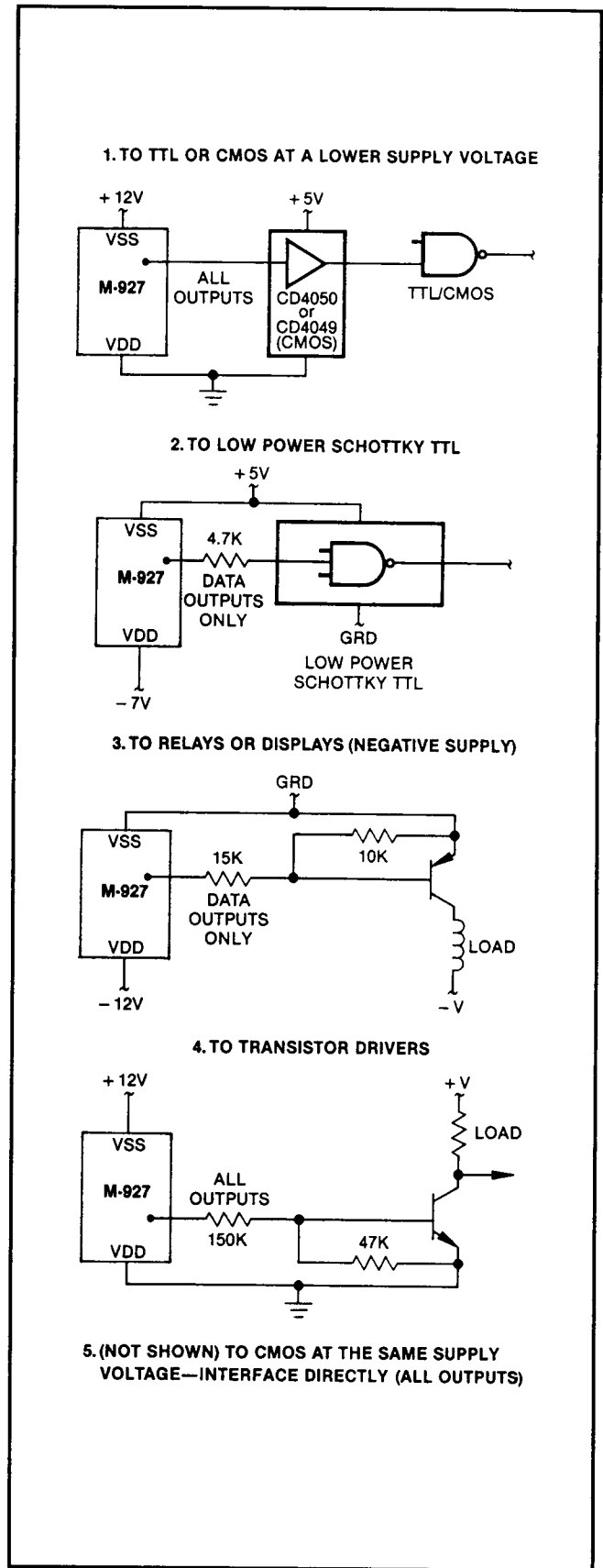
Figure 3 Output Interface Techniques

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Table 2 Pin Functions

Pin	Number	Description
– V + V	13 30	Negative and positive power supply connections (11 to 13.5 VDC).
POR POROUT	12 9	Power-On Reset. Receiver enable/disable input and output. A logic 1 applied to pin 12 drives pin 9 to logic 1, resets all detection circuits, drives the OFF-HOOK output to logic 0, and forces the DATA outputs to the "D" column of the currently enabled output format (see Table 1). A logic 0 applied to pin 12 enables the detection circuits, provided that $\overline{LC}$ has been at logic 0 for 100 ms, causing OFF-HOOK to go to logic 1.
CLEAR	8	Receiver enable/disable input. A logic 1 applied to the CLEAR input instantaneously resets all detection circuits and forces the DATA outputs to the "D" column of the currently enabled output format (see Table 1). A logic 0 applied to the CLEAR input immediately enables the detection circuits, provided that $\overline{LC}$ has remained at logic 0 or has not been at logic 1 for longer than 300 ms.
$\overline{LC}$	38	Loop Current Not input. $\overline{LC}$ is both a receiver enable/disable input and a rotary dial pulse input. A logic 0 represents an off-hook condition, an interdigital pause, or a make period. A logic 1 represents an on-hook condition or a break period. For DTMF operation only, $\overline{LC}$ can be connected to – V; then, with POR connected as shown in Figure 3, the receiver is enabled as long as CLEAR is at logic 0.
TIP RING	40 1	AC-coupled, balanced DTMF or single-ended input to the differential amplifier.
DAO	2	Differential Amplifier Output. Primarily used for testing.
FHO FLO	3 6	High Frequency group and Low Frequency group bandsplit filter outputs. Used only for testing.
$\overline{ES}$	31	Early Split Not input. When pulled to logic 0, $\overline{ES}$ enables the BD output.
	32	For factory use only. Connect to logic 0.
BD	29	Button Down output. When enabled by $\overline{ES}$ being at logic 0, BD goes to the logic 1 state 16 ms after a tone pair is detected. BD then returns to logic 0 approximately 25 ms after the tone pair ends.
	28	For factory use only. Leave open.
RD	10	Rotary Dial output. RD provides an early dial pulse presence signal that starts at the leading edge of the first break pulse and ends 100 ms after the trailing edge of the last pulse.
OFF-HOOK	11	Output. OFF-HOOK goes to the logic 1 state 100 ms after $\overline{LC}$ is pulled to logic 0. OFF-HOOK goes to the logic 0 state 300 ms after $\overline{LC}$ is pulled to logic 1.
DTI RDI	7 39	DTMF Inhibit input and Rotary Dial Inhibit input. For mixed DTMF and rotary dial operation, connect DTI and RDI to – V. For rotary dial operation only, connect DTI to + V. For DTMF operation only, connect RDI to + V. For mode locking on the first digit detected, connect both DTI and RDI to STROBE. The mode lock will be held until the detection circuits are reset by the POR, CLEAR, or $\overline{LC}$ inputs.
FCA FCB	20 21	Format Control A input and Format Control B input. As shown in Table 1, FCA and FCB determine the DATA output format. By holding both inputs at logic 1, all DATA outputs will remain at logic 1 until FCA and/or FCB are pulled to logic 0.
DATA 0 DATA 1 DATA 2 DATA 3 DATA 4 DATA 5 DATA 6 DATA 7 DATA 8 DATA 9 DATA 10 DATA 11	27 26 25 24 23 22 19 18 17 16 15 14	Data outputs. See Table 1 for the outputs associated with each output format. A DTMF digit is recognized when it has persisted for 40 ms. A rotary dial digit is recognized when an interdigital pause is detected.
STROBE	34	Valid data output. When DTMF digits are being detected, STROBE goes to the logic 1 state 10 microseconds after the DATA outputs change, and returns to the logic 0 state 25 ms after the loss or change of either tone constituting the detected digit. When rotary dial digits are being detected, STROBE goes to logic 1 for 200 ms after the interdigital pause is recognized. To read DATA during DTMF signal presence, use the leading edge of STROBE. To read DATA after DTMF signal presence, use the trailing edge of STROBE.
HOLD	33	Input. For applications where the output data has to remain unchanged for an extended time period, whether or not additional digits have been received, pull HOLD to logic 1 after STROBE goes to logic 1.
XTAL IN XTAL OUT	4 5	Input and output connections for a 3.579 MHz color burst television crystal.
447 kHz 881 Hz 20 Hz	35 36 37	For external use. Actual frequencies are XTAL frequency divided by 8, XTAL frequency divided by 4064, and XTAL frequency divided by 178,816. These are 50 percent duty cycle, PMOS logic level signals.

Table 3 Specifications

(− V = 0 V   + V = 12 V   Ambient Temperature = 25° C)

	Parameter	Min	Typ	Max	Units	Conditions
Logic Inputs	Logic 0 Voltage	− 0.3	—	2	V	
	Logic 1 Voltage	10	—	12.3	V	
	Capacitance	—	—	15	pF	
	Input Current	—	—	± 50	µA	
DC Signaling at $\overline{LC}$ Input	Logic 0 Voltage	− 0.3	—	2	V	
	Logic 1 Voltage	10	—	12.3	V	
	Off-Hook Recognition	95	—	105	ms	$\overline{LC}$ at 0 V
	Off-Hook Blanking (Note 1)	285	—	315	ms	$\overline{LC}$ at 0 V
	Break Recognition	24.5	—	29.5	ms	$\overline{LC}$ at 12 V
	Make Recognition	7	—	11	ms	$\overline{LC}$ at 0 V
	End of Digit Recognition	95	—	105	ms	$\overline{LC}$ at 0 V
	Rotary Interdigital Blanking	190	—	210	ms	$\overline{LC}$ at 0 V
	On-Hook Recognition	290	—	310	ms	$\overline{LC}$ at 12 V
TIP and RING Inputs	Input Impedance	450	—	—	kohm	at 1 kHz
	Common Mode Noise Tolerance, 15 to 100 Hz	60	—	—	Vrms	
	Dial Tone Tolerance	− 5	—	—	dBm (Note 2)	f ≤ 500 Hz
	Precise Dial Tone Tolerance	0	—	—	dBm (Note 2)	each tone, 350 and 440 Hz
	Signal Detect Level	− 30	—	+ 6	dBm (Note 2)	per tone
	Signal Reject Level	− 40	—	—	dBm (Note 2)	per tone
	Signal Detect Bandwidth	− 1.5% − 2	—	+ 1.5% + 2	Hz	
	Signal Reject Bandwidth	− 3.5%	—	+ 3.5%	Hz	
	Twist	—	± 10	—	dB	
	Noise Tolerance	− 43	—	—	dBm	(Note 4)
	Signal-to-Noise Ratio	—	—	18	dB	(Note 4)
	Signal Detect Time	—	—	40	ms	
	Signal Reject Time	20	—	—	ms	
	Interdigital Pause Detect Time	—	—	40	ms	
	Interdigital Pause Reject Time	22	—	—	ms	
DATA Outputs	Logic 0 Voltage	—	—	7	V	with 1 mA output current
	Logic 1 Voltage	10	—	—	V	with − 100 µA output current
	Logic 0 Current	1	—	—	mA	
	Logic 1 Current	− 0.1	—	—	mA	
	STROBE Output Delay	10	—	—	µs	measured from appearance of digit at DATA outputs
	BD Output Delay	—	—	16	ms	measured from appearance of tones at receiver
Non-DATA Outputs	Logic 0 Voltage	—	—	2	V	with 100 µA output current
	Logic 1 Voltage	10	—	—	V	with − 100 µA output current
	Logic 0 Current	0.1	—	—	mA	
	Logic 1 Current	− 0.1	—	—	mA	
Power	Supply Voltage (Operating)	11	12	13.5	V	+ V referenced to − V
	Supply Ripple (Note 3)	—	—	30	mV	
	Supply Current	—	—	85	mA	

Notes:
1. Off-hook blanking is the delay between $\overline{LC}$ going to logic 0 (after having been at logic 1 for more than 300 ms) and enabling of the digit detection circuits.
2. dBm = decibels above or below a reference power of one milliwatt into a 600-ohm load.
3. A bypass capacitor may be necessary. The internal digital logic of the M-927 may generate ripple voltages.
4. With the signal level − 25 dBm per tone, the signal 50 ms on and 50 ms off, no twist or frequency deviation, all 16 digits signalled randomly, 0 through 3 kHz flat Gaussian noise, and an error rate of less than one in 10,000. This is essentially the test method of EIA, USITA, and AT&T, except that the signal level is decreased to reflect the increased sensitivity of the M-927.
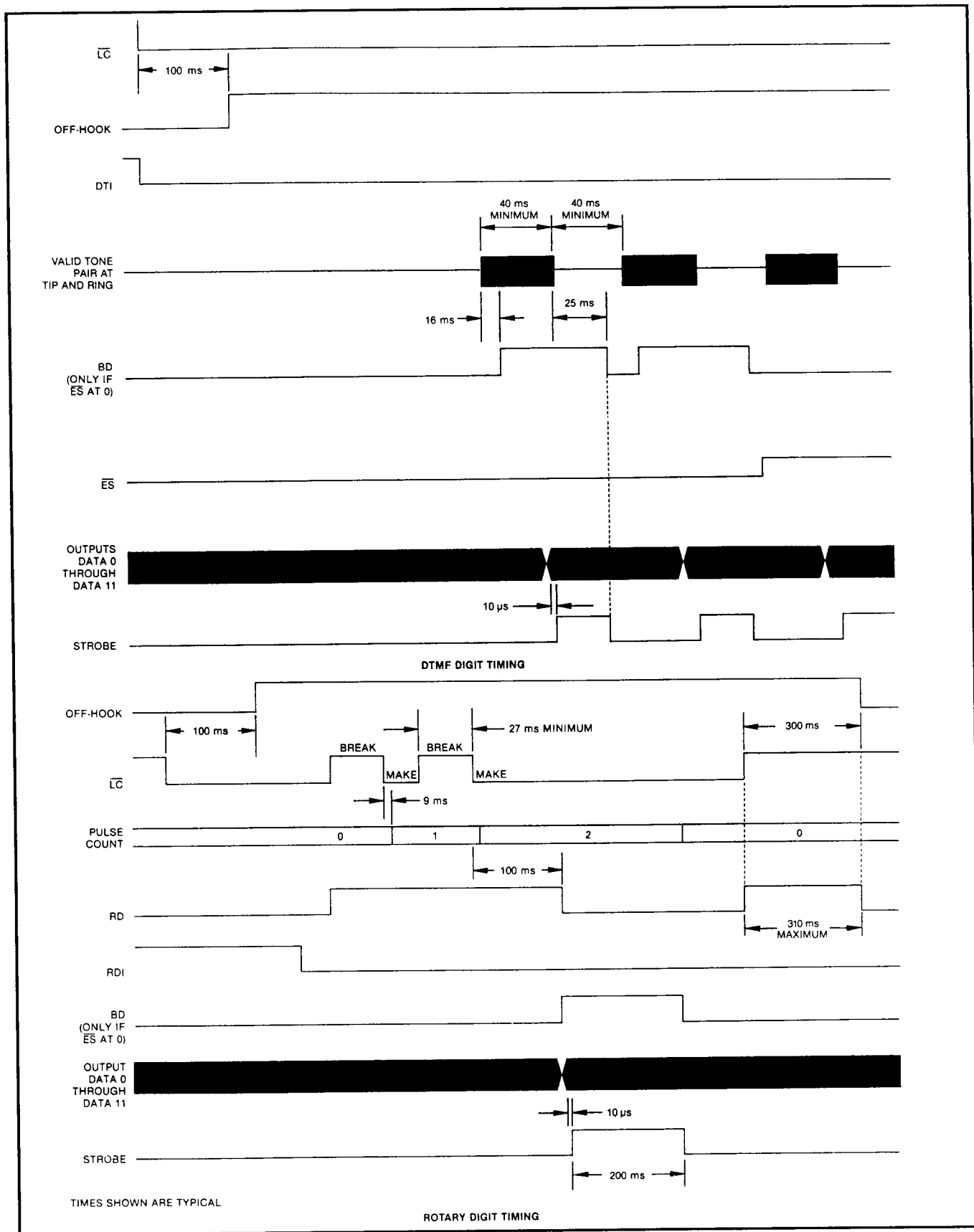
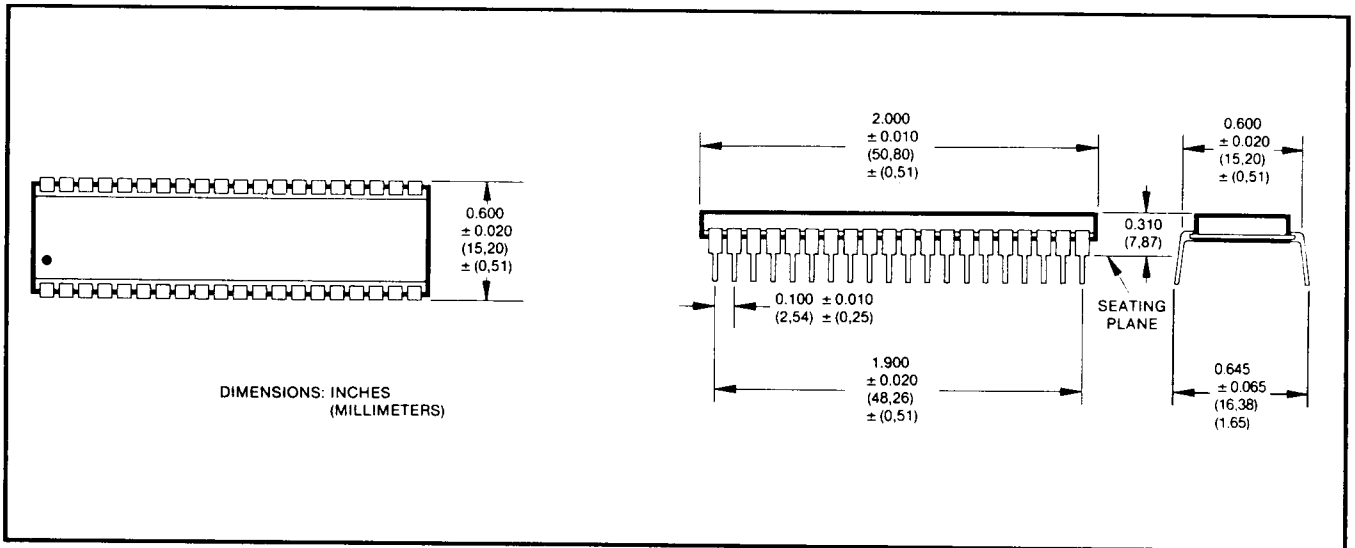**Teltone Corporation,** 22121-20th Avenue SE, Bothell, Washington 98021-4408 U.S.A. Phone: 1-800-426-3926 or 206-487-1515 Fax: 206-487-2288

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Figure 4 Timing Diagram

Figure 5 Package Dimensions

DIMENSIONS: INCHES
(MILLIMETERS)

2.000
± 0.010
(50,80)
± (0,51)

0.600
± 0.020
(15,20)
± (0,51)

0.600
± 0.020
(15,20)
± (0,51)

0.310
(7,87)

0.100 ± 0.010
(2,54) ± (0,25)

SEATING
PLANE

1.900
± 0.020
(48,26)
± (0,51)

0.645
± 0.065
(16,38)
(1.65)
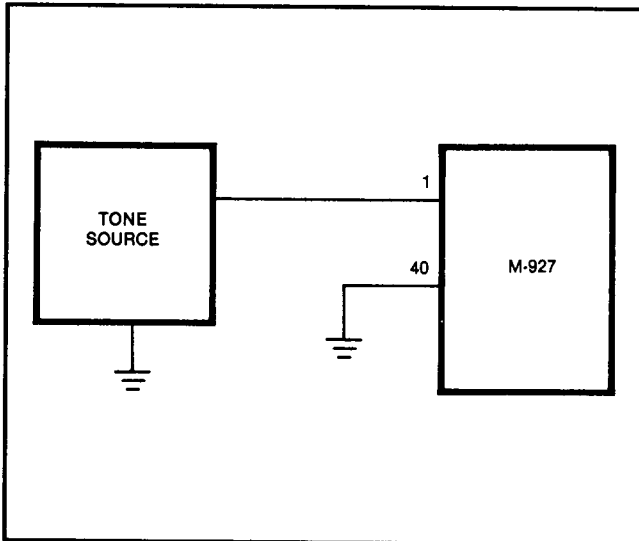
Figure 6 Single-Ended Input

TONE
SOURCE

M-927

1

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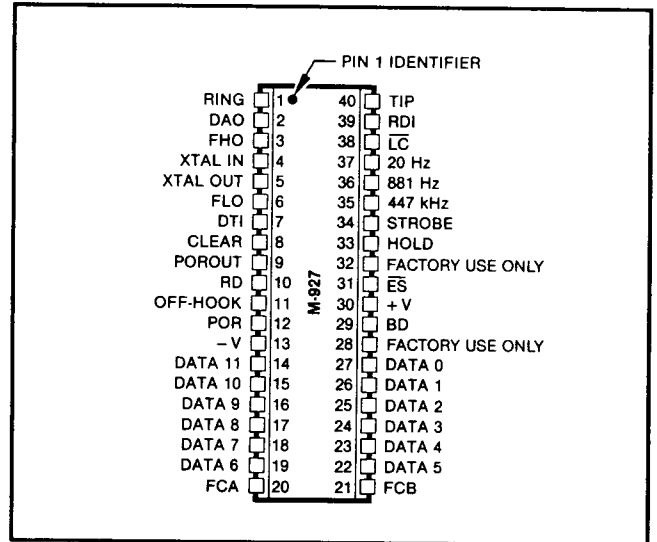
Figure 7 Pin Configuration

PIN 1 IDENTIFIER

RING	1	40	TIP
DAO	2	39	RDI
FHO	3	38	LC
XTAL IN	4	37	20 Hz
XTAL OUT	5	36	881 Hz
FLO	6	35	447 kHz
DTI	7	34	STROBE
CLEAR	8	33	HOLD
POROUT	9	32	FACTORY USE ONLY
RD	10	31	ES
OFF-HOOK	11	30	+V
POR	12	29	BD
−V	13	28	FACTORY USE ONLY
DATA 11	14	27	DATA 0
DATA 10	15	26	DATA 1
DATA 9	16	25	DATA 2
DATA 8	17	24	DATA 3
DATA 7	18	23	DATA 4
DATA 6	19	22	DATA 5
FCA	20	21	FCB

M-927

Table 4 Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)..14.5 V
Power Dissipation ....1.3 W
Voltage on Pins 1 and 40 ....(+V + 250 V) to (−V − 250 V)
Voltage on Any Pin Except 1 and 40 ....(+V + 0.3 V) to (−V − 0.3 V)
Storage Temperature Range ....−40° to 150° C
Operating Temperature Range ....0° to 70° C
Lead Soldering Temperature............................260° C for 5 seconds at 0.035 inches from package

Notes:
1. Exceeding these ratings may damage the M-927.
2. +V referenced to −V. −V may be at ground.