87C196LB
SPECIFICATION UPDATE

Release Date: November, 1998
Order Number: 273002-004

The 87C196LB may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

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REVISION HISTORY

Rev. Date	Version	Description
11/3/98	004	Added documentation changes 3 and 4.
08/07/98	003	Added errata 3 and errata 4, specification change 1, and documentation changes 1 and 2.
04/07/97	002	Added errata 2.
02/03/97	001	This is the new Specification Update Document. It contains all identified errata published prior to this date.

PREFACE

As of July, 1996, Intel has consolidated available historical device and documentation errata into this document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order #
87C196Lx Supplement to 8XC196Kx, 8XC196Jx, 87C196CA User's Manual	272973
87C196LB-20 MHz CHMOS 16-bit Microcontroller datasheet	272807

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 87C196LB product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	A	B	C			
1	X	X	X	7	NoFix	J1850 Transmitter Stall Upon Bus Short
2	X	X	X	8	NoFix	Executing Routines in the User's ROM While the Device is Operating in Serial Programming Mode
3	X	X	X	9	NoFix	Design Consideration: Non Bonded Out Port Pin Logic
4	X	X	X	11	NoFix	RSTSRC Register Functionality

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
	A	B	C			
1			X	12	Doc	AC Characteristics–Table 9

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	A	B	C			
						None for this revision of the Specification Update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	272973-001	14	Doc	Page 6-1, Figure 6-1
2	272973-001	14	Doc	Page 6-2, Figure 6-3
3	272973-002	14	Doc	Page 2-5, Section 2.4, Paragaph 1
4	272973-002	15	Doc	Page 2-6, Figure 2-5

IDENTIFICATION INFORMATION

Markings

87C196LB processors may be identified electrically according to device type and stepping. Refer to the data sheet for instructions on how to obtain the identifier number.

ERRATA

1. J1850 Transmitter Stall Upon Bus Short

PROBLEM: Under certain fault conditions during the transmission of a J1850 message byte, it is possible that the J1850 transmitter state machine may stall resulting in immediate termination of a transmission in progress. Under this condition, further message transmissions from the J1850 module are prohibited until the transmit state machine is reset, either by outside message activity or the execution of a software workaround.

This problem is typically encountered when the J1850 module is transmitting and a bus short to either VSS or VCC occurs on the J1850 bus. A bus short is a fault condition, which under typical operation should not occur. An abrupt stall of the J1850 module during transmission of a message frame is typically seen as an error condition by other nodes on the network. External stimulation, such as reception of a message transmitted by another node, or the execution of the software workaround will reset the J1850 transmit state machine.

In the event of a j1850 transmitter stall, a software workaround may be executed in the absence of external stimuli to reset the J1850 transmit state machine. Execution of the workaround unlocks the J1850 transmitter from a stalled condition. The following workarounds must be executed to guarantee self recovery from a transmit state machine stall.

Case 1: Upon a transmit error (Bit 0, J1850_STAT register = 1).

1. Set the ABORT bit in J1850_CMD register; write data 10h.
2. Clear the ABORT bit in the J1850_CMD register; write data 00h.
3. Overflow the J1850_TX buffer; write same data (ex. 00h) three times to force Overflow condition.
4. Set the ABORT bit in the J1850_CMD register; write data 10h.

Case 2: Prior to a message transmission.

1. Set the ABORT bit in J1850_CMD register; write data 10h.
2. Clear the ABORT bit in the J1850_CMD register; write data 00h.
3. Overflow the J1850_TX buffer; write same data (ex. 00h) three times to force Overflow condition.
4. Set the ABORT bit in the J1850_CMD register; write data 1xh (where x is a non-zero value less than 8h.)

The two implementations of the software workaround are similar except for the last value written to the command register. The write to the J1850_CMD register does two things, setting of the ABORT bit and writing a value to the J1850 MSG bits. The value written to the J1850 MSG bits changes, as noted above, depending on the condition under which the workaround is implemented. This change is necessary to prevent extra “invalid symbols” from being transmitted on the J1850 bus. The above sequences of commands reset the J1850 transmit state machine and enable immediate transmission of a new message.

NOTE:

The three successive writes to the J1850_TX buffer will create an overflow condition and result in a J1850_STAT interrupt. The overflow interrupt occurs immediately after writing the third byte to the J1850_TX register, the user software must be prepared to handle overflow conditions as a result of executing the software workaround.

STATUS: NoFix. Refer to the Summary Table of Changes to determine the affected stepping(s).

2. Executing Routines in the User’s ROM While the Device is Operating in Serial Programming Mode

PROBLEM: All code fetches above the first 8K bytes of user ROM while the device is operating in serial port programming mode will be directed to external memory. Therefore, if the user wants to call any routines in the user ROM, the entire routine must be within the first 8K bytes of memory (0A000 – 0BFFFH in serial port programming mode). For example, if the RISM “GO” command is used with a target address of 0C000H, the device will attempt to fetch code from external memory rather than the on-board ROM.

IMPLICATION: This errata only affects code fetches from the user ROM. Data fetches to the entire ROM work correctly. It is not possible to execute code from above the first 8K byte of user ROM while the device is operating in Serial Port Programming mode.

WORKAROUND: None.

STATUS: NoFix. Refer to the Summary Table of Changes to determine the affected stepping(s).

3. Design Consideration: Non Bonded Out Port Pin Logic

PROBLEM: The 87C196LB contains one input only and six I/O ports, Port 0 through Port 6. Each of these seven ports consists of eight-bits, and may function as LSIO or Special Function. The controller is available only in 52ld PLCC packaging, constraining the total I/O, and limiting the number of available port pins on any given port.

When programming the LB micro, the user software must ensure that values contained in unused bits of the port registers are not relied upon for any operation, such as a conditional branch or jump instruction. These bits should be masked off in the user software.

Port 0: Port 0 is an eight-bit port with shared functionality between the Analog to Digital converter (SFR) and a high impedance input only port. There are six Port 0 pins bonded out, P0.2 through P0.7. The P0.0 and P0.1 pins are not bonded out and the analog inputs for these two channels at the multiplexer are tied to V_{REF}. Therefore, initiating a conversion on ACH1 results in a value equal to full scale (3FFH). The digital inputs for these two channels are tied to ground, therefore reading P0.0 or P0.1 results in a digital "0". However, it is recommended that the user software not rely on the value read from the P0.0 or P0.1 bit locations for any operation.

Port 1: Port 1 is an eight-bit port with shared functionality between the EPA (Event Processor Array) and a low speed input/output (LSIO) port. There are four Port 1 pins bonded out, P1.0 through P1.3. The P1.4 through P1.7 pins have been removed from the device and is not available to the programmer. Corresponding bits in the port registers have been "hard-wired" to provide the following results when read. However, it is recommended that the user software not rely on the value read from the P1.4 through P1.7 registers for any operations.

Register Bits		When Read
P1_PIN.x	(x = 4,5,6,7)	1
P1_REG.x	(x = 4,5,6,7)	1
P1_DIR.x	(x = 4,5,6,7)	1
P1_MODE.x	(x = 4,5,6,7)	0

Port 2: Port 2 is an eight-bit port with shared functionality between multiple SFR function and a low speed input/output (LSIO) port. Port 2 has six of the eight pins bonded out, P2.0 through P2.2, P2.4 and P2.6, P2.7. P2.3 and P2.5 have been removed from the device and are not available to the programmer. Corresponding bits in the port registers have been "hard-wired"

to provide the following results when read. However, it is recommended that the user software not rely on the value read from the P2.3 and P2.5 registers for any operations.

Register Bits		When Read
P2_PIN.x	(x = 3,5)	1
P2_REG.x	(x = 3,5)	1
P2_DIR.x	(x = 3,5)	1
P2_MODE.x	(x = 3,5)	0

Port 3, Port 4: Port 3 and Port 4 are eight-bit, bidirectional, memory-mapped I/O ports. They can be addressed only with indirect or indexed addressing and cannot be windowed. Ports 3 and 4 provide the multiplexed address/data bus. In programming modes, ports 3 and 4 serve as the programming bus (PBUS). Port 3 and 4 can also serve as LSIO when executing from internal memory. The entire Port 3 and Port 4 logic exists on the LB micro.

Port 5: Port 5 is an eight-bit, bidirectional port which can be configured to supply the bus-control signals (for external operation) or LSIO when running from internal memory. The LB micro has three Port 5 pins available, P5.0, P5.2 and P5.3. The remaining Port 5 pins, P5.1, P5.4 through P5.7 are not bonded out in the 52ld package, however, the port logic associated with these Port 5 bits remains. It is important that the users software does not rely on values contained in the non-bonded Port 5 bits. The value in these bit locations may be undefined after power-up reset, and thus the user software must not rely on these bit locations for any device operation.

Port 6: Port 6 is an eight-bit, bidirectional port which can be configured for special function (SSIO, EPA) or to operate as LSIO. Six of the Port 6 pins are bonded out in the 52ld package, P6.0, P6.1 and P6.4 through P6.7. The remaining two pins, P6.2 and P6.3 have been removed from the device and are not available to the programmer. Corresponding bits in the port registers have been “hard-wired” to provide the following results when read. However, it is recommended that the user software not rely on the value read from the P6.2 and P6.3 registers for any operations.

Register Bits		When Read
P6_PIN.x	(x = 2,3)	1
P6_REG.x	(x = 2,3)	1
P6_DIR.x	(x = 2,3)	1
P6_MODE.x	(x = 2,3)	0

IMPLICATION: Failure to abide by the above may result in unpredictable operation of the user's software.

WORKAROUND: As described above.

STATUS: NoFix. Refer to the Summary Table of Changes to determine the affected stepping(s).

4. RSTSRC Register Functionality

PROBLEM: The RSTSRC register was designed to be initialized to 00h on a V_{CC} power-up condition. However, due to a product erratum, the RSTSRC register may not be initialized to 00h on a V_{CC} power-up condition. As a result, the state of the RSTSRC register on a V_{CC} power-up condition is indeterminate.

IMPLICATION: Applications that rely on the RSTSRC register to be 00h on V_{CC} power-up may be adversely affected.

STATUS: NoFix. Refer to the Summary Table of Changes to determine the affected stepping(s).

SPECIFICATION CHANGES

1. AC Characteristics–Table 9

ISSUE: Four AC parameters have been changed as follows:

- Old

  T_{CHCL} max = t + 20 ns
  T_{CLLH} min = -10 ns
  T_{RLCL} min = 0 ns
  T_{CLWL} min = -5 ns

- New

  T_{CHCL} max = t + 25 ns
  T_{CLLH} min = -15 ns
  T_{RLCL} min = -5 ns
  T_{CLWL} min = -10 ns

AFFECTED DOCUMENTS: *87C196LB-20 MHz CHMOS 16-bit Microcontroller* datasheet (order number 272807)

SPECIFICATION CLARIFICATIONS

None for this revision of the specification update.

DOCUMENTATION CHANGES

1. Page 6-1, Figure 6-1

ISSUE: SSIO0-CLK register address is incorrect. The SSIO0-CLK address should be 1FB5h.

- Old

  Address: 1F95h

- New

  Address: 1FB5h

AFFECTED DOCUMENTS: *8XC196LX Supplement to 8XC196Kx, 8XC196Jx, 87C196CA User's Manual* (order number 272973)

2. Page 6-2, Figure 6-3

ISSUE: SSIO1-CLK register address is incorrect. The SSIO1-CLK address should be 1FB7h.

- Old

  Address: 1F97h

- New

  Address: 1FB7h

AFFECTED DOCUMENTS: *8XC196LX Supplement to 8XC196Kx, 8XC196Jx, 87C196CA User's Manual* (order number 272973)

3. Page 2-5, Section 2.4, Paragaph 1

PROBLEM: Description of CLKOUT frequencies in paragraph 1 of section 2.4 is incorrect.

- Old

  2.4 External Timing

  You can control the output frequency on the CLKOUT pin by programming two uneraseable PROM bits. Figure 2-5 illustrates the read-only USFR1, which reflects the state of the uneraseable PROM bits. You can select from one of three frequencies: f/2, f/4, or f/8. As figure 2-2 on page 2-3 shows, the configurable divider accepts the outputs of the clock generators (f/2) and further divides the frequency to produce the desired output frequency. The CLK1:0 bits control the divisor (divide f/2 by either 1, 2, or 4).

- New

  2.4 External Timing

  You can control the output frequency on the CLKOUT pin by programming two uneraseable PROM bits. Figure 2-5 illustrates the read-only USFR1, which reflects the state of the uneraseable PROM bits. You can select from one of three frequencies: f, f/2, or f/4. As figure 2-2 on page 2-3 shows, the configurable divider accepts the outputs of the clock generators (f/2) and further divides (or multiplies) the frequency to produce the desired output frequency. The CLK1:0 bits control the divisor (divide f/2 by either 1/2, 1, or 2).

AFFECTED DOCUMENTS: *8XC196Lx Supplement to 8XC196Kx, 8XC196Jx, 87C196CA User's Manual* (order number 272973)

4. Page 2-6, Figure 2-5

PROBLEM: The CLKOUT frequencies listed in the figure are incorrect.

- Old

CLK1	CLK2	
0	0	divide by 1 (CLKOUT=f/2)
0	1	divide by 2 (CLKOUT=f/4)
1	0	divide by 4 (CLKOUT=f/8)
1	1	divide by 1 (CLKOUT=f/2)

- New

CLK1	CLK2	
0	0	divide by 1 (CLKOUT=f/2)
0	1	multiply by 2 (CLKOUT=f)
1	0	divide by 2 (CLKOUT=f/4)
1	1	divide by 1 (CLKOUT=f/2)

AFFECTED DOCUMENTS: *8XC196Lx Supplement to 8XC196Kx, 8XC196Jx, 87C196CA User's Manual* (order number 272973)