REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added device types 05 through 10. Added case outlines X, Z, and T. Redrew entire document.	96-08-23	K. A. Cottongim
B	Added device types 11 through 13. Added case outline U.	96-10-22	K. A. Cottongim
C	Made changes in accordance with NOR 5962-R289-97. -sld	97-04-28	K. A. Cottongim
D	Table I; Changed the max limit for the operating supply current test I_{CC} for device types 05-10 from 130 mA to 135 mA. Table I; Changed the max limit for data retention current (I_{CCDR1}) for device types 05-10 from 3.0 mA to 7.0 mA. Add vendor cage 88379 for device types 11, 12, and 13 per letter dated 1 MAY 1997. -sld	98-02-18	K. A. Cottongim
E	Add device type 14.	98-06-22	K. A. Cottongim
F	Changes to case outlines U and X.	99-04-30	K. A. Cottongim

REV																				
SHEET																				
REV	F	F	F	F	F	F	F	F	F	F										
SHEET	15	16	17	18	19	20	21	22	23	24										

REV STATUS OF SHEETS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Steve L. Duncan

CHECKED BY
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APPROVED BY
Kendall A. Cottongim

DRAWING APPROVAL DATE
95-11-07

REVISION LEVEL
F

DEFENSE SUPPLY CENTER COLUMBUS
P. O. BOX 3990
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, MEMORY, DIGITAL, SRAM,
512K x 8-BIT, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-95613**

SHEET 1 OF 24

DSCC FORM 2233
APR 97

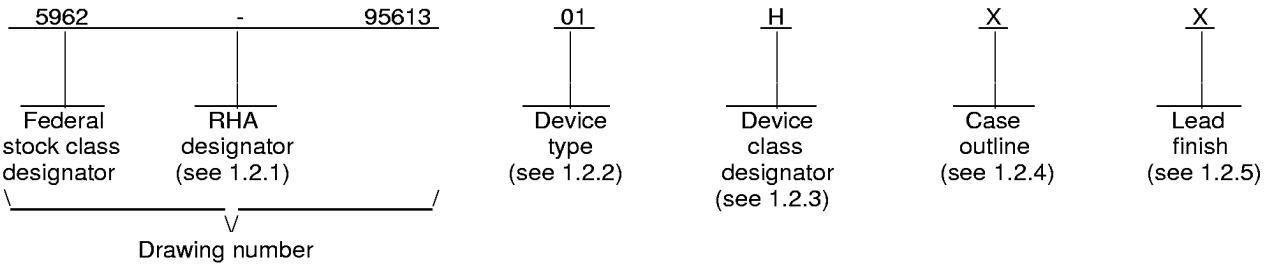
5962-E165-99

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents one product assurance class, class H (high reliability) for monolithic microcircuits to be processed in accordance with of MIL-PRF-38534. A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	WMS512K8-120	512K x 8 bit SRAM	120 ns
02	WMS512K8-100	512K x 8 bit SRAM	100 ns
03	WMS512K8-85	512K x 8 bit SRAM	85 ns
04	WMS512K8-70	512K x 8 bit SRAM	70 ns
05	ACT-S512K8N-055,WMS512K8-55	512K x 8 bit SRAM	55 ns
06	ACT-S512K8N-045,WMS512K8-45	512K x 8 bit SRAM	45 ns
07	ACT-S512K8N-035,WMS512K8-35	512K x 8 bit SRAM	35 ns
08	ACT-S512K8N-025,WMS512K8-25	512K x 8 bit SRAM	25 ns
09	ACT-S512K8N-020,WMS512K8-20	512K x 8 bit SRAM	20 ns
10	ACT-S512K8N-017,WMS512K8-17	512K x 8 bit SRAM	17 ns
11	ACT-S512K8M-045,WMS512K8M-45	512K x 8 bit SRAM	45 ns
12	ACT-S512K8M-035,WMS512K8M-35	512K x 8 bit SRAM	35 ns
13	ACT-S512K8M-025,WMS512K8M-25	512K x 8 bit SRAM	25 ns
14	WMS512K8-15	512K x 8 bit SRAM	15 ns

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device performance documentation
H	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
T	See figure 1	32	SOJ, ceramic, evolutionary pinout
U	See figure 1	36	Flatpack, ceramic, with or without pedestal
X	See figure 1	36	Flatpack, ceramic, with non-conductive tie bar, with or without pedestal
Y	See figure 1	32	DIP, ceramic, single cavity
Z	See figure 1	36	SOJ, ceramic

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Signal voltage range (V_g)	-0.5 V dc to V_{CC} +0.5
Power dissipation (P_D)	1.1 W max
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input low voltage range (V_{IL})	-0.3 V dc to +0.8 V dc
Input high voltage range (V_{IH})	+2.2 V dc to V_{CC} +0.3 V dc
Output low voltage, maximum (V_{OL})	+0.4 V dc
Output high voltage, minimum (V_{OH})	+2.4 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. The following specification, standards, and handbook form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device class H shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for applicable device class. Therefore, the tests and inspections herein may not be performed for applicable device class (see MIL-PRF-38534). Futhermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figures 4 and 5.

3.2.5 Block diagram. The block diagram shall be as specified on figure 6.

3.2.6 Output load circuit. The output load circuit shall be as specified on figure 7.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in QML-38534.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance submitted to DSCC-VA shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38534 and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table 1 of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$, $V_{SS} = 0$ Vdc, $+4.5$ Vdc $\le V_{CC} \le +5.5$ Vdc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
DC parameters							
Operating supply current	I_{CC}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 5 MHz, V_{CC} = 5.5 Vdc	1,2,3	01-04		50	mA
				05-10		160	
				11-14		200	
Standby current	I_{SB}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, f = 5 MHz, V_{CC} = 5.5 Vdc	1,2,3	01-04		1	mA
				05-10		20	
				11-14		30	
Input leakage current	I_{LI}	V_{CC} = 5.5 V dc, V_{IN} = GND or V_{CC}	1,2,3	All		10	μA
Output leakage current	I_{LO}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, V_{OUT} = GND or V_{CC}	1,2,3	All		10	μA
Output low voltage	V_{OL}	V_{CC} = +4.5 V dc, I_{OL} = 2.1 mA	1,2,3	01-06		0.4	V
		V_{CC} = +4.5V dc, I_{OL} = 8.0 mA		07-14		0.4	
Output high voltage	V_{OH}	V_{CC} = +4.5 V dc, I_{OH} = -1.0 mA	1,2,3	01-06	2.4		V
		V_{CC} = +4.5V dc, I_{OH} = -4.0 mA		07-14	2.4		
Data Retention Characteristics							
Data Retention Supply voltage	V_{DR}	$\overline{CS} \ge V_{CC}$ -0.2	1,2,3	All	2.0	5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V	1,2,3	01-04		0.4	mA
				05-10, 14		7.0	
				11-13		10.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{SS} = 0 Vdc +4.5 Vdc $\le V_{CC} \le$ +5.5 Vdc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Capacitance							
Input capacitance	C_{IN}	V_{IN} = 0 V, f = 1.0 MHz, $T_A = +25°C$, Case outlines T and Y	4	01-04 05-14		12 20	pF
		V_{IN} = 0 V, f = 1.0 MHz, $T_A = +25°C$, Case outlines X, U, and Z	4	01-04 05-14		20 12	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V, f = 1.0 MHz, $T_A = +25°C$, Case outlines T and Y	4	01-04 05-14		12 20	pF
		V_{OUT} = 0 V, f = 1.0 MHz, $T_A = +25°C$, Case outlines X, U, and Z	4	01-04 05-14		20 12	pF
Functional testing							
Functional tests		See 4.3.1c	7,8A,8B	All			
Read cycle AC timing characteristics							
Read cycle time	t_{RC}	See figure 4	9,10,11	01 02 03 04 05 06,11 07,12 08,13 09 10 14	120 100 85 70 55 45 35 25 20 17 15		ns
Address access time	t_{AA}	See figure 4	9,10,11	01 02 03 04 05 06,11 07,12 08,13 09 10 14		120 100 85 70 55 45 35 25 20 17 15	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ $V_{SS} = 0$ Vdc $+4.5$ Vdc $\le V_{CC} \le +5.5$ Vdc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Read cycle AC timing characteristics - Continued.							
Output hold from address change	t_{OH}	See figure 4	9,10,11	01-04, 14	5		ns
				05-13	0		
Chip select access time	t_{ACS}	See figure 4	9,10,11	01		120	ns
				02		100	
				03		85	
				04		70	
				05		55	
				06,11		45	
				07,12		35	
				08,13		25	
				09		20	
				10		17	
				14		15	
Output Enable to output valid	t_{OE}	See figure 4	9,10,11	01		60	ns
				02		50	
				03		40	
				04,11		35	
				05-07,12		25	
				08,13		12	
				09		10	
				10		9	
				14		8	
Chip Select to output in low impedance 2/	t_{CLZ}	See figure 4	9,10,11	01-04	10		ns
				05-07, 11,12	4		
				08-10, 13,14	2		
Output Enable to output in low impedance 2/	t_{OLZ}	See figure 4	9,10,11	01-04	5		ns
				05-14	0		
Chip Select high to output in high impedance 2/	t_{CHZ}	See figure 4	9,10,11	01,02		35	ns
				03,04		25	
				05,06		20	
				07,11,12		15	
				08,13		12	
				09		10	
				10		9	
				14		8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ $V_{SS} = 0$ Vdc $+4.5$ Vdc $\le V_{CC} \le +5.5$ Vdc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Read cycle AC timing characteristics - Continued.							
Output Enable high to output in high impedance 2/	t_{OHZ}	See figure 4	9,10,11	01,02		35	ns
				03,04		25	
				05,06		20	
				07,11,12		15	
				08,13		12	
				09		10	
				10		9	
				14		8	
Write cycle AC timing							
Write cycle time	t_{WC}	See figure 5	9,10,11	01	120		ns
				02	100		
				03	85		
				04	70		
				05	55		
				06,11	45		
				07,12	35		
				08,13	25		
				09	20		
				10	17		
				14	15		
Chip Select to end of write	t_{CW}	See figure 5	9,10,11	01	100		ns
				02	80		
				03	75		
				04	60		
				05	50		
				06,11	35		
				07,12	25		
				08	15		
				09,10	14		
				13	17		
				14	13		
Address valid to end of write	t_{AW}	See figure 5	9,10,11	01	100		ns
				02	80		
				03	75		
				04	60		
				05	50		
				06,11	35		
				07,12	25		
				08	15		
				09,10	14		
				13	17		
				14	13		

See footnotes at end of table.

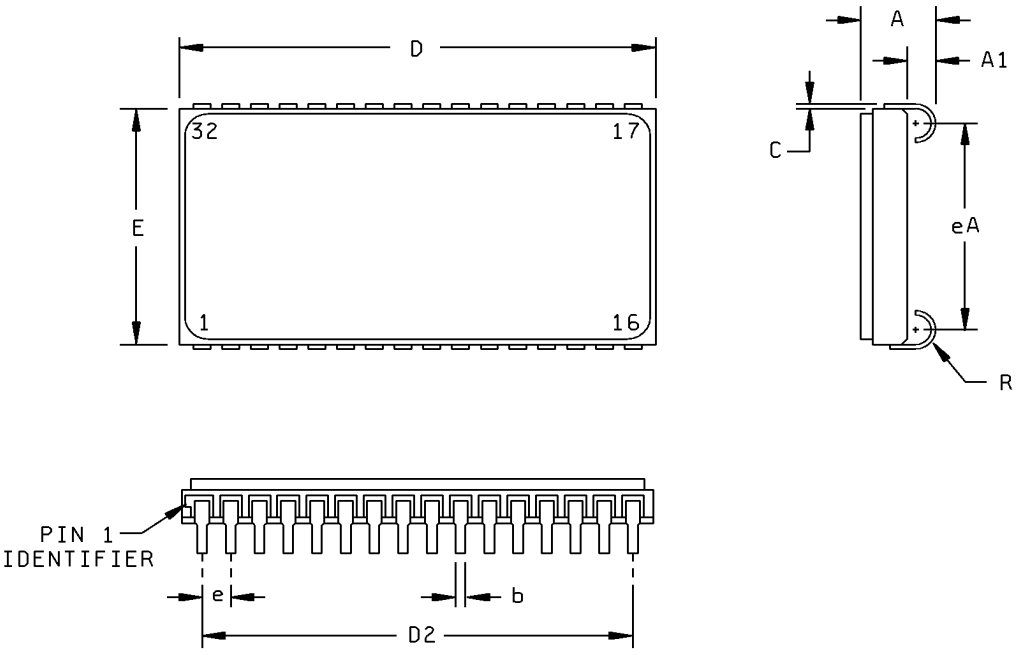
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{SS} = 0 Vdc +4.5 Vdc $\le V_{CC} \le$ +5.5 Vdc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Write cycle AC timing - Continued.							
Data Valid to end of write	t_{DW}	See figure 5	9,10,11	01,02 03,04,11 05,06 07,12 08,09 10 13 14	40 30 25 20 10 9 15 8		ns
Address setup time	t_{AS}	See figure 5	9,10,11	All	2		ns
Write pulse width	t_{WP}	See figure 5	9,10,11	01,02 03,04 05 06,11 07,12 08 09,10 13 14	60 50 40 35 25 15 14 17 13		ns
Write enable to output in high impedance 2/	t_{WHZ}	See figure 5	9,10,11	01,02 03-05 06 07 11,12 08,13 09,10 14		35 25 15 20 15 10 9 8	ns
Address hold time	t_{AH}	See figure 5	9,10,11	01-06 07-13	5 0		ns
Output active from 2/ end of write	t_{OW}	See figure 5	9,10,11	01-06 07-13	5 0		ns
Data hold time	t_{DH}	See figure 5	9,10,11	All	0		ns

1/ Unless otherwise specified, the AC test conditions are as follows:
Input pulse levels: V_{IL} = 0 V and V_{IH} = 3.0 V.
Input rise and fall times: 5 nanoseconds.
Input and output timing reference levels: 1.5 V, ± 0.5 V.
Output loading: See figure 7.
Unless otherwise specified the DC test conditions are as follows:
V_{IL} = 0.3 V, $V_{IH} = V_{CC}$ -0.3 V.

2/ Parameters shall be tested as part of device characterization and after design and process changes. Parameters shall be to the limits specified in table I for all lots not specifically tested.

Case outline T.

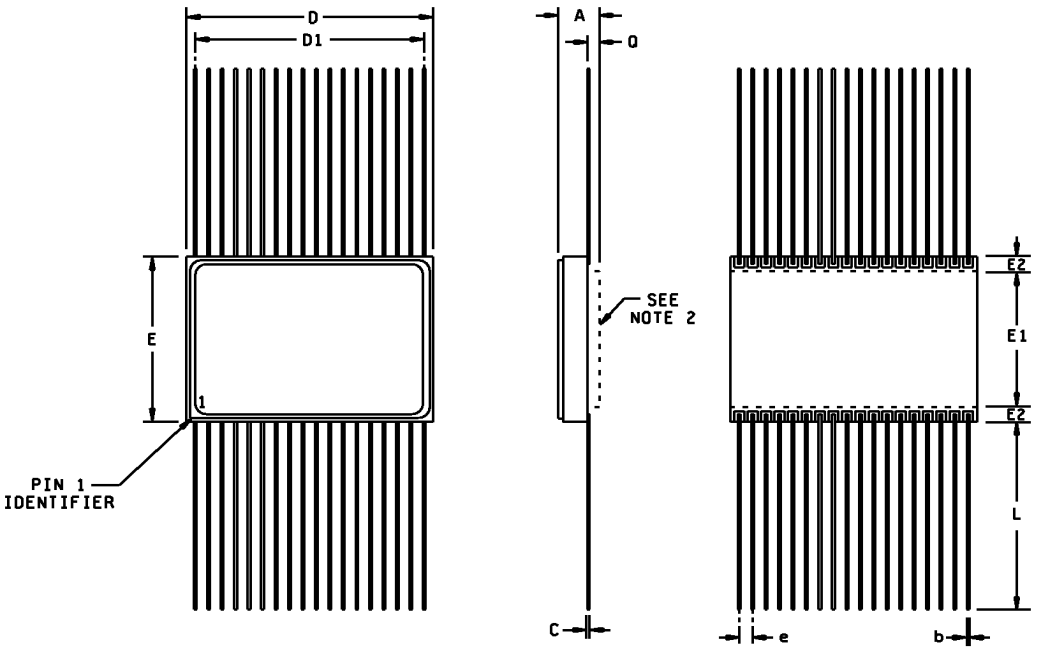


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.69	3.96	0.106	0.156
A1	1.02	1.52	0.040	0.060
b	0.38	0.48	0.015	0.019
C	0.15	0.25	0.006	0.010
D	20.83	21.34	0.820	0.840
D2	18.92	19.18	0.745	0.755
E	10.80	11.05	0.425	0.435
e	1.27 TYP		0.050 TYP	
eA	9.30	9.80	0.366	0.386
R	0.89 TYP		0.035 TYP	

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s).

Case outline U.



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.26	3.18	0.089	0.125
b	0.38	0.48	0.015	0.019
C	0.08	0.18	0.003	0.007
D	23.11	23.62	0.910	0.930
D1	21.46	21.72	0.845	0.855
E	12.83	13.08	0.505	0.515
E1	9.78	10.03	0.385	0.395
E2	1.40	1.65	0.055	0.065
e	1.27 TYP		0.050 TYP	
L	7.62	8.89	0.300	0.350
Q	0.38	0.96	0.015	0.038

NOTE:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. The case outline U is available in either a pedestal or non-pedestal package. The Q dimension only applies to the pedestal version of case outline U.

FIGURE 1. Case outline(s) - Continued.

Case outline X.

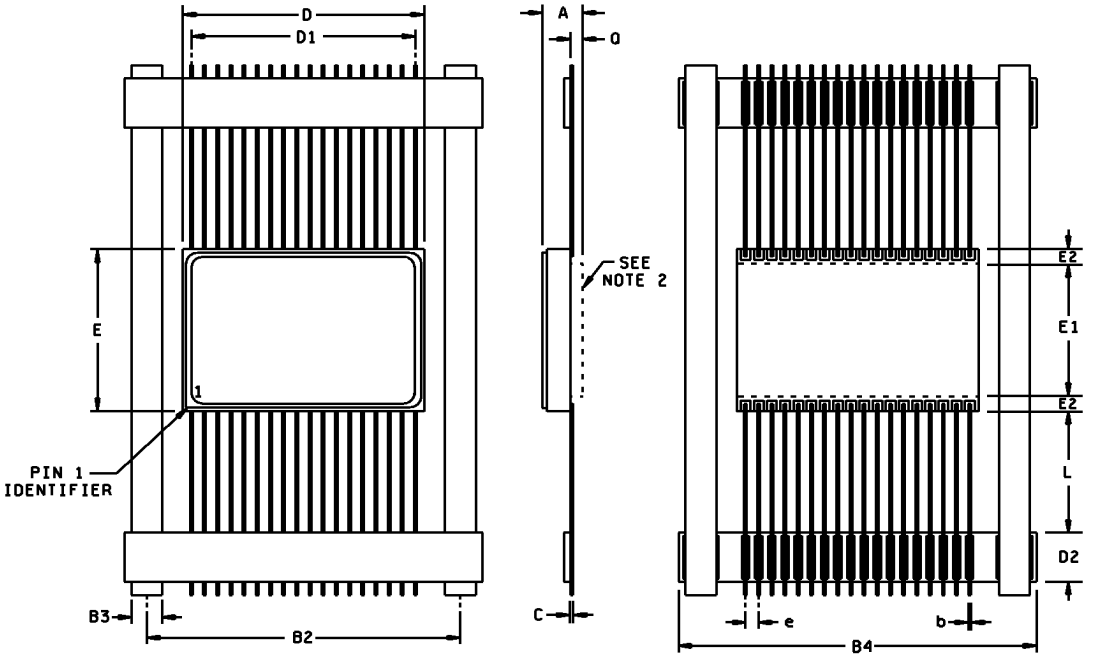


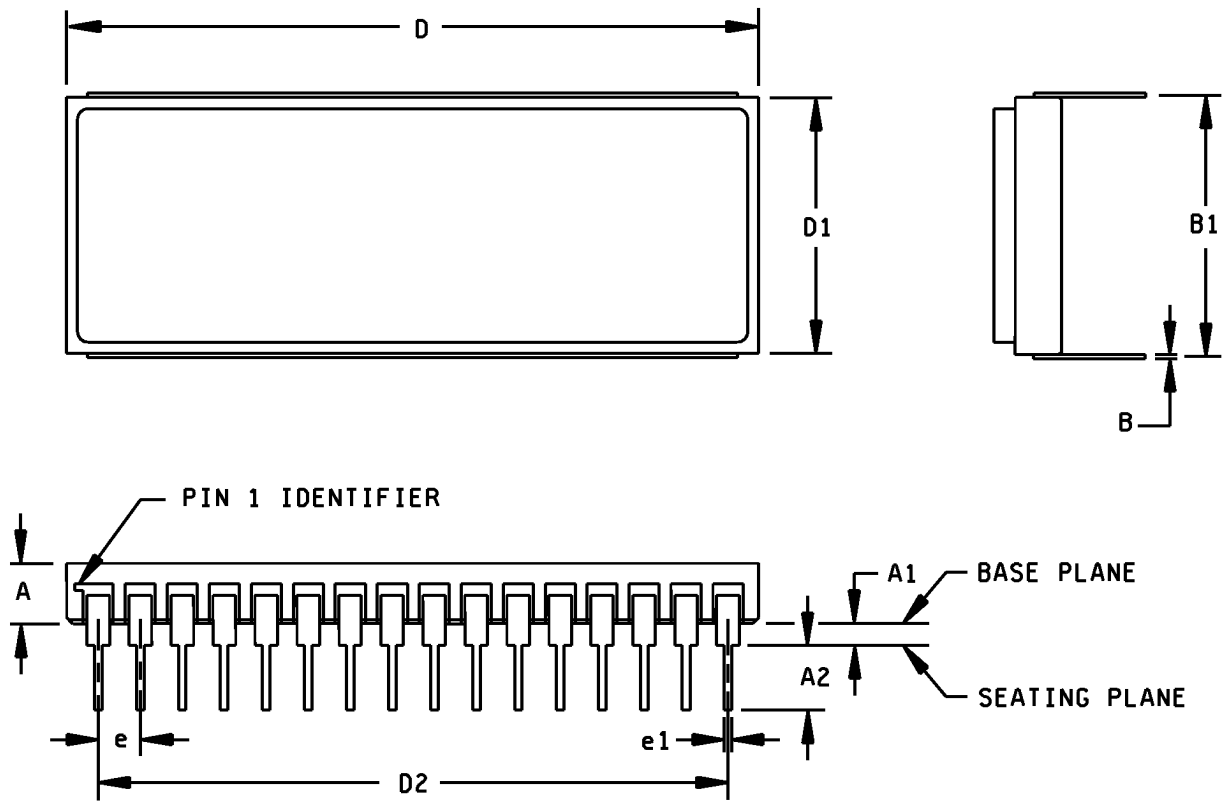
FIGURE 1. Case outline(s) - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.31	3.18	0.091	0.125
b	0.38	0.48	0.015	0.019
B2	32.64 TYP		1.285 TYP	
B3	3.81 TYP		0.150 TYP	
B4	37.72	38.48	1.485	1.515
C	0.08	0.18	0.003	0.007
D	23.11	23.62	0.910	0.930
D1	21.46	21.72	0.845	0.855
D2	4.83	5.33	0.190	0.210
E	12.83	13.08	0.505	0.515
E1	9.78	10.03	0.385	0.395
E2	1.40	1.65	0.055	0.065
e	1.27 TYP		0.050 TYP	
L	12.19	13.21	0.480	0.520
Q	0.38	0.64	0.015	0.025

NOTE:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. The case outline X is available in either a pedestal or non-pedestal package. The Q dimension only applies to the pedestal version of case outline X.

FIGURE 1. Case outline(s) - Continued.

Case outline Y.

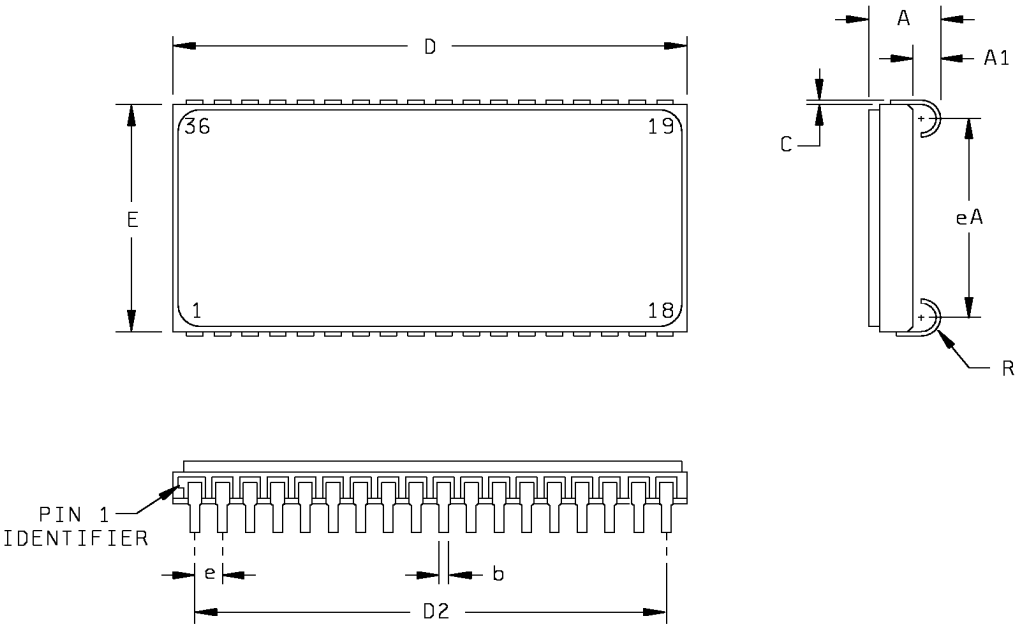


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.48	5.13	0.137	0.202
A1	0.48	1.52	0.019	0.060
A2	3.18		0.125	
B	0.23	0.30	0.009	0.012
B1	14.99	15.49	0.590	0.610
D	40.56	42.82	1.597	1.686
D1	14.73	15.34	0.580	0.604
D2	37.90	38.30	1.492	1.508
e	2.41	2.67	0.095	0.105
e1	0.41	0.51	0.016	0.020

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. For solder lead finish, dimensions B and e1 will increase by +0.003" (+.008 mm).

Figure 1. Case outline(s) - Continued.

Case outline Z.



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.54	4.67	0.136	0.184
A1	1.02	1.52	0.040	0.060
b	0.38	0.48	0.015	0.019
C	0.15	0.25	0.006	0.010
D	23.11	23.62	0.910	0.930
D2	21.46	21.72	0.845	0.855
E	10.80	11.05	0.425	0.435
e	1.27 TYP		0.050 TYP	
eA	9.30	9.80	0.366	0.386
R	0.89 TYP		0.035 TYP	

NOTE
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.

FIGURE 1. Case outline(s) - Continued.

Device types	All	Device types	All
Case outlines	T and Y	Case outlines	T and Y
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A18	17	I/O3
2	A16	18	I/O4
3	A14	19	I/O5
4	A12	20	I/O6
5	A7	21	I/O7
6	A6	22	$\overline{CS}$
7	A5	23	A10
8	A4	24	$\overline{OE}$
9	A3	25	A11
10	A2	26	A9
11	A1	27	A8
12	A0	28	A13
13	I/O0	29	$\overline{WE}$
14	I/O1	30	A17
15	I/O2	31	A15
16	V_{SS}	32	V_{CC}

FIGURE 2. Terminal connections.

Device types	05, 06, 07, 08, 09, and 10l	Device types	05, 06, 07, 08, 09, and 10
Case outlines	U, X, and ,Z	Case outlines	U, X,, and Z
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A0	19	NC
2	A1	20	A10
3	A2	21	A11
4	A3	22	A12
5	A4	23	A13
6	$\overline{CS}$	24	A14
7	I/O0	25	I/O4
8	I/O1	26	I/O5
9	V_{CC}	27	V_{CC}
10	V_{SS}	28	V_{SS}
11	I/O2	29	I/O6
12	I/O3	30	I/O7
13	$\overline{WE}$	31	$\overline{OE}$
14	A5	32	A15
15	A6	33	A16
16	A7	34	A17
17	A8	35	A18
18	A9	36	NC

FIGURE 2. Terminal connections - Continued.

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data out	Active
L	H	H	Output disable	High Z	Active
L	X	L	Write	Data in	Active

NOTES:
1. H = V_{IH} = High Logic Level.
2. L = V_{IL} = Low Logic Level.
3. X = Do not care (either high or low).
4. High Z = High Impedance state.

FIGURE 3. Truth Table.

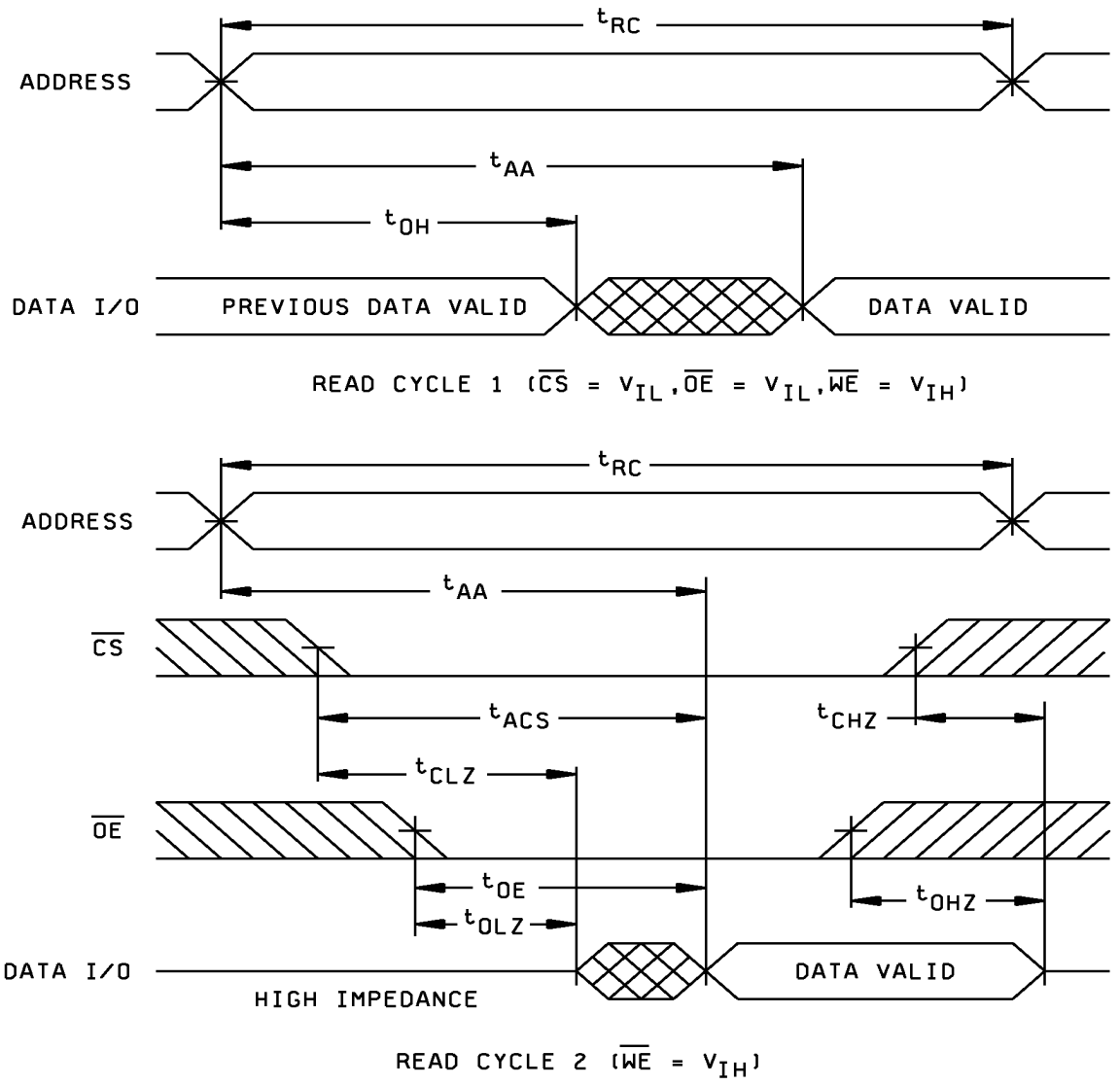
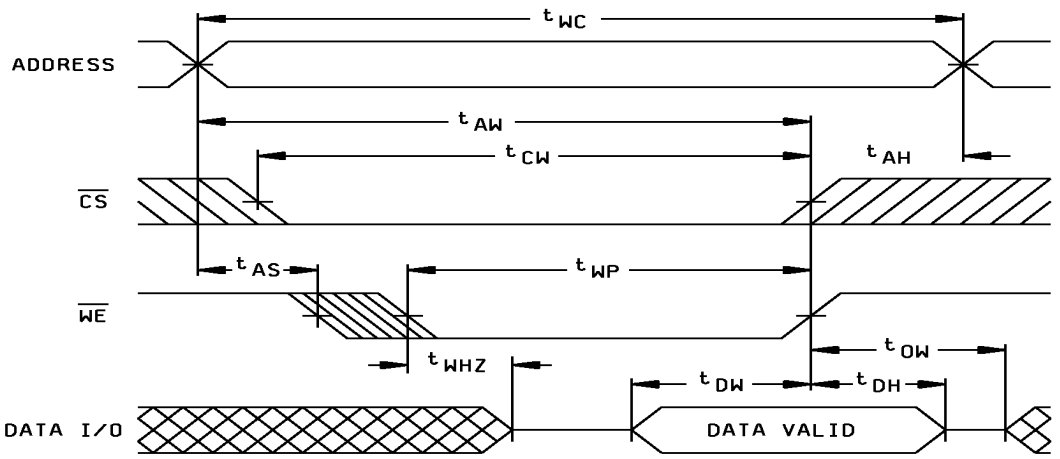
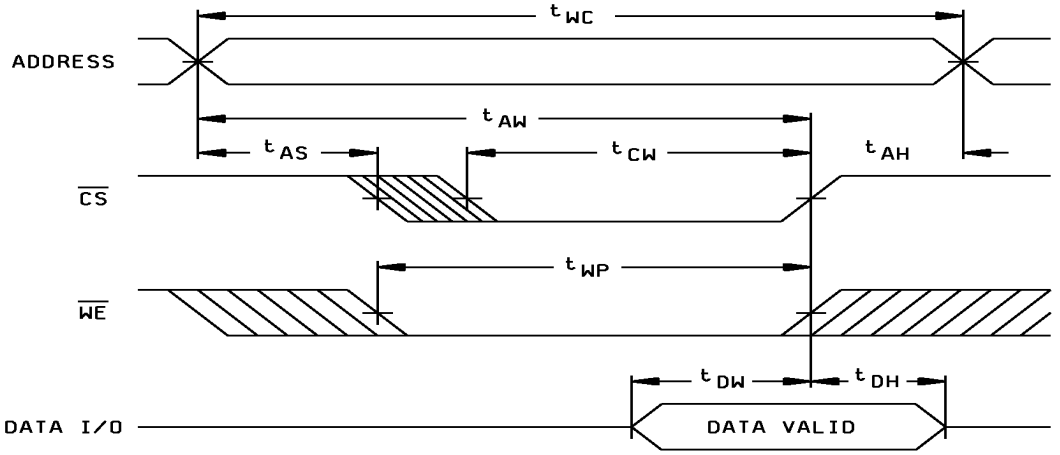


FIGURE 4. Read cycle timing diagram.



WRITE CYCLE 1 $\overline{WE}$ CONTROLLED



WRITE CYCLE 2 $\overline{CS}$ CONTROLLED

FIGURE 5. Write cycle timing diagram.

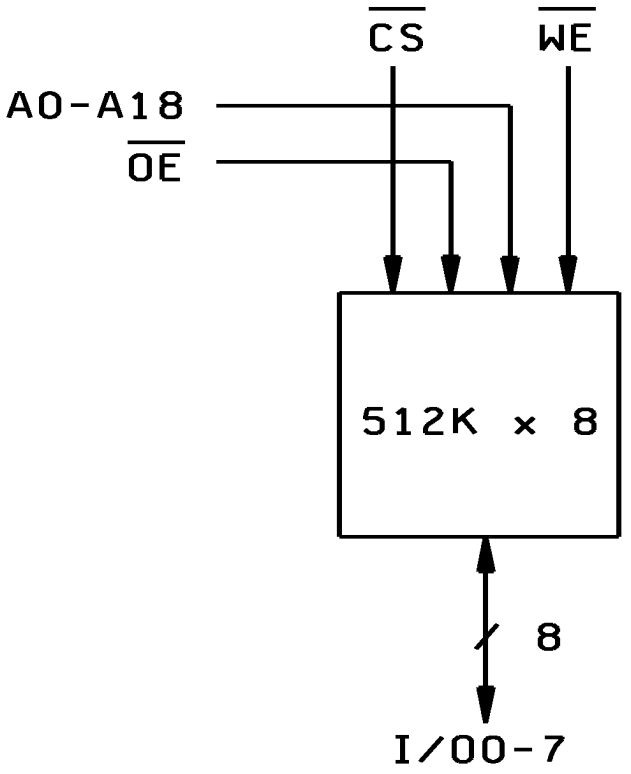
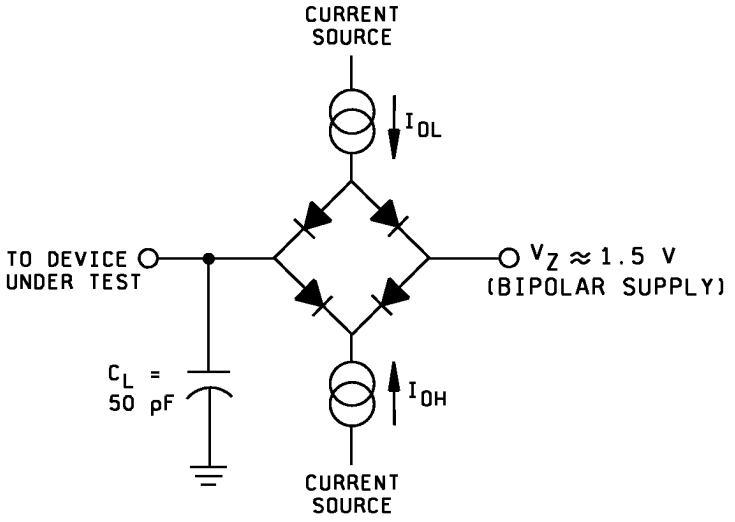


FIGURE 6. Block diagram.



Parameter	Typ.	Unit
Input pulse level	0 - 3.0	V
Input rise and fall	5	ns
Input and output reference level	1.5	V
Output load capacitance	50	pF

NOTES:
1. V_Z is programmable from -2 V to +7 V.
2. I_{OL} and I_{OH} are programmable from 0 to 16 mA.
3. Tester impedance is ZO = 75 ohms.
4. V_Z is typically the midpoint of V_{OH} and V_{OL}.
5. I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.
6. ATE tester includes jig capacitance.

FIGURE 7. Output load circuit.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,4,7,9
Final electrical parameters	1*,2,3,4,7,8A,8B,9,10,11
Group A test requirements	1,2,3,4,7,8A,8B,9,10,11
Group C end-point electrical parameters	1,2,3,4,7,8A,8B,9,10,11
MIL-STD-883, group E end-point electrical parameters for RHA devices	Subgroups** (in accordance with method 5005, group A test table)

* PDA applies to subgroup 1.
** When applicable to this standard microcircuit drawing, the subgroups shall be defined.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table on figure 3.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes H and K shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes H and K for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table II herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

d. For device classes H and K, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-7603.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, P. O. Box 3990, Columbus, Ohio 43216-5000, or telephone (614) 692-0676.

6.6 Sources of supply. Sources of supply are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 99-04-30

Approved sources of supply for SMD 5962-95613 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9561301HTA	54230	WMS512K8-120DE
5962-9561301HTC	54230	WMS512K8-120DE
5962-9561301HYA	54230	WMS512K8-120C
5962-9561301HYC	54230	WMS512K8-120C
5962-9561302HTA	54230	WMS512K8-100DE
5962-9561302HTC	54230	WMS512K8-100DE
5962-9561302HYA	54230	WMS512K8-100C
5962-9561302HYC	54230	WMS512K8-100C
5962-9561303HTA	54230	WMS512K8-85DE
5962-9561303HTC	54230	WMS512K8-85DE
5962-9561303HYA	54230	WMS512K8-85C
5962-9561303HYC	54230	WMS512K8-85C
5962-9561304HTA	54230	WMS512K8-70DE
5962-9561304HTC	54230	WMS512K8-70DE
5962-9561304HYA	54230	WMS512K8-70C
5962-9561304HYC	54230	WMS512K8-70C
5962-9561305HTA	54230	WMS512K8-55DE
5962-9561305HTC	54230	WMS512K8-55DE
5962-9561305HUA	88379	ACT-S512K8N-055F3Q
5962-9561305HUC	88379	ACT-S512K8N-055F3Q
5962-9561305HUA	54230	WMS512K8-55FT
5962-9561305HUC	54230	WMS512K8-55FT
5962-9561305HXC	54230	WMS512K8-55F
5962-9561305HYA	54230	WMS512K8-55C
5962-9561305HYC	54230	WMS512K8-55C
5962-9561305HYA	88379	ACT-S512K8N-055P4Q
5962-9561305HYC	88379	ACT-S512K8N-055P4Q
5962-9561305HZA	54230	WMS512K8-55DJ
5962-9561305HZC	54230	WMS512K8-55DJ
5962-9561305HZA	88379	ACT-S512K8N-055F4Q
5962-9561305HZC	88379	ACT-S512K8N-055F4Q

1/ The lead finish for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the manufacturer to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9561306HTA	54230	WMS512K8-45DE
5962-9561306HTC	54230	WMS512K8-45DE
5962-9561306HUA	88379	ACT-S512K8N-045F3Q
5962-9561306HUC	88379	ACT-S512K8N-045F3Q
5962-9561306HUA	54230	WMS512K8-45FT
5962-9561306HUC	54230	WMS512K8-45FT
5962-9561306HXC	54230	WMS512K8-45F
5962-9561306HYA	54230	WMS512K8-45C
5962-9561306HYC	54230	WMS512K8-45C
5962-9561306HYA	88379	ACT-S512K8N-045P4Q
5962-9561306HYC	88379	ACT-S512K8N-045P4Q
5962-9561306HZA	54230	WMS512K8-45DJ
5962-9561306HZC	54230	WMS512K8-45DJ
5962-9561306HZA	88379	ACT-S512K8N-045F4Q
5962-9561306HZC	88379	ACT-S512K8N-045F4Q
5962-9561307HTA	54230	WMS512K8-35DE
5962-9561307HTC	54230	WMS512K8-35DE
5962-9561307HUA	88379	ACT-S512K8N-035F3Q
5962-9561307HUC	88379	ACT-S512K8N-035F3Q
5962-9561307HUA	54230	WMS512K8-35FT
5962-9561307HUC	54230	WMS512K8-35FT
5962-9561307HXC	54230	WMS512K8-35F
5962-9561307HYA	54230	WMS512K8-35C
5962-9561307HYC	54230	WMS512K8-35C
5962-9561307HYA	88379	ACT-S512K8N-035P4Q
5962-9561307HYC	88379	ACT-S512K8N-035P4Q
5962-9561307HZA	54230	WMS512K8-35DJ
5962-9561307HZC	54230	WMS512K8-35DJ
5962-9561307HZA	88379	ACT-S512K8N-035F4Q
5962-9561307HZC	88379	ACT-S512K8N-035F4Q

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Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9561308HTA	54230	WMS512K8-25DE
5962-9561308HTC	54230	WMS512K8-25DE
5962-9561308HUA	88379	ACT-S512K8N-025F3Q
5962-9561308HUC	88379	ACT-S512K8N-025F3Q
5962-9561308HUA	54230	WMS512K8-25FT
5962-9561308HUC	54230	WMS512K8-25FT
5962-9561308HXC	54230	WMS512K8-25F
5962-9561308HYA	54230	WMS512K8-25C
5962-9561308HYC	54230	WMS512K8-25C
5962-9561308HYA	88379	ACT-S512K8N-025P4Q
5962-9561308HYC	88379	ACT-S512K8N-025P4Q
5962-9561308HZA	54230	WMS512K8-25DJ
5962-9561308HZC	54230	WMS512K8-25DJ
5962-9561308HZA	88379	ACT-S512K8N-025F4Q
5962-9561308HZC	88379	ACT-S512K8N-025F4Q
5962-9561309HTA	54230	WMS512K8-20DE
5962-9561309HTC	54230	WMS512K8-20DE
5962-9561309HUA	88379	ACT-S512K8N-020F3Q
5962-9561309HUC	88379	ACT-S512K8N-020F3Q
5962-9561309HUA	54230	WMS512K8-20FT
5962-9561309HUC	54230	WMS512K8-20FT
5962-9561309HXC	54230	WMS512K8-20F
5962-9561309HYA	54230	WMS512K8-20C
5962-9561309HYC	54230	WMS512K8-20C
5962-9561309HYA	88379	ACT-S512K8N-020P4Q
5962-9561309HYC	88379	ACT-S512K8N-020P4Q
5962-9561309HZA	54230	WMS512K8-20DJ
5962-9561309HZC	54230	WMS512K8-20DJ
5962-9561309HZA	88379	ACT-S512K8N-020F4Q
5962-9561309HZC	88379	ACT-S512K8N-020F4Q
5962-9561310HTA	54230	WMS512K8-17DE
5962-9561310HTC	54230	WMS512K8-17DE
5962-9561310HUA	88379	ACT-S512K8N-017F3Q
5962-9561310HUC	88379	ACT-S512K8N-017F3Q
5962-9561310HUA	54230	WMS512K8-17FT
5962-9561310HUC	54230	WMS512K8-17FT
5962-9561310HXC	54230	WMS512K8-17F
5962-9561310HYA	54230	WMS512K8-17C
5962-9561310HYC	54230	WMS512K8-17C
5962-9561310HYA	88379	ACT-S512K8N-017P4Q
5962-9561310HYC	88379	ACT-S512K8N-017P4Q
5962-9561310HZA	54230	WMS512K8-17DJ
5962-9561310HZC	54230	WMS512K8-17DJ
5962-9561310HZA	88379	ACT-S512K8N-017F4Q
5962-9561310HZC	88379	ACT-S512K8N-017F4Q

1/ The lead finish for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the manufacturer to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9561311HTC	54230	WMS512K8M-45DE
5962-9561311HTA	54230	WMS512K8M-45DE
5962-9561311HYA	54230	WMS512K8M-45C
5962-9561311HYC	54230	WMS512K8M-45C
5962-9561311HYA	88379	ACT-S512K8M-045P4Q
5962-9561311HYC	88379	ACT-S512K8M-045P4Q
5962-9561312HTA	54230	WMS512K8M-35DE
5962-9561312HTC	54230	WMS512K8M-35DE
5962-9561312HYA	54230	WMS512K8M-35C
5962-9561312HYC	54230	WMS512K8M-35C
5962-9561312HYA	88379	ACT-S512K8M-035P4Q
5962-9561312HYC	88379	ACT-S512K8M-035P4Q
5962-9561313HTA	54230	WMS512K8M-25DE
5962-9561313HTC	54230	WMS512K8M-25DE
5962-9561313HYA	54230	WMS512K8M-25C
5962-9561313HYC	54230	WMS512K8M-25C
5962-9561313HYA	88379	ACT-S512K8M-025P4Q
5962-9561313HYC	88379	ACT-S512K8M-025P4Q
5962-9561314HTA	54230	WMS512K8-15DE
5962-9561314HTC	54230	WMS512K8-15DE
5962-9561314HYA	54230	WMS512K8-15C
5962-9561314HYC	54230	WMS512K8-15C

1/ The lead finish for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the manufacturer to determine its availability.

2/ Caution. Do not use this number for item acquistion. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
54230	White Electronics Designs Corporation 3601 East University Drive Phoenix, AZ 85034-7217
88379	Aeroflex Circuit Technology Corporation 35 South Service Road Plainview, NY 11803-4193

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