CYPRESS SEMICONDUCTOR

Multipurpose BiCMOS PLD

Features

- **16 I/O macrocells, each having:**
  - **— Programmable combinatorial synchronous and asynchronous modes**
  - **— Registers configurable to T-type and D-type**
  - **— Array feedback from I/O pin or register**
- **160 product terms**
- **Available in 24-pin, 300-mil PDIP and cerDIP, and 28-pin, J-leaded chip carriers, PLCCs, and LCCs**

Functional Description

The CY7B326 is a 24-pin, multipurpose, high-performance PLD with 16 I/O macrocells, 4 dedicated inputs, and 2 global clock inputs.

CLK1 provides the synchronous clock input for one bank of eight macrocells, and CLK2 provides the synchronous clock input for the other bank of eight macrocells. Output enable and selection of asynchronous or synchronous clock source are controlled with one dedicated product term per macrocell. An asynchronous reset product term is provided for each macrocell.

Each macrocell also has a register that can be programmed to be a D-type or T-type register. Other programmable options include output polarity, registered or combinatorial output, feedback to the array from the I/O pin or from the register output, and whether the dedicated product term controls the output enable or the register clock.

The CY7B326 is available in a wide variety of packages including 24-pin, 300-mil plastic and ceramic DIPs, 28-pin, square J-leaded, ceramic chip carriers, 28-pin PLCCs, and 28-pin ceramic LCCs.

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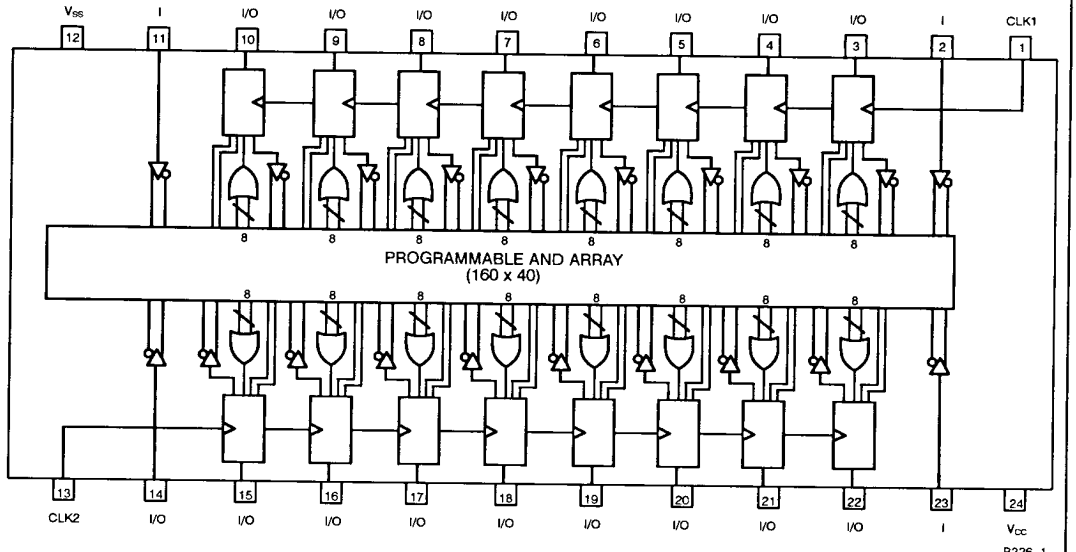
Logic Block Diagram



Selection Guide

		7B326-10	7B326-15	7B326-17
I_{CC1} (mA)	Commercial	150	150	
	Military		170	170
t_{PD} (ns)	Commercial	12	15	
	Military		15	17
t_s (ns)	Commercial	10	12	
	Military		12	15
t_{CO} (ns)	Commercial	10	12	
	Military		12	15

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to + 150°C

Ambient Temperature with Power Applied ..... – 55°C to + 125°C

Supply Voltage to Ground Potential ..... – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to V_{CC} Max.

DC Input Voltage ..... – 0.5V to + 5.5V

DC Input Current ..... – 30 mA to + 5 mA (except during programming)

DC Program Voltage 9.5V

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 5%
Military[1]	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8 mA		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs[2]		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs[2]			0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$, V_{CC} = Max.		–250	50	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \leq V_{OUT} \leq V_{CC}$		–100	100	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3]		–30	–130	mA
I_{CC1}	Power Supply Current Standby	V_{CC} = Max., V_{IH} = GND, Outputs Open	Com'l		150	mA
			Mil		170	
I_{CC2}	Power Supply Current at Frequency	V_{CC} = Max., Outputs Disabled (in High Z State), Device Operating at f_{MAX}	Com'l		170	mA
			Mil		190	

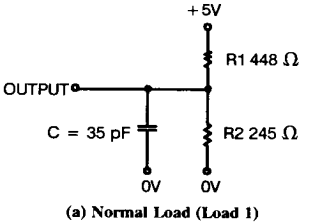
Capacitance[4]

Parameters	Description	Typical	Max.	Units
C_{IN}	Input Capacitance	11	10	pF
C_{OUT}	Output Capacitance	9	10	pF

Notes:

1. t_A is the "instant on" case temperature.
2. Minimum DC input voltage is –0.3V. During transitions, the inputs may undershoot to –2.0V for periods less than 20 ns.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by ground degradation.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



(a) Normal Load (Load 1)

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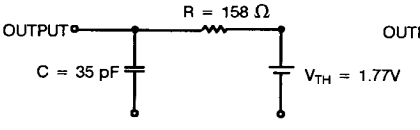

(b) Thévenin Equivalent (Load 1)

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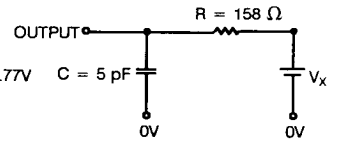
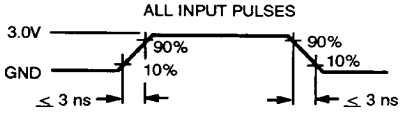


(c) Three-state Delay Load (Load 2)

B326-9

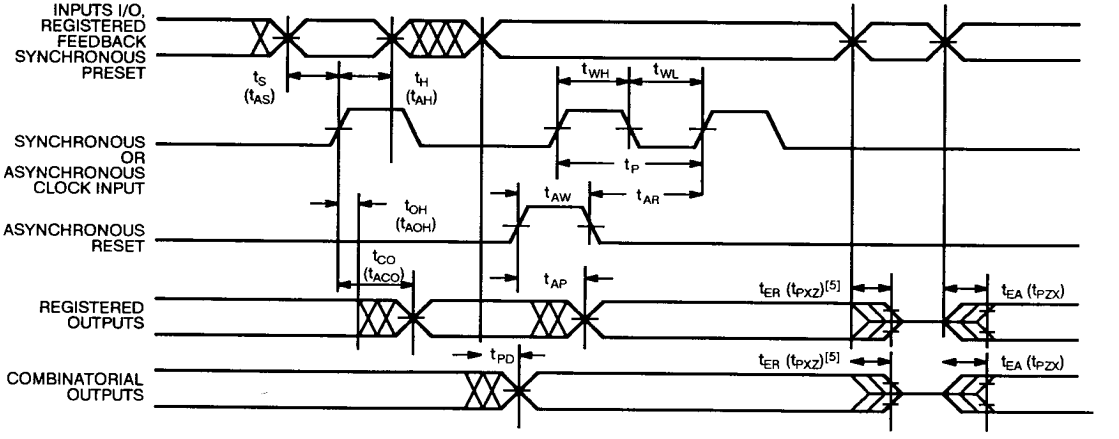


(d)

B326-2

Parameter	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	V_{OH}, 0.5V, V_X B326-3
$t_{ER(+)}$	2.6V	V_{OL}, 0.5V, V_X B326-4
$t_{EA(+)}$	V_{TH}	V_X, 0.5V, V_{OH} B326-5
$t_{EA(-)}$	V_{TH}	V_X, 0.5V, V_{OL} B326-6

Switching Waveform



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Switching Characteristics[5]

Parameters	Description		7B326-12		7B326-15		7B326-17		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[7]	Com'l		12		15			ns
		Mil				15		17	
t_{EA}	Input to Output Enable Delay	Com'l		12		15			ns
		Mil				15		17	
t_{ER}	Input to Output Disable Delay[8]	Com'l		12		15			ns
		Mil				15		17	
t_{CO}	Clock to Output Delay[7]	Com'l		10		12			ns
		Mil				12		15	
t_S	Input or Feedback Set-Up Time	Com'l	10		12				ns
		Mil			12		15		
t_H	Input Hold Time	Com'l	0		0				ns
		Mil			0		0		
t_P	External Clock Period (t_{CO} + t_S)	Com'l	20		24				ns
		Mil			24		30		
t_{WH}	Clock Width HIGH[4]	Com'l	7		9				ns
		Mil			10		11		
t_{WL}	Clock Width LOW[4]	Com'l	7		9				ns
		Mil			10		11		
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[9]	Com'l	50		41.7				MHz
		Mil			41.7		33.3		
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[4,10]	Com'l	71.4		55.6				MHz
		Mil			50		45.5		
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CNT})$)[6]	Com'l	50		40				MHz
		Mil			40		33.3		
t_{CNT}	Minimum Clock Period with Internal Feedback[11]	Com'l		20		25			ns
		Mil				25		30	
t_{AW}	Asynchronous Reset Width	Com'l	8		10				ns
		Mil			10		12		
t_{AR}	Asynchronous Reset Recovery Time	Com'l	10		12				ns
		Mil			12		15		
t_{AP}	Asynchronous Reset to Registered Output Delay	Com'l		12		14			ns
		Mil				14		17	
t_{OH}	Output Data Stable Time from Synchronous Clock Input	Com'l	1		1				ns
		Mil			1		1		
t_{AS}	Input Set-Up Time to Asynchronous Clock	Com'l	10		12				ns
		Mil			12		14		
t_{AH}	Input Hold Time from Asynchronous Clock	Com'l	10		12				ns
		Mil			12		14		
t_{ACO}	Asynchronous Clock to Output Delay	Com'l		20		25			ns
		Mil				25		30	
t_{ACNT}	Minimum Asynchronous Clock Period with Internal Feedback	Com'l		20		25			ns
		Mil				25		30	

Switching Characteristics[5] (continued)

Parameters	Description		7B326-12 Min.	7B326-12 Max.	7B326-15 Min.	7B326-15 Max.	7B326-17 Min.	7B326-17 Max.	Units
f_{MAXA1}	External Maximum Frequency Asynchronous ($1/(t_{AS} + t_{ACO})$)	Com'l	33.3		27				MHz
		Mil			27		22.7		
f_{MAXA2}	Internal Maximum Frequency Asynchronous $1/t_{ACNT}$	Com'l	50		40				MHz
		Mil			40		33.3		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input	Com'l	1.5		1.5				ns
		Mil			1		1		

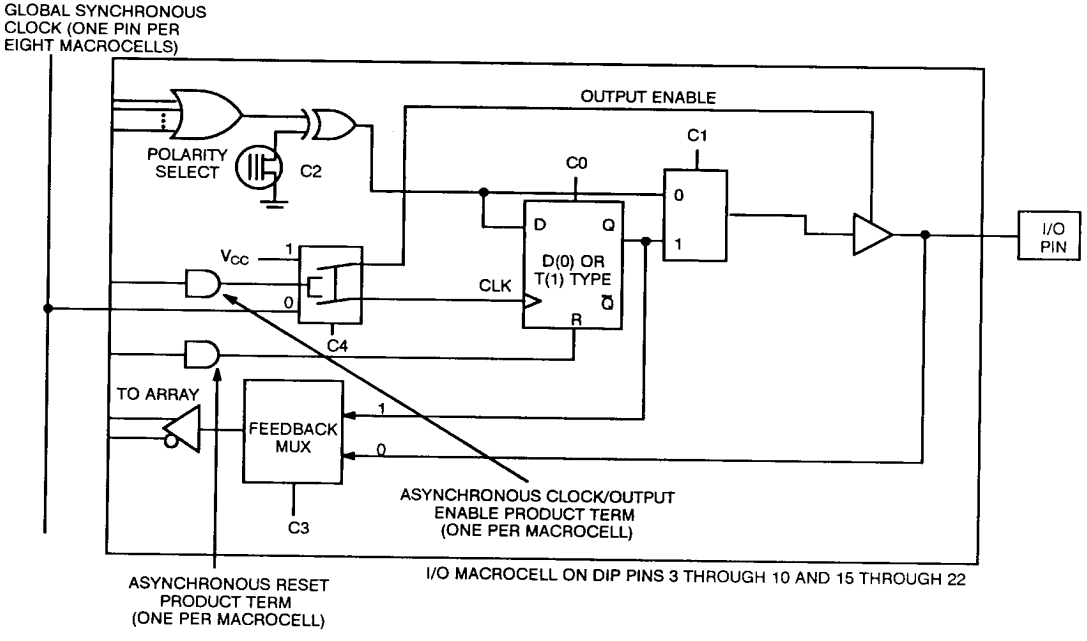
Notes:

5. AC test load used for all parameters except where noted.
6. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate. This parmeter is tested periodically by sampling product.
7. This specification is guaranteed for all device outputs changing state in a given access cycle.
8. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max.
9. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
10. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
11. This parameter is calculated from the clock period at f_{MAX} internal (f_{MAX3}) as measured (see Note 10) minus t_S.

Programming

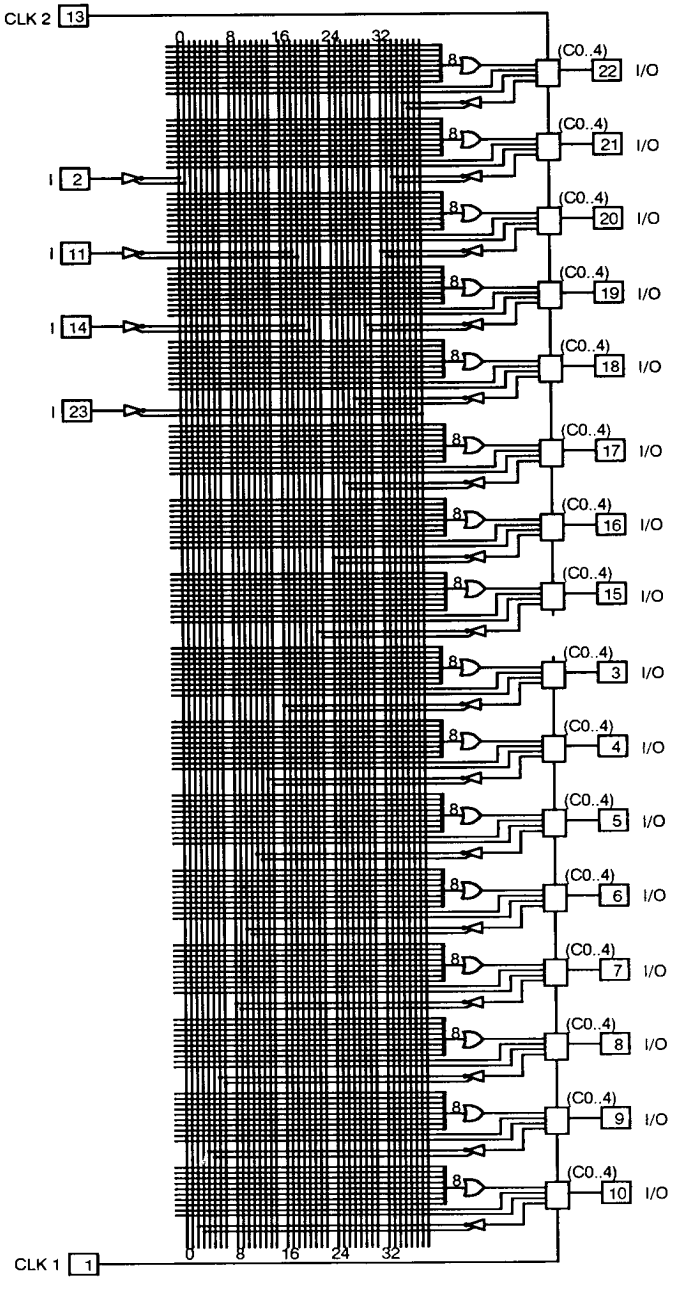
The CY7B326 can be programmed using the QuickPro II programmer available from Cypress Semiconductor and also with Data I/O, Logical Devices, STAG, and other programmers. Please contact your local Cypress representative for further information.

I/O Macrocell



B326-11

Block Diagram



Ordering Information

t_{PD} (ns)	f_{MAX2} (MHz)	Ordering Code	Package Type	Operating Range
12	71	CY7B326-12PC	P13	Commercial
		CY7B326-12DC	D14	
		CY7B326-12JC	J64	
15	55	CY7B326-12PC	P13	Commercial
		CY7B326-15DC	D14	
		CY7B326-15JC	J64	
	50	CY7B326-15DMB	D14	Military
		CY7B326-15LMB	L64	
17	45	CY7B326-17DMB	D14	Military
		CY7B326-17LMB	L64	

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