



M48T212Y M48T212V

5.0V or 3.3V TIMEKEEPER[®] Supervisor

FEATURES SUMMARY

- INTEGRATED REAL TIME CLOCK, POWER-FAIL CONTROL CIRCUIT, BATTERY AND CRYSTAL
- CONVERTS LOW POWER SRAM INTO NVRAMs
- YEAR 2000 COMPLIANT (4-Digit Year)
- BATTERY LOW FLAG
- MICROPROCESSOR POWER-ON RESET
- PROGRAMMABLE ALARM OUTPUT ACTIVE IN THE BATTERY BACKED-UP MODE
- WATCHDOG TIMER
- AUTOMATIC POWER-FAIL CHIP DESELECT AND WRITE PROTECTION
- CHOICE OF WRITE PROTECT VOLTAGES (V_{PFD} = Power-fail Deselect Voltage):
 - M48T212Y: $V_{CC} = 4.5$ to $5.5V$
 $4.2V \leq V_{PFD} \leq 4.5V$
 - M48T212V: $V_{CC} = 3.0$ to $3.6V$
 $2.7V \leq V_{PFD} \leq 3.0V$
- PACKAGING INCLUDES A 44-LEAD SOIC AND SNAPHAT[®] TOP (to be ordered separately)

Figure 1. 44-pin SOIC Package

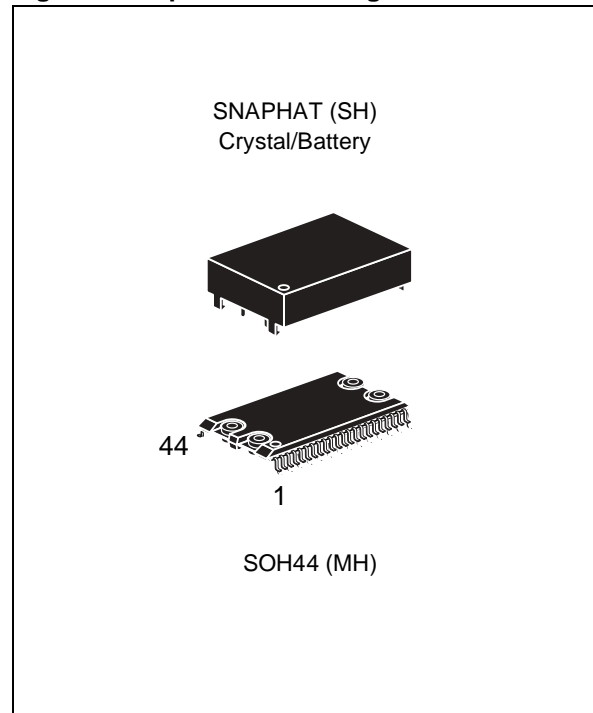


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DESCRIPTION

The M48T212Y/V are self-contained devices that include a real time clock (RTC), programmable alarms, a watchdog timer, and two external chip enable outputs which provide control of up to four (two in parallel) external low-power static RAMs.

Access to all TIMEKEEPER[®] functions and the external RAM is the same as conventional byte-wide SRAM. The 16 TIMEKEEPER Registers offer Century, Year, Month, Date, Day, Hour, Minute, Second, Calibration, Alarm, Watchdog, and Flags. Externally attached static RAMs are controlled by the M48T212Y/V via the $\overline{E1CON}$ and $\overline{E2CON}$ signals (see Table 3., page 8).

The 44-pin, 330mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT[®] housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be

mounted on top of the SOIC package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SOIC and battery/crystal packages are shipped separately in plastic anti-static tubes or in Tape & Reel form. For the-44 lead SOIC, the battery/crystal package (e.g., SNAPHAT) part number is "M4TXX-BR12SH" (see Table 20., page 30).

Caution: Do not place the SNAPHAT battery/crystal top in conductive foam, as this will drain the lithium button-cell battery.

Figure 2. Logic Diagram

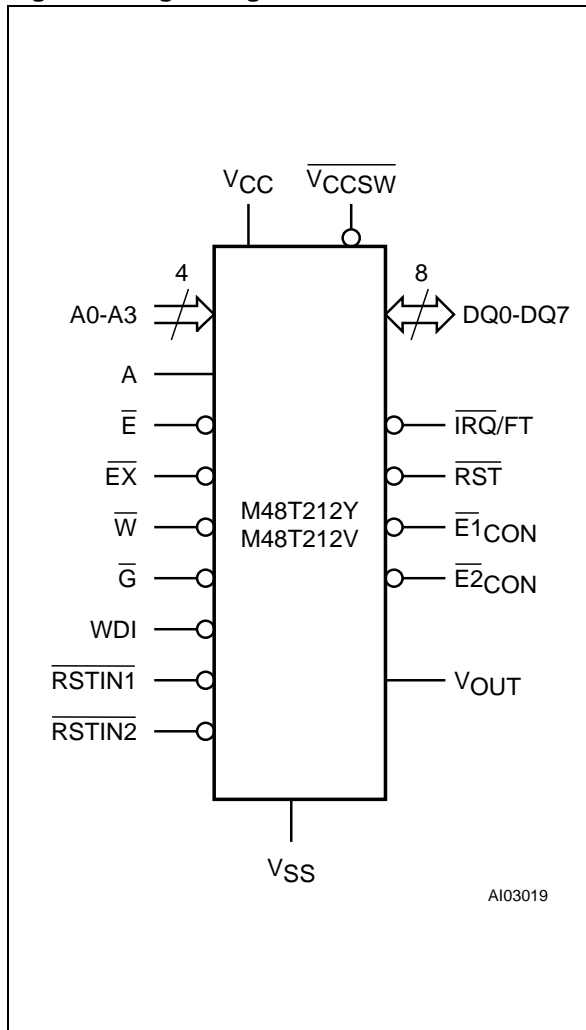


Table 1. Signal Names

| | |
|----------------------------|-----------------------------------|
| A0-A3 | Address Inputs |
| DQ0-DQ7 | Data Inputs/Outputs |
| $\overline{\text{RSTIN1}}$ | Reset 1 Input |
| $\overline{\text{RSTIN2}}$ | Reset 2 Input |
| $\overline{\text{RST}}$ | Reset Output (Open Drain) |
| WDI | Watchdog Input |
| A | Bank Select Input |
| $\overline{\text{E}}$ | Chip Enable Input |
| $\overline{\text{EX}}$ | External Chip Enable Input |
| $\overline{\text{G}}$ | Output Enable Input |
| $\overline{\text{W}}$ | WRITE Enable Input |
| $\overline{\text{E1CON}}$ | RAM Chip Enable 1 Output |
| $\overline{\text{E2CON}}$ | RAM Chip Enable 2 Output |
| $\overline{\text{IRQ/FT}}$ | Int/Freq Test Output (Open Drain) |
| $\overline{\text{Vccsw}}$ | VCC Switch Output |
| VOUT | Supply Voltage Output |
| VCC | Supply Voltage |
| VSS | Ground |
| NC | Not Connected internally |

Figure 3. SOIC Connections

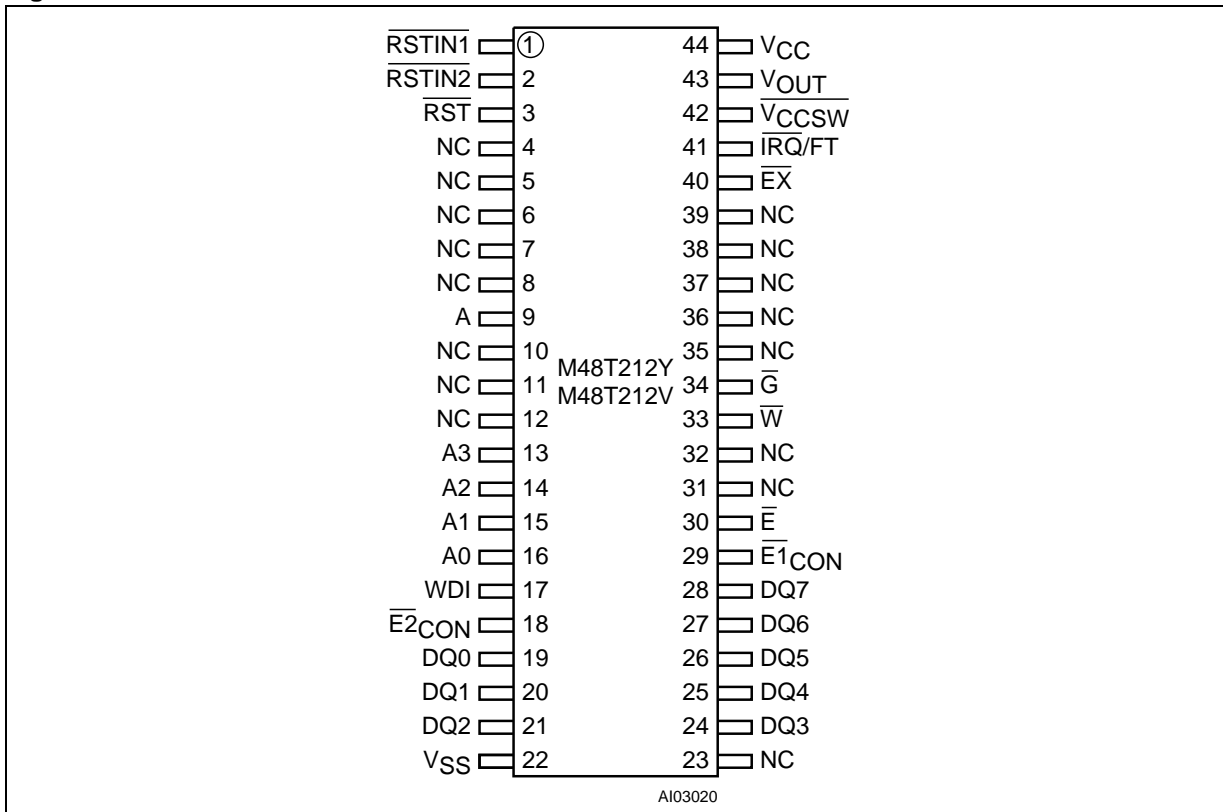
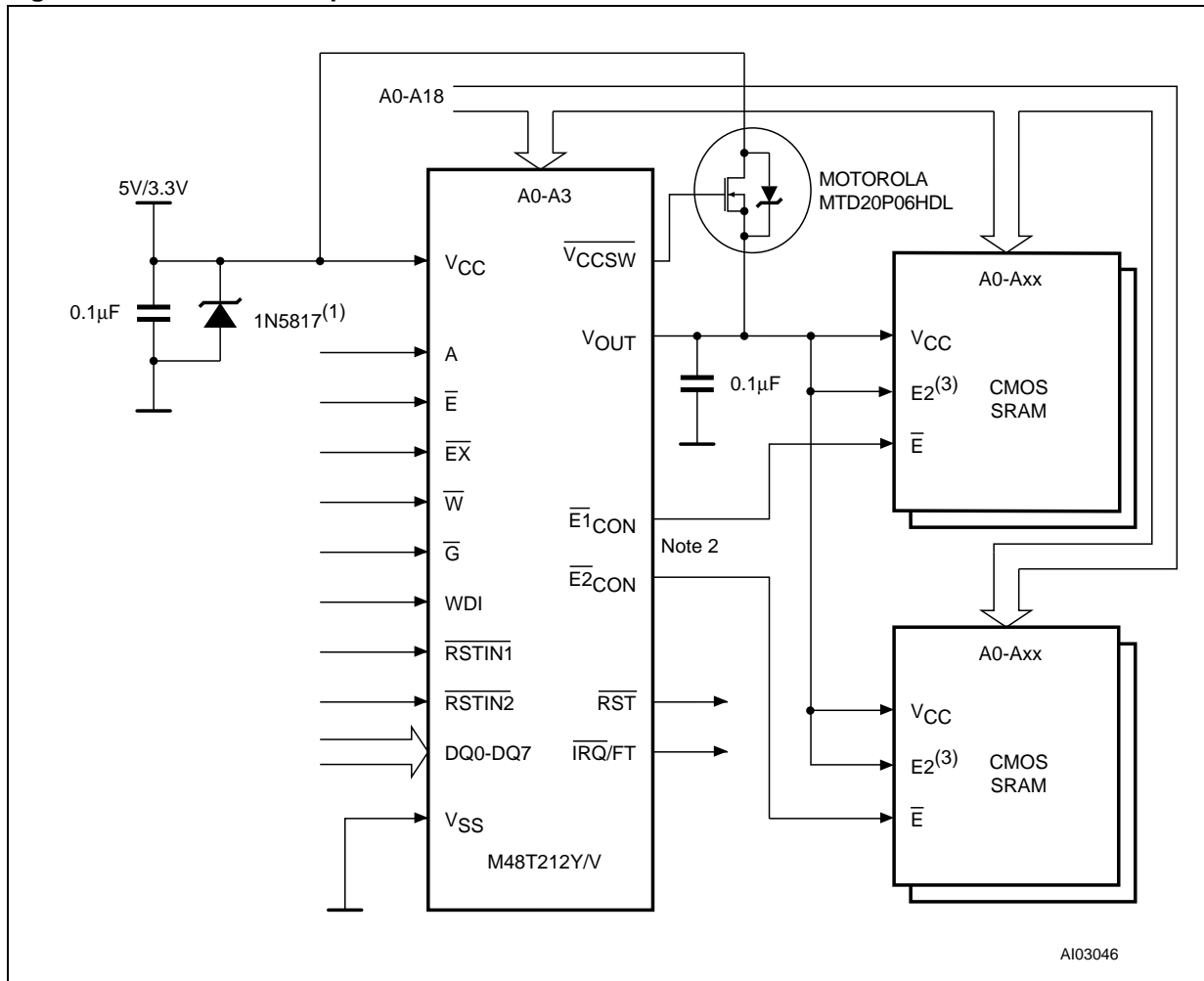


Figure 4. Hardware Hookup



- Note: 1. See description in Power Supply Decoupling and Undershoot Protection.
 2. Traces connecting E1CON and E2CON to external SRAM should be as short as possible.
 3. If the second chip enable pin (E2) is unused, it should be tied to VOUT.

OPERATION

Automatic backup and write protection for an external SRAM is provided through V_{OUT}, E_{1CON} and E_{2CON} pins. (Users are urged to insure that voltage specifications, for both the SUPERVISOR chip and external SRAM chosen, are similar). The SNAPHAT[®] containing the lithium energy source used to permanently power the real time clock is also used to retain RAM data in the absence of V_{CC} power through the V_{OUT} pin.

The chip enable outputs to RAM (E_{1CON} and E_{2CON}) are controlled during power transients to prevent data corruption. The date is automatically adjusted for months with less than 31 days and corrects for leap years (valid until 2100). The internal watchdog timer provides programmable alarm windows.

The nine clock bytes (Fh-9h and 1h) are not the actual clock counters, they are memory locations consisting of BiPORT[™] READ/WRITE memory cells within the static RAM array. Clock circuitry updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

Byte 8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting. Byte 7h contains the watchdog timer setting. The watchdog

timer can generate either a reset or an interrupt, depending on the state of the Watchdog Steering Bit (WDS). Bytes 6h-2h include bits that, when programmed, provide for clock alarm functionality.

Alarms are activated when the register content matches the month, date, hours, minutes, and seconds of the clock registers. Byte 1h contains century information. Byte 0h contains additional flag information pertaining to the watchdog timer, alarm and battery status.

The M48T212Y/V also has its own Power-Fail Detect circuit. This control circuitry constantly monitors the supply voltage for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the TIMEKEEPER[®] register data and external SRAM, providing data security in the midst of unpredictable system operation. As V_{CC} falls below V_{SO}, the control circuitry automatically switches to the battery, maintaining data and clock operation until valid power is restored.

Address Decoding

The M48T212Y/V accommodates 4 address lines (A3-A0) which allow access to the sixteen bytes of the TIMEKEEPER clock registers. All TIMEKEEPER registers reside in the SUPERVISOR chip itself. All TIMEKEEPER registers are accessed by enabling E (Chip Enable).

Table 2. Operating Modes

| Mode | V _{CC} | E | G | W | DQ7-DQ0 | Power |
|----------|--|-----------------|-----------------|-----------------|------------------|-----------------|
| Deselect | 4.5V to 5.5V or 3.0V to 3.6V | V _{IH} | X | X | High-Z | Standby |
| WRITE | | V _{IL} | X | V _{IL} | D _{IN} | Active |
| READ | | V _{IL} | V _{IL} | V _{IH} | D _{OUT} | Active |
| READ | | V _{IL} | V _{IH} | V _{IH} | High-Z | Active |
| Deselect | V _{SO} to V _{PFD} (min) ⁽¹⁾ | X | X | X | High-Z | CMOS Standby |
| Deselect | ≤ V _{SO} ⁽¹⁾ | X | X | X | High-Z | Battery Back-Up |

Note: X = V_{IH} or V_{IL}; V_{SO} = Battery Back-up Switchover Voltage

1. See Table 14., page 25 for details.

Table 3. Truth Table for SRAM Bank Select

| Mode | V _{CC} | EX | A | E _{1CON} | E _{2CON} | Power |
|----------|--|------|------|-------------------|-------------------|-----------------|
| Select | 4.5V to 5.5V or 3.0V to 3.6V | Low | Low | Low | High | Active |
| | | Low | High | High | Low | Active |
| Deselect | | High | X | High | High | Standby |
| Deselect | V _{SO} to V _{PFD} (min) ⁽¹⁾ | X | X | High | High | CMOS Standby |
| Deselect | ≤ V _{SO} ⁽¹⁾ | X | X | High | High | Battery Back-Up |

Note: X = V_{IH} or V_{IL}; V_{SO} = Battery Back-up Switchover Voltage

1. See Table 14., page 25 for details.

Figure 5. Chip Enable Control and Bank Select Timing

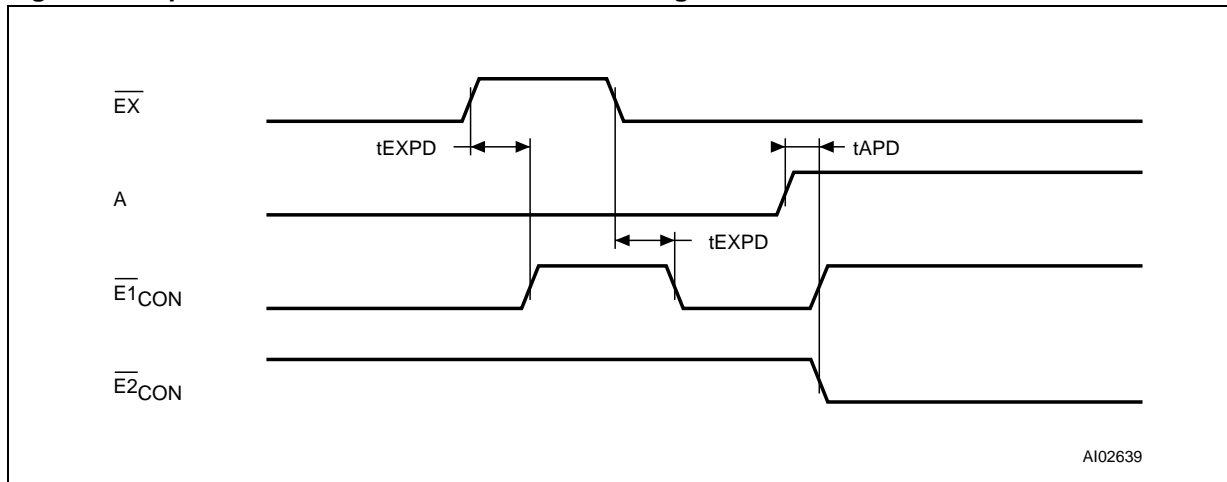


Table 4. Chip Enable Control and Bank Select Characteristics

| Symbol | Parameter | M48T212Y | | M48T212V | | Unit |
|------------|---|----------|-----|----------|-----|------|
| | | -70 | | -85 | | |
| | | Min | Max | Min | Max | |
| t_{EXPD} | \overline{EX} to $\overline{E1CON}$ or $\overline{E2CON}$ (Low or High) | | 10 | | 15 | ns |
| t_{APD} | A to $\overline{E1CON}$ or $\overline{E2CON}$ (Low or High) | | 10 | | 15 | ns |

READ Mode

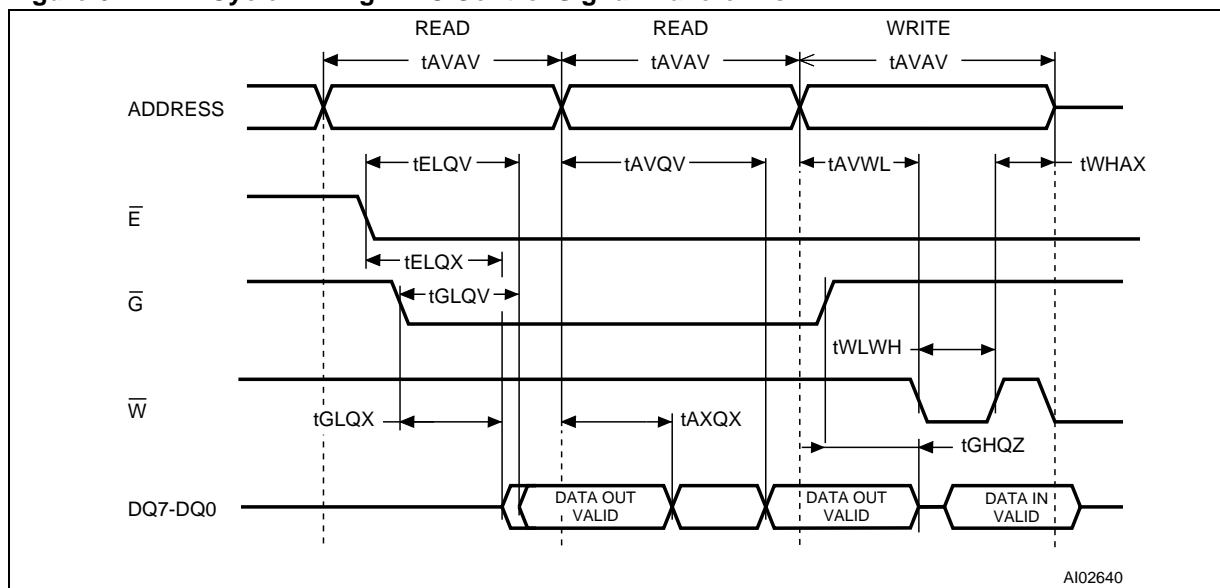
The M48T212Y/V executes a READ cycle whenever \overline{W} (WRITE Enable) is high and \overline{E} (Chip Enable) is low. The unique address specified by the address inputs (A3-A0) defines which one of the on-chip TIMEKEEPER® registers is to be accessed. When the address presented to the M48T212Y/V is in the range of 0h-Fh, one of the on-board TIMEKEEPER registers is accessed and valid data will be available to the eight data output drivers within t_{AVQV} after the address input signal is stable, providing that the \overline{E} and \overline{G} access times

are also satisfied. If they are not, then data access must be measured from the latter occurring signal (\overline{E} or \overline{G}) and the limiting parameter is either t_{ELQV} for \overline{E} or t_{GLQV} for \overline{G} rather than the address access time.

When \overline{EX} input is low, an external SRAM location will be selected.

Note: Care should be taken to avoid taking both \overline{E} and \overline{EX} low simultaneously to avoid bus contention.

Figure 6. READ Cycle Timing: RTC Control Signal Waveforms



Note: \overline{EX} is assumed High.

Table 5. READ Mode AC Characteristics

| Symbol | Parameter ⁽¹⁾ | M48T212Y | | M48T212V | | Unit |
|------------------|---|----------|-----|----------|-----|------|
| | | -70 | | -85 | | |
| | | Min | Max | Min | Max | |
| t_{AVAV} | Read Cycle Time | 70 | | 85 | | ns |
| t_{AVQV} | Address Valid to Output Valid | | 70 | | 85 | ns |
| t_{ELQV} | Chip Enable Low to Output Valid | | 70 | | 85 | ns |
| t_{GLQV} | Output Enable Low to Output Valid | | 25 | | 35 | ns |
| $t_{ELQX}^{(2)}$ | Chip Enable Low to Output Transition | 5 | | 5 | | ns |
| $t_{GLQX}^{(2)}$ | Output Enable Low to Output Transition | 0 | | 0 | | ns |
| $t_{EHQZ}^{(2)}$ | Chip Enable High to Output Hi-Z | | 20 | | 25 | ns |
| $t_{GHQZ}^{(2)}$ | Output Enable High to Output Hi-Z | | 20 | | 25 | ns |
| t_{AXQX} | Address Transition to Output Transition | 5 | | 5 | | ns |

Note: 1. Valid for Ambient Operating Temperature: $T_A = 0$ to 70°C or -40 to 85°C ; $V_{CC} = 4.5$ to 5.5V or 3.0 to 3.6V (except where noted).
 2. $C_L = 5\text{pF}$.



WRITE Mode

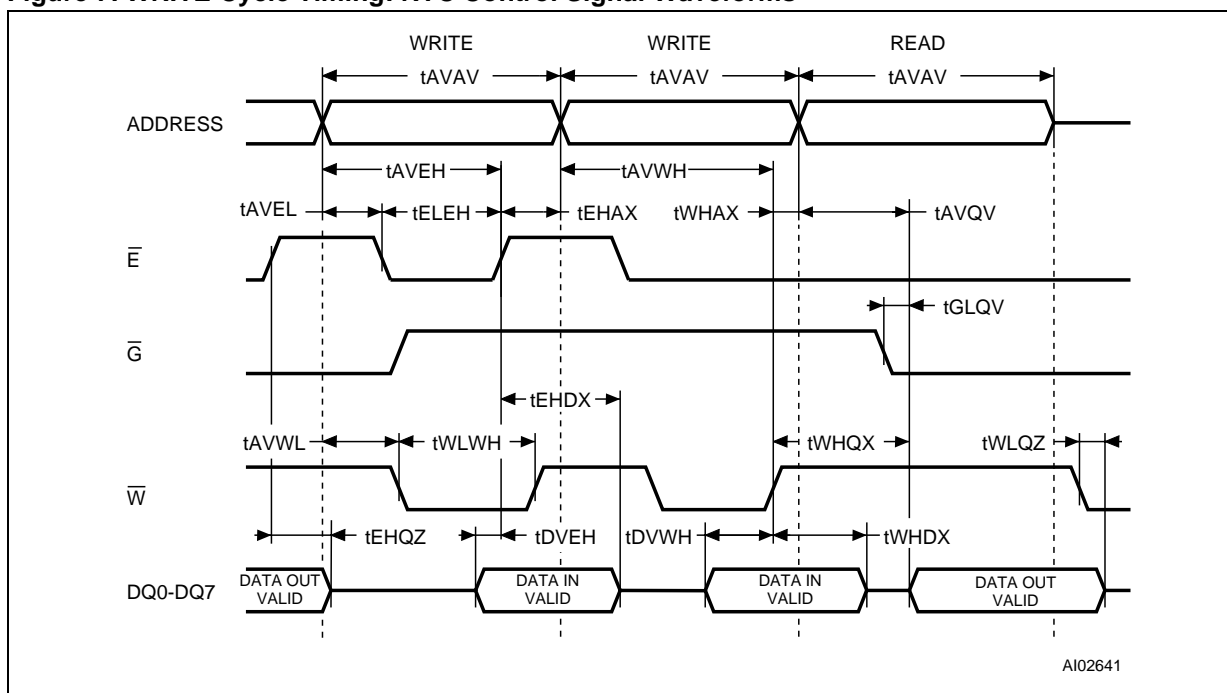
The M48T212Y/V is in the WRITE Mode whenever \overline{W} (WRITE Enable) and \overline{E} (Chip Enable) are in a low state after the address inputs are stable. The start of a WRITE is referenced from the latter occurring falling edge of \overline{W} or \overline{E} . A WRITE is terminated by the earlier rising edge of \overline{W} or \overline{E} . The addresses must be held valid throughout the cycle. \overline{E} or \overline{W} must return high for a minimum of t_{E-HAX} from Chip Enable or t_{WHAX} from WRITE Enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward.

\overline{G} should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on \overline{E} and \overline{G} a low on \overline{W} will disable the outputs t_{WLQZ} after \overline{W} falls.

When \overline{E} is low during the WRITE, one of the on-board TIMEKEEPER® registers will be selected and data will be written into the device. When \overline{EX} is low (and \overline{E} is high) an external SRAM location is selected.

Note: Care should be taken to avoid taking both \overline{E} and \overline{EX} low simultaneously to avoid bus contention.

Figure 7. WRITE Cycle Timing: RTC Control Signal Waveforms



Note: \overline{EX} is assumed High.

Table 6. WRITE Mode AC Characteristics

| Symbol | Parameter ⁽¹⁾ | M48T212Y | | M48T212V | | Unit |
|------------------------------------|---|----------|-----|----------|-----|------|
| | | -70 | | -85 | | |
| | | Min | Max | Min | Max | |
| t _{AVAV} | Write Cycle Time | 70 | | 85 | | ns |
| t _{AVWL} | Address Valid to Write Enable Low | 0 | | 0 | | ns |
| t _{AVEL} | Address Valid to Chip Enable Low | 0 | | 0 | | ns |
| t _{WLWH} | Write Enable Pulse Width | 45 | | 55 | | ns |
| t _{LELH} | Chip Enable Low to Chip Enable High | 50 | | 60 | | ns |
| t _{WHAX} | Write Enable High to Address Transition | 0 | | 0 | | ns |
| t _{EHAX} | Chip Enable High to Address Transition | 0 | | 0 | | ns |
| t _{DVWH} | Input Valid to Write Enable High | 25 | | 30 | | ns |
| t _{DVEH} | Input Valid to Chip Enable High | 25 | | 30 | | ns |
| t _{WHDX} | Write Enable High to Input Transition | 0 | | 0 | | ns |
| t _{EHDX} | Chip Enable High to Input Transition | 0 | | 0 | | ns |
| t _{WLQZ} ^(2,3) | Write Enable Low to Output High-Z | | 20 | | 25 | ns |
| t _{AVWH} | Address Valid to Write Enable High | 55 | | 65 | | ns |
| t _{AVEH} | Address Valid to Chip Enable High | 55 | | 65 | | ns |
| t _{WHQX} ^(2,3) | Write Enable High to Output Transition | 5 | | 5 | | ns |

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C or -40 to 85°C; V_{CC} = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
 2. C_L = 5pF
 3. If \overline{E} goes low simultaneously with \overline{W} going low, the outputs remain in the high impedance state.

Data Retention Mode

With valid V_{CC} applied, the M48T212Y/V can be accessed as described above with READ or WRITE cycles. Should the supply voltage decay, the M48T212Y/V will automatically deselect, write protecting itself (and any external SRAM) when V_{CC} falls between V_{PFD} (max) and V_{PFD} (min). This is accomplished by internally inhibiting access to the clock registers via the \bar{E} signal. At this time, the Reset pin (\overline{RST}) is driven active and will remain active until V_{CC} returns to nominal levels.

External RAM access is inhibited in a similar manner by forcing $\overline{E1CON}$ and $\overline{E2CON}$ to a high level. This level is within 0.2 volts of the V_{BAT} . $\overline{E1CON}$ and $\overline{E2CON}$ will remain at this level as long as V_{CC} remains at an out-of-tolerance condition.

When V_{CC} falls below battery back-up switchover voltage (V_{SO}), power input is switched from the V_{CC} pin to the SNAPHAT[®] battery and the clock registers and external SRAM are maintained from the attached battery supply. All outputs become high impedance. The V_{OUT} pin is capable of supplying 100 μ A of current to the attached memory with less than 0.3V drop under this condition. On power up, when V_{CC} returns to a nominal value, write protection continues for 200ms (max) by inhibiting $\overline{E1CON}$ or $\overline{E2CON}$.

The \overline{RST} signal also remains active during this time (see Figure 15., page 26).

Note: Most low power SRAMs on the market today can be used with the M48T212Y/V TIME-KEEPER[®] SUPERVISOR. There are, however

some criteria which should be used in making the final choice of an SRAM to use. The SRAM must be designed in a way where the chip enable input disables all other inputs to the SRAM. This allows inputs to the M48T212Y/V and SRAMs to be "Don't care" once V_{CC} falls below V_{PFD} (min). The SRAM should also guarantee data retention down to $V_{CC} = 2.0V$. The chip enable access time must be sufficient to meet the system needs with the chip enable output propagation delays included.

If the SRAM includes a second chip enable pin ($\overline{E2}$), this pin should be tied to V_{OUT} .

If data retention lifetime is a critical parameter for the system, it is important to review the data retention current specifications for the particular SRAMs being evaluated. Most SRAMs specify a data retention current at 3.0V. Manufacturers generally specify a typical condition for room temperature along with a worst case condition (generally at elevated temperatures). The system level requirements will determine the choice of which value to use.

The data retention current value of the SRAMs can then be added to the I_{BAT} value of the M48T212Y/V to determine the total current requirements for data retention. The available battery capacity for the SNAPHAT[®] of your choice can then be divided by this current to determine the amount of data retention available (see Table 20., page 30).

For a further more detailed review of lifetime calculations, please see Application Note AN1012.

CLOCK OPERATION

TIMEKEEPER® Registers

The M48T212Y/V offers 16 internal registers which contain TIMEKEEPER®, Alarm, Watchdog, Flag, and Control data. These registers are memory locations which contain external (user accessible) and internal copies of the data (usually referred to as BiPORT™ TIMEKEEPER cells).

The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy. TIMEKEEPER and Alarm Registers store data in BCD. Control, Watchdog and Flags Registers store data in Binary Format.

Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. The BiPORT TIMEKEEPER cells in the RAM array are only data registers and not the actual clock counters, so updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ Bit, D6 in the Control Register (8h). As long as a '1' remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating occurs 1 second after the READ Bit is reset to a '0.'

Setting the Clock

Bit D7 of the Control Register (8h) is the WRITE Bit. Setting the WRITE Bit to a '1,' like the READ Bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 7., page 15).

Resetting the WRITE Bit to a '0' then transfers the values of all time registers (Fh-9h, 1h) to the actual TIMEKEEPER counters and allows normal operation to resume. After the WRITE Bit is reset, the next clock update will occur one second later.

Note: Upon power-up following a power failure, the READ Bit will automatically be set to a '1.' This will prevent the clock from updating the TIMEKEEPER registers, and will allow the user to read the exact time of the power-down event.

Resetting the READ Bit to a '0' will allow the clock to update these registers with the current time. The WRITE Bit will be reset to a '0' upon power-up.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP Bit is located at Bit D7 within the Seconds Register (9h). Setting it to a '1' stops the oscillator. When reset to a '0,' the M48T212Y/V oscillator starts within one second.

Note: It is not necessary to set the WRITE Bit when setting or resetting the FREQUENCY TEST Bit (FT) or the STOP Bit (ST).

Table 7. TIMEKEEPER® Register Map

| Address | | | | | | | | | Function/Range BCD Format | |
|---------|-----------|------------------|------------|-------------|------------------------|-------------|-----|---------|------------------------------|-------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| Fh | 10 Years | | | | Year | | | | Year | 00-99 |
| Eh | 0 | 0 | 0 | 10M | Month | | | | Month | 01-12 |
| Dh | 0 | 0 | 10 Date | | Date: Day of Month | | | | Date | 01-31 |
| Ch | 0 | FT | 0 | 0 | 0 | Day of Week | | | Day | 01-7 |
| Bh | 0 | 0 | 10 Hours | | Hours (24 Hour Format) | | | | Hours | 00-23 |
| Ah | 0 | 10 Minutes | | | Minutes | | | | Min | 00-59 |
| 9h | ST | 10 Seconds | | | Seconds | | | | Sec | 00-59 |
| 8h | W | R | S | Calibration | | | | Control | | |
| 7h | WDS | BMB4 | BMB3 | BMB2 | BMB1 | BMB0 | RB1 | RB0 | Watchdog | |
| 6h | AFE | 0 | ABE | AI 10M | Alarm Month | | | | A Month | 01-12 |
| 5h | RPT4 | RPT5 | AI 10 Date | | Alarm Date | | | | A Date | 01-31 |
| 4h | RPT3 | 0 | AI 10 Hour | | Alarm Hour | | | | A Hour | 00-23 |
| 3h | RPT2 | Alarm 10 Minutes | | | Alarm Minutes | | | | A Min | 00-59 |
| 2h | RPT1 | Alarm 10 Seconds | | | Alarm Seconds | | | | A Sec | 00-59 |
| 1h | 1000 Year | | | | 100 Year | | | | Century | 00-99 |
| 0h | WDF | AF | Y | BL | Y | Y | Y | Y | Flag | |

Keys: S = Sign Bit

FT = Frequency Test Bit

R = READ Bit

W = WRITE Bit

ST = Stop Bit

0 = Must be set to '0'

BL = Battery Low Flag (Read only)

BMB0-BMB4 = Watchdog Multiplier Bits

AFE = Alarm Flag Enable Flag

RB0-RB1 = Watchdog Resolution Bits

WDS = Watchdog Steering Bit

ABE = Alarm in Battery Back-Up Mode Enable Bit

RPT1-RPT5 = Alarm Repeat Mode Bits

WDF = Watchdog Flag (Read only)

AF = Alarm Flag (Read only)

Y = '1' or '0'

Setting the Alarm Clock

Address locations 6h-2h contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, date, hour, minute, or second or repeat every year, month, day, hour, minute, or second. It can also be programmed to go off while the M48T212Y/V is in the battery back-up to serve as a system wake-up call.

Bits RPT5-RPT1 put the alarm in the repeat mode of operation. Table 8 shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

Note: User must transition address (or toggle chip enable) to see Flag Bit change.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT5-RPT1, the AF (Alarm Flag) is set.

If AFE (Alarm Flag Enable) is also set, the alarm condition activates the IRQ/FT pin. To disable alarm, write '0' to the Alarm Date registers and RPT1-5. The IRQ/FT output is cleared by a READ to the Flags Register as shown in Figure 8. A subsequent READ of the Flags Register is necessary to see that the value of the Alarm Flag has been reset to '0.'

The IRQ/FT pin can also be activated in the battery back-up mode. The IRQ/FT will go low if an alarm occurs and both ABE (Alarm in Battery Back-up Mode Enable) and AFE are set. The ABE and AFE Bits are reset during power-up, therefore an alarm generated during power-up will only set AF. The user can read the Flag Register at system boot-up to determine if an alarm was generated while the M48T212Y/V was in the deselect mode during power-up. Figure 9., page 17 illustrates the back-up mode alarm timing.

Figure 8. Alarm Interrupt Reset Waveforms

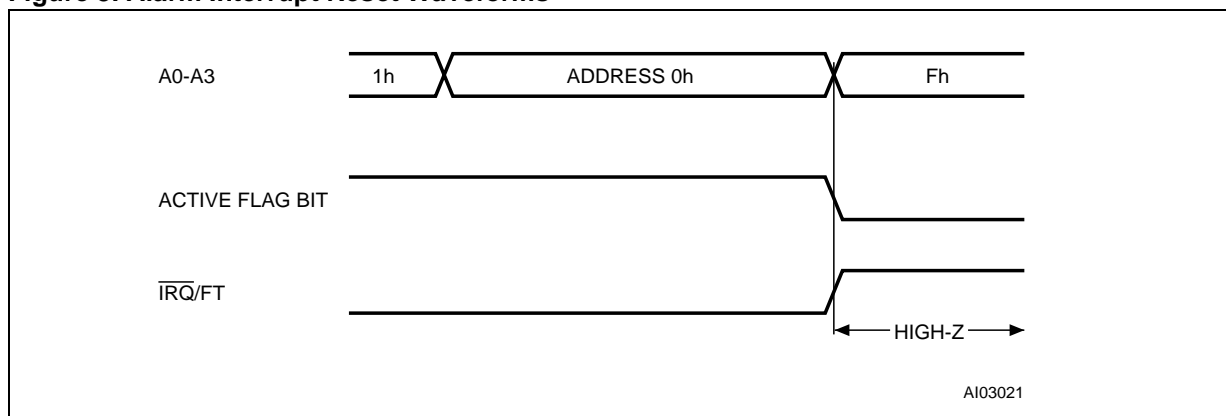
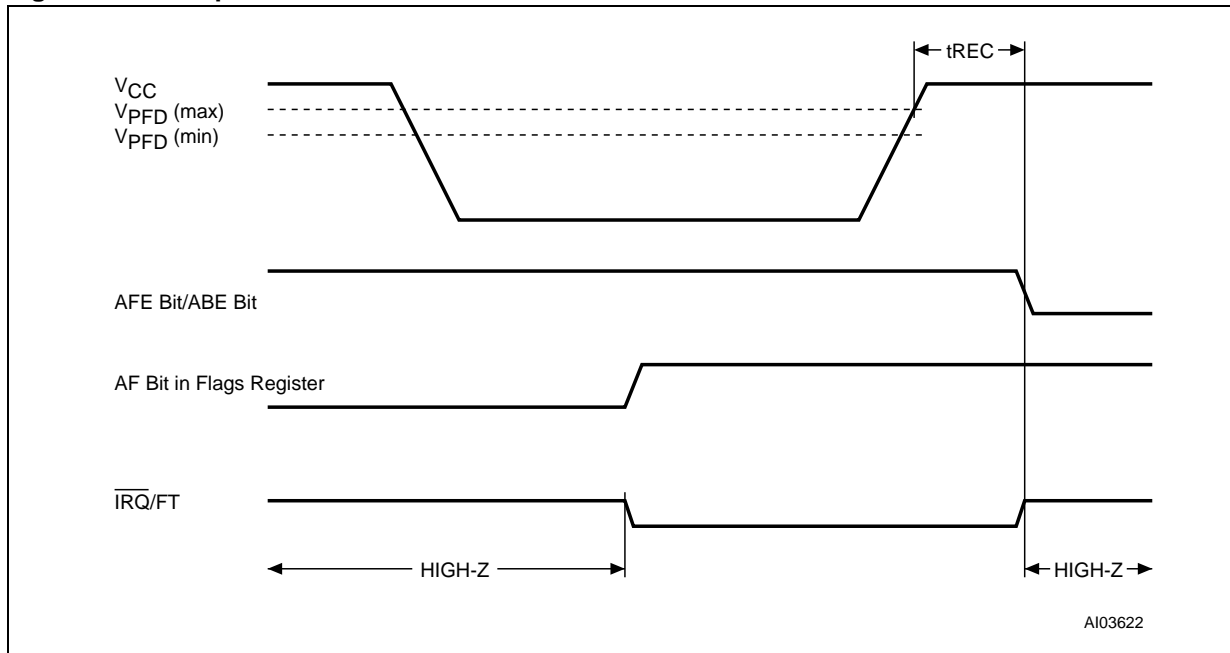


Table 8. Alarm Repeat Modes

| RPT5 | RPT4 | RPT3 | RPT2 | RPT1 | Alarm Setting |
|------|------|------|------|------|-----------------|
| 1 | 1 | 1 | 1 | 1 | Once per Second |
| 1 | 1 | 1 | 1 | 0 | Once per Minute |
| 1 | 1 | 1 | 0 | 0 | Once per Hour |
| 1 | 1 | 0 | 0 | 0 | Once per Day |
| 1 | 0 | 0 | 0 | 0 | Once per Month |
| 0 | 0 | 0 | 0 | 0 | Once per Year |

Figure 9. Back-up Mode Alarm Waveforms



Watchdog Timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the Watchdog Register, address 7h.

Bits BMB4-BMB0 store a binary multiplier and the two lower-order bits RB1-RB0 select the resolution, where 00=1/16 second, 01=1/4 second, 10=1 second, and 11=4 seconds. The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the Watchdog Register = 3×1 or 3 seconds).

Note: Accuracy of timer is within \pm the selected resolution.

If the processor does not reset the timer within the specified period, the M48T212Y/V sets the WDF (Watchdog Flag) and generates a watchdog interrupt or a microprocessor reset. WDF is reset by reading the Flags Register (Address 0h).

The most significant bit of the Watchdog Register is the Watchdog Steering Bit (WDS). When set to a '0,' the watchdog will activate the IRQ/FT pin when timed-out. When WDS is set to a '1,' the watchdog will output a negative pulse on the RST pin for 40 to 200 ms. The Watchdog register, AFE, ABE, and FT Bits will reset to a '0' at the end of a

Watchdog time-out when the WDS Bit is set to a '1.'

The watchdog timer can be reset by two methods:

1. a transition (high-to-low or low-to-high) can be applied to the Watchdog Input pin (WDI) or
2. the microprocessor can perform a WRITE of the Watchdog Register.

The time-out period then starts over. The WDI pin should be tied to V_{SS} if not used. The watchdog will be reset on each transition (edge) seen by the WDI pin. In the order to perform a software reset of the watchdog timer, the original time-out period can be written into the Watchdog Register, effectively restarting the count-down cycle.

Should the watchdog timer time-out, and the WDS Bit is programmed to output an interrupt, a value of 00h needs to be written to the Watchdog Register in order to clear the IRQ/FT pin. This will also disable the watchdog function until it is again programmed correctly. A READ of the Flags Register will reset the Watchdog Flag (Bit D7; Register 0h).

The watchdog function is automatically disabled upon power-down and the Watchdog Register is cleared. If the watchdog function is set to output to the IRQ/FT pin and the frequency test function is activated, the watchdog or alarm function prevails and the frequency test function is denied.

V_{CC} Switch Output

V_{CCsw} output goes low when V_{OUT} switches to V_{CC} turning on a customer supplied P-Channel MOSFET (see Figure 4., page 7). The Motorola MTD20P06HDL is recommended. This MOSFET in turn connects V_{OUT} to a separate supply when the current requirement is greater than I_{OUT1} (see Table 14., page 25). This output may also be used simply to indicate the status of the internal battery switchover comparator, which controls the source (V_{CC} or battery) of the V_{OUT} output.

Power-on Reset

The M48T212Y/V continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the RST pulls low (open drain) and remains low on power-up for t_{rec} after V_{CC} passes V_{PFD} (max). The RST pin is an open drain output and an appropriate pull-up resistor to V_{CC} should be chosen to control rise time.

appropriate pull-up resistor to V_{CC} should be chosen to control rise time.

Note: If the RST output is fed back into either of the RSTIN inputs (for a microprocessor with a bi-directional reset) then a 1kΩ (max) pull-up resistor is recommended.

Reset Inputs (RSTIN1 & RSTIN2)

The M48T212Y/V provides two independent inputs which can generate an output reset. The duration and function of these resets is identical to a reset generated by a power cycle. Table 9 and Figure 10 illustrate the AC reset characteristics of this function. During the time RST is enabled (t_{R1HRH} & t_{R2HRH}), the Reset Inputs are ignored.

Note: RSTIN1 and RSTIN2 are each internally pulled up to V_{CC} through a 100KΩ resistor.

Figure 10. (RSTIN1 & RSTIN2) Timing Waveforms

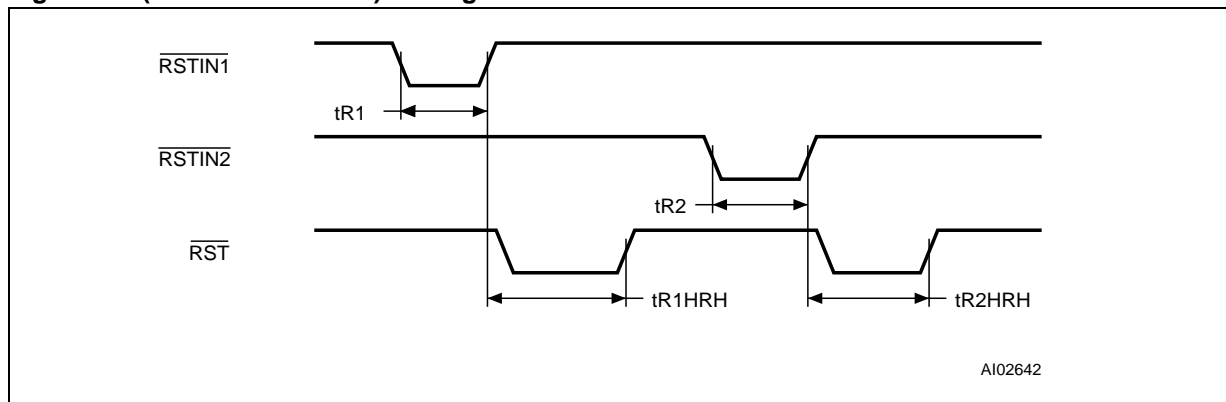


Table 9. Reset AC Characteristics

| Symbol | Parameter ⁽¹⁾ | Min | Max | Unit |
|-----------------------------------|---------------------------|-----|-----|------|
| t _{R1} ⁽²⁾ | RSTIN1 Low to RSTIN1 High | 200 | | ns |
| t _{R2} ⁽³⁾ | RSTIN2 Low to RSTIN2 High | 100 | | ms |
| t _{R1HRH} ⁽⁴⁾ | RSTIN1 High to RST High | 40 | 200 | ms |
| t _{R2HRH} ⁽⁴⁾ | RSTIN2 High to RST High | 40 | 200 | ms |

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C or -40 to 85°C; V_{CC} = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
 2. Pulse width less than 50ns will result in no RESET (for noise immunity).
 3. Pulse width less than 20ms will result in no RESET (for noise immunity).
 4. C_L = 5pF (see Figure 14., page 24).

Calibrating the Clock

The M48T212Y/V is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed ± 35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month (see Figure 11., page 21). When the Calibration circuit is properly employed, accuracy improves to better than $+1/-2$ ppm at 25°C.

The oscillation rate of crystals changes with temperature. The M48T212Y/V design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in Figure 12., page 21. The number of times pulses which are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five Calibration bits found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration bits occupy the five lower-order bits (D4-D0) in the Control Register 8h. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign Bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles.

If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is $+4.068$ or -2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent $+10.7$ or -5.35 seconds per month

which corresponds to a total range of $+5.5$ or -2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M48T212Y/V may require. The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. Calibration values, including the number of seconds lost or gained in a given period, can be found in Application Note, "AN934, TIMEKEEPER® Calibration."

This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the Calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{\text{IRQ/FT}}$ pin. The pin will toggle at 512Hz, when the Stop Bit (ST, D7 of 9h) is '0,' the Frequency Test Bit (FT, D6 of Ch) is '1,' the Alarm Flag Enable Bit (AFE, D7 of 6h) is '0,' and the Watchdog Steering Bit (WDS, D7 of 7h) is '1' or the Watchdog Register (7h=0) is reset.

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a $+20$ ppm oscillator frequency error, requiring a -10 (WR001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency.

The $\overline{\text{IRQ/FT}}$ pin is an open drain output which requires a pull-up resistor to V_{CC} for proper operation. A 500-10k Ω resistor is recommended in order to control the rise time. The FT Bit is cleared on power-up.

Battery Low Warning

The M48T212Y/V automatically performs battery voltage monitoring upon power-up and at factory-programmed time intervals of approximately 24 hours. The Battery Low (BL) Bit, Bit D4 of Flags Register 0h, will be asserted if the battery voltage is found to be less than approximately 2.5V. The BL Bit will remain asserted until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24-hour interval.

If a battery low is generated during a power-up sequence, this indicates that the battery is below approximately 2.5 volts and may not be able to maintain data integrity in the SRAM. Data should be considered suspect and verified as correct. A fresh battery should be installed.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised due to the fact that a nominal V_{CC} is supplied. In order to insure data integrity during

subsequent periods of battery back-up mode, the battery should be replaced. The SNAPHAT[®] battery/crystal top should be replaced with V_{CC} powering the device to avoid data loss.

Note: this will cause the clock to lose time during the time interval the battery crystal is removed.

The M48T212Y/V only monitors the battery when a nominal V_{CC} is applied to the device. Thus applications which require extensive durations in the battery back-up mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial.

Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique.

Initial Power-on Defaults

Upon application of power to the device, the following register bits are set to a '0' state: WDS, BMB0-BMB4, RB0-RB1, AFE, ABE, W, and FT (see Tabel 10).

Table 10. Default Values

| Condition | W | R | FT | AFE | ABE | WATCHDOG Register ⁽¹⁾ |
|--|---|---|----|-----|-----|----------------------------------|
| Initial Power-up (Battery Attach for SNAPHAT) ⁽²⁾ | 0 | 0 | 0 | 0 | 0 | 0 |
| RESET ⁽³⁾ | 0 | 0 | 0 | 0 | 0 | 0 |
| Power-down ⁽⁴⁾ | 0 | 1 | 0 | 1 | 1 | 0 |
| Subsequent Power-up | 0 | 1 | 0 | 0 | 0 | 0 |

- Note: 1. WDS, BMB0-BMB4, RB0, RB1.
 2. State of other control bits undefined.
 3. State of other control bits remains unchanged.
 4. Assuming these bits set to '1' prior to power-down.



Figure 11. Crystal Accuracy Across Temperature

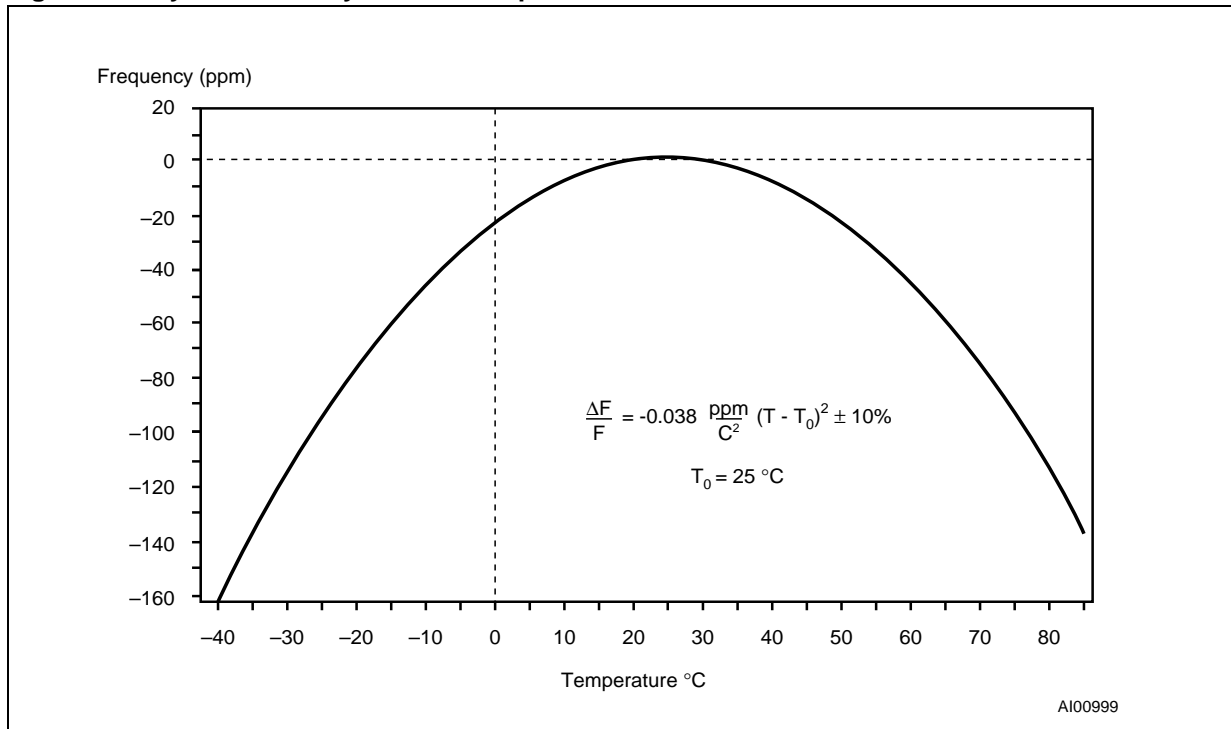
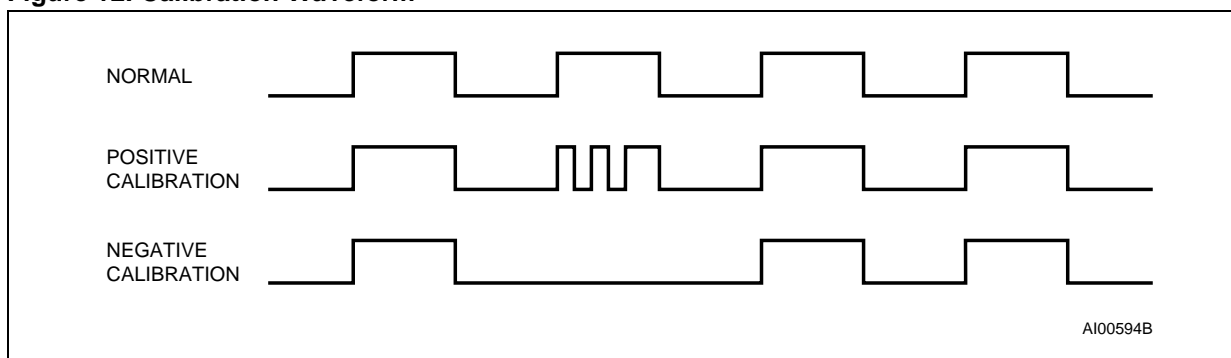


Figure 12. Calibration Waveform

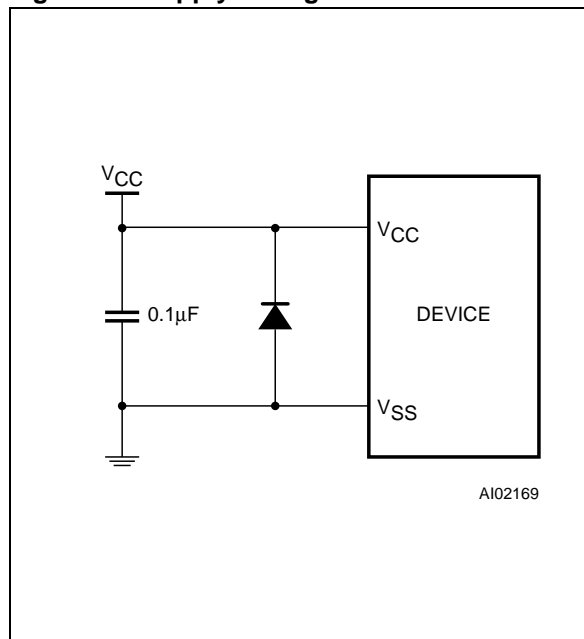


V_{CC} Noise And Negative Going Transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1μF (as shown in Figure 13) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, STMicroelectronics recommends connecting a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBR5120T3 is recommended for surface mount.

Figure 13. Supply Voltage Protection



MAXIMUM RATING

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is

not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 11. Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit | |
|-----------------------------------|--|-------------------------------|-------------|----|
| T _A | Ambient Operating Temperature | 0 to 70 | °C | |
| T _{STG} | Storage Temperature | SNAPHAT® | -40 to 85 | °C |
| | | SOIC | -55 to 125 | °C |
| T _{SLD} ^(1,2) | Lead Solder Temperature for 10 seconds | 260 | °C | |
| V _{IO} | Input or Output Voltage | -0.3 to V _{CC} + 0.3 | V | |
| V _{CC} | Supply Voltage | M48T212Y | -0.3 to 7.0 | V |
| | | M48T212V | -0.3 to 4.6 | V |
| I _O | Output Current | 20 | mA | |
| P _D | Power Dissipation | 1 | W | |

Note: 1. For SO package, standard (SnPb) lead finish: Reflow at peak temperature of 225°C (total thermal budget not to exceed 180°C for between 90 to 150 seconds).
 2. For SO package, Lead-free (Pb-free) lead finish: Reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).

CAUTION: Negative undershoots below -0.3V are not allowed on any pin while in the Battery Back-up mode.

CAUTION: Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measure-

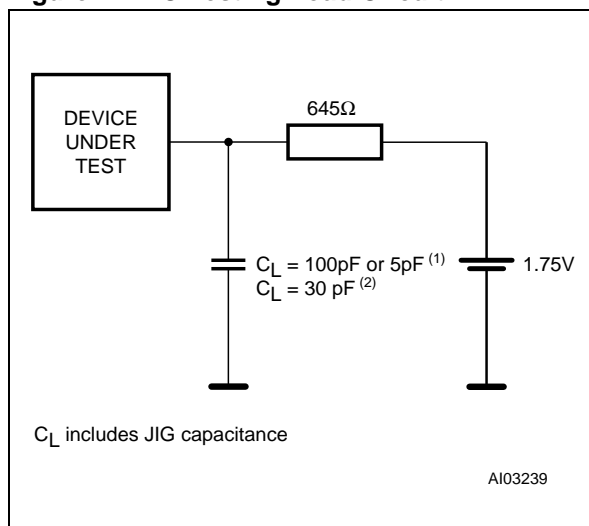
ment Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 12. DC and AC Measurement Conditions

| Parameter | | M48T212Y | M48T212V |
|---------------------------------------|---------|-------------|-------------|
| V _{CC} Supply Voltage | | 4.5 to 5.5V | 3.0 to 3.6V |
| Ambient Operating Temperature | Grade 1 | 0 to 70°C | 0 to 70°C |
| | Grade 6 | -40 to 85°C | -40 to 85°C |
| Load Capacitance (C _L) | | 100pF | 50pF |
| Input Rise and Fall Times | | ≤ 5ns | ≤ 5ns |
| Input Pulse Voltages | | 0 to 3V | 0 to 3V |
| Input and Output Timing Ref. Voltages | | 1.5V | 1.5V |

Note: Output High Z is defined as the point where data is no longer driven.

Figure 14. AC Testing Load Circuit



Note: Excluding open-drain output pins; 50pF for M48T212V.

1. DQ0-DQ7
2. $\overline{E1}_{CON}$ and $\overline{E2}_{CON}$

Table 13. Capacitance

| Symbol | Parameter ^(1,2) | Min | Max | Unit |
|---------------------------------|----------------------------|-----|-----|------|
| C _{IN} | Input Capacitance | | 10 | pF |
| C _{OUT} ⁽³⁾ | Input/Output Capacitance | | 10 | pF |

Note: 1. Effective capacitance measured with power supply at 5V (M48T212Y) or 3.3V (M48T212V); sampled only, not 100% tested.
 2. At 25°C, f = 1MHz.
 3. Outputs deselected.

Table 14. DC Characteristics

| Sym | Parameter | Test Condition ⁽¹⁾ | M48T212Y | | | M48T212V | | | Unit |
|----------------------------------|--|--|----------|------|-----------------------|----------|---------------------------|-----------------------|------|
| | | | -70 | | | -85 | | | |
| | | | Min | Typ | Max | Min | Typ | Max | |
| I _{LI} ⁽²⁾ | Input Leakage Current | 0V ≤ V _{IN} ≤ V _{CC} | | | ±1 | | | ±1 | μA |
| I _{LO} ⁽³⁾ | Output Leakage Current | 0V ≤ V _{OUT} ≤ V _{CC} | | | ±1 | | | ±1 | μA |
| I _{CC} | Supply Current | Outputs open | | 8 | 15 | | 4 | 10 | mA |
| I _{CC1} | Supply Current (Standby) TTL | $\bar{E} = V_{IH}$ | | | 5 | | | 3 | mA |
| I _{CC2} | Supply Current (Standby) CMOS | $\bar{E} = V_{CC} - 0.2$ | | | 3 | | | 2 | mA |
| I _{BAT} | Battery Current OSC ON | V _{CC} = 0V | | 575 | 800 | | 575 | 800 | nA |
| | Battery Current OSC ON ⁽⁴⁾ | | | 950 | 1250 | | 950 | 1250 | nA |
| | Battery Current OSC OFF | | | | 100 | | | 100 | nA |
| V _{IL} | Input Low Voltage | | -0.3 | | 0.8 | -0.3 | | 0.8 | V |
| V _{IH} | Input High Voltage | | 2.2 | | V _{CC} + 0.3 | 2.0 | | V _{CC} + 0.3 | V |
| V _{OL} | Output Low Voltage | I _{OL} = 2.1mA | | | 0.4 | | | 0.4 | V |
| | Output Low Voltage (open drain) ⁽⁵⁾ | I _{OL} = 10mA | | | 0.4 | | | 0.4 | V |
| V _{OH} | Output High Voltage | I _{OH} = -1.0mA | 2.4 | | | 2.4 | | | V |
| V _{OHB} ⁽⁶⁾ | V _{OH} Battery Back-up | I _{OUT2} = -1.0μA | 2.0 | | 3.6 | 2.0 | | 3.6 | V |
| I _{OUT1} ⁽⁷⁾ | V _{OUT} Current (Active) | V _{OUT1} > V _{CC} - 0.3 | | | 100 | | | 70 | mA |
| I _{OUT2} | V _{OUT} Current (Battery Back-up) | V _{OUT2} > V _{BAT} - 0.3 | | | 100 | | | 100 | μA |
| V _{PPFD} | Power-fail Deselect Voltage | | 4.2 | 4.35 | 4.5 | 2.7 | 2.9 | 3.0 | V |
| V _{SO} | Battery Back-up Switchover Voltage | | | 3.0 | | | V _{PPFD} - 100mV | | V |
| V _{BAT} | Battery Voltage | | | 3.0 | | | 3.0 | | V |

- Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C or -40 to 85°C; V_{CC} = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. RSTIN1 and RSTIN2 internally pulled-up to V_{CC} through 100KΩ resistor. WDI internally pulled-down to V_{SS} through 100KΩ resistor.
3. Outputs deselected.
4. I_{BAT} (OSC ON) = Industrial Temperature Range - Grade 6 device.
5. For IRQ/FT & RST pins (Open Drain).
6. Conditioned outputs ($\bar{E}1_{CON}$ - $\bar{E}2_{CON}$) can only sustain CMOS leakage currents in the battery back-up mode. Higher leakage currents will reduce battery life.
7. External SRAM must match TIMEKEEPER® SUPERVISOR chip V_{CC} specification.

Figure 15. Power Down/Up Mode AC Waveforms

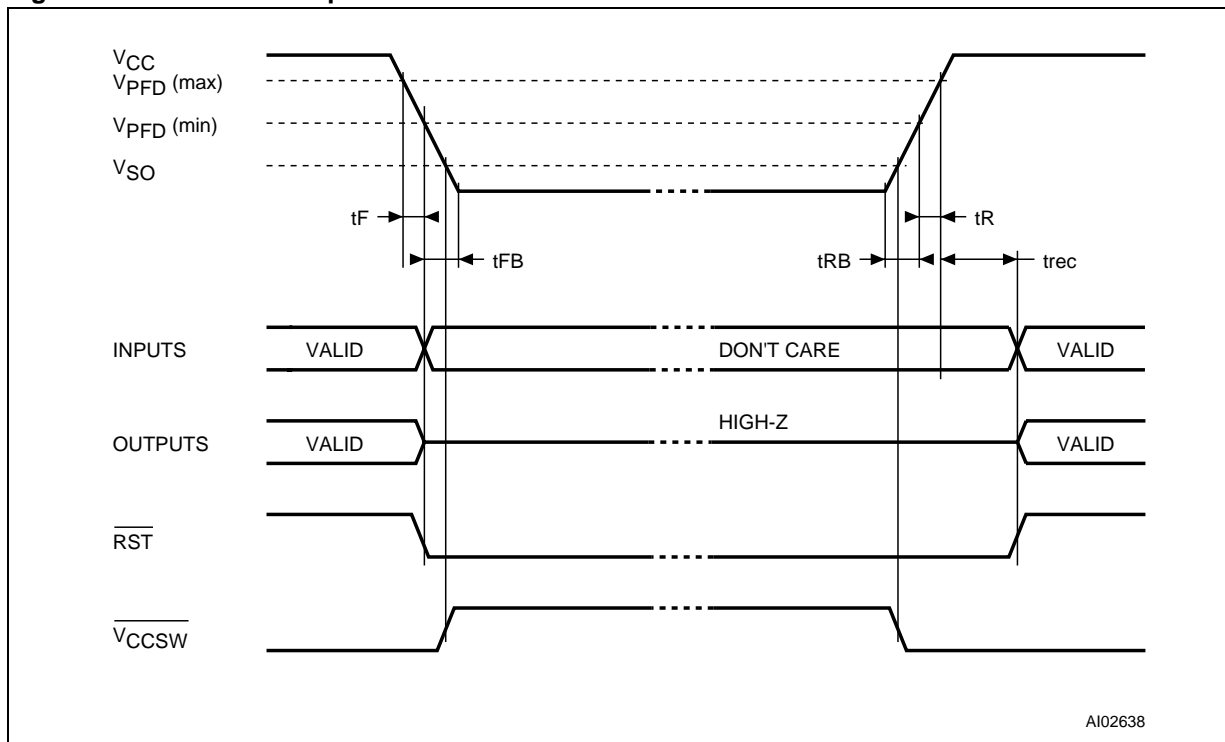


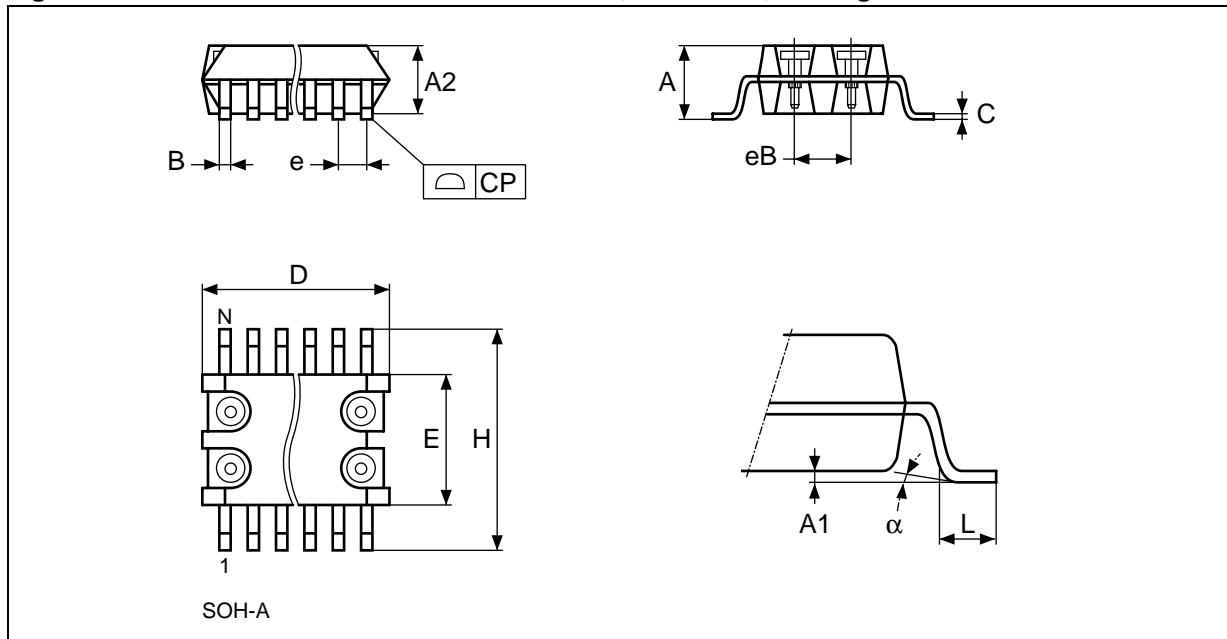
Table 15. Power Down/Up Mode AC Characteristics

| Symbol | Parameter ⁽¹⁾ | Min | Max | Unit |
|-----------|---|----------|-----|---------|
| t_F | $V_{PPFD}(\max)$ to $V_{PPFD}(\min)$ V_{CC} Fall Time | 300 | | μs |
| t_{FB} | $V_{PPFD}(\min)$ to V_{SS} V_{CC} Fall Time | M48T212Y | 10 | μs |
| | | M48T212V | 150 | μs |
| t_R | $V_{PPFD}(\min)$ to $V_{PPFD}(\max)$ V_{CC} Rise Time | 10 | | μs |
| t_{RB} | V_{SS} to $V_{PPFD}(\min)$ V_{CC} Rise Time | 1 | | μs |
| t_{rec} | $V_{PPFD}(\max)$ to \overline{RST} High | 40 | 200 | ms |

Note: 1. Valid for Ambient Operating Temperature: $T_A = 0$ to $70^\circ C$ or -40 to $85^\circ C$; $V_{CC} = 4.5$ to $5.5V$ or 3.0 to $3.6V$ (except where noted).

PACKAGE MECHANICAL INFORMATION

Figure 16. SOH44 – 44-lead Plastic Small Outline, SNAPHAT, Package Outline

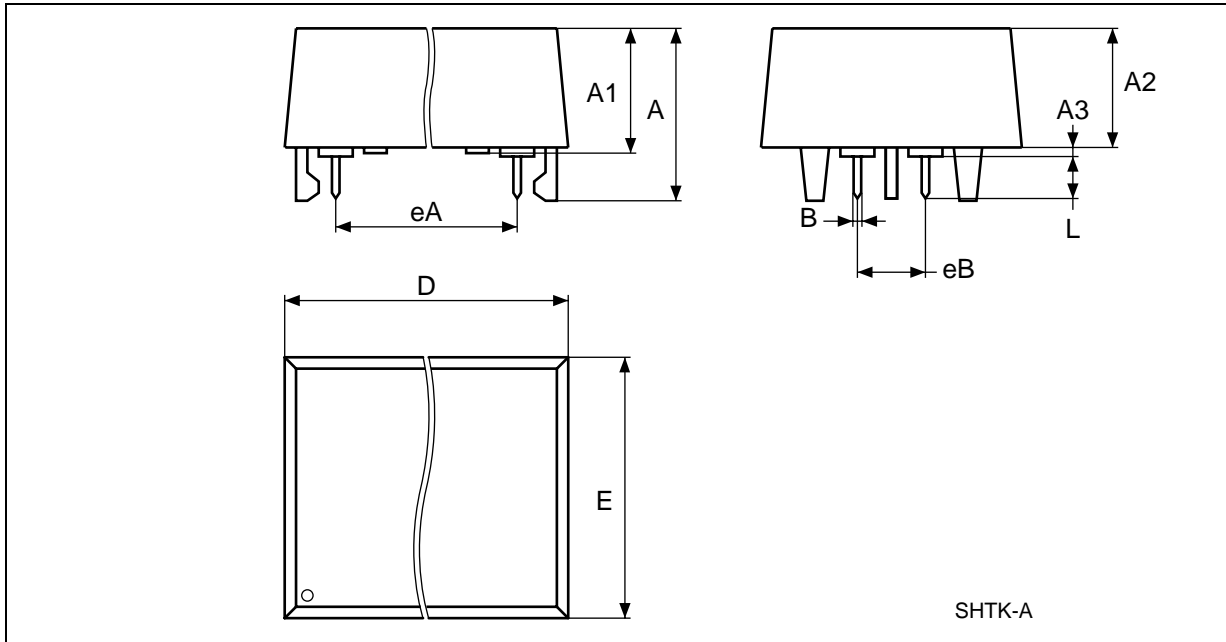


Note: Drawing is not to scale.

Table 16. SOH44 – 44-lead Plastic Small Outline, SNAPHAT, Package Mechanical Data

| Symb | mm | | | inches | | |
|----------|------|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 3.05 | | | 0.120 |
| A1 | | 0.05 | 0.36 | | 0.002 | 0.014 |
| A2 | | 2.34 | 2.69 | | 0.092 | 0.106 |
| B | | 0.36 | 0.46 | | 0.014 | 0.018 |
| C | | 0.15 | 0.32 | | 0.006 | 0.012 |
| D | | 17.71 | 18.49 | | 0.697 | 0.728 |
| E | | 8.23 | 8.89 | | 0.324 | 0.350 |
| e | 0.81 | – | – | 0.032 | – | – |
| eB | | 3.20 | 3.61 | | 0.126 | 0.142 |
| H | | 11.51 | 12.70 | | 0.453 | 0.500 |
| L | | 0.41 | 1.27 | | 0.016 | 0.050 |
| α | | 0° | 8° | | 0° | 8° |
| N | 44 | | | 44 | | |
| CP | | | 0.10 | | | 0.004 |

Figure 17. SH – 4-pin SNAPHAT Housing for 48 mAh Battery & Crystal, Package Outline

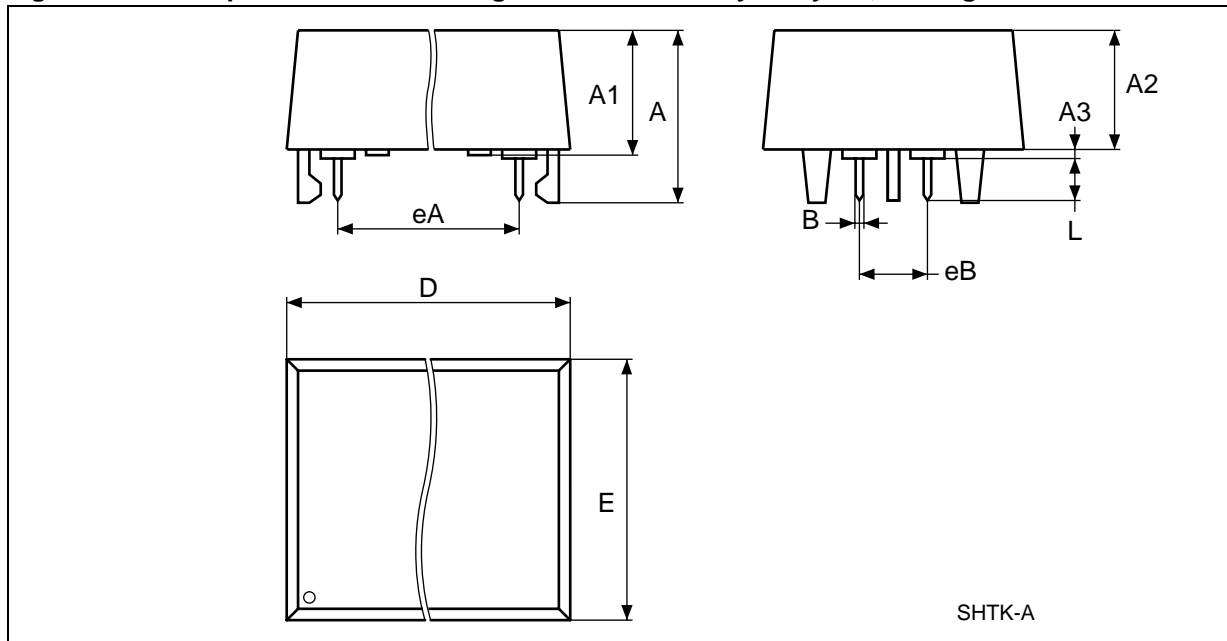


Note: Drawing is not to scale.

Table 17. SH – 4-pin SNAPHAT Housing for 48 mAh Battery & Crystal, Package Mech. Data

| Symb | mm | | | inches | | |
|------|-----|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 9.78 | | | 0.385 |
| A1 | | 6.73 | 7.24 | | 0.265 | 0.285 |
| A2 | | 6.48 | 6.99 | | 0.255 | 0.275 |
| A3 | | | 0.38 | | | 0.015 |
| B | | 0.46 | 0.56 | | 0.018 | 0.022 |
| D | | 21.21 | 21.84 | | 0.835 | 0.860 |
| E | | 14.22 | 14.99 | | 0.560 | 0.590 |
| eA | | 15.55 | 15.95 | | 0.612 | 0.628 |
| eB | | 3.20 | 3.61 | | 0.126 | 0.142 |
| L | | 2.03 | 2.29 | | 0.080 | 0.090 |

Figure 18. SH – 4-pin SNAPHAT Housing for 120mAh Battery & Crystal, Package Outline



Note: Drawing is not to scale.

Table 18. SH – 4-pin SNAPHAT Housing for 120mAh Battery & Crystal, Package Mech. Data

| Symb | mm | | | inches | | |
|------|-----|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 10.54 | | | 0.415 |
| A1 | | 8.00 | 8.51 | | 0.315 | .0335 |
| A2 | | 7.24 | 8.00 | | 0.285 | 0.315 |
| A3 | | | 0.38 | | | 0.015 |
| B | | 0.46 | 0.56 | | 0.018 | 0.022 |
| D | | 21.21 | 21.84 | | 0.835 | 0.860 |
| E | | 17.27 | 18.03 | | 0.680 | .0710 |
| eA | | 15.55 | 15.95 | | 0.612 | 0.628 |
| eB | | 3.20 | 3.61 | | 0.126 | 0.142 |
| L | | 2.03 | 2.29 | | 0.080 | 0.090 |

PART NUMBERING

Table 19. Ordering Information Example

| | | | | | | |
|--|------|------|-----|----|---|----|
| Example: | M48T | 212Y | -70 | MH | 1 | TR |
| Device Type | | | | | | |
| M48T | | | | | | |
| Supply and Write Protect Voltage | | | | | | |
| 212Y = $V_{CC} = 4.5$ to $5.5V$; $4.2V \leq V_{PFD} \leq 4.5V$ | | | | | | |
| 212V = $V_{CC} = 3.0$ to $3.6V$; $2.7V \leq V_{PFD} \leq 3.0V$ | | | | | | |
| Speed | | | | | | |
| -70 = 70ns (for M48T212Y) | | | | | | |
| -85 = 85ns (for M48T212V) | | | | | | |
| Package | | | | | | |
| MH ⁽¹⁾ = SOH44 | | | | | | |
| Temperature Range | | | | | | |
| 1 = 0 to 70°C | | | | | | |
| 6 = -40 to 85°C | | | | | | |
| Shipping Method | | | | | | |
| blank = Tubes (Not for New Design - Use E) | | | | | | |
| E = Lead-free Package (ECO [⊗] PACK [®]), Tubes | | | | | | |
| F = Lead-free Package (ECO [⊗] PACK [®]), Tape & Reel | | | | | | |
| TR = Tape & Reel (Not for New Design - Use F) | | | | | | |

Note: 1. The SOIC package (SOH44) requires the SNAPHAT[®] battery package which is ordered separately under the part number "M4Txx-BR12SH" in plastic tube or "M4Txx-BR12SHTR" in Tape & Reel form (see Table 20).

Caution: Do not place the SNAPHAT battery package "M4Txx-BR12SH" in conductive foam as it will drain the lithium button-cell battery.

For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.

Table 20. SNAPHAT[®] Battery Table

| Part Number | Description | Package |
|--------------|----------------------------------|---------|
| M4T28-BR12SH | Lithium Battery (48mAh) SNAPHAT | SH |
| M4T32-BR12SH | Lithium Battery (120mAh) SNAPHAT | SH |

REVISION HISTORY

Table 21. Document Revision History

| Date | Rev. # | Revision Details |
|--------------|--------|--|
| October 1999 | 1.0 | First Issue |
| 01-Mar-00 | 2.0 | Document Layout changed; Default Values table added (Table 10) |
| 21-Apr-00 | 3.0 | From Preliminary Data to Data Sheet |
| 10-Nov-00 | 3.1 | Table 16 changed |
| 30-May-01 | 3.2 | Changed "Controller" references to "SUPERVISOR" |
| 10-Sep-01 | 4.0 | Reformatted; added temp./voltage info. to tables (Table 14, 5, 6, 15, 9); added E2 to Hookup (Figure 4); Improve text in "Setting the Alarm Clock" section |
| 13-May-02 | 4.1 | Modify reflow time and temperature footnote (Table 11) |
| 16-Jul-02 | 4.1 | Updated DC Characteristics, footnotes (Table 14) |
| 27-Mar-03 | 5.0 | v2.2 template applied; updated test condition (Table 14) |
| 31-Mar-04 | 6.0 | Reformatted; updated with Pb-free information (Table 11, 19) |

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