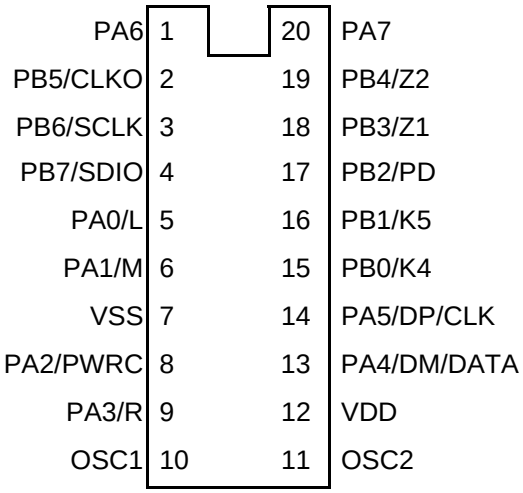
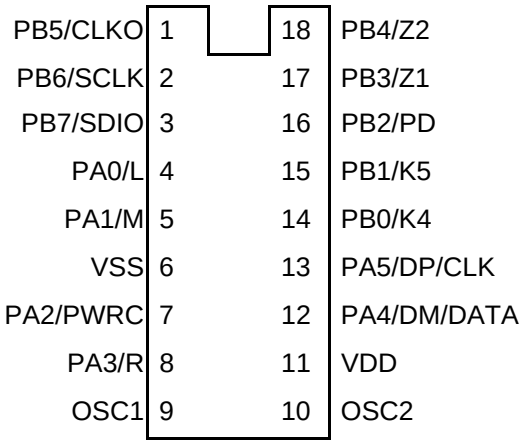
1. Features

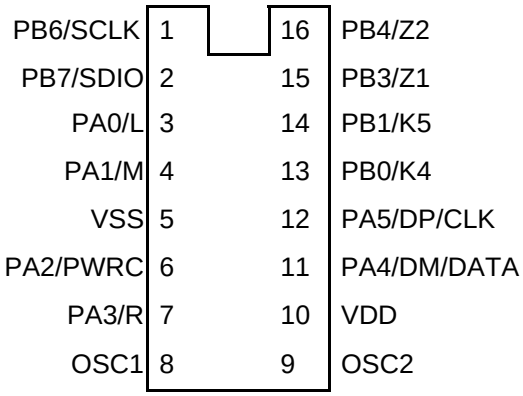
The followings are some of the features on the hardware and software :

- Special designed MCU for USB+PS/2
- Meet low-speed (1.5Mbps) USB spec Version 1.1
- Support 1 device address and 3 endpoints
- Working with Agilent ADNS-2610, ADNS-2620, ADNS-2051, ADNS-5020 or PixArt PAN101B, PAN3101 optical mouse sensor
- Fully CMOS static design
- 8-bit data bus
- On chip EPROM size: 2.5 K words
- Internal RAM size: 80 bytes
- 37 single word instructions
- 14-bit instructions
- 8-level stacks
- Operating voltage: 4.0 V ~ 5.25 V
- External oscillator frequency: 6-MHz/18-MHz/24-MHz
- Internal operation frequency: 12-MHz
- Addressing modes include direct, indirect and relative addressing modes
- Power-on Reset
- Power edge-detector Reset
- Sleep Mode for power saving
- 4 interrupt sources:
  - -TMR0 timer
  - -USB Endpoint 0
  - -USB Endpoint 1
  - -USB Endpoint 2
- TMR0: 8-bit timer
- 2 types of oscillator can be selected by programming option:
  XTAL－Standard crystal oscillator
  HFXT－High frequency crystal oscillator
- On-chip RC oscillator based Watchdog Timer (WDT)
- 16 I/O pins with their own independent direction control

2. Pin Assignment







3. Pin Function Description

Pin Name	I/O	Function Description
PB0/K4	I/O	Port B bit 0/Button 4/Optional internal 80K pull-up resistor
PB1/K5	I/O	Port B bit 1/Button 5/Optional internal 80K pull-up resistor
PB2/PD	I/O	Port B bit 2/PD signal for photo sensor/Optional internal 80K pull-up resistor
PB3/Z1	I/O	Port B bit 3/Input for Z1 axis/Optional internal 30K pull-down resistor mode
PB4/Z2	I/O	Port B bit 4/Input for Z2 axis/Optional internal 30K pull-down resistor
PB5/CLKO	I/O	Port B bit 5/Oscillation clock output for photo sensor/Optional internal 80K pull-up resistor
PB6/SCLK	I/O	Port B bit 6/Serial clock to Agilent sensor/Optional internal 80K pull-up resistor

Pin Name	I/O	Function Description
PB7/SDIO	I/O	Port B bit 7/Serial data from Agilent sensor/Optional internal 80K pull-up resistor
PA0/L	I/O	Port A bit 0/Left button input/Internal 80K pull-up resistor
PA1/M	I/O	Port A bit 1/Middle button input/Internal 80K pull-up resistor
PA2/PWR_C	I/O	Port A bit 2/Power control/Internal 80K Pull-up/Open drain output
PA3/R	I/O	Port A bit 3/Right button input/Internal 80K pull-up resistor
PA4/DM/DATA	I/O	USB D- or PS/2 data USB mode need 7.5K pull-up resistor to VDD
PA5/DP/CLK	I/O	USB D+ or PS/2 clock Port A bit 5 for PS2 mode internal 7.5K pull-up resistor
PA6	I/O	Port A bit 6/Internal 80K Pull-up
PA7	I/O	Port A bit 7/Internal 80K Pull-up
OSC1	I	Oscillator Input
OSC2	O	Oscillator Output
VDD		Power supply
VSS		Ground

4. Memory Map

(A) Register Map

Address	Description
BANK0	
00	Indirect Addressing Register
01	TMR0
02	PCL
03	STATUS0
04	MSR
05	Port A
06	Port B
0A	PCHLAT
0B	INTCON0
25	EP2TXC
26	EP0TXC
27	EP1TXC
28	USBDA
29	USBSCR
2A	EP0RXS
2B	INTCON1
2C	STATUS1
30~67	General purpose register
68~6F	USB FIFO ENDPOINT2
70~77	USB FIFO ENDPOINT0
78~7F	USB FIFO ENDPOINT1
BANK1	
01	OPTION
05	CPIOA
06	CPIOB

(1) IAR (Indirect Address Register): R00

Addressing this location will use the content of MSR to address data memory (not a physical register)

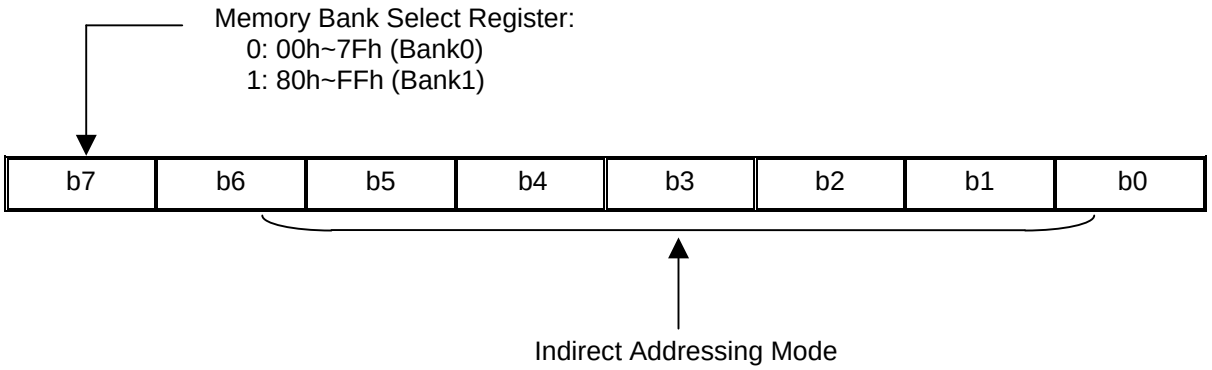
(2) TMR0: R01

(3) PC (Program Counter): R02, R0A

(4) STATUS (Status register): R03

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	/PF	Power down bit
4	/TF	WDT timer overflow bit
5	RP0	Register Bank select bit 0: 00h~7Fh (Bank0) 1: 80h~FFh (Bank1)
7~6	--	General purpose bit

(5) MSR (Memory Bank Select Register): R04



(6) PORT A: R05

PA7~PA0, PORTA data register

(7) PORT B: R06

PB7~PB0, PORTB data register

(8) PCHLAT: R0A

Write buffer for the upper 4 bits of the Program counter

(9) INTCON0 (Interrupt Status Register): R0B

Bit	Symbol	Function
1~0	--	Read as “0”
2	T0IF	Set when TMR0 overflows
4~3	--	Read as “0”
5	T0IE	0: Disable TMR0 interrupt 1: Enable TMR0 interrupt
6	--	Read as “0”
7	GIS	0: Disable global interrupt 1: Enable global interrupt

(10) OPTION: R81

Bit	Symbol	Function
0	PS0	Prescaler rate
1	PS1	Prescaler rate
2	PS2	Prescaler rate
3	PSA	Prescaler assignment bit
6~4	--	Read as “0”
7	/RBPU	0: Enable all the pull-up and pull-down resistors on PORTB 1: Disable all the pull-up and pull-down resistors on PORTB

(11) CPIOA: R85

PORTA data direction register

0: Output mode/1: Input mode

(12) CPIOB: R86

PORTB data direction register

0: Output mode/1: Input mode

USB FUNCTION REGISTERS

(13) EP2TXC: R25

USB Endpoint 2 transmit configuration

Bit	Symbol	Function
0	COUNT0	The number of data bytes to be transmitted during an IN packet
1	COUNT1	The number of data bytes to be transmitted during an IN packet
2	COUNT2	The number of data bytes to be transmitted during an IN packet
3	COUNT3	The number of data bytes to be transmitted during an IN packet
4	EP2EN	Enable Endpoint 2
5	STALL	Stall bit, Bit 5 is cleared when a SETUP packet is received
6	DATA 1/0	Bit 6 must be set to 0 or 1 to select the DATA packet toggle state
7	INEN	This bit is cleared when a ACK packet is received

(14) EP0TXC: R26

USB Endpoint 0 transmit configuration

Bit	Symbol	Function
0	COUNT0	The number of data bytes to be transmitted during an IN packet
1	COUNT1	The number of data bytes to be transmitted during an IN packet
2	COUNT2	The number of data bytes to be transmitted during an IN packet
3	COUNT3	The number of data bytes to be transmitted during an IN packet
4	ERR	A received DATA packet error occurred during a SETUP or OUT data phase
5	STALL	Stall bit, Bit 5 is cleared when a SETUP packet is received
6	DATA 1/0	Bit 6 must be set to 0 or 1 to select the DATA packet toggle state
7	INEN	This bit is cleared when a SETUP packet is received

(15) EP1TXC: R27

USB Endpoint 1 transmit configuration

Bit	Symbol	Function
0	COUNT0	The number of data bytes to be transmitted during an IN packet
1	COUNT1	The number of data bytes to be transmitted during an IN packet
2	COUNT2	The number of data bytes to be transmitted during an IN packet
3	COUNT3	The number of data bytes to be transmitted during an IN packet
4	EP1EN	Enable Endpoint 1
5	STALL	Stall bit, Bit 5 is cleared when a SETUP packet is received
6	DATA 1/0	Bit 6 must be set to 0 or 1 to select the DATA packet toggle state
7	INEN	This bit is cleared when a ACK packet is received

(16) USBDA: R28

USB device address

Bit	Symbol	Function
6~0	ADR6~0	This is a USB device address register
7	--	Read as “0”

(17) USBSCR: R29

USB status and control

Bit	Symbol	Function
0	BUSACT	BUSACT is set by SIE if any USB activity signal is detected. The user porgram should check and clear this bit periodically to detect any loss of bus activity. Writing a “0” to this bit clear it. Writing a “1” to this bit not set it.
1	Force K	0: Not forcing 1: Force K (D+ HIGH, D - Low)
2	Force J	0: Not forcing 1: Force J (D+ Low, D - High)
3	STAOUTS	0: Disable control read transfer 1: Enable control read transfer
4	ENOUTS	0: Disable control writer transfer 1: Enable control writer transfer
7~5	--	Read as “0”

(18) EP0RXS: R2A

USB Endpoint 0 receive status

Bit	Symbol	Function
0	SETUP	Bit 0 is set to 1 when a SETUP packet is received
1	OUT	Bit 1 is set to 1 when a OUT packet received
2	IN	Bit 2 is set to 1 when a IN packet received
3	DATA 1/0	DATA Toggle status
4	COUNT0	The number of bytes received in DATA packet
5	COUNT1	The number of bytes received in DATA packet
6	COUNT2	The number of bytes received in DATA packet
7	COUNT3	The number of bytes received in DATA packet

(19) INTCON1: R2B

Interrupt control register1

Bit	Symbol	Function
0	EP0IF	Endpoin 0 interrupt flag
1	EP1IF	Endpoin 1 interrupt flag
2	EP2IF	Endpoin 2 interrupt flag
3	--	Read as “0”
4	EP0IE	Endpoint 0 interrupt enable bit, 0: Disable/1: Enable
5	EP1IE	Endpoint 1 interrupt enable bit, 0: Disable/1: Enable
6	EP2IE	Endpoint 2 interrupt enable bit, 0: Disable/1: Enable
7	--	Read as “0”

(20) STATUS1: R2C

Status register1

Bit	Symbol	Function
0	PS2CLK	PS2 CLK pull-up, 0: Disable/1: Enable
1	PB5/CLKO	0: PB5/1: CLKO
2	USBPS2	0: USB mode/1: PS2 mode
3	SUSPEND	0: Normal mode/1: Sleep mode
4	POR	Power on reset
5	USBR	USB reset
7~6	--	Read as “0”

(B) Program Memory

Address	Description
000-9FF	Program memory
000	Reset vector
004	Interrupt vector

5. SPECIAL FUNTION REGISTER SUMMARY

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	POR	Other reset
00h	IAR	Addressing this location will use the content of MSR to address data memory								0000 0000	0000 0000
01h	TMR0	Timer0 registe								xxxx xxxx	uuuu uuuu
02h	PCL	Program counter's low byte								0000 0000	0000 0000
03h	STATUS			RP0	/TO	/PD	Z	DC	C	--01 1xxx	--q quuu
04h	MSR	Indirect data memory address register								xxxx xxxx	uuuu uuuu
05h	PORTA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	xxxx xxxx	uuuu uuuu
06h	PORTB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	xxxx xxxx	uuuu uuuu
0Ah	PCH					PCH3	PCH2	PCH1	PCH0	---- 0000	---- 0000
0Bh	INTCON0	GIE		T0IE			T0IF			0-0- -0--	0-0- -0--
25h	EP2TXC	INEN	DATA1/0	STALL	EN2EN	COUNT3	COUNT2	COUNT1	COUNT0	0000 0000	0000 0000
26h	EP0TXC	INEN	DATA1/0	STALL	ERR	COUNT3	COUNT2	COUNT1	COUNT0	0000 0000	0000 0000
27h	EP1TXC	INEN	DATA1/0	STALL	EP1EN	COUNT3	COUNT2	COUNT1	COUNT0	0000 0000	0000 0000
28h	USBDA		ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	0000 0000	0000 0000

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	POR	Other reset
29h	USBSCR				ENOUTS	STAOUTS	FORCEJ	FORCEK	BUSACT	---0 0000	---0 0000
2Ah	EP0RXS	COUNT3	COUNT2	COUNT1	COUNT0	DATA1/0	IN	OUT	SETUP	0000 0000	0000 0000
2Bh	INTCON1		EP2IE	EP1IE	EP0IE		EP2IF	EP1IF	EP0IF	-000 -000	-000 -000
2Ch	STATUS1			USBR	POR	SUSPED	USB/PS2	PB5/CLKO	PS2CLK	--01 0100	--01 0uuu
81h	OPTION	/RBPU				PSA	PS2	PS1	PS0	1--- 1111	1--- 1111
85h	CPIOA	CPIOA7	CPIOA6	CPIOA5	CPIOA4	CPIOA3	CPIOA2	CPIOA1	CPIOA0	1111 1111	uuuu uuuu
86h	CPIOB	CPIOB7	CPIOB6	CPIOB5	CPIOB4	CPIOB3	CPIOB2	CPIOB1	CPIOB0	1111 1111	uuuu uuuu

Note: u=unchanged, x=unknown, -=unimplemented, read as “0”

q=value depends on the condition of the following table

STATUS0 BITS THEIR SIGNIFICANCE

/TO	/PD	Condition
1	1	Power on reset
0	1	WDT reset
0	0	WDT wake_up
u	u	USB reset durning normal operation
1	0	Interrupt wake_up from sleep

RESET CONDITON FOR SPECIAL REGISTER

Condition	Porgram counter	Status0 register
Power on reset	000h	--01 1xxx
USB reset durning normal operation	000h	--0u uuuu
WDT reset	000h	--00 1uuu
WDT wake_up	PC+1	--u0 0uuu
Interrupt wake_up from sleep	PC+1	uuu1 0uuu

x=unknown, u=unchanged, q=value depends on condtion, -=unimplemented,read as “0”

6. Instruction Set

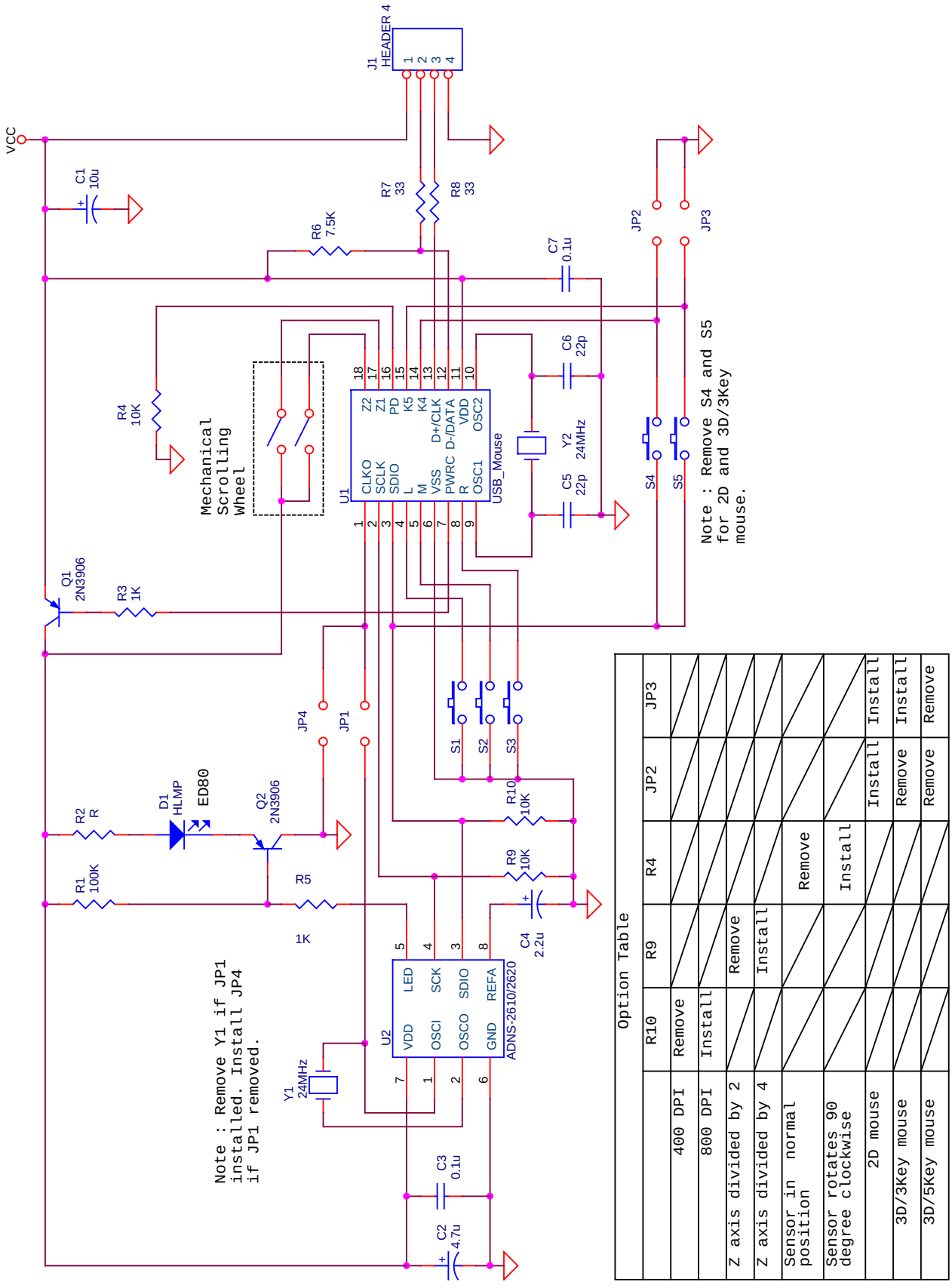
Instruction Code	Mnemonic Operands	Function	Operating	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMODE register	W→TMODE	None
010000 00000100	RET	Return from subroutine	Stack→PC	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO R	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R, t	Load register	R→t	Z
111010 iiiiiiii	LDWI i	Load immediate to W	i→W	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0~3) ↔R(4~7)] →t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1→t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R→t	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R – W→t or (R+/W+1→t)	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	R – 1→t	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	R – 1→t	None
010010 trrrrrrr	ANDWR R, t	AND W and register	R ∩ W→t	Z
110100 iiiiiiii	ANDWI i	AND W and immediate	i ∩ W→W	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z
110101 iiiiiiii	IORWI i	Inclu. OR W and immediate	i ∪ W→W	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
110110 iiiiiiii	XORWI i	Exclu. OR W and immediate	i ⊕ W→W	Z
011111 trrrrrrr	COMR R, t	Complement register	/R→t	Z
010110 trrrrrrr	RRR R, t	Rotate right register	R(n) →R(n-1), C→R(7), R(0)→C	C
010101 trrrrrrr	RLR R, t	Rotate left register	R(n)→r(n+1), C→R(0), R(7)→C	C
010000 1xxxxxxx	CLRW	Clear working register	0→W	Z
010001 0rrrrrrr	CLRR R	Clear register	0→R	Z
0000bb brrrrrrr	BCR R, b	Bit clear	0→R(b)	None
0010bb brrrrrrr	BSR R, b	Bit set	1→R(b)	None
0001bb brrrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None

Instruction Code	Mnemonic Operands	Function	Operating	Status
100nnn nnnnnnnn	LCALL n	Long CALL subroutine	n→PC, PC+1→Stack	None
101nnn nnnnnnnn	LJUMP n	Long JUMP to address	n→PC	None
110111 iiiiiiii	ADDWI i	Add immediate to W	W+i→W	C,HC,Z
110001 iiiiiiii	RTWI i	Return, place immediate to W	Stack→PC,i→W	None
111000 iiiiiiii	SUBWI i	Subtract W from immediate	i-W→W	C,HC,Z
010000 00001001	RTFI	Reture from interrupt	Stack→PC,1→GIS	None

Note :

W	:	Working register	b	:	Bit position
WT	:	Watchdog timer	t	:	Target
TMODE	:	TMODE mode register		0	: Working register
CPIO	:	Control I/O port register		1	: General register
TF	:	Timer overflow flag	R	:	General register address
PF	:	Power loss flag	C	:	Carry flag
PC	:	Program Counter	HC	:	Half carry
OSC	:	Oscillator	Z	:	Zero flag
Inclu.	:	Inclusive '∪'	/	:	Complement
Exclu.	:	Exclusive '⊕'	x	:	Don't care
AND	:	Logic AND '∩'	i	:	Immediate data (8 bits)
			n	:	Immediate address

9. Application Circuit



Option Table

	R10	R9	R4	JP2	JP3
400 DPI	Remove				
800 DPI	Install				
Z axis divided by 2		Remove			
Z axis divided by 4		Install			
Sensor in normal position			Remove		
Sensor rotates 90 degree clockwise			Install		
2D mouse				Install	Install
3D/3Key mouse				Remove	Install
3D/5Key mouse				Remove	Remove