ANALOG DEVICES

Low Cost, Low Power Stereo Audio Codec

Preliminary Technical Data   AD74122

FEATURES

2.5V Stereo Audio Codec with 3.3 V Tolerant Digital Interface
Supports 8kHz to 48 kHz Sample Rates
Supports 16/20/24-Bit Word Lengths
Multibit Sigma Delta Modulators with
   "Perfect Differential Linearity Restoration" for
   Reduced Idle Tones and Noise Floor
Data Directed Scrambling DACs - Least Sensitive to Jitter
Performance (20 Hz to 20 kHz)
   85 dB ADC Dynamic Range
   93 dB DAC Dynamic Range
Digitally Programmable Input/Output Gain
On-chip Volume Controls Per Output Channel
Software Controllable Clickless Mute
Supports 256xFs, 512xF$_s$ and 768xFs Master Mode Clocks
Master Clock Pre-Scaler for use with DSP master clocks
On-Chip Reference
 20-Lead TSSOP Package

APPLICATIONS

Digital Video Camcorders (DVC)
Portable Audio Devices (Walkman, PDAs etc.)
Audio Processing
Voice Processing
Telematic Systems
General Purpose Analog I/O

GENERAL DESCRIPTION

The AD74122 is a front-end processor for general purpose audio and voice applications. It features two multi-bit $\Sigma\Delta$ A/D conversion channels and two multi-bit $\Sigma\Delta$ D/A conversion channels. The ADC channels provide >70 dB SNR and the DAC channels provide >80dB SNR both over an audio signal bandwidth.
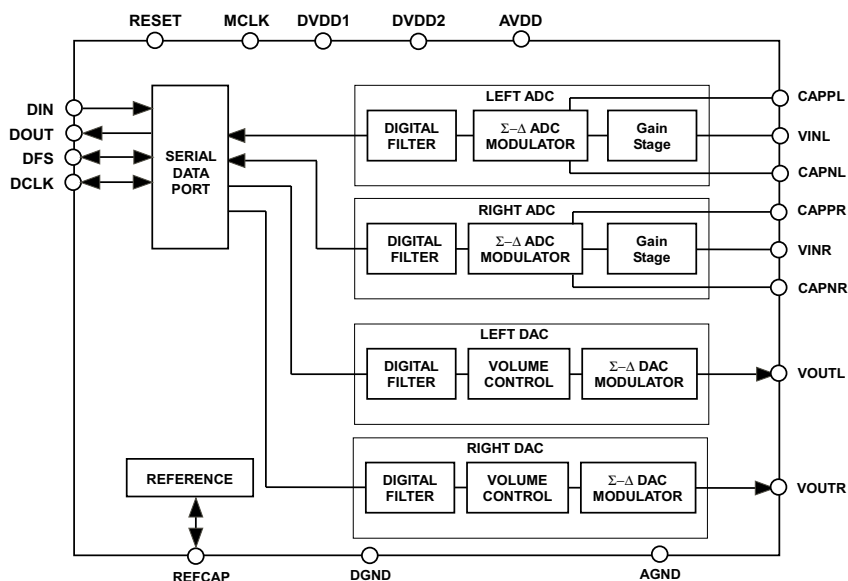
The AD74122 is particularly suitable for a variety of applications where stereo input and output channels are required, including audio sections of Digital Video Camcorders, portable personal audio devices and telematic applications. Its high quality performance also make it suitable for speech and telephony applications such as speech recognition and synthesis and modern feature phones.

An on-chip reference voltage is included but can be overdriven by an external reference source if required.

The AD74122 offers sampling rates which, depending on MCLK selection and MCLK divider ratio, range from 8 kHz in the voiceband range to 48 kHz in the audio range.

The AD74122 is available in 20 lead TSSOP package option and is specified for the automotive temperature range of -40°C to +105°C.

FUNCTIONAL BLOCK DIAGRAM

AD74122–SPECIFICATIONS (AVDD =2.5V ±5%, DVDD2 = 2.5V ±5%, DVDD1 = 2.5V ±5%, f_{CLKIN} = 12.288 MHz, f_{SAMP} = 48 kHz, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

PARAMETER	Min	Typ	Max	Units	Test Conditions
ANALOG-TO-DIGITAL CONVERTERS					
ADC Resolution		24		Bits	
Signal to Noise Ratio (SNR)	70	77		dB	
Dynamic Range					
(20 Hz to 20 kHz, -60 dB Input)					
No Filter		85		dB	f_S=48kHz
	78	85		dB	f_S=16kHz
With A-Weighted Filter		92		dB	f_S=48kHz
Total Harmonic Distortion + Noise		-67		dB	f_S=48kHz
		-75		dB	f_S=16kHz
Programmable Input Gain		12		dB	
Gain Step Size			3	dB	
Offset Error	-55	30	80	mV	
Gain Error		-1.5		dB	
Full Scale Input Voltage		0.5		Vrms	
Input Resistance		10		kΩ	
Input Capacitance			15	pF	
Common Mode Input Volts		1.125		V	
Crosstalk		100		dB	ADC Input Signal=1.0kHz, 0dB; DAC Output=DC
DIGITAL-TO-ANALOG CONVERTERS					
DAC Resolution		24		Bits	
Signal to Noise Ratio (SNR)	80	89		dB	
Dynamic Range					
(20 Hz to 20 kHz, -60 dB Input)					
No Filter		93		dB	f_S=48kHz
	84	93		dB	f_S=16kHz
With A-Weighted Filter		95		dB	f_S=48kHz
Total Harmonic Distortion + Noise		-88		dB	f_S=48kHz
		-88	-81	dB	f_S=16kHz
DC Accuracy					
Offset Error	-75	10	50	mV	
Gain Error	-1.0	0.2	1.0	dB	
Volume Control Step Size					
(1023 Linear Steps)		0.098		%	
Volume Control Range (Max Attenuation)		60		dB	
Mute Attenuation		-100		dB	
De-emphasis Gain Error		+/- 0.1		dB	
Full Scale Output Voltage		0.5		Vrms	
Output Resistance		145		Ω	
Common Mode Output Volts		1.125		V	
Crosstalk		95		dB	ADC Input Signal=AGND; DAC Output Level=1.0kHz, 0dB
REFERENCE (Internal)					
Absolute Voltage, V_{REF}		1.125		V	
V_{REF} TC		TBD		ppm/°C	

REV.PrG

| PARAMETER | AD74122 | | | Units | Test Conditions |
	Min	Typ	Max		
ADC DECIMATION FILTER[1]					f_S=48kHz
Pass Band			21.5	kHz	
Pass Band Ripple			0.2	mdB	
Transition Band		5		kHz	
Stop Band	26.5			kHz	
Stop Band Attenuation	120			dB	
Group Delay		910		μs	
Low Group Delay Mode		87		μs	
DAC INTERPOLATION FILTER[1]					f_S=48kHz
Pass Band			21.5	kHz	
Pass Band Ripple			10	mdB	
Transition Band		5		kHz	
Stop Band	26.5			kHz	
Stop Band Attenuation	75			dB	
Group Delay		505		μs	
Low Group Delay Mode		55		μs	
LOGIC INPUT					
V_{INH}, Input High Voltage	DVDD1 - 0.8		DVDD1	V	
V_{INL}, Input Low Voltage	0		0.8	V	
Input Current -10		+10		μA	
Input Capacitance			10	pF	
LOGIC OUTPUT					
V_{OH}, Output High Voltage	DVDD1 - 0.4		DVDD1	V	
V_{OL}, Output Low Voltage	0		0.4	V	
Three-State Leakage Current	-10		+10	μA	
POWER SUPPLIES					
AVDD	2.375		2.75	V	
DVDD2	2.25		2.75	V	
DVDD1	2.25		3.36	V	
Power Supply Rejection Ratio					
1kHz, 300mV p-p Signal at Analog Supply Pins		72		dB	
50/60Hz, 300mV p-p Signal at Analog Supply Pins		73		dB	

NOTES
[1]Guaranteed by Design
Specifications subject to change without notice.

Table I. Current Summary (AVDD= 2.5V; DVDD1=2.5V; DVDD2=2.5V)

Conditions	AVDD Current	DVDD1 Current	DVDD2 Current	Total Current (Max)
ADC, Reference, Ref-Amp On	TBD	TBD	TBD	
DAC, Reference, Ref-Amp On	TBD	TBD	TBD	
Reference, Ref-Amp On	TBD	TBD	TBD	
All Sections On	TBD	TBD	TBD	TBD
Powerdown Mode	TBD	TBD	TBD	TBD

NOTES
All Values are typical unless otherwise noted.
Max values are quoted with DVDD1=3.6V
Sample Rates quoted are for 16kHz and (48kHz)

AD74122–SPECIFICATIONS

(AVDD =2.5V ±5%, DVDD2 = 2.5V ±5%, DVDD1 = 2.5V ±5%, f_{CLKIN} = 12.288 MHz, f_{SAMP} = 48 kHz, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter		Min	Max	Unit	Comments
MASTER CLOCK AND RESET					
t_{MH}	MCLK High	25		ns	
t_{ML}	MCLK Low	25		ns	
t_{RES}	RESET Low	20		ns	
t_{RS}	DIN Setup Time	5		MCLKs	To RESET Rising Edge[1]
t_{RH}	DIN Hold Time	5		MCLKs	To RESET Rising Edge[1]
SERIAL PORT					
t_{FD}	DFS Delay		5	ns	From DCLK Rising Edge[2]
t_{FS}	DFS Setup Time	5		ns	To DCLK FallingEdge
t_{FH}	DFS Hold Time	5		ns	From DCLK Falling Edge
t_{DD}	DOUT Delay		5	ns	From DCLK Rising Edge
t_{DS}	DIN Setup Time	10		ns	To DCLK Falling Edge
t_{DH}	DIN Hold Time	10		ns	From DCLK Falling Edge
t_{DT}	DOUT Three-State		25	ns	From DCLK Rising Edge
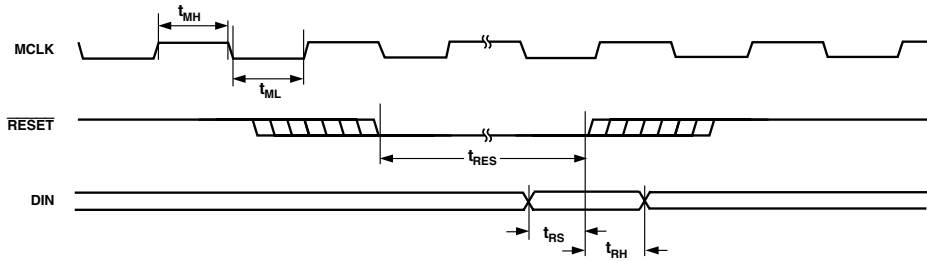
Figure <reset.eps> MCLK and RESET Timing
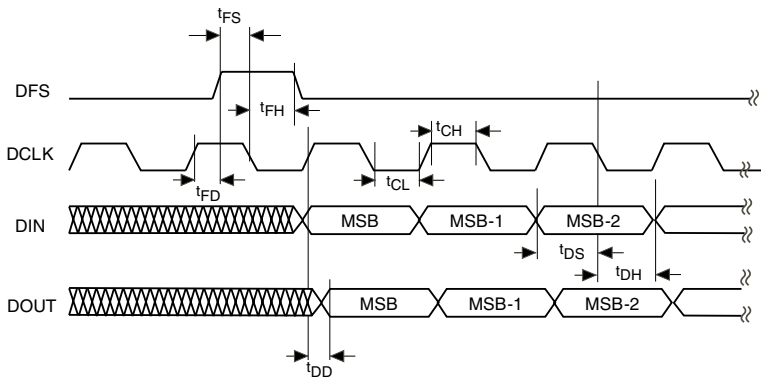
Figure <sporttiming.eps>. Serial Port Timing
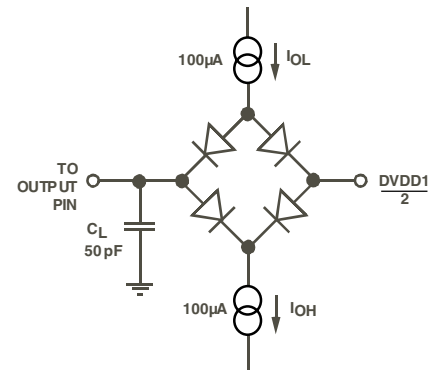
Figure <loadcircuit.eps>. Load Circuit for Digital Output Timing Specification

TEMPERATURE RANGE

Parameter	Min	Max	Unit
Specifications Guaranteed	-40	+105	ºC
Storage	-65	+150	ºC

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C, unless otherwise noted.)

AVDD, DVDD2 to AGND, DGND

$\quad\quad\quad\quad\quad\quad\quad\quad$ −0.3 V to +3.0 V

DVDD1 to AGND, DGND $\quad\quad$ -0.3 V to +4.5 V

AGND to DGND $\quad\quad\quad\quad$ −0.3 V to +0.3 V

Digital I/O Voltage to DGND $\quad$ −0.3 V to DVDD1 + 0.3 V

Operating Temperature Range

$\quad$ Automotive (Y Version) $\quad\quad$ −40°C to +105°C

Storage Temperature Range $\quad$ -65°C to +150°C

Junction Temperature $\quad\quad\quad\quad$ 150°C

20 Lead TSSOP, θ_{JA} Thermal Impedance $\quad$ 150.4°C/W

Lead Temperature, Soldering

$\quad$ Vapour Phase (60 sec) $\quad\quad\quad\quad$ 215°C

$\quad$ Infrared (15 sec) $\quad\quad\quad\quad\quad$ 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Range	Package
AD74122YRU	-40ºC to +105ºC	RU-20

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD74122 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD74122

PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	I/O	Description
1	DCLK	I/O	Data Port Serial Clock
2	DIN	I	Data Port Serial Data Input. The state of DIN on the rising edge of RESET determines the operating mode of the interface, see Data Port Interface section for more information
3	DFS	I/O	Data Port Frame Synchronisation signal
4	DOUT	O	Data Port Serial Data Output
5	$\overline{\text{RESET}}$	I	Powerdown/Reset Input
6	AVDD		Analog Power Supply Connection
7	CAPN2		Filter Capacitor for Channel 2 (Right Channel) Negative
8	CAPP2		Filter Capacitor for Channel 2 (Right Channel) Positive
9	VOUTL	O	Analog Output - Left Channel
10	VINR	I	Analog Input - Right Channel
11	VINL	I	Analog Input - Left Channel
12	VOUTL	O	Analog Output - Right Channel
13	CAPP1		Filter Capacitor for Left Channel (Positive)
14	CAPN1		Filter Capacitor for Left Channel (Negative)
15	REFCAP	I/O	Internal Reference Decoupling Capacitor - Can also be used for connection of an external reference
16	AGND		Analog Ground Connection
17	DGND		Digital Ground Connection
19	DVDD2		Digital Power Supply Connection (Core)
19	DVDD1		Digital Power Supply Connection (Interface)
20	MCLK	I	External Master Clock Input

PIN CONFIGURATION

20-Lead TSSOP

(RU-20)

```
        DCLK  1 ●          20  MCLK
         DIN  2            19  DVDD1
         DFS  3            18  DVDD2
        DOUT  4            17  DGND
       RESET  5   AD74122  16  AGND
        AVDD  6   TOP VIEW 15  REFCAP
       CAPNR  7 (Not to Scale) 14  CAPPR
       CAPNL  8            13  CAPPL
       VOUTL  9            12  VOUTR
        VINR 10            11  VINL
```
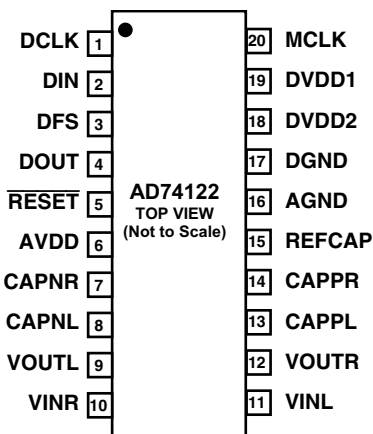
FUNCTIONAL DESCRIPTION

General Description

The AD74122 is a 2.5V stereo codec. It comprises two ADC and two DAC channels with single ended inputs and outputs. Signal conditioning and programmable gain stages are also provided. Each of these sections are described in further detail below. The AD74122 is controlled by means of a flexible serial interface port (SPORT) which can be programmed to accomodate many industry standard DSPs and Microcontrollers. The AD74122 can be set to operate as a master or slave device. The AD74122 can also be set to operate with sample rates of 8KHz to 48KHz depending on the values of MCLK and the MCLK prescalers. On chip digital filtering is provided for the DAC and ADC channels with a low group delay option to reduce the delays through the filters when operating at lower sample rates. Figure <modulators.eps> shows a block diagram of a DAC and ADC channel in the AD74122. Figure <filter.eps> shows a block diagram of the filter arrangement of the ADC and DAC filters.
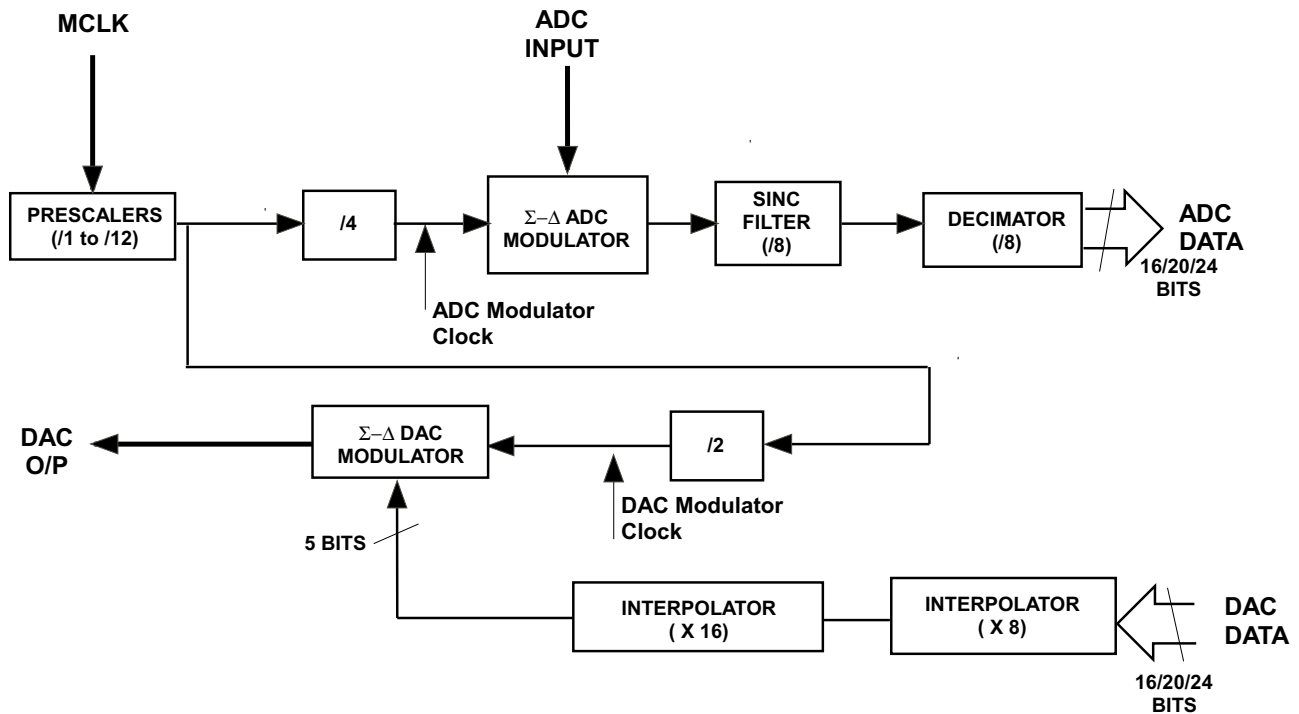
Figure <modulators.eps>. ADC and DAC Engine
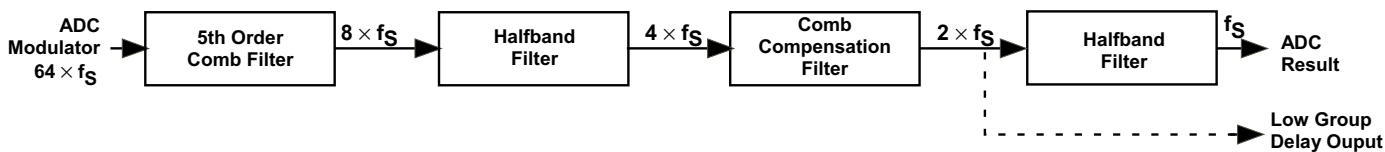
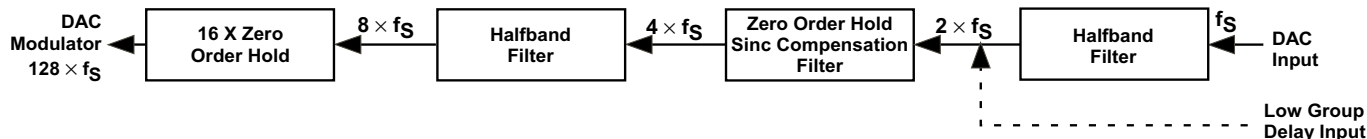Figure <ADC Filter.eps>. ADC Filter Section

Figure <dac filter.eps>. DAC Filter Section

ADC Section

There are two ADC channels in the AD74122, configured as a stereo pair. Each ADC channel can be independently muted under software control. Each ADC has single input pin with additional pins for decoupling/filter capacitors. Each ADC channel has an independent input amplifier gain stage which can be programmed in steps of +3dB, from 0dB to +12dB. The input amplifier gain settings are set by programming the appropriate bits in Control Register E for the left ADC and Control Register H for the right ADC. The AD74122 input channels employ a multi-bit sigma-delta conversion technique, which provides a high resolution output with system filtering being implemented on-chip. Sigma-delta converters employ a technique known as over-sampling, where the sampling rate is many times the highest frequency of interest. The oversampling ratio for the ADC is 64 and a decimation filter is used to reduce the output to standard sample rates. The maximum sample rate is 48kHz.

ADC CAPP and CAPN Pins

The ADC channel requires two external capacitors to act as charge resevoirs for the switched capacitor inputs of the sigma-delta modulator. These capacitors isolate the outputs of the PGA stage from glitches generated by the sigma-delta modulator. The capacitor also forms a low pass filter with the output impedance of the PGA (approximately 124Ω) which helps to isolate noise from the modulator engine. The capacitors should be of good quality such as NPO or polyproplene film and values from 100pF to 1nF are suitable.

Peak Readback

The AD74122 can store the highest ADC value from each channel in order to facilatate level adjustment of the input signal. Programming the Peak Enable bit in Control Register H with a 1 will enable ADC Peak Level Reading. The Peak values are stored as a 6 bit number from 0dB to -63dB in 1dB steps. Reading Control Register F and I will give the highest ADC values for the left ADC and right ADC respectively, since the bit was set. The ADC Peak registers are automatically cleared after reading.

Decimator Section

The digital decimation filter has a passband ripple of ±0.002dB and a stopband attenuation of 120dB. The filter is an FIR type with a linear phase response. The group delay at 48kHz is 910us. Output sample rates up to 48 kHz are supported.

Input Signal swing

Each ADC input has an input range of 0.5 V_{RMS} / 1.414 V_{P-P} about a bias point equal to V_{REFCAP} (See Figure <ADC_cct>). The analog input can also be AC coupled to the AD74122 as shown which will automatically bias the signal to the V_{REFCAP} value internally. This allows signals biased around a voltage other than V_{REFCAP} to be connected directly to the AD74122.
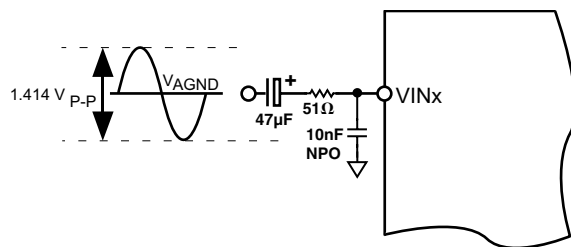
Figure <ADC_cct.eps>.Input Swing

DAC Section

The AD74122 has two DAC channels arranged as a stereo pair, with two, single-ended, analog outputs. Each channel has it's own independently programmable attenuator. Control Register G controls the attenuation factor for the left DAC while Control Register J controls the attenuation factor for the right DAC. Each of these registers is 10 bits wide giving 1024 steps of attenuation. AD74122 output channels employ a multi-bit sigma-delta conversion technique, which provides a high quality output with system filtering being implemented on-chip.

Output Signal swing

Each DAC input has an output range of 0.5 V_{RMS} / 1.414 V_{P-P} (Single-Ended) about a bias point equal to V_{REFCAP} (See Figure <DAC_cct>)
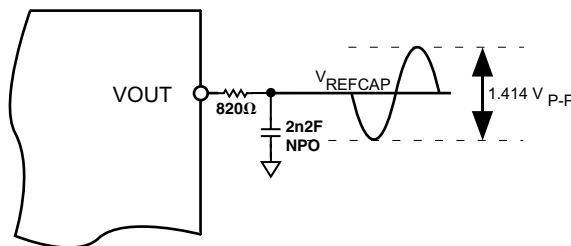
Figure <DAC_cct>

Low Group Delay

It is possible to bypass much of the digital filtering by enabling the Low Group Delay function in Control Register C. By reducing the amount of filtering the AD74122 applies to input and output samples the time delay between the sampling interval and when the sample is available is greatly reduced. This can be of benefit in applications such as telematics where minimal time delays are important. When the Low Group Delay function is enabled the sample rate becomes IMCLK/128.

Reference

The AD74122 features an on-chip reference whose nominal value is 1.125 V. A 10 nF capacitor applied at the REFCAP pin is necessary to stabilise the referrence. (See Figure <REFCAP_Int>)

Figure <REFCAP_Int.eps>

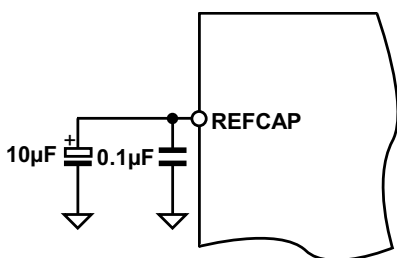If it is required an external reference can be used as the reference source of the ADC and DAC sections. This may be desirable in situations where multiple devices are required to use the same value of reference or because of a better temperature coefficient specifications. The internal reference can be disabled via Control Register A and the external reference applied at the REFCAP pin (See Figure <REFCAP_Ext>). External references should be of a suitable value such that the voltage swing of the inputs or outputs is not effected by being too close to the power supply rails.
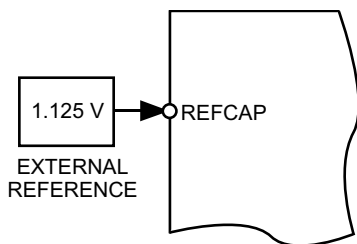

Figure <REFCAP_Ext.eps>

Master Clocking Scheme

The update rate of the AD74122's ADC and DAC channels require an internal master clock (IMCLK) which is 256 times that sample update rate (IMCLK = 256 * F_S). In order to provide some flexibility in selecting sample rates, the device has a series of three master clock pre-scalers which are programmable and allow the user to choose a range of convenient sample rates from a single external master clock. The master clock signal to the AD74122 is applied at the MCLK pin. The MCLK signal is passed through a series of three programmable MCLK pre-scalers (divider) circuits which can be selected to reduce the resulting Internal MCLK (IMCLK) frequency if required. The first and second MCLK pre-scalers provides divider ratios of /1 (pass through), /2, /3 while the third pre-scaler provides divider ratios of /1 (pass through), /2, /4.
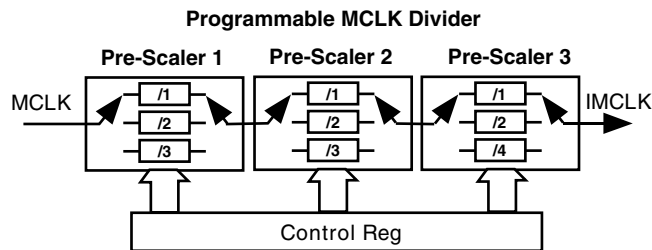
Programmable MCLK Divider

Figure <MCLK_Divider>

The divider ratios will allow more convenient sample rate selection from a common MCLK which may be required in many voice related applications. Control Register B should be programmed to achieve the desired divider ratios.

Selecting Sample Rates

The sample rate at which the convertor runs is always 256 times the IMCLK rate. IMCLK is the Internal Master Clock and is the output from the Master Clock Prescaler. The default sample rate is 48kHz (based on an external MCLK of 12.288MHz). In this mode the ADC modulator is clocked at 3.072MHz and the DAC modulator is clocked at 6.144MHz.. Sample rates which are lower than 256 X MCLK can be acheived by using the MCLK prescaler.

Example 1: f_{SAMP} = 48 kHz and 8 kHz required

MCLK = $48 \times 10^3 \times 256$ = 12.288 MHz to cater for 48 kHz f_{SAMP}

For f_{SAMP} = 8 kHz, it is necessary to use the /3 setting in Pre-Scaler 1, the /2 setting in Pre-Scaler 2 and pass through in Pre-Scaler 3. This results in an IMCLK = $8 \times 10^3 \times 256$ = 2.048 MHz (= 12.288 MHz/6).

Example 2: fSAMP = 44.1 kHz and 11.025 kHz required

MCLK = $44.1 \times 10^3 \times 256$ = 11.2896 MHz to cater for 44.1 kHz f_{SAMP}

For f_{SAMP} = 11.025 kHz, it is necessary to use the /1 setting in Pre-Scaler 1 and the /4 setting in Pre-Scaler 2 and pass through in Pre-Scaler 3. This results in an IMCLK = $11.025 \times 10^3 \times 256$ = 2.8224 MHz (= 11.2896 MHz/4).

Reseting the AD74122

The AD74122 can be reset by bringing the RESET pin low. Following a reset the internal circuitry of the AD74122 ensures that the internal registers are reset to their default settings and the on-chip RAM is purged of previous data samples. The DIN pin is sampled to determine if the AD74122 is required to operate in Master or Slave mode. The reset process takes 3072 MCLK periods and the user should not attempt to program the AD74122 during this time.

AD74122

Power Supplies and Grounds

The AD74122 features three separate supplies: AVDD, DVDD1 and DVDD2.

AVDD is the supply to the analog section of the device and must therefore be of sufficient quality to preserve the AD74122's performance characteristics. It is nominally a 2.5 V supply.

DVDD1 is the supply for the digital interface section of the device. It is fed from the digital supply voltage of the DSP or controller to which the device is interfaced and allows the AD74122 to interface with devices operating at supplies of between 2.5 V -5% to 3.3 V + 10%.

DVDD2 is the supply for the digital core of the AD74122. It is nominally a 2.5 V supply.

Accessing the Internal Registers

The AD74122 has 10 registers which can be programmed to control the functions of the AD74122. Each register is 10 bits wide and is written to or read from using a 16 bit write or read operation with the exception of Control Registers F and I which are read-only. Table <CWordDescription> shows the format of the data transfer operation. The Control Word is made up of a Read/Write bit, the register address and the data to be written to the device. Note that in a read operation the data field is ignored by the device. Access to the control registers is via the serial port through one of the operating modes described below.

Serial Port

The AD74122 contains a flexible serial interface port which is used to program and read the control registers of the codec and to send and receive DAC and ADC audio data. The serial port is compatible with many popular DSPs and can be programmed to operate in a variety of modes depending on which one best suits the DSP being used. The serial port can be set to operate as a Master or Slave device which is discussed below. Figure <SportTiming.eps> shows a timing diagram of the serial port.

Serial Port Operating Modes

The serial port of the codec can be programmed to operate in a variety of modes depending on the requirements and flexibility of the DSP to which it is connected. The two principal modes or operation are Mixed Mode and Data Mode.

Mixed Mode

Mixed Mode allows for the control registers of the codec to be programmed and read back. It also allows data to be sent to the DACs and data to be read from the ADCs. In Mixed Mode there are seperate data slots each with its own frame syncronisation signal (DFS) for Control, Left Channel and Right Channel information. The Codec powers up in Mixed Mode by default to allow the control registers to be programmed. Figure <DSP16MM16.eps> shows the default setting for Mixed Mode.

Data Mode

Data Mode can be used when programming or reading the control registers is no longer required. Data Mode will provide a frame synchronisation (DFS) pulse for each channel of data. Once the part has been programmed into Data Mode the only way to change the control registers is to perform a hardware reset to put the codec back into Mixed Mode. Figure <DSP16DM16.eps> shows the default setting for Data Mode.

Data Word Length

The AD74122 can be programmed to send ADC audio data and receive DAC audio data in different word length formats of 16, 20 or 24 bits. The default mode is 16 bits but this can be changed by programming Control Register C for the appropriate word length.

Selecting Master or Slave Mode

The initial operating mode of the codec is determined by the state of the DIN pin during the first five MCLKs following a reset. If the DIN pin is high during this time Slave Mode is selected. In Slave Mode the DFS and DCLK pins are inputs and the control signals for these pins must be provided by the DSP or other controller. If the DIN pin is low immediately following a reset the codec will operate in Master Mode.

Master Mode Operation

In Master Mode the DFS and DCLK pins are outputs from the codec. This is the easiest mode to use the codec in as the correct timing relationship between sample rate, DCLK and DFS is controlled by the codec.

Slave Mode Operation

In Slave Mode the DFS and DCLK pins are inputs to the codec. Care need to be exercised when designing a system to operate the codec in this mode as the relationship between the sample rate, DCLK and DFS needs to be controlled by the DSP or other controller and must be compatible with the internal DAC/ADC engine of the codec. Figure <engine.eps> shows a block diagram of the DAC engine and the codecs serial port. The sample rate for the DAC engine is determined by the MCLK and MCLK prescalers. The DAC engine will read data from the DAC Left Data and DAC Right Data at this rate. It is therefore important that the serial port is updated at the rate as any error between the two will accumulate and eventually cause the DAC engine to resynchronise with the serial port which will cause erroneous values on the DAC output pins.

In most cases it is easy to keep a DSP in synchronisation with the codec if they are both run from the same clock or the DSP clock is a multiple of the codecs MCLK. In this case there will be a fixed relationship between the instruction cycle time of the DSP program and the codec so a timer could be used to accurately control the DAC updates. If a timer is not available the Multi-Frame-Sync (MFS) mode could be used to generate a DFS pulse every 16 or 32 DCLKs allowing the DSP to accurately control the number of DCLKs between updates using an Auto Buffering or DMA type technique. In all cases for Slave Mode operation there should be 128 DCLKs (Normal Mode) or 256 DCLKs (Fast Mode) between DAC updates.The ADC operates in a similar manner, however, if the DSP does not read an ADC result this will only appear as a missed sample and will not be audible.
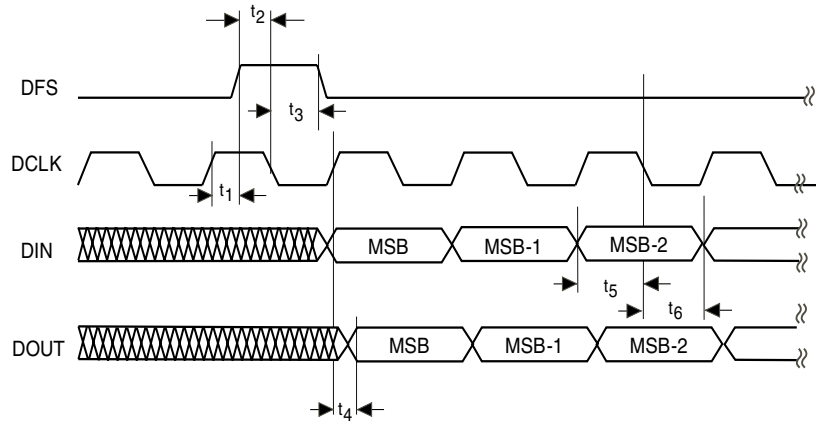
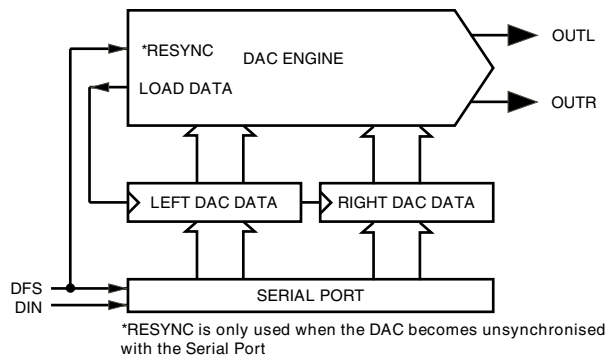*Figure <Sport Timing> Serial Port (SPORT) Timing*

Figure <engine.eps> DAC Engine

Table <Op Mode>Serial Mode Selection

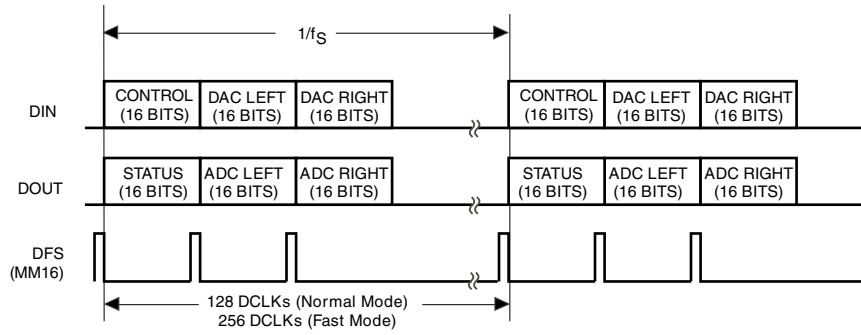| CRD:3 $\overline{\text{DM}}$/MM	CRD:2 DSP Mode	CRC:5,4 Word Width	Operating Mode	Figure
0	0	16	16 Bit Data Mode	Figure <dsp16dm16.eps>
0	1	16	32 Bit Data Mode	Figure <dsp32dm16.eps>
1	0	16	16 Bit Mixed Mode	Figure <dsp16mm16.eps>
1	1	16	32 Bit Mixed Mode	Figure <dsp32mm16.eps>
0	0	>16	16 Bit Data Mode	Figure <dsp16dm24.eps>
0	1	>16	32 Bit Data Mode	Figure <dsp32dm24.eps>
1	0	>16	16 Bit Mixed Mode	Figure <dsp16mm24.eps>
1	1	>16	32 Bit Mixed Mode	Figure <dsp32mm24.eps>

Figure <dsp16mm16.eps> 16 Bit Mixed Mode :Word Length = 16 Bits

Figure <dsp16mm24.eps>16 Bit Mixed Mode: Word Length = 24 Bits
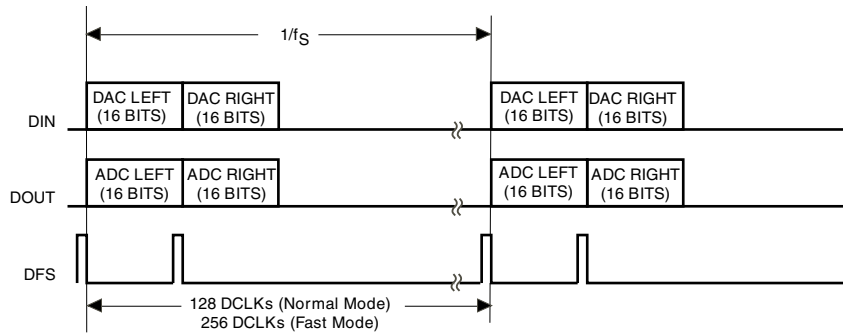
Figure <dsp16dm16.eps> 16 Bit Data Mode : Word Length = 16 Bits
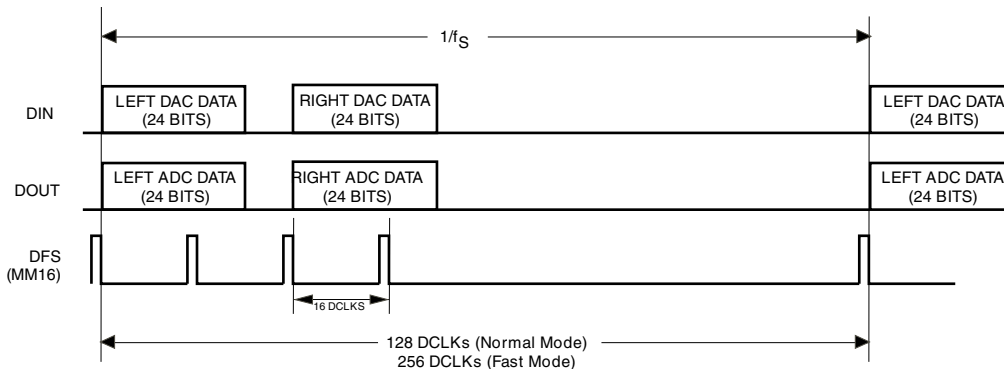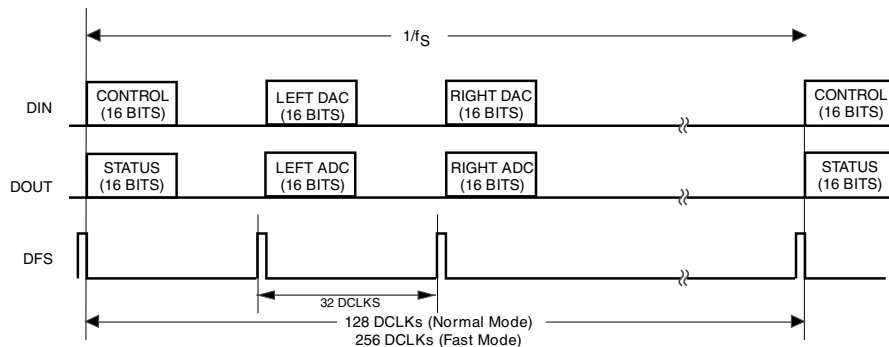
Figure <dsp16dm24.eps> 16 Bit Data Mode : Word Length = 24 Bits

Figure <dsp32mm16.eps> 32 Bit Mixed Mode : Word Length = 16 Bits
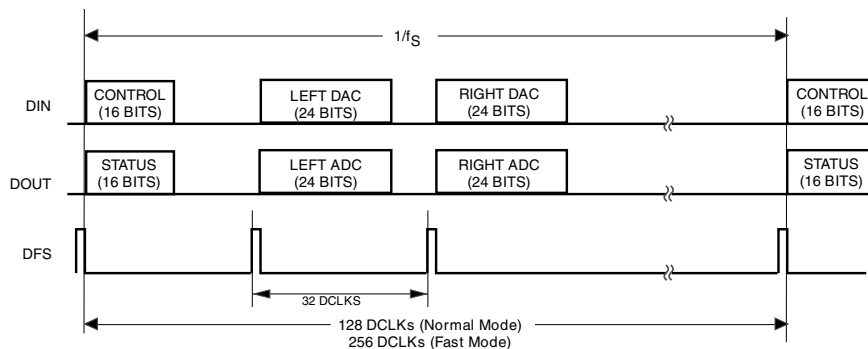
Figure <dsp32mm24.eps> 32 Bit Mixed Mode : Word Length = 24 Bits
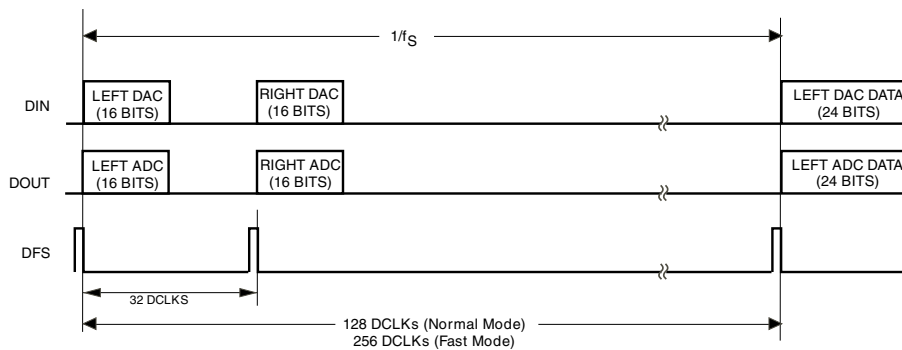
Figure <dsp32dm16.eps> 32 Bit Data Mode : Word Length = 16 Bits
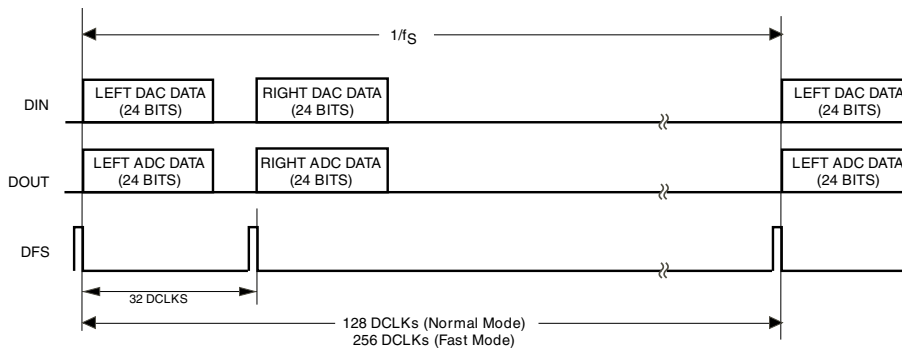
Figure <dsp32dm24.eps> 32 Bit Data Mode : Word Length = 24 Bits

AD74122
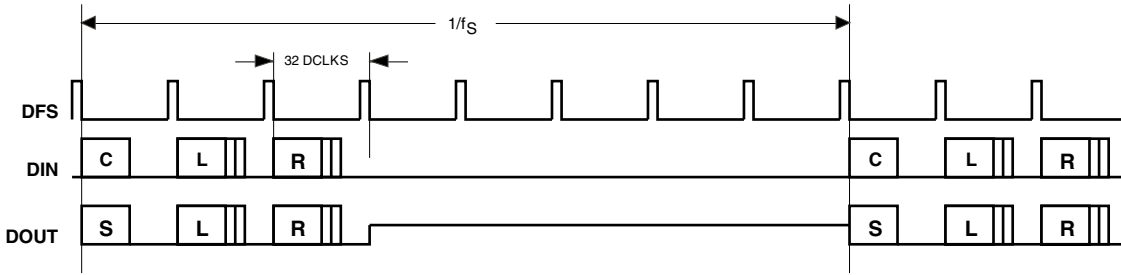
Figure <mfs32mm.eps>. Mutli Frame Sync 32 Bit Mixed Mode
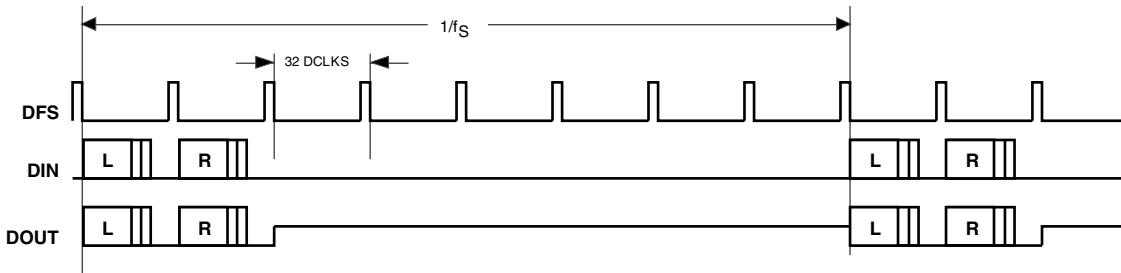
Figure <mfs32dm.eps>. Mutli Frame Sync 32 Bit Data Mode
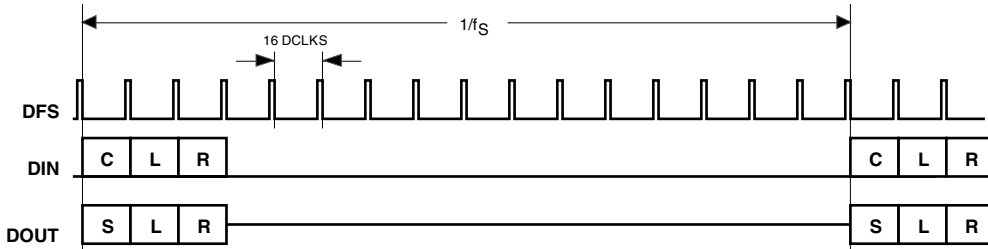
Figure <mfs16mm.eps> . Mutli Frame Sync 16 Bit Mixed Mode
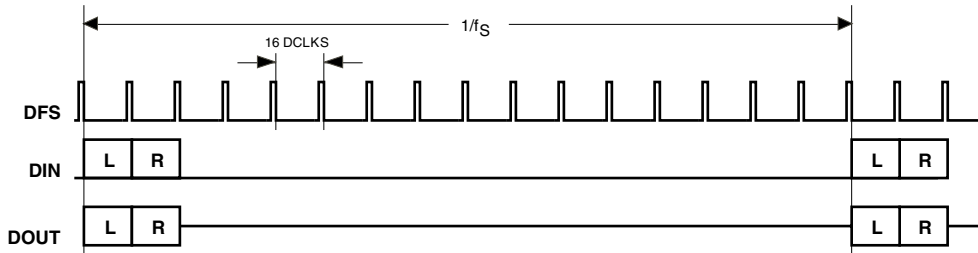
Figure <mfs16mm.eps> . Mutli Frame Sync 16 Bit Data Mode

Table <MFS Mode>Multi Frame Sync Selection

CRD:9 $\overline{\text{MFS}}$	CRD:3 DM/MM	CRC:2 DSP Mode	Operating Mode	Figure
1	0	0	16 Bit Data Mode	Figure <mfs16dm.eps>
1	0	1	32 Bit Data Mode	Figure <mfs32dm.eps>
1	1	0	16 Bit Mixed Mode	Figure <mfs16mm.eps>
1	1	1	32 Bit Mixed Mode	Figure <mfs32mm.eps>

Table <ContRegMap>. Control Register Map

Address(Binary)	Name	Description	Type	Width	Reset Setting
0 0 0 0	CRA	Control Register A	R/W	10	TBD
0 0 0 1	CRB	Control Register B	R/W	10	TBD
0 0 1 0	CRC	Control Register C	R/W	10	TBD
0 0 1 1	CRD	Control Register D	R/W	10	TBD
0 1 0 0	CRE	Control Register E	R/W	10	TBD
0 1 0 1	CRF	Control Register F	R	10	TBD
0 1 1 0	CRG	Control Register G	R/W	10	TBD
0 1 1 1	CRH	Control Register H	R/W	10	TBD
1 0 0 0	CRI	Control Register I	R	10	TBD
1 0 0 1	CRJ	Control Register J	R/W	10	TBD

Table <>Control Word Description

$\overline{R}$/W	Address	Res	Data Field
15	14,13,12,11	10	9, 8, 7, 6 , 5 ,4, 3, 2, 1, 0

Bit	Field	Description
15	$\overline{R}$/W	When this bit is high the contents of the data field will be written to the register specified by the Address Field. When this bit is low a read of the register specified by the Address Field will occur at the next sample interval. The contents of the Data Field are ignored.
14-11	Register Address	This 4-bit field is used to select one of the 12 Control Registers of the AD74122.
10	Reserved	This bit is reserved and should always be programmed with zero.
9-0	Data Field	This 10-bit field holds the data the is to be written to or read from the register specified in the Address Field.

Table <cra.eps>. Control Register A

$\overline{R}$/W	ADDRESS	RES	FUNCTION									
			ADCR Input Amplifier	ADCR	DACR	ADCL Input Amplifier	ADCL	DACL	Reference	Reference Amplifier	RESET	Reserved
15	14,13,12,11	10	9	8	7	6	5	4	3	2	1	0
1	0000	0	0=Off 1=On	0=Off 1=On	0=Off 1=On	0=Off 1=On	0=Off 1=On	0=Off 1=On	0=Off 1=On	0=Off 1=On	0=Default 1=Reset	0

Table <crb.eps>. Control Register B

$\overline{R}/W$	ADDRESS	RES	FUNCTION					
			ADC Modulator Clock	DAC Modulator Clock	Res	Third MCLK Divider	Second MCLK Divider	First MCLK Divider
15	14,13,12,11	10	9	8	7,6	5,4	3,2	1,0
1	0001	0	0=64 × f_s 1=32 × f_s	0=128 × f_s 1=64 × f_s	0	00=Divide by 1 01=Divide by 2 10=Divide by 4 11=Divide by 1	00=Divide by 1 01=Divide by 2 10=Divide by 3 11=Divide by 1	00=Divide by 1 01=Divide by 2 10=Divide by 3 11=Divide by 1

Table <crc.eps>. Control Register C

$\overline{R}/W$	ADDRESS	RES	Function				
			Reserved	DAC & ADC Word Width	Low Group Delay	DAC De-Emphasis	ADC High Pass Filter
15	14,13,12,11	10	9,8,7,6	5,4	3	2,1	0
1	0010	0	0	00=16 Bits 01=20 Bits 10=24 Bits 11=24 Bits	0=Disabled 1=Enabled	00=None 01=44.1kHz 10=32kHz 11=48kHz	0=Disabled 1=Enabled

Table <crd.eps>. Control Register D

$\overline{R}/W$	ADDRESS	RES	FUNCTION					
			Multi Frame Sync	Reserved	DM/MM	DSP Mode	Fast DCLK	Master/$\overline{Slave}$
15	14,13,12,11	10	9	8,7,6,5,4	3	2	1	0
1	0011	0	0 = Normal Mode 1= MFS Mode	0	0 = Data Mode 1 = Mixed Mode	0=16 Bits 1= 32 Bits	0=128 × f_s 1= 256 × f_s	0=Slave 1=Master

Table <cre.eps>. Control Register E

$\overline{R}/W$	ADDRESS	RES	FUNCTION				
			Reserved	ADCL Peak Enable	ADCL Gain	ADCL Mute	DACL Mute
15	14,13,12,11	10	9,8,7,6	5	4,3,2	1	0
1	0100	0	0	0=Disabled 1=Peak Enable	000=0dB 001=3dB 010=6dB 011=9dB 1XX=12dB	0=Normal 1=Mute	0=Normal 1=Mute

Table <crf.eps>. Control Register F

$\overline{R}$/W	ADDRESS	RES	FUNCTION	
			Reserved	ADCL Input Peak Level
15	14,13,12,11	10	9,8,7,6	5,4,3,2,1,0
0	0101	0	0	000000 = 0dBFS 000001 = –1dBFS 000010 = -2dBFS 111110 = -62dBFS 111111 = -63dBFS

Table <crg.eps>. Control Register G

$\overline{R}$/W	ADDRESS	RES	Function
			DACL Volume
15	14,13,12,11	10	9,8,7,6,5,4,3,2,1,0
0	0110	0	0000000000 = 0dBFS 0000000001 = (1023/1024)dBFS 0000000010 =(1022/1024)dBFS 1111111110 = (2/1024)dBFS 1111111111 = (1/1024)dBFS

Table <crh.eps>. Control Register H

$\overline{R}$/W	ADDRESS	RES	FUNCTION				
			Reserved	ADCR Peak Enable	ADCR Gain	ADCR Mute	DACR Mute
15	14,13,12,11	10	9,8,7,6	3	4,3,2	1	0
1	0111	0	0	0=Disabled 1=Peak Enable	000=0dB 001=3dB 010=6dB 011=9dB 1XX=12dB	0=Normal 1=Mute	0=Normal 1=Mute

Table <cri.eps>. Control Register I

$\overline{R}$/W	ADDRESS	RES	FUNCTION	
			Reserved	ADCR Input Peak Level
15	14,13,12,11	10	9,8,7,6	5,4,3,2,1,0
0	0101	0	0	000000 = 0dBFS 000001 = –1dBFS 000010 = -2dBFS 111110 = -62dBFS 111111 = -63dBFS

AD74122

Table <crj.eps>. Control Register J

$\overline{R}$/W	ADDRESS	RES	Function
			DACR Volume
15	14,13,12,11	10	9,8,7,6,5,4,3,2,1,0
1	1001	0	0000000000 = 0dBFS 0000000001 = (1023/1024)dBFS 0000000010 =(1022/1024)dBFS 1111111110 = (2/1024)dBFS 1111111111 = (1/1024)dBFS

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