# CS51312

# Synchronous CPU Buck Controller for 12 V Only Applications

The CS51312 is a synchronous dual NFET Buck Regulator Controller. It is designed to power the core logic of the latest high performance CPUs and ASICs from a single 12 V input. It uses the $V^{2}$™ control method to achieve the fastest possible transient response and best overall regulation. It incorporates many additional features required to ensure the proper operation and protection of the CPU and Power system. The CS51312 provides the industry's most highly integrated solution, minimizing external component count, total solution size, and cost.

The CS51312 is specifically designed to power Intel's Pentium® II processor and includes the following features: 5−bit DAC with 1.2% tolerance, Power−Good output, overcurrent hiccup mode protection, overvoltage protection, $V_{CC}$ monitor, Soft Start, adaptive voltage positioning, adaptive FET non−overlap time, and remote sense. The CS51312 will operate over a 9.0 V to 20 V ($V_{CC2}$) range using either single or dual input voltage and is available in 16 lead narrow body surface mount package.

### Features

- Synchronous Switching Regulator Controller for CPU $V_{CORE}$
- Dual N−Channel MOSFET Synchronous Buck Design
- $V^{2}$ Control Topology
- 200 ns Transient Loop Response
- 5−Bit DAC with 1.2% Tolerance
- Hiccup Mode Overcurrent Protection
- 40 ns Gate Rise and Fall Times (3.3 nF Load)
- 65 ns Adaptive FET Non−Overlap Time
- Adaptive Voltage Positioning
- Power Good Output Monitors Regulator Output
- 5.0 V/12 V or 12 V−Only Operation
- $V_{CC}$ Monitor Provides Undervoltage Lockout
- OVP Output Monitors Regulator Output
- Multifunctional COMP Pin Provides ENABLE, Soft Start, and Hiccup Timing in Addition to Control Loop Compensation



ON Semiconductor™

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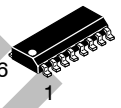
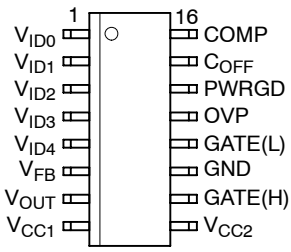



**SO−16**
**D SUFFIX**
**CASE 751B**

**MARKING DIAGRAM**


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

**PIN CONNECTIONS**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| CS51312GD16 | SO−16 | 48 Units/Rail |
| CS51312GDR16 | SO−16 | 2500 Tape & Reel |

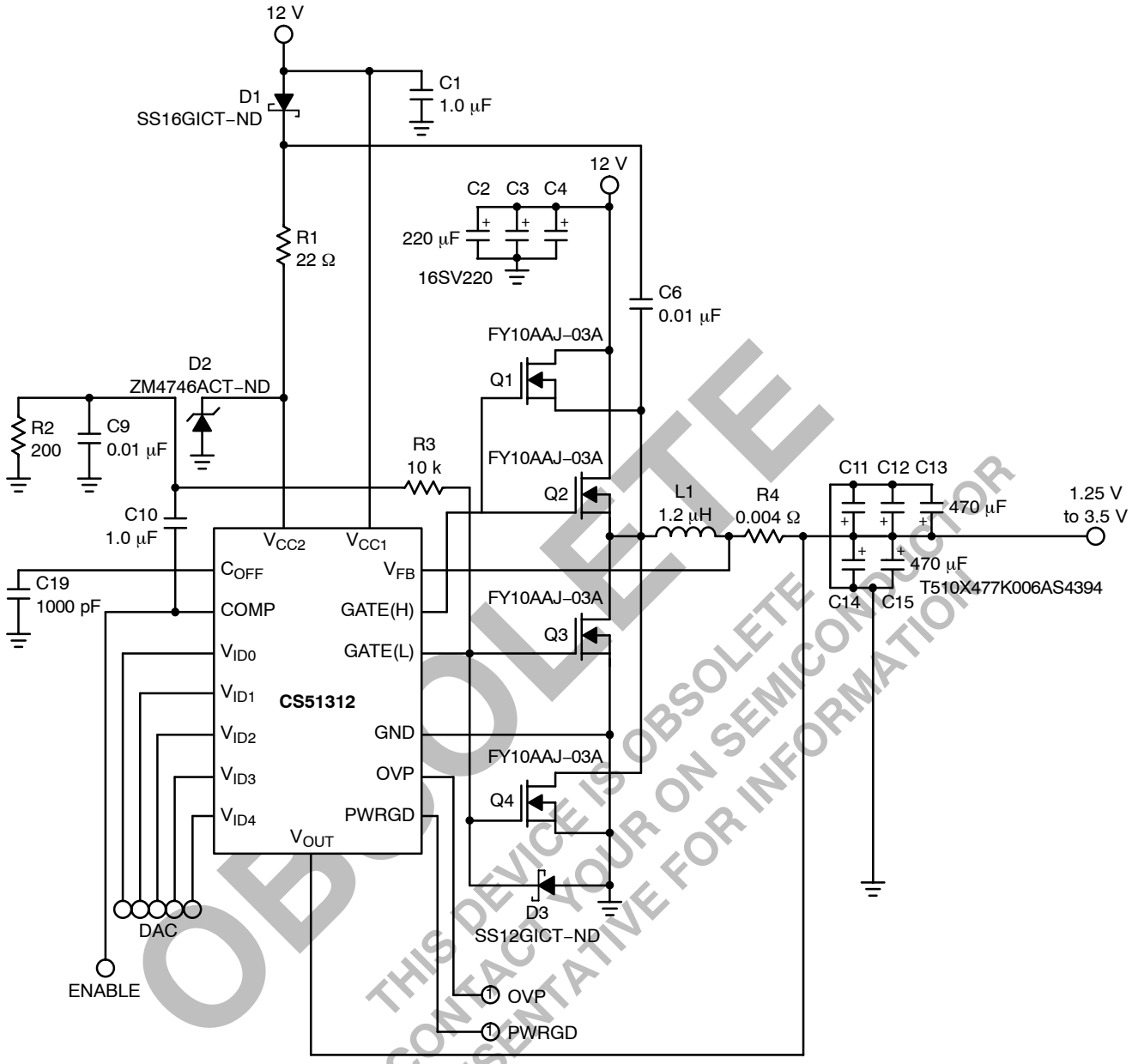



**Figure 1. Application Diagram, 12 V to 16 A High Performance Converter**

## ABSOLUTE MAXIMUM RATINGS*

| Rating | | Value | Unit |
|---|---|---|---|
| Operating Junction Temperature, $T_J$ | | 150 | °C |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak | °C |
| Storage Temperature Range, $T_S$ | | −65 to +150 | °C |
| ESD Susceptibility | | 2.0 | kV |

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

## ABSOLUTE MAXIMUM RATINGS

| Pin Name | Pin Symbol | $V_{MAX}$ | $V_{MIN}$ | $I_{SOURCE}$ | $I_{SINK}$ |
|---|---|---|---|---|---|
| IC Bias and Low Side Driver Power Input | $V_{CC1}$ | 16 | −0.3 | N/A | 1.5 A Peak, 200 mA DC |
| IC High Side Driver Power Input | $V_{CC2}$ | 20 V | −0.3 V | N/A | 1.5 A Peak, 200 mA DC |
| Compensation Pin | COMP | 6.0 V | −0.3 V | 1.0 mA | 5.0 mA |
| Voltage Feedback Input, Output Voltage Sense Pin, Voltage ID DAC Inputs | $V_{FB}$, $V_{OUT}$, $V_{ID0-4}$ | 6.0 V | −0.3 V | 1.0 mA | 1.0 mA |
| Off−Time Pin | $C_{OFF}$ | 6.0 V | −0.3 V | 1.0 mA | 50 mA |
| High−Side FET Driver | GATE(H) | 20 V | −0.3 V DC | 1.5 A Peak, 200 mA DC | 1.5 A Peak, 200 mA DC |
| Low−Side FET Driver | GATE(L) | 16 V | −0.3 V DC | 1.5 A Peak, 200 mA DC | 1.5 A Peak, 200 mA DC |
| Power Good Output | PWRGD | 6.0 V | −0.3 V | 1.0 mA | 30 mA |
| Overvoltage Protection | OVP | 15 V | −0.3 V | 30 mA | 1.0 mA |
| Ground | GND | 0 V | 0 V | 1.5 A Peak, 200 mA DC | N/A |

**ELECTRICAL CHARACTERISTICS** (0°C < $T_A$ < 70°C; 0°C < $T_J$ < 125°C; 9.0 V < $V_{CC1}$ < 14 V; 9.0 V ≤ $V_{CC2}$ ≤ 20 V; 2.0 V DAC Code ($V_{ID4}$ = $V_{ID3}$ = $V_{ID2}$ = $V_{ID1}$ = 0, $V_{ID0}$ = 1.0) $C_{GATE(H)}$ = $C_{GATE(L)}$ = 3.3 nF, $C_{OFF}$ = 390 pF; unless otherwise specified.)

| Characteristic | Test Conditions | |
|---|---|---|

**Voltage Identification DAC**

| | | | | | Measure $V_{FB}$ = $V_{COMP}$, $V_{CC}$ = 12 V. Note 2 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 75°C ≤ $T_J$ ≤ 125°C | | | | 25°C ≤ $T_J$ ≤ 75°C | | | | |
| $V_{ID4}$ | $V_{ID3}$ | $V_{ID2}$ | $V_{ID1}$ | $V_{ID0}$ | Min | Typ | Max | ±Tol | Min | Typ | Max | ±Tol | Unit |
| 1 | 0 | 0 | 0 | 0 | 3.483 | 3.525 | 3.567 | 1.2% | 3.455 | 3.525 | 3.596 | 2.0% | V |
| 1 | 0 | 0 | 0 | 1 | 3.384 | 3.425 | 3.466 | 1.2% | 3.357 | 3.425 | 3.494 | 2.0% | V |
| 1 | 0 | 0 | 1 | 0 | 3.285 | 3.325 | 3.365 | 1.2% | 3.259 | 3.325 | 3.392 | 2.0% | V |
| 1 | 0 | 0 | 1 | 1 | 3.186 | 3.225 | 3.264 | 1.2% | 3.161 | 3.225 | 3.290 | 2.0% | V |
| 1 | 0 | 1 | 0 | 0 | 3.087 | 3.125 | 3.163 | 1.2% | 3.063 | 3.125 | 3.188 | 2.0% | V |
| 1 | 0 | 1 | 0 | 1 | 2.989 | 3.025 | 3.061 | 1.2% | 2.965 | 3.025 | 3.086 | 2.0% | V |
| 1 | 0 | 1 | 1 | 0 | 2.890 | 2.925 | 2.960 | 1.2% | 2.875 | 2.925 | 2.975 | 1.7% | V |
| 1 | 0 | 1 | 1 | 1 | 2.791 | 2.825 | 2.859 | 1.2% | 2.777 | 2.825 | 2.873 | 1.7% | V |
| 1 | 1 | 0 | 0 | 0 | 2.692 | 2.725 | 2.758 | 1.2% | 2.679 | 2.725 | 2.771 | 1.7% | V |
| 1 | 1 | 0 | 0 | 1 | 2.594 | 2.625 | 2.657 | 1.2% | 2.580 | 2.625 | 2.670 | 1.7% | V |
| 1 | 1 | 0 | 1 | 0 | 2.495 | 2.525 | 2.555 | 1.2% | 2.482 | 2.525 | 2.568 | 1.7% | V |
| 1 | 1 | 0 | 1 | 1 | 2.396 | 2.425 | 2.454 | 1.2% | 2.389 | 2.425 | 2.461 | 1.5% | V |
| 1 | 1 | 1 | 0 | 0 | 2.297 | 2.325 | 2.353 | 1.2% | 2.290 | 2.325 | 2.360 | 1.5% | V |
| 1 | 1 | 1 | 0 | 1 | 2.198 | 2.225 | 2.252 | 1.2% | 2.192 | 2.225 | 2.258 | 1.5% | V |
| 1 | 1 | 1 | 1 | 0 | 2.099 | 2.125 | 2.151 | 1.2% | 2.093 | 2.125 | 2.157 | 1.5% | V |
| 0 | 0 | 0 | 0 | 0 | 2.050 | 2.075 | 2.100 | 1.2% | 2.044 | 2.075 | 2.106 | 1.5% | V |
| 0 | 0 | 0 | 0 | 1 | 2.001 | 2.025 | 2.049 | 1.2% | 1.995 | 2.025 | 2.055 | 1.5% | V |
| 0 | 0 | 0 | 1 | 0 | 1.953 | 1.975 | 1.997 | 1.1% | 1.945 | 1.975 | 2.005 | 1.5% | V |
| 0 | 0 | 0 | 1 | 1 | 1.904 | 1.925 | 1.946 | 1.1% | 1.896 | 1.925 | 1.954 | 1.5% | V |
| 0 | 0 | 1 | 0 | 0 | 1.854 | 1.875 | 1.896 | 1.1% | 1.847 | 1.875 | 1.903 | 1.5% | V |
| 0 | 0 | 1 | 0 | 1 | 1.805 | 1.825 | 1.845 | 1.1% | 1.798 | 1.825 | 1.852 | 1.5% | V |
| 0 | 0 | 1 | 1 | 0 | 1.755 | 1.775 | 1.795 | 1.1% | 1.748 | 1.775 | 1.802 | 1.5% | V |
| 0 | 0 | 1 | 1 | 1 | 1.706 | 1.725 | 1.744 | 1.1% | 1.699 | 1.725 | 1.751 | 1.5% | V |
| 0 | 1 | 0 | 0 | 0 | 1.656 | 1.675 | 1.694 | 1.1% | 1.650 | 1.675 | 1.700 | 1.5% | V |
| 0 | 1 | 0 | 0 | 1 | 1.607 | 1.625 | 1.643 | 1.1% | 1.601 | 1.625 | 1.649 | 1.5% | V |
| 0 | 1 | 0 | 1 | 0 | 1.558 | 1.575 | 1.593 | 1.1% | 1.551 | 1.575 | 1.599 | 1.5% | V |
| 0 | 1 | 0 | 1 | 1 | 1.508 | 1.525 | 1.542 | 1.1% | 1.502 | 1.525 | 1.548 | 1.5% | V |
| 0 | 1 | 1 | 0 | 0 | 1.459 | 1.475 | 1.491 | 1.1% | 1.453 | 1.475 | 1.497 | 1.5% | V |
| 0 | 1 | 1 | 0 | 1 | 1.409 | 1.425 | 1.441 | 1.1% | 1.404 | 1.425 | 1.446 | 1.5% | V |
| 0 | 1 | 1 | 1 | 0 | 1.360 | 1.375 | 1.390 | 1.1% | 1.354 | 1.375 | 1.396 | 1.5% | V |
| 0 | 1 | 1 | 1 | 1 | 1.310 | 1.325 | 1.340 | 1.1% | 1.305 | 1.325 | 1.345 | 1.5% | V |
| 1 | 1 | 1 | 1 | 1 | 1.225 | 1.250 | 1.275 | 2.0% | 1.225 | 1.250 | 1.275 | 2.0% | V |

2. The IC power dissipation in a typical application with $V_{CC}$ = 12 V, switching frequency $f_{SW}$ = 250 kHz, 50 nc MOSFETs and $R_{\theta JA}$ = 115°C/W yields an operating junction temperature rise of approximately 52°C, and a junction temperature of 77°C with an ambient temperature of 25°C.

**ELECTRICAL CHARACTERISTICS (continued)** ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $9.0\ V < V_{CC1} < 14\ V$; $9.0\ V \le V_{CC2} \le 20\ V$; 2.0 V DAC Code ($V_{ID4} = V_{ID3} = V_{ID2} = V_{ID1} = 0$, $V_{ID0} = 1.0$) $C_{GATE(H)} = C_{GATE(L)} = 3.3$ nF, $C_{OFF} = 390$ pF; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Voltage Identification DAC (continued)** | | | | | |
| Line Regulation | $9.0\ V \le V_{CC} \le 14\ V$ | – | 0.01 | – | %/V |
| Input Threshold | $V_{ID4}$, $V_{ID3}$, $V_{ID2}$, $V_{ID1}$, $V_{ID0}$ | 1.0 | 1.25 | 2.4 | V |
| Input Pull−Up Resistance | $V_{ID4}$, $V_{ID3}$, $V_{ID2}$, $V_{ID1}$, $V_{ID0}$ | 25 | 50 | 100 | kΩ |
| Pull−Up Voltage | – | 5.48 | 5.65 | 5.82 | V |
| **Error Amplifier** | | | | | |
| $V_{FB}$ Bias Current | $0.2\ V \le V_{FB} \le 3.5\ V$ | −7.0 | 0.1 | 7.0 | μA |
| COMP Source Current | $V_{COMP}$ = 1.2 V to 3.6 V, $V_{FB}$ = 1.9 V | 15 | 30 | 60 | μA |
| COMP Sink Current | $V_{COMP}$ = 1.2 V, $V_{FB}$ = 2.1 V | 30 | 60 | 120 | μA |
| Open Loop Gain | $C_{COMP}$ = 0.1 μF | – | 80 | – | dB |
| Unity Gain Bandwidth | $C_{COMP}$ = 0.1 μF | – | 50 | – | kHz |
| PSRR @ 1.0 kHz | $C_{COMP}$ = 0.1 μF | – | 70 | – | dB |
| Transconductance | – | – | 32 | – | mmho |
| Output Impedance | – | – | 0.5 | – | MΩ |
| **GATE(H) and GATE(L)** | | | | | |
| High Voltage at 100 mA | Measure $V_{CC1/2}$ − GATE(L)/(H) | – | 1.2 | 2.1 | V |
| Low Voltage at 100 mA | Measure GATE(L)/(H) | – | 1.0 | 1.5 | V |
| Rise Time | 1.6 V < GATE(H)/(L) < ($V_{CC1/2}$ − 2.5 V) | – | 40 | 80 | ns |
| Fall Time | ($V_{CC1/2}$ − 2.5 V) > GATE(L)/(H) > 1.6 V | – | 40 | 80 | ns |
| GATE(H) to GATE(L) Delay | GATE(H) < 2.0 V, GATE(L) > 2.0 V, $V_{CC1/2}$ = 12 V | 30 | 65 | 110 | ns |
| GATE(L) to GATE(H) Delay | GATE(L) < 2.0 V, GATE(H) > 2.0 V, $V_{CC1/2}$ = 12 V | 30 | 65 | 110 | ns |
| GATE Pull−Down | Resistance to GND. Note 3 | 20 | 50 | 115 | kΩ |
| **Overcurrent Protection** | | | | | |
| OVC Comparator Offset Voltage | $0\ V \le V_{OUT} \le 3.5\ V$ | 77 | 86 | 101 | mV |
| Discharge Threshold Voltage | – | 0.2 | 0.25 | 0.3 | V |
| $V_{OUT}$ Bias Current | $0.2\ V \le V_{OUT} \le 3.5\ V$ | −7.0 | 0.1 | 7.0 | μA |
| OVC Latch Discharge Current | $V_{COMP}$ = 1.0 V | 100 | 800 | 2500 | μA |
| **PWM Comparator** | | | | | |
| PWM Comparator Offset Voltage | $0\ V \le V_{FB} \le 3.5\ V$ | 0.99 | 1.1 | 1.23 | V |
| Transient Response | $V_{FB}$ = 0 to 3.5 V | – | 200 | 300 | ns |
| **$C_{OFF}$** | | | | | |
| Off−Time | – | 1.0 | 1.6 | 2.3 | μs |
| Charge Current | $V_{COFF}$ = 1.5 V | – | 550 | – | μA |
| Discharge Current | $V_{COFF}$ = 1.5 V | – | 25 | – | mA |

3. Guaranteed by design, not 100% tested in production.

**ELECTRICAL CHARACTERISTICS (continued)** (0°C < $T_A$ < 70°C; 0°C < $T_J$ < 125°C; 9.0 V < $V_{CC1}$ < 14 V; 9.0 V ≤ $V_{CC2}$ ≤ 20 V; 2.0 V DAC Code ($V_{ID4}$ = $V_{ID3}$ = $V_{ID2}$ = $V_{ID1}$ = 0, $V_{ID0}$ = 1.0) $C_{GATE(H)}$ = $C_{GATE(L)}$ = 3.3 nF, $C_{OFF}$ = 390 pF; unless otherwise specified.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Power Good Output** | | | | | |
| PWRGD Sink Current | $V_{FB}$ = 1.7 V, $V_{PWRGD}$ = 1.0 V | 0.5 | 4.0 | 15 | mA |
| PWRGD Upper Threshold | % of Nominal DAC Code | 5.0 | 8.5 | 12 | % |
| PWRGD Lower Threshold | % of Nominal DAC Code | −12 | −8.5 | −5.0 | % |
| PWRGD Output Low Voltage | $V_{FB}$ = 1.7 V, $I_{PWRGD}$ = 500 μA | – | 0.2 | 0.3 | V |
| **Overvoltage Protection (OVP) Output** | | | | | |
| OVP Source Current | OVP = 1.0 V | 1.0 | 10 | 25 | mA |
| OVP Threshold | % of Nominal DAC Code | 5.0 | 8.5 | 12 | % |
| OVP Pull−Up Voltage | $I_{OVP}$ = 1.0 mA, $V_{CC1}$ − $V_{OVP}$ | – | 1.1 | 1.5 | V |
| **General Electrical Specifications** | | | | | |
| $V_{CC1}$ Monitor Start Threshold | – | 7.9 | 8.4 | 8.9 | V |
| $V_{CC1}$ Monitor Stop Threshold | – | 7.6 | 8.1 | 8.6 | V |
| Hysteresis | Start−Stop | 0.15 | 0.3 | 0.6 | V |
| $V_{CC1}$ Supply Current | No Load on GATE(H), GATE(L) | – | 9.5 | 16 | mA |
| $V_{CC2}$ Supply Current | No Load on GATE(H), GATE(L) | – | 2.5 | 4.5 | mA |



## PACKAGE PIN DESCRIPTION

| PACKAGE PIN # SO−16 | PIN SYMBOL | FUNCTION |
|---|---|---|
| 1, 2, 3, 4, 5 | $V_{ID0}$−$V_{ID4}$ | Voltage ID DAC inputs. These pins are internally pulled up to 5.65 V if left open. $V_{ID4}$ selects the DAC range. When $V_{ID4}$ is high (logic one), the Error Amp reference range is 2.125 V to 3.525 V with 100 mV increments. When $V_{ID4}$ is low (logic zero), the Error Amp reference voltage is 1.325 V to 2.075 V with 50 mV increments. |
| 6 | $V_{FB}$ | Error amp inverting input, PWM comparator non−inverting input, current limit comparator non−inverting input, PWRGD and OVP comparator input. |
| 7 | $V_{OUT}$ | Current limit comparator inverting input. |
| 8 | $V_{CC1}$ | Input power supply pin for the internal circuitry and low side gate driver. Decouple with filter capacitor to GND. |
| 9 | $V_{CC2}$ | Input power supply pin for the high side gate driver. Decouple with filter capacitor to GND. |
| 10 | GATE(H) | High side switch FET driver pin. |
| 11 | GND | Ground pin and IC substrate connection. |
| 12 | GATE(L) | Low side synchronous FET driver pin. |
| 13 | OVP | Overvoltage protection pin. Drives high when overvoltage condition is detected on $V_{FB}$. |
| 14 | PWRGD | Power Good Output. Open collector output drives low when $V_{FB}$ is out of regulation. |
| 15 | $C_{OFF}$ | Off−Time Capacitor pin. A capacitor from this pin to GND sets the off time for the regulator. |
| 16 | COMP | Error amp output. PWM comparator inverting input. A capacitor on this pin provides error amp compensation, and determines the Soft Start and hiccup timing. Pulling COMP below 1.1 V (typ) turns off both GATE drivers and shuts down the regulator. |

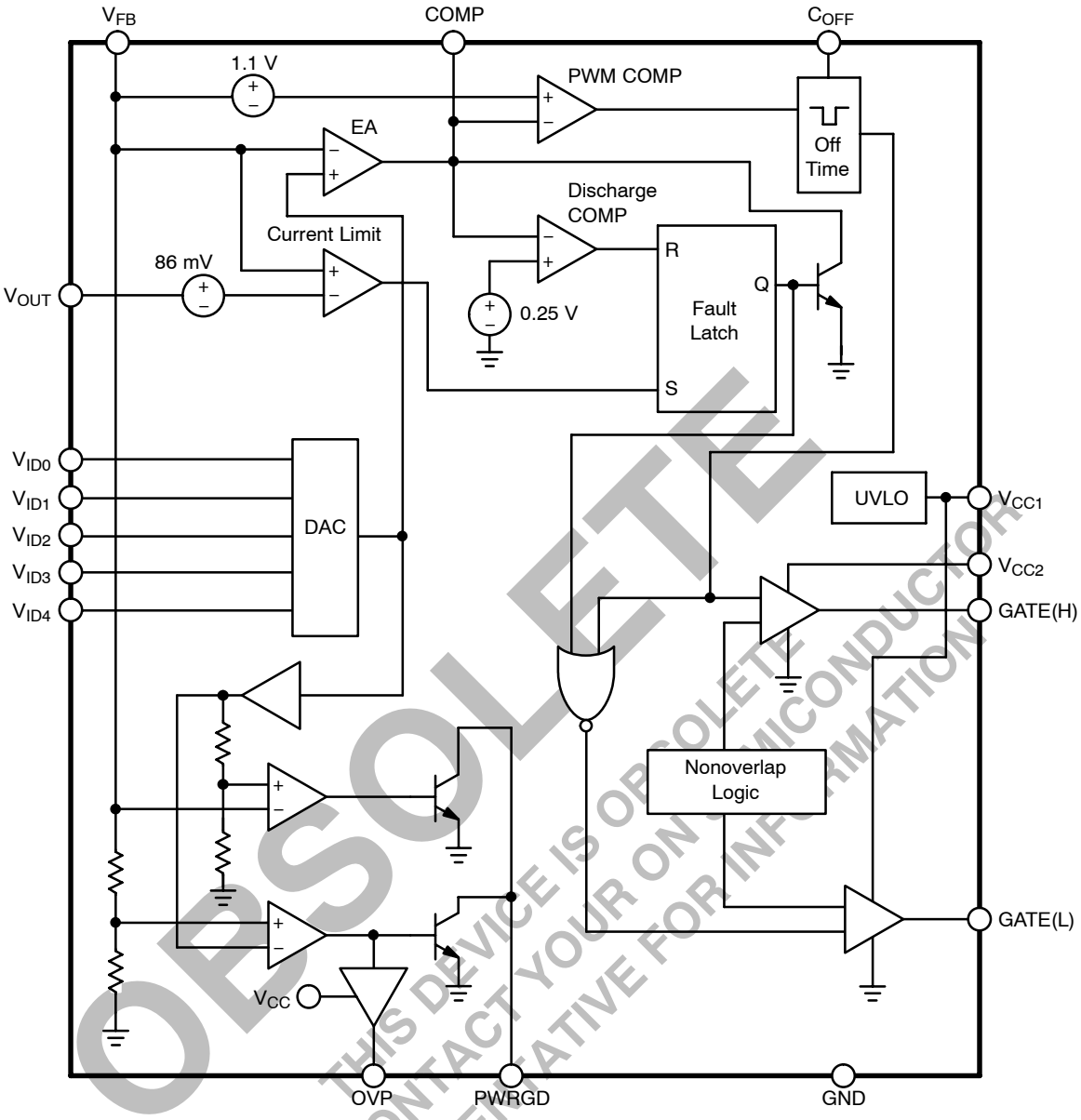



**Figure 2. Block Diagram**

## TYPICAL PERFORMANCE CHARACTERISTICS

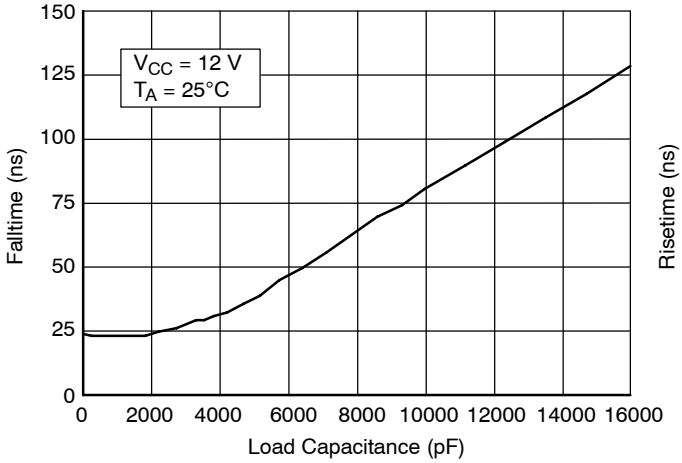



**Figure 3. GATE(H) and GATE(L) Falltime vs. Load Capacitance**

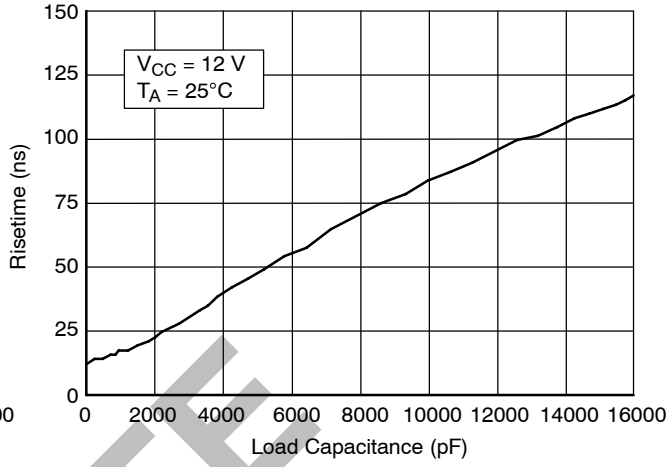



**Figure 4. GATE(H) and GATE(L) Risetime vs. Load Capacitance**

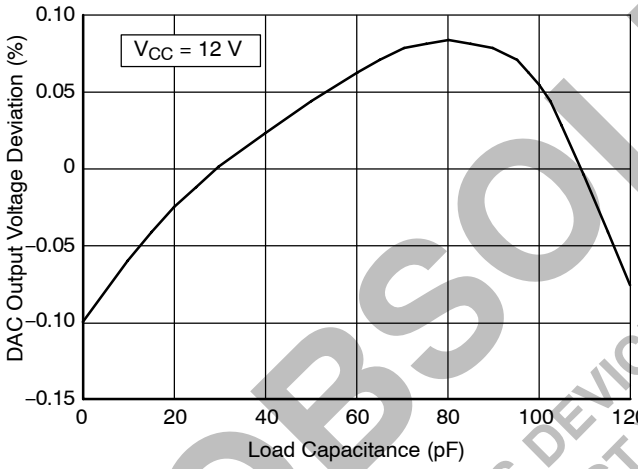



**Figure 5. DAC Output Voltage vs. Temperature, DAC Code = 00001**

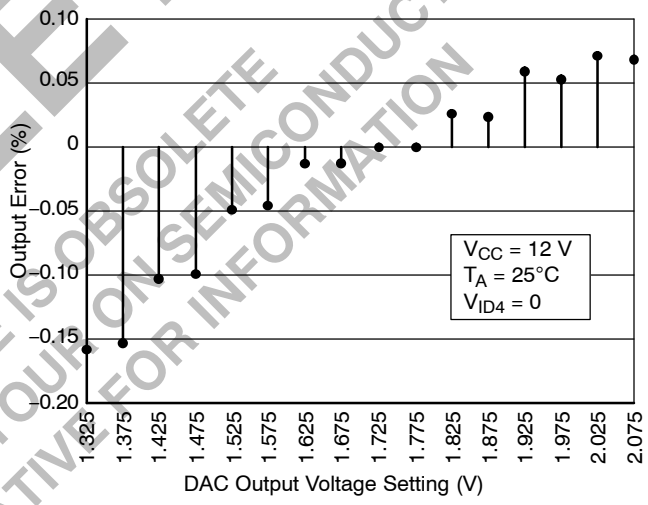



**Figure 6. Percent Output Error vs. DAC Output Voltage Setting, $V_{ID4}$ = 0**

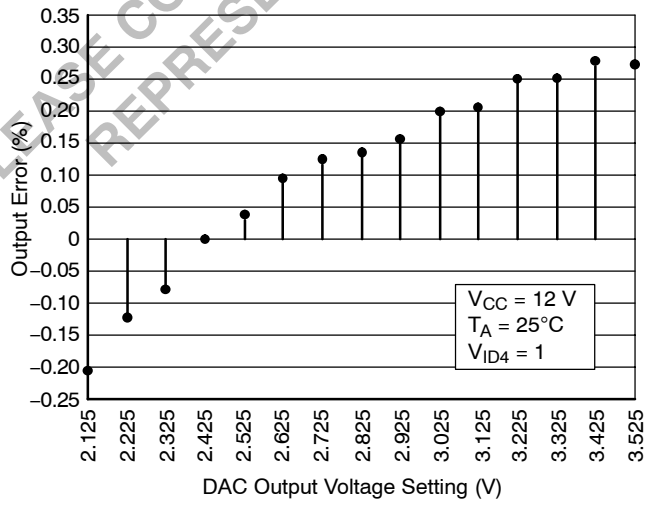



**Figure 7. Percent Output Error vs. DAC Output Voltage Setting, $V_{ID4}$ = 1**

## APPLICATIONS INFORMATION

### THEORY OF OPERATION

#### V² Control Method

The $V^2$ method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.

The $V^2$ control method is illustrated in Figure 8. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to 0% or 100% duty cycle as required.

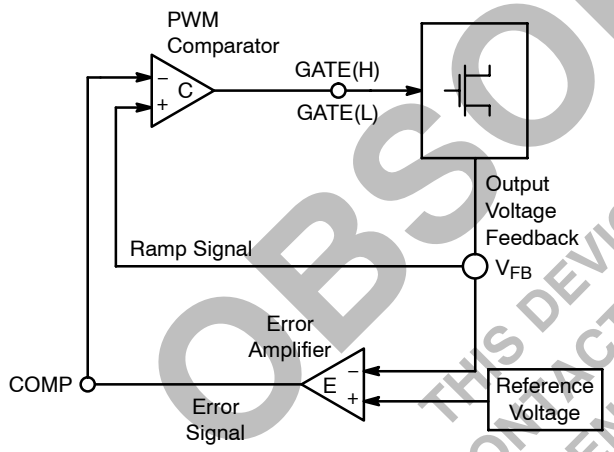



**Figure 8. $V^2$ Control Diagram**

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the $V^2$ control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the $V^2$ control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this 'slow' feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation.

A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The $V^2$ method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

#### Constant Off−Time

To minimize transient response, the CS51312 uses a Constant Off−Time method to control the rate of output pulses. During normal operation, the Off−Time of the high side switch is terminated after a fixed period, set by the $C_{OFF}$ capacitor. Every time the $V_{FB}$ pin exceeds the COMP pin voltage an Off−Time is initiated. To maintain regulation, the $V^2$ Control Loop varies switch On−Time. The PWM comparator monitors the output voltage ramp, and terminates the switch On−Time.

Constant Off−Time provides a number of advantages. Switch Duty Cycle can be adjusted from 0 to 100% on a pulse−by pulse basis when responding to transient conditions. Both 0% and 100% Duty Cycle operation can be maintained for extended periods of time in response to Load or Line transients.

#### Programmable Output

The CS51312 is designed to provide two methods for programming the output voltage of the power supply. A five bit on board digital to analog converter (DAC) is used to program the output voltage within two different ranges. The first range is 2.125 V to 3.525 V in 100 mV steps, the second is 1.325 V to 2.075 V in 50 mV steps, depending on the digital input code. If all five bits are left open, the CS51312 enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the $V_{FB}$ pin, as in traditional controllers. The CS51312 is specifically designed to meet or exceed Intel's Pentium II specifications.

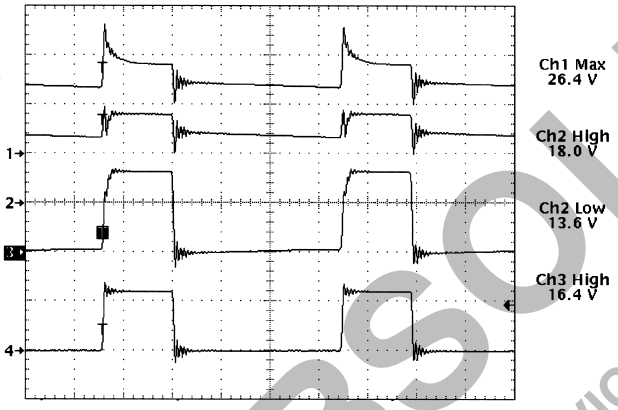
#### Error Amplifier

The COMP pin is the output of the error amplifier. A capacitor to GND compensates the error amplifier loop. Additionally, the built in offset on the PWM Comparator

non−inverting input provides the hiccup timing for the Overcurrent Protection, Soft Start function, and regulator output enable.

### $V_{CC2}$ Charge Pump

In order to fully turn on the high side NFET, a voltage greater than the input voltage must be applied to $V_{CC2}$ to bias the GATE(H) driver. Referring to the application diagram on page 2; a simple charge pump circuit can be implemented for this purpose through capacitor C6, resistor R1, and diodes D1 and D2. The input voltage, less the drop in D1 is stored in C6 during the off−time period. When the high−side FET turns on, it drives the inductor switching node and C6 high causing Schottky diode D1 to reverse bias. The charge stored in C6 is transferred to $V_{CC2}$ through R1. Zener diode D2 clamps the $V_{CC2}$ voltage to 18 V to prevent the $V_{CC2}$ from exceeding its 20 V Max rating (see Figure 9).




Channel 1 – Charge Pump Switching Node (10 V/div)
Channel 2 – $V_{CC2}$ (10 V/div)
Channel 3 – GATE(H) (10 V/div)
Channel 4 – Inductor Switching Node (10 V/div)

**Figure 9. $V_{CC2}$ Charge Pump Operation (1.0 μs/div)**

### Startup

The CS51312 provides a controlled startup of regulator output voltage and features Programmable Soft Start implemented through the Error Amp and external Compensation Capacitor. This feature, combined with overcurrent protection, prevents stress to the regulator power components and overshoot of the output voltage during startup.

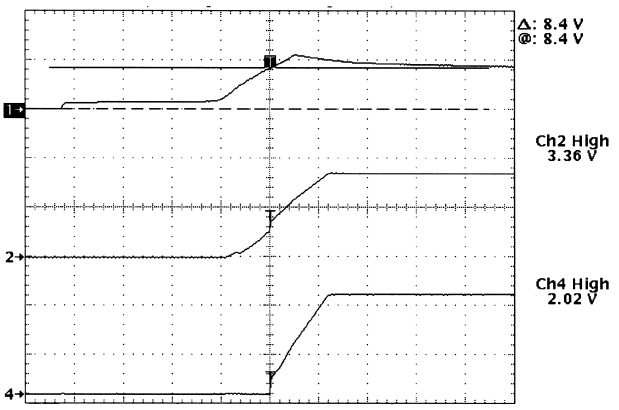
As Power is applied to the regulator, the CS51312 Undervoltage Lockout circuit (UVL) monitors the ICs supply voltage ($V_{CC1}$) which is typically connected to the +12 V input. The UVL circuit prevents the NFET gates from being activated until $V_{CC1}$ exceeds the 8.4 V (typ) threshold. Hysteresis of 300 mV (typ) is provided for noise immunity. The Error Amp Capacitor connected to the COMP pin is charged by a 30 μA current source. This capacitor must be charged to 1.1 V (typ) so that it exceeds the PWM comparator's offset before the $V^2$ PWM control loop permits switching to occur.

When $V_{CC1}$ has exceeded 8.4 V and COMP has charged to 1.1 V, the upper Gate driver (GATE(H)) is activated, turning on the upper FET. This causes current to flow through the output inductor and into the output capacitors and load according to the following equation:

$$I = (V_{IN} - V_{OUT}) \times \frac{T}{L}$$

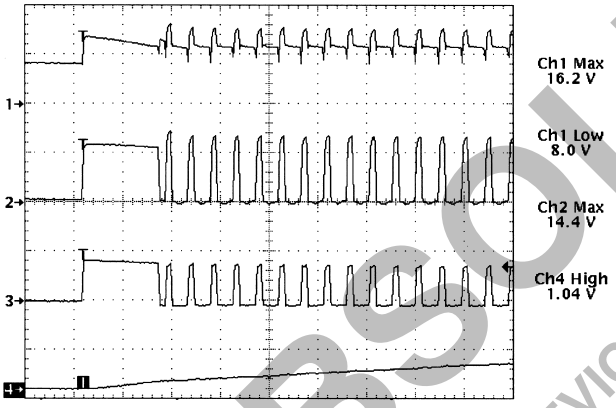
GATE(H) and the upper NFET remain on and inductor current ramps up until the initial pulse is terminated by either the PWM control loop or the overcurrent protection. This initial surge of in−rush current minimizes startup time, but avoids overstressing of the regulator's power components.

The PWM comparator will terminate the initial pulse if the regulator output exceeds the voltage on the COMP pin plus the 1.1 V PWM comparator offset prior to the drop across the current sense resistor exceeding the current limit threshold. In this case, the PWM control loop has achieved regulation and the initial pulse is then followed by a constant off time as programmed by the $C_{OFF}$ capacitor. The COMP capacitor will continue to slowly charge and the regulator output voltage will follow it, less the 1.1 V PWM offset, until it achieves the voltage programmed by the DAC's VID input. The Error Amp will then source or sink current to the COMP cap as required to maintain the correct regulator DC output voltage. Since the rate of increase of the COMP pin voltage is typically set much slower than the regulator's slew capability, inrush current, output voltage, and duty cycle all gradually increase from zero. (See Figures 10 and 11).




Channel 1 – Regulator Input Voltage and $V_{CC1}$ (10 V/div)
Channel 2 – COMP (2.0 V/div)
Channel 3 – Regulator Output Voltage (1.0 V/div)

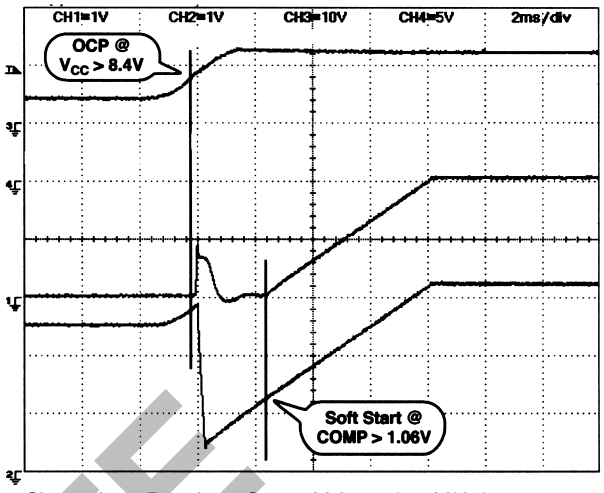
**Figure 10. Normal Startup (5.0 ms/div)**




Channel 1 – $V_{CC2}$ (10 V/div)
Channel 2 – GATE(H) (10 V/div)
Channel 3 – Inductor Switching Node (10 V/div)
Channel 4 – Regulator Output Voltage (2.0 V/div)

**Figure 11. Normal Startup Showing Initial Pulse Followed by Soft Start (5.0 μs/div)**

If the voltage across the Current Sense resistor generates a voltage difference between the $V_{FB}$ and $V_{OUT}$ pins that exceeds the OVC Comparator Offset Voltage (86 mV typical), the Fault latch is set. This causes the COMP pin to be quickly discharged, turning off GATE(H) and the upper NFET since the voltage on the COMP pin is now less than the 1.1 V PWM comparator offset. The Fault latch is reset when the voltage on the COMP decreases below the discharge threshold voltage (0.25 V typical). The COMP capacitor will again begin to charge, and when it exceeds the 1.1 V PWM comparator offset, the regulator output will Soft Start normally (see Figure 12).




Channel 1 – Regulator Output Voltage (1.0 V/div)
Channel 2 – COMP Pin (1.0 V/div)
Channel 3 – $V_{CC}$ (10 V/div)

**Figure 12. Startup with COMP Pre−Charged to 2.0 V (2.0 ms/div)**

When driving large capacitive loads, the COMP must charge slowly enough to avoid tripping the CS51312 overcurrent protection. The following equation can be used to ensure unconditional startup:

$$\frac{I_{CHG}}{C_{COMP}} < \frac{I_{LIM} - I_{LOAD}}{C_{OUT}}$$

where:
$I_{CHG}$ = COMP Source Current (30 μA typical);
$C_{COMP}$ = COMP Capacitor value (0.1 μF typical);
$I_{LIM}$ = Current Limit Threshold;
$I_{LOAD}$ = Load Current during startup;
$C_{OUT}$ = Total Output Capacitance.

### Normal Operation

During normal operation, Switch Off−Time is constant and set by the $C_{OFF}$ capacitor. Switch On−Time is adjusted by the $V^2$ Control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current and the ESR of the output capacitors

### Transient Response

The CS51312 $V^2$ Control Loop's 200 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse−by−pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained

by the output capacitor(s) during the time required to slew the inductor current.

Overall load transient response is further improved through a feature called “Adaptive Voltage Positioning”. This technique pre−positions the output capacitors voltage to reduce total output voltage excursions during changes in load.

Holding tolerance to 1.0% allows the error amplifiers reference voltage to be targeted +25 mV high without compromising DC accuracy. A “Droop Resistor” connects the Error Amps feedback pin ($V_{FB}$) to the output capacitors and load and carries the output current. With no load, there is no DC drop across this resistor, producing an output voltage tracking the Error amps, including the +25 mV offset. When the full load current is delivered, a 50 mV drop is developed across this resistor. This results in output voltage being offset −25 mV low.

The benefit of Adaptive Voltage Positioning is that additional margin is provided for a load transient before reaching the output voltage specification limits. When load current suddenly increases from its minimum level, the output capacitor is pre−positioned +25 mV. Conversely, when load current suddenly decreases from its maximum level, the output capacitor is pre−positioned −25 mV. For best Transient Response, a combination of a number of high frequency and bulk output capacitors are usually used.

## PROTECTION AND MONITORING FEATURES

### Overcurrent Protection

A hiccup mode current limit protection feature is provided, requiring only the COMP capacitor to implement. The CS51312 provides overcurrent protection by sensing the current through a “Droop” resistor, using an internal current sense comparator. The comparator compares the voltage drop through the “Droop” resistor to an internal reference voltage of 86 mV (typical).

If the voltage drop across the “Droop” resistor exceeds this threshold, the current sense comparator allows the fault latch to be set. This causes the regulator to stop switching.

During this over current condition, the CS51312 stays off for the time it takes the COMP pin capacitor to discharge to its lower 0.25 V threshold. As soon as the COMP pin reaches 0.25 V, the Fault latch is reset (no overcurrent condition present) and the COMP pin is charged with a 30 μA current source to a voltage 1.1 V greater than the $V_{FB}$ voltage. Only at this point the regulator attempts to restart normally by delivering short gate pulses to both FETs. This protection scheme minimizes thermal stress to the regulator components, input power supply, and PC board traces, as the over current condition persists. Upon removal of the overload, the fault latch is cleared, allowing normal operation to resume.

### Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the $V^2$ control topology and requires no additional external components. The control loop responds to an overvoltage condition within 200 ns, causing the top MOSFET to shut off, disconnecting the regulator from its input voltage. This results in a “crowbar” action to clamp the output voltage and prevents damage to the load. The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low. Additionally, a dedicated Overvoltage protection (OVP) output pin (pin 13) is provided in the CS51312. The OVP signal will go high (overvoltage condition), if the output voltage ($V_{CC(CORE)}$) exceeds the regulation voltage by 8.5% of the voltage set by the particular DAC code. The OVP pin can source up to 25 mA of current that can be used to drive an SCR to crowbar the power supply.

### Power Good Circuit

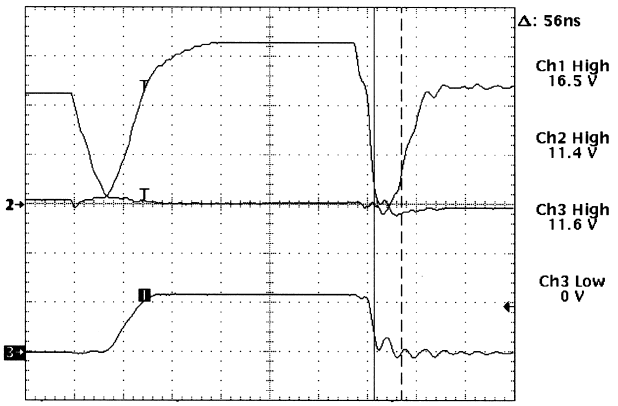
The Power Good pin (pin 14) is an open−collector signal consistent with TTL DC specifications. It is externally pulled up, and is pulled low (below 0.3 V) when the regulator output voltage typically exceeds ±8.5% of the nominal output voltage. Maximum output voltage deviation before Power Good is pulled low is ±12%.

### Output Enable

On/off control of the regulator outputs can be implemented by pulling the COMP pins low. It is required to pull the COMP pins below the 1.1 V PWM comparator offset voltage in order to disable switching on the GATE drivers.

### Adaptive FET Non−Overlap

The CS51312 includes circuitry to prevent the simultaneous conduction of both the high and low side NFETs. This is necessary to prevent efficiency reducing “shoot−through” current from flowing from the input voltage to ground through the two NFETs. Prior to either GATE(H) or GATE(L) driving high, the other GATE must reach its low state. Since GATE rise and fall times vary with loading, this results in a variable delay from the start of turn−off until the start of turn−on (see Figure 13).




Channel 1 – GATE(H) (5.0 V/div)
Channel 2 – GATE(L) (5.0 V/div)
Channel 3 – Inductor Switching Node (10 V/div)

**Figure 13. Adaptive FET Non−Overlap (100 ns/div)**

## CS51312−BASED $V_{CC(CORE)}$ BUCK REGULATOR DESIGN EXAMPLE

### Step 1: Definition of the Design Specifications

The output voltage tolerance can be affected by any or all of the following reasons:

1. buck regulator output voltage setpoint accuracy;
2. output voltage change due to discharging or charging of the bulk decoupling capacitors during a load current transient;
3. output voltage change due to the ESR and ESL of the bulk and high frequency decoupling capacitors, circuit traces, and vias;
4. output voltage ripple and noise.

Budgeting the tolerance is left up to the designer who must take into account all of the above effects and provide an output voltage that will meet the specified tolerance at the load.

The designer must also ensure that the regulator component temperatures are kept within the manufacturer's specified ratings at full load and maximum ambient temperature..

### Step 2: Selection of the Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the regulator output voltage. Key specifications for output capacitors are their ESR (Equivalent Series Resistance), and ESL (Equivalent Series Inductance). For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

In order to determine the number of output capacitors the maximum voltage transient allowed during load transitions has to be specified. The output capacitors must hold the output voltage within these limits since the inductor current can not change with the required slew rate. The output capacitors must therefore have a very low ESL and ESR.

The voltage change during the load current transient is:

$$\Delta V_{OUT} = \Delta I_{OUT} \times \left(\frac{ESL}{\Delta t} + ESR + \frac{t_{TR}}{C_{OUT}}\right)$$

where:

$\Delta I_{OUT} / \Delta t$ = load current slew rate;

$\Delta I_{OUT}$ = load transient;

$\Delta t$ = load transient duration time;

ESL = Maximum allowable ESL including capacitors, circuit traces, and vias;

ESR = Maximum allowable ESR including capacitors and circuit traces;

$t_{TR}$ = output voltage transient response time.

The designer has to independently assign values for the change in output voltage due to ESR, ESL, and output capacitor discharging or charging. Empirical data indicates that most of the output voltage change (droop or spike depending on the load current transition) results from the total output capacitor ESR.

The maximum allowable ESR can then be determined according to the formula

$$ESR_{MAX} = \frac{\Delta V_{ESR}}{\Delta I_{OUT}}$$

where $\Delta V_{ESR}$ = change in output voltage due to ESR (assigned by the designer).

Once the maximum allowable ESR is determined, the number of output capacitors can be found by using the formula

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

where:

$ESR_{CAP}$ = maximum ESR per capacitor (specified in manufacturer's data sheet);

$ESR_{MAX}$ = maximum allowable ESR.

The actual output voltage deviation due to ESR can then be verified and compared to the value assigned by the designer:

$$\Delta V_{ESR} = \Delta I_{OUT} \times ESR_{MAX}$$

Similarly, the maximum allowable ESL is calculated from the following formula:

$$ESL_{MAX} = \frac{\Delta V_{ESL} \times \Delta t}{\Delta I}$$

where:

$\Delta I/\Delta T$ = load current slew rate (as high as 20 A/μs);

$\Delta V_{ESL}$ = change in output voltage due to ESL.

The actual maximum allowable ESL can be determined by using the equation:

$$ESL_{MAX} = \frac{ESL_{CAP}}{\text{Number of output capacitors}}$$

where $ESL_{CAP}$ = maximum ESL per capacitor (it is estimated that a 10 × 12 mm Aluminum Electrolytic capacitor has approximately 4.0 nH of package inductance).

The actual output voltage deviation due to the actual maximum ESL can then be verified:

$$\Delta V_{ESL} = \frac{ESL_{MAX} \times \Delta I}{\Delta t}$$

The designer now must determine the change in output voltage due to output capacitor discharge during the transient:

$$\Delta V_{CAP} = \frac{\Delta I \times \Delta t_{TR}}{C_{OUT}}$$

where:

$\Delta t_{TR}$ = the output voltage transient response time (assigned by the designer);

$\Delta V_{CAP}$ = output voltage deviation due to output capacitor discharge;

$\Delta I$ = Load step.

The total change in output voltage as a result of a load current transient can be verified by the following formula:

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{ESL} + \Delta V_{CAP}$$

**Step 3: Selection of the Duty Cycle, Switching Frequency, Switch On−Time ($T_{ON}$) and Switch Off−Time ($T_{OFF}$)**

The duty cycle of a buck converter (including parasitic losses) is given by the formula:

$$\text{Duty Cycle} = D = \frac{V_{OUT} + (V_{HFET} + V_L + V_{DROOP})}{V_{IN} + V_{LFET} - V_{HFET} - V_L}$$

where:

$V_{OUT}$ = buck regulator output voltage;

$V_{HFET}$ = high side FET voltage drop due to $R_{DS(ON)}$;

$V_L$ = output inductor voltage drop due to inductor wire DC resistance;

$V_{DROOP}$ = droop (current sense) resistor voltage drop;

$V_{IN}$ = buck regulator input voltage;

$V_{LFET}$ = low side FET voltage drop due to $R_{DS(ON)}$.

**Step3a: Calculation of Switch On−Time**

The Switch On−Time (time during which the switching MOSFET in a synchronous buck topology is conducting) is determined by:

$$T_{ON} = \frac{\text{Duty Cycle}}{F_{SW}}$$

where $F_{SW}$ = regulator switching frequency selected by the designer.

Higher operating frequencies allow the use of smaller inductor and capacitor values. Nevertheless, it is common to select lower frequency operation because a higher frequency results in lower efficiency due to MOSFET gate charge losses. Additionally, the use of smaller inductors at higher frequencies results in higher ripple current, higher output voltage ripple, and lower efficiency at light load currents.

**Step 3b: Calculation of Switch Off−Time**

The Switch Off−Time (time during which the switching MOSFET is not conducting) can be determined by:

$$T_{OFF} = \frac{1.0}{F_{SW}} - T_{ON}$$

The $C_{OFF}$ capacitor value has to be selected in order to set the Off−Time, $T_{OFF}$, above:

$$C_{OFF} = \frac{\text{Period} \times (1.0 - D)}{3980}$$

where:

3980 is a characteristic factor of the CS51312;

D = Duty Cycle.

**Step 4: Selection of the Output Inductor**

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response. There are many factors to consider in selecting the inductor including cost, efficiency, EMI and ease of manufacture. The inductor must be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. There are a variety of materials and types of magnetic cores that could be used for this application. Among them are ferrites, molypermalloy cores (MPP), amorphous and powdered iron cores. Powdered iron cores are very commonly used. Powdered iron cores are very suitable due to their high saturation flux density and have low loss at high frequencies, a distributed gap and exhibit very low EMI.

The inductor value can be determined by:

$$L = \frac{(V_{IN} - V_{OUT}) \times t_{TR}}{\Delta I}$$

where:

$V_{IN}$ = input voltage;

$V_{OUT}$ = output voltage;

$t_{TR}$ = output voltage transient response time (assigned by the designer);

$\Delta I$ = load transient.

The inductor ripple current can then be determined:

$$\Delta I_L = \frac{V_{OUT} \times T_{OFF}}{L}$$

where:

$\Delta I_L$ = inductor ripple current;

$V_{OUT}$ = output voltage;

$T_{OFF}$ = switch Off−Time;

L = inductor value.

The designer can now verify if the number of output capacitors from Step 2 will provide an acceptable output voltage ripple (1.0% of output voltage is common). The formula below is used:

$$\Delta I_L = \frac{\Delta V_{OUT}}{ESR_{MAX}}$$

Rearranging we have:

$$ESR_{MAX} = \frac{\Delta V_{OUT}}{\Delta I_L}$$

where

$ESR_{MAX}$ = maximum allowable ESR;

$\Delta V_{OUT}$ = 1.0% × $V_{OUT}$ = maximum allowable output voltage ripple ( budgeted by the designer );

$\Delta I_L$ = inductor ripple current;

$V_{OUT}$ = output voltage.

The number of output capacitors is determined by:

$$\text{Number of capacitors} = \frac{ESR_{CAP}}{ESR_{MAX}}$$

where $ESR_{CAP}$ = maximum ESR per capacitor (specified in manufacturer's data sheet).

The designer must also verify that the inductor value yields reasonable inductor peak and valley currents (the inductor current is a triangular waveform):

$$I_{L(PEAK)} = I_{OUT} + \frac{\Delta I_L}{2.0}$$

where:

$I_{L(PEAK)}$ = inductor peak current;

$I_{OUT}$ = load current;

$\Delta I_L$ = inductor ripple current.

$$I_{L(VALLEY)} = I_{OUT} - \frac{\Delta I_L}{2.0}$$

where $I_{L(VALLEY)}$ = inductor valley current.

**Step 5: Selection of the Input Capacitors**

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the input supply lines. A key specification for input capacitors is their ripple current rating. The input capacitor should also be able to handle the input RMS current $I_{IN(RMS)}$.

The combination of the input capacitors $C_{IN}$ discharges during the on−time.

The input capacitor discharge current is given by:

$$I_{CINDIS(RMS)} = \sqrt{\frac{\left[\begin{array}{l} I_{L(PEAK)}^2 \\ + (I_{L(PEAK)} \times I_{L(VALLEY)}) \\ + I_{L(VALLEY)}^2 \end{array}\right] \times D}{3.0}}$$

where:

$I_{CINDIS(RMS)}$ = input capacitor discharge current;

$I_{L(PEAK)}$ = inductor peak current;

$I_{L(VALLEY)}$ = inductor valley current.

$C_{IN}$ charges during the off−time, the average current through the capacitor over one switching cycle is zero:

$$I_{CIN(CH)} = I_{CIN(DIS)} \times \frac{D}{1.0 - D}$$

where:

$I_{CIN(CH)}$ = input capacitor charge current;

$I_{CIN(DIS)}$ = input capacitor discharge current;

D = Duty Cycle.

The total Input RMS current is:

$$I_{CIN(RMS)} = \sqrt{\begin{array}{l}(I_{CIN(DIS)}^2 \times D) \\ + (I_{CIN(CH)}^2 \times (1.0 - D))\end{array}}$$

The number of input capacitors required is then determined by:

$$N_{CIN} = \frac{I_{CIN(RMS)}}{I_{RIPPLE}}$$

where:

$N_{CIN}$ = number of input capacitors;

$I_{CIN(RMS)}$ = total input RMS current;

$I_{RIPPLE}$ = input capacitor ripple current rating (specified in manufacturer's data sheets).

The total input capacitor ESR needs to be determined in order to calculate the power dissipation of the input capacitors:

$$ESR_{CIN} = \frac{ESR_{CAP}}{N_{CIN}}$$

where:

$ESR_{CIN}$ = total input capacitor ESR;

$ESR_{CAP}$ = maximum ESR per capacitor (specified in manufacturer's data sheets);

$N_{CIN}$ = number of input capacitors.

Once the total ESR of the input capacitors is known, the input capacitor ripple voltage can be determined using the formula:

$$V_{CIN(RMS)} = I_{CIN(RMS)} \times ESR_{CIN}$$

where:

$V_{CIN(RMS)}$ = input capacitor RMS voltage;

$I_{CIN(RMS)}$ = total input RMS current;

$ESR_{CIN}$ = total input capacitor ESR.

The designer must determine the input capacitor power loss in order to ensure there isn't excessive power dissipation through these components. The following formula is used:

$$P_{CIN(RMS)} = I_{CIN(RMS)}^2 \times ESR_{CIN}$$

where:

$P_{CIN(RMS)}$ = input capacitor RMS power dissipation;

$I_{CIN(RMS)}$ = total input RMS current;

$ESR_{CIN}$ = total input capacitor ESR.

**Step 6: Selection of the Input Inductor**

A common requirement is that the buck controller must not disturb the input voltage. One method of achieving this is by using an input inductor and a bypass capacitor. The input inductor isolates the supply from the noise generated in the switching portion of the buck regulator and also limits the inrush current into the input capacitors upon power up. The inductor's limiting effect on the input current slew rate becomes increasingly beneficial during load transients. The worst case is when the load changes from no load to full load (load step), a condition under which the highest voltage

change across the input capacitors is also seen by the input inductor. The inductor successfully blocks the ripple current while placing the transient current requirements on the input bypass capacitor bank, which has to initially support the sudden load change.

The minimum inductance value for the input inductor is therefore:

$$L_{IN} = \frac{\Delta V}{(dI/dt)_{MAX}}$$

where:

$L_{IN}$ = input inductor value;

$\Delta V$ = voltage seen by the input inductor during a full load swing;

$(dI/dt)_{MAX}$ = maximum allowable input current slew rate.

The designer must select the LC filter pole frequency so that at least 40 dB attenuation is obtained at the regulator switching frequency. The LC filter is a double−pole network with a slope of −2.0, a roll−off rate of —40 dB/dec, and a corner frequency:

$$f_C = \frac{1.0}{2.0\pi\sqrt{LC}}$$

where:

L = input inductor;

C = input capacitor(s).

### Step 7: Selection of the Switching FET

#### FET Basics

The use of the MOSFET as a power switch is propelled by two reasons: 1) *Its very high input impedance;* and 2) *Its very fast switching times.* The electrical characteristics of a MOSFET are considered to be those of a perfect switch. Control and drive circuitry power is therefore reduced. Because the input impedance is so high, it is voltage driven. The input of the MOSFET acts as if it were a small capacitor, which the driving circuit must charge at turn on. The lower the drive impedance, the higher the rate of rise of $V_{GS}$, and the faster the turn−on time. Power dissipation in the switching MOSFET consists of 1) conduction losses, 2) leakage losses, 3) turn−on switching losses, 4) turn−off switching losses, and 5) gate−transitions losses. The latter three losses are proportional to frequency. For the conducting power dissipation rms values of current and resistance are used for true power calculations. The fast switching speed of the MOSFET makes it indispensable for high−frequency power supply applications. Not only are switching power losses minimized, but also the maximum usable switching frequency is considerably higher. Switching time is independent of temperature. Also, at higher frequencies, the use of smaller and lighter components (transformer, filter choke, filter capacitor) reduces overall component cost while using less space for more efficient packaging at lower weight.

The MOSFET has purely capacitive input impedance. No DC current is required. It is important to keep in mind the drain current of the FET has a negative temperature coefficient. Increase in temperature causes higher on−resistance and greater leakage current. $V_{DS(ON)}$ should be low to minimize power dissipation at a given $I_D$, and $V_{GS}$ should be high to accomplish this. MOSFET switching times are determined by device capacitance, stray capacitance, and the impedance of the gate drive circuit. Thus the gate driving circuit must have high momentary peak current sourcing and sinking capability for switching the MOSFET. The input capacitance, output capacitance and reverse−transfer capacitance also increase with increased device current rating.

Two considerations complicate the task of estimating switching times. First, since the magnitude of the input capacitance, $C_{ISS}$, varies with $V_{DS}$, the RC time constant determined by the gate−drive impedance and $C_{ISS}$ changes during the switching cycle. Consequently, computation of the rise time of the gate voltage by using a specific gate−drive impedance and input capacitance yields only a rough estimate. The second consideration is the effect of the "Miller" capacitance, $C_{RSS}$, which is referred to as $C_{DG}$ in the following discussion. For example, when a device is on, $V_{DS(ON)}$ is fairly small and $V_{GS}$ is about 12 V. $C_{DG}$ is charged to $V_{DS(ON)} − V_{GS}$, which is a negative potential if the drain is considered the positive electrode. When the drain is "off", $C_{DG}$ is charged to quite a different potential. In this case the voltage across $C_{DG}$ is a positive value since the potential from gate−to−source is near zero volts and $V_{DS}$ is essentially the drain supply voltage. During turn−on and turn−off, these large swings in gate−to−drain voltage tax the current sourcing and sinking capabilities of the gate drive. In addition to charging and discharging $C_{GS}$, the gate drive must also supply the displacement current required by $C_{DG}(I_{GATE} = C_{DG}\ dV_{DG}/dt)$. Unless the gate−drive impedance is very low, the $V_{GS}$ waveform commonly plateaus during rapid changes in the drain−to−source voltage.

The most important aspect of FET performance is the Static Drain−To−Source On−Resistance ($R_{DS(ON)}$), which effects regulator efficiency and FET thermal management requirements. The On−Resistance determines the amount of current a FET can handle without excessive power dissipation that may cause overheating and potentially catastrophic failure. As the drain current rises, especially above the continuous rating, the On−Resistance also increases. Its positive temperature coefficient is between +0.6%/C and +0.85%/C. The higher the On−Resistance the larger the conduction loss is. Additionally, the FET gate charge should be low in order to minimize switching losses and reduce power dissipation.

Both logic level and standard FETs can be used.

Voltage applied to the FET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the FET gates will be driven rail−to−rail due to overshoot caused by the capacitive load they present to the controller IC.

**Step 7a: Selection of the Switching (Upper) FET**

The designer must ensure that the total power dissipation in the FET switch does not cause the power component's junction temperature to exceed 150°C.

The maximum RMS current through the switch can be determined by the following formula:

$$I_{RMS(H)} = \sqrt{\frac{\left[\begin{array}{l} I_{L(PEAK)}^2 \\ + (I_{L(PEAK)} \times I_{L(VALLEY)}) \\ + I_{L(VALLEY)}^2 \end{array}\right] \times D}{3.0}}$$

where:

$I_{RMS(H)}$ = maximum switching MOSFET RMS current;
$I_{L(PEAK)}$ = inductor peak current;
$I_{L(VALLEY)}$ = inductor valley current;
D = Duty Cycle.

Once the RMS current through the switch is known, the switching MOSFET conduction losses can be calculated:

$$P_{RMS(H)} = I_{RMS(H)}^2 \times R_{DS(ON)}$$

where:

$P_{RMS(H)}$ = switching MOSFET conduction losses;
$I_{RMS(H)}$ = maximum switching MOSFET RMS current;
$R_{DS(ON)}$ = FET drain−to−source on−resistance

The upper MOSFET switching losses are caused during MOSFET switch−on and switch−off and can be determined by using the following formula:

$$P_{SWH} = P_{SWH(ON)} + P_{SWH(OFF)} = \frac{V_{IN} \times I_{OUT} \times (t_{RISE} + t_{FALL})}{6.0T}$$

where:

$P_{SWH(ON)}$ = upper MOSFET switch−on losses;
$P_{SWH(OFF)}$ = upper MOSFET switch−off losses;
$V_{IN}$ = input voltage;
$I_{OUT}$ = load current;
$t_{RISE}$ = MOSFET rise time (from FET manufacturer's switching characteristics performance curve);
$t_{FALL}$ = MOSFET fall time (from FET manufacturer's switching characteristics performance curve);
$T = 1/F_{SW}$ = period.

The total power dissipation in the switching MOSFET can then be calculated as:

$$P_{HFET(TOTAL)} = P_{RMSH} + P_{SWH(ON)} + P_{SWH(OFF)}$$

where:

$P_{HFET(TOTAL)}$ = total switching (upper) MOSFET losses;
$P_{RMSH}$ = upper MOSFET switch conduction Losses;
$P_{SWH(ON)}$ = upper MOSFET switch−on losses;
$P_{SWH(OFF)}$ = upper MOSFET switch−off losses.

Once the total power dissipation in the switching FET is known, the maximum FET switch junction temperature can be calculated:

$$T_J = T_A + (P_{HFET(TOTAL)} \times R_{\theta JA})$$

where:

$T_J$ = FET junction temperature;
$T_A$ = ambient temperature;
$P_{HFET(TOTAL)}$ = total switching (upper) FET losses;
$R_{\theta JA}$ = upper FET junction−to−ambient thermal resistance.

**Step 7b: Selection of the Synchronous (Lower) FET**

The switch conduction losses for the lower FET can be calculated as follows:

$$P_{RMSL} = I_{RMS}^2 \times R_{DS(ON)} = \left(I_{OUT} \times \sqrt{(1.0 - D)}\right)^2 \times R_{DS(ON)}$$

where:

$P_{RMSL}$ = lower MOSFET conduction losses;
$I_{OUT}$ = load current;
D = Duty Cycle;
$R_{DS(ON)}$ = lower FET drain−to−source on−resistance.

The synchronous MOSFET has no switching losses, except for losses in the internal body diode, because it turns on into near zero voltage conditions. The MOSFET body diode will conduct during the non−overlap time and the resulting power dissipation (neglecting reverse recovery losses) can be calculated as follows:

$$P_{SWL} = V_{SD} \times I_{LOAD} \times \text{non−overlap time} \times F_{SW}$$

where:

$P_{SWL}$ = lower FET switching losses;
$V_{SD}$ = lower FET source−to−drain voltage;
$I_{LOAD}$ = load current
Non−overlap time = GATE(L)−to−GATE(H) or GATE(H)−to−GATE(L) delay (from CS51312 data sheet Electrical Characteristics section);
$F_{SW}$ = switching frequency.

The total power dissipation in the synchronous (lower) MOSFET can then be calculated as:

$$P_{LFET(TOTAL)} = P_{RMSL} + P_{SWL}$$

where:

$P_{LFET(TOTAL)}$ = Synchronous (lower) FET total losses;
$P_{RMSL}$ = Switch Conduction Losses;
$P_{SWL}$ = Switching losses.

Once the total power dissipation in the synchronous FET is known the maximum FET switch junction temperature can be calculated:

$$T_J = T_A + (P_{LFET(TOTAL)} \times R_{\theta JA})$$

where:

$T_J$ = MOSFET junction temperature;
$T_A$ = ambient temperature;
$P_{LFET(TOTAL)}$ = total synchronous (lower) FET losses;
$R_{\theta JA}$ = lower FET junction−to−ambient thermal resistance.

**Step 8: Control IC Power Dissipation**

The power dissipation of the IC varies with the MOSFETs used, $V_{CC}$, and the CS51312 operating frequency. The average MOSFET gate charge current typically dominates the control IC power dissipation.

The IC power dissipation is determined by the formula:

$$P_{CONTROLIC} = I_{CC1}V_{CC1} + P_{GATE(H)} + P_{GATE(L)}$$

where:

$P_{CONTROLIC}$ = control IC power dissipation;
$I_{CC1}$ = IC quiescent supply current;
$V_{CC1}$ = IC supply voltage;
$P_{GATE(H)}$ = upper MOSFET gate driver (IC) losses;
$P_{GATE(L)}$ = lower MOSFET gate driver (IC) losses.

The upper (switching) MOSFET gate driver (IC) losses are:

$$P_{GATE(H)} = Q_{GATE(H)} \times F_{SW} \times V_{GATE(H)}$$

where:

$P_{GATE(H)}$ = upper MOSFET gate driver (IC) losses;
$Q_{GATE(H)}$ = total upper MOSFET gate charge;
$F_{SW}$ = switching frequency;
$V_{GATE(H)}$ = upper MOSFET gate voltage.

The lower (synchronous) MOSFET gate driver (IC) losses are:

$$P_{GATE(L)} = Q_{GATE(L)} \times F_{SW} \times V_{GATE(L)}$$

where:

$P_{GATE(L)}$ = lower MOSFET gate driver (IC) losses;
$Q_{GATE(L)}$ = total lower MOSFET gate charge;
$F_{SW}$ = switching frequency;
$V_{GATE(L)}$ = lower MOSFET gate voltage.

The junction temperature of the control IC is primarily a function of the PCB layout, since most of the heat is removed through the traces connected to the pins of the IC.

**Step 9: Slope Compensation**

Voltage regulators for today's advanced processors are expected to meet very stringent load transient requirements. One of the key factors in achieving tight dynamic voltage regulation is low ESR at the CPU input supply pins. Low ESR at the regulator output results in low output voltage ripple. The consequence is, however, that there's very little voltage ramp at the control IC feedback pin ($V_{FB}$) and regulator sensitivity to noise and loop instability are two undesirable effects that can surface. The performance of the CS51312−based CPU $V_{CC(CORE)}$ regulator is improved when a fixed amount of slope compensation is added to the output of the PWM Error Amplifier (COMP pin) during the regulator Off−Time. Referring to Figure 14, the amount of voltage ramp at the COMP pin is dependent on the gate voltage of the lower (synchronous) FET and the value of resistor divider formed by R1and R2.

$$V_{SLOPECOMP} = V_{GATE(L)} \times \left(\frac{R2}{R1 + R2}\right) \times \left(1.0 - e^{\frac{-t}{\tau}}\right)$$

where:

$V_{SLOPECOMP}$ = amount of slope added;
$V_{GATE(L)}$ = lower MOSFET gate voltage;
R1, R2 = voltage divider resistors;
$t = t_{OFF}$ (switch off−time);
$\tau$ = RC constant determined by C1 and the parallel combination of R1, R2 (Figure 14), neglecting the low driver output impedance.

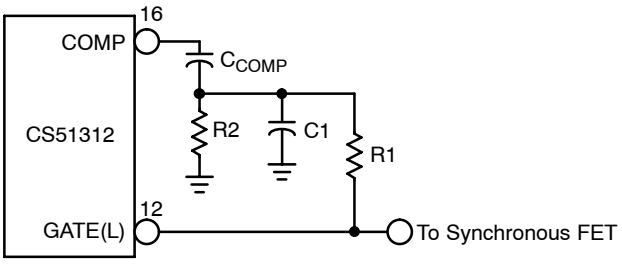



**Figure 14. Small RC Filter Provides the Proper Voltage Ramp at the Beginning of Each On−Time Cycle**

The artificial voltage ramp created by the slope compensation scheme results in improved control loop stability provided that the RC filter time constant is smaller than the off−time cycle duration (time during which the lower MOSFET is conducting). It is important that the series combination of R1 and R2 is high enough in resistance to avoid loading the GATE(L) pin.

#### Step 10: Selection of Current Limit Filter Components

In some applications, the current limit comparator may falsely trigger due to noise, load transients, or high inductor ripple currents. A filter circuit such as the one shown in Figure 15 can be added to prevent this. The RC time constant of this filter is equal to $(R_{FB} + R_{OUT}) \times C_{SENSE}$. Increasing the RC time constant will reduce the sensitivity of the circuit, but increase the time required to detect an overcurrent condition. The value of $R_{FB} + R_{OUT}$ should be kept to 510 Ω or lower to avoid significant DC offsets due to the $V_{FB}$ and $V_{OUT}$ bias currents.

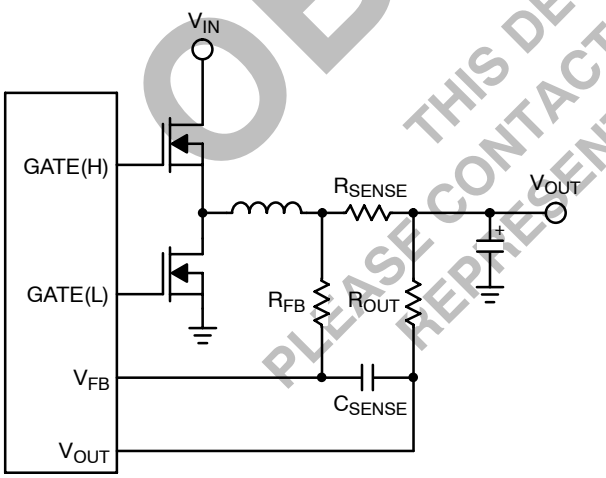



**Figure 15. Current Limit Filter Circuit**

## "DROOP" RESISTOR FOR ADAPTIVE VOLTAGE POSITIONING AND CURRENT LIMIT

Adaptive voltage positioning is used to help keep the output voltage within specification during load transients. To implement adaptive voltage positioning a "Droop Resistor" must be connected between the output inductor and output capacitors and load. This resistor carries the full load current and should be chosen so that both DC and AC tolerance limits are met.

In order to determine the droop resistor value the nominal voltage drop across it at full load has to be calculated. This voltage drop has to be such that the output voltage at full load is above the minimum DC tolerance spec:

$$V_{DROOP(TYP)} = \frac{V_{DAC(MIN)} - V_{DC(MIN)}}{1.0 + R_{DROOP(TOLERANCE)}}$$

#### Current Limit

The current limit setpoint has to be higher than the normal full load current. Attention has to be paid to the current rating of the external power components as these are the first to fail during an overload condition. The MOSFET continuous and pulsed drain current rating at a given case temperature has to be accounted for when setting the current limit trip point.

#### Nominal Current Limit Setpoint

From the overcurrent detection data in the electrical characteristics table:

$$V_{TH(TYP)} = 86\ mV$$

$$I_{CL(NOM)} = \frac{V_{TH(TYP)}}{R_{SENSE(NOM)}}$$

#### Design Rules for Using a Droop Resistor

The basic equation for laying an embedded resistor is:

$$R_{AR} = \rho \times \frac{L}{A} \text{ or } R = \rho \times \frac{L}{(W \times t)}$$

where:

A = W × t = cross−sectional area;
ρ = the copper resistivity (μΩ−mil);
L = length (mils);
W = width (mils);
t = thickness (mils).

An embedded PC trace resistor has the distinct advantage of near zero cost implementation. However, this droop resistor can vary due to three reasons: 1) the sheet resistivity variation caused by variation in the thickness of the PCB layer; 2) the mismatch of L/W; and 3) temperature variation.

#### 1) Sheet Resistivity

For one ounce copper, the thickness variation is typically 1.26 mil to 1.48 mil. Therefore the error due to sheet resistivity is:

$$\frac{1.48 - 1.26}{1.37} = \pm\ 8.0\%$$

#### 2) Mismatch Due to L/W

The variation in L/W is governed by variations due to the PCB manufacturing process. The error due to L/W mismatch is typically 1.0%.

#### 3) Thermal Considerations

Due to $I^2 \times R$ power losses the surface temperature of the droop resistor will increase causing the resistance to

increase. Also, the ambient temperature variation will contribute to the increase of the resistance, according to the formula:

$$R = R_{20}[1.0 + \alpha_{20}(T - 20)]$$

where:

$R_{20}$ = resistance at 20°C;

$\alpha$ = 0.00393/°C

T= operating temperature;

R = desired droop resistor value.

For temperature T = 50°C, the % R change = 12%.

#### Droop Resistor Tolerance

| | |
|---|---|
| Tolerance due to sheet resistivity variation | ±8.0% |
| Tolerance due to L/W error | 1.0% |
| Tolerance due to temperature variation | 12% |
| Total tolerance for droop resistor | 21% |

#### Droop Resistor Length, Width, and Thickness

The minimum width and thickness of the droop resistor should primarily be determined on the basis of the current−carrying capacity required, and the maximum permissible droop resistor temperature rise. PCB manufacturer design charts can be used in determining current−carrying capacity and sizes of etched copper conductors for various temperature rises above ambient.

## THERMAL MANAGEMENT

#### Thermal Considerations for Power MOSFETs

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of 150°C or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:

$$\text{Thermal Impedance} = \frac{T_{J(MAX)} - T_A}{\text{Power}}$$

A heatsink may be added to TO−220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

## EMI MANAGEMENT

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.

## LAYOUT GUIDELINES

When laying out the CPU buck regulator on a printed circuit board, the following checklist should be used to ensure proper operation of the CS51312.

1. Rapid changes in voltage across parasitic capacitors and abrupt changes in current in parasitic inductors are major concerns for a good layout.
2. Keep high currents out of sensitive ground connections.
3. Avoid ground loops as they pick up noise. Use star or single point grounding.
4. For high power buck regulators on double−sided PCBs a single ground plane (usually the bottom) is recommended.
5. Even though double sided PCBs are usually sufficient for a good layout, four−layer PCBs are the optimum approach to reducing susceptibility to noise. Use the two internal layers as the power and GND planes, the top layer for power connections and component vias, and the bottom layer for the noise sensitive traces.
6. Keep the inductor switching node small by placing the output inductor, switching and synchronous FETs close together.
7. The MOSFET gate traces to the IC must be as short, straight, and wide as possible.
8. Use fewer, but larger output capacitors, keep the capacitors clustered, and use multiple layer traces with heavy copper to keep the parasitic resistance low.
9. Place the switching MOSFET as close to the +5.0 V input capacitors as possible.
10. Place the output capacitors as close to the load as possible.
11. Place the $V_{FB}$, $V_{OUT}$ filter resistors (510 Ω) in series with the $V_{FB}$ and $V_{OUT}$ pins as close as possible to the pins.
12. Place the $C_{OFF}$ and COMP capacitors as close as possible to the $C_{OFF}$ and COMP pins.
13. Place the current limit filter capacitor between the $V_{FB}$ and $V_{OUT}$ pins, as close as possible to the pins.
14. Connect the filter components of the following pins: $V_{FB}$, $V_{OUT}$, $C_{OFF}$, and COMP to the GND pin with a single trace, and connect this local GND trace to the output capacitor GND.
15. The “Droop” Resistor (embedded PCB trace) has to be wide enough to carry the full load current.
16. Place the $V_{CC}$ bypass capacitor as close as possible to the IC.

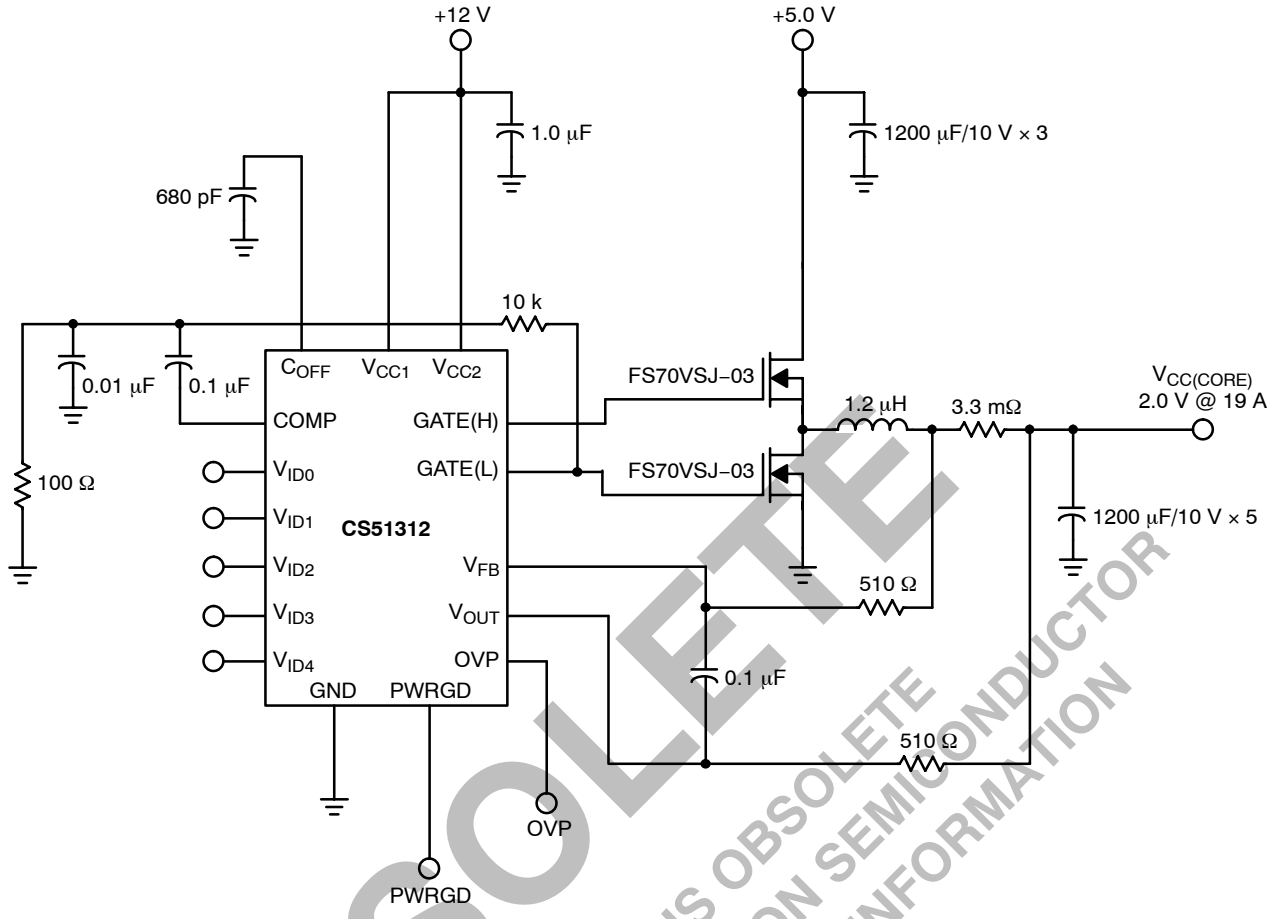
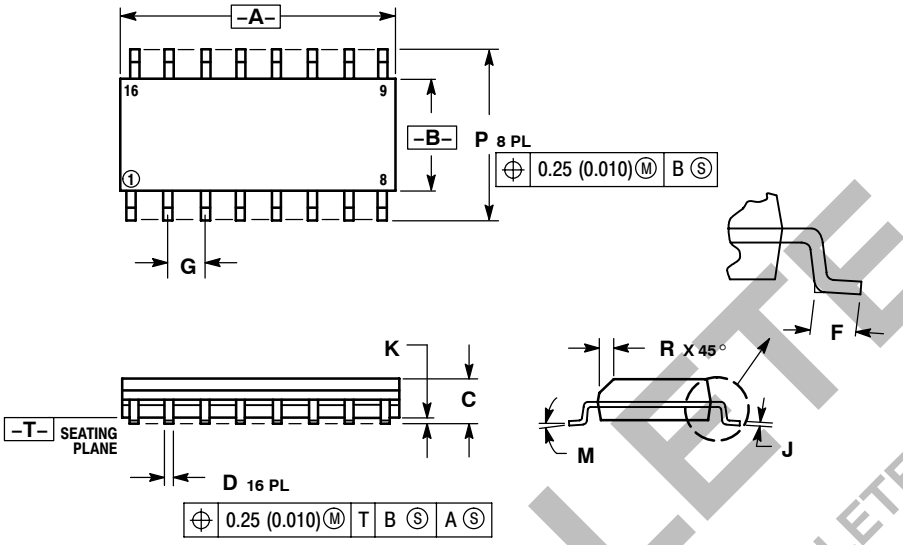



**Figure 16. Additional Application Circuit, 5.0 V/12 V to 2.0 V/19 A Converter**

## PACKAGE DIMENSIONS

**SO−16**
**D SUFFIX**
CASE 751B−05
ISSUE J




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |



**PACKAGE THERMAL DATA**

| Parameter | | SO−16 | Unit |
|---|---|---|---|
| $R_{\Theta JC}$ | Typical | 28 | °C/W |
| $R_{\Theta JA}$ | Typical | 115 | °C/W |

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