

Off-Line Critical Conduction Switching Power Supply with Voltage and Current Limiting

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APPLICATION NOTE

ABSTRACT

The need for a small, economical solution for switching power supplies and for battery chargers has increased. These applications generally require both voltage limiting and current limiting. These must be very efficient and produce a low amount of EMI radiated noise. The MC33364 is a critical conduction control IC that can be configured in a resonant turn-off mode to reduce the amount of EMI generated during turn-off of the power MOSFET. The MC33341 is a secondary side controller that contains the band gap reference to provide a very tight tolerance voltage reference. The MC33341 also allows for current limiting thus providing an almost square loop of voltage and current needed for lithium-ion battery charging. Combining these two devices produces a much more cost-effective solution than other approaches offer.

THE CLASSIC APPROACH

In prior years, a very cost efficient and economical design approach was demanded for battery chargers and power supplies. The unit had to be current limited on the secondary side and provide the proper voltage output. The supply often did not support universal input. One circuit approach to meet this need is shown in Figure 1. This is a classical blocking oscillator. This circuit has its roots back to the old vacuum tube days, and was updated by Bob Haver in 1984 and presented at various switching power supply seminars [1], [2]. This is a variable frequency unit that operates in what is known today as the critical conduction mode.

The unit starts by having the gate of the TMOS™ or power MOSFET turned on by the series resistors R1 and R2. The

current through the primary of the coupled inductor transformer ramps up linearly. The auxiliary winding on the transformer is phased to provide positive (in phase) gate voltage. The TMOS device is “turned off” when the primary current produces approximately 0.7 volts across the source resistor (R_{source}), the bipolar junction transistor (BJT) becomes forward biased and “turns on”.

When the BJT is “turned on”, the charge on the gate is removed and the TMOS power FET is “turned off”. The auxiliary voltage is reversed as the voltage on the primary is reversed in order to release its stored energy to the secondary. As long as there is energy flowing to the secondary, the auxiliary voltage is negative and the gate voltage is negative. The small signal diode (1N914) in series with the collector of the BJT keeps the device from operating in a reverse mode. In lieu of 1N914, a 1N4148 or 1N4150 may be used.

With the TMOS power FET in the “off” mode, the coupled energy stored in the air gap of the inductor is released to the secondary. The secondary energy flows to the load by way of Schottky diode D2. When the coupled energy is depleted, the voltage across the both the primary, secondary and auxiliary windings decreases to zero.

The transformer is not a perfect device, so there is a small amount of energy remaining in the primary. This is the energy in the leakage inductance of the primary. This causes the voltage across the transformer to start to ring with the Coss capacitance of the FET. This “turn-off” ring has the effect of reducing the drain-source voltage of the FET, and causes the auxiliary winding to develop a positive voltage. This positive voltage, along with two resistors R1 and R2 places a positive voltage on the gate of the TMOS power FET; this restarts the energy storage cycle.

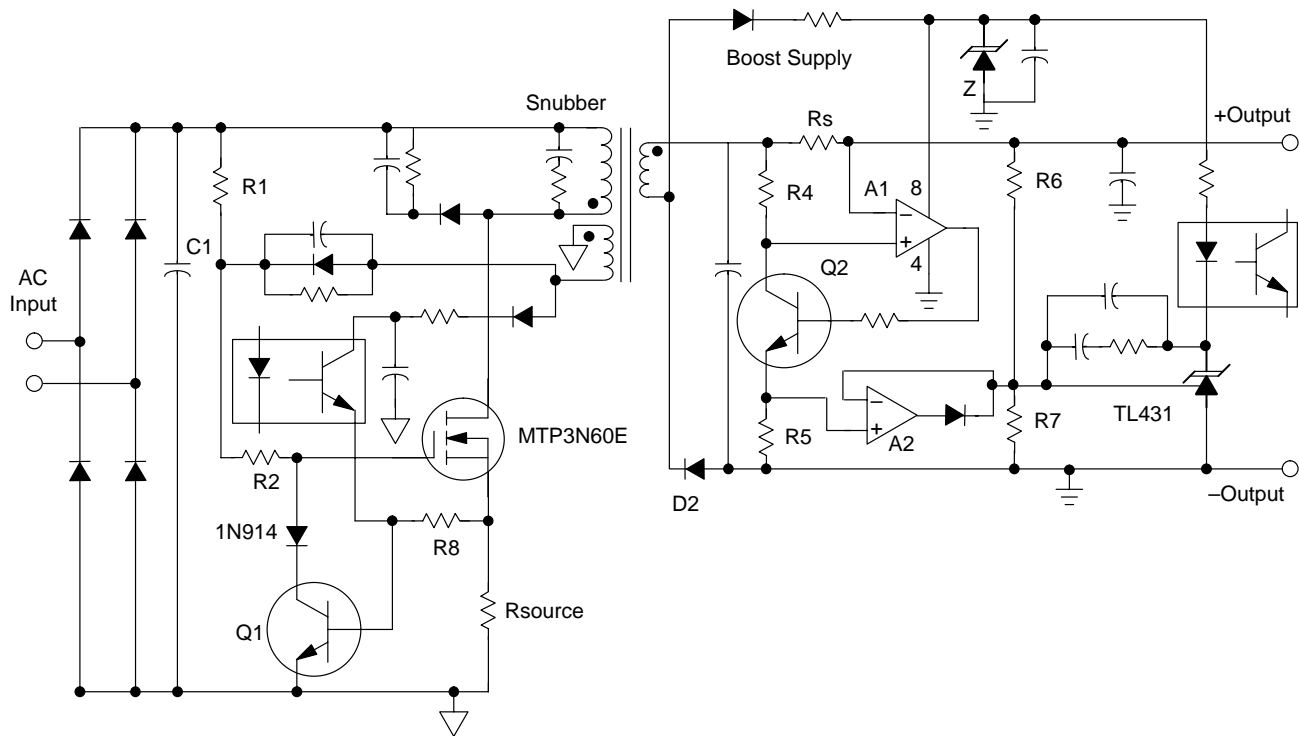


Figure 1. Blocking Oscillator with voltage and current limit on the secondary side

Classic Voltage and Current Feedback

The secondary side contains all the control functions. The voltage feedback is determined by the classic TL431 with resistors R6 and R7. The voltage across R7 is 2.54 volts. The current through the LED of the optocoupler causes the NPN photo-transistor to conduct, thereby developing a small voltage across the resistor R8, which produces an offset voltage to the base of Q1. This causes the primary current to be reduced during a switching or energy storage cycle.

The current limiting is accomplished by the section to the left of the voltage divider resistors R6 and R7. The series resistor, Rs, has the same voltage across it as R4. The ratio of R4/Rs can be thought as a current gain. The operational amplifier, A1, provides current to the base of a high hFE NPN transistor to maintain VR4 equal to VRs. (In some applications Q2 is an N-channel JFET.) The current through R4 is the same current through R5. When voltage across R5 (VR5) exceeds 2.54 volts, the buffer stage composed of A2 and the series diode increases the voltage across R7, which causes the LED current to increase and raises the offset voltage on the primary side. Only when VR5 exceeds the TL431 reference voltage is the current limit applied.

In order to have the operational amplifiers A1 and A2 (MC33072) function properly, a boosted supply voltage is necessary. This is accomplished by using the forward voltage mode of the transformer. This boosted supply voltage is limited by the zener, Z.

The maximum load current can be defined by Equation 1:

$$I_{LoadMax} = \frac{2.5}{R5} * \frac{R4}{Rs} \tag{1}$$

As an example, if the maximum is 3.0 amps, Rs is chosen to dissipate less than 0.5 watts at full load. This calculates to be a 0.05556 ohm resistor, therefore a more practical value of 0.05 ohm is chosen, which is typically composed of two 0.1 ohm resistors. The next item to be chosen is the current gain. A value of 200 would produce a maximum current of 15 mA through R4 and R5. This would make R4 equal to 10 ohms (0.05 * 200 = 10). The value of R5 then becomes 166.667 ohms. This value can be created by using two series resistors, a 160 ohm and a 6.8 ohm, both of which are 0.25 watt or less.

The effect of the feedback is to create a square output characteristic as shown in Figure 2. Because there is no perfect square output characteristic, the current is raised slightly. In this case only a 150 ohm resistor would be used for R5 which raises the output current to 3.33 amps. A 160 ohm resistor would provide 3.125 amps.

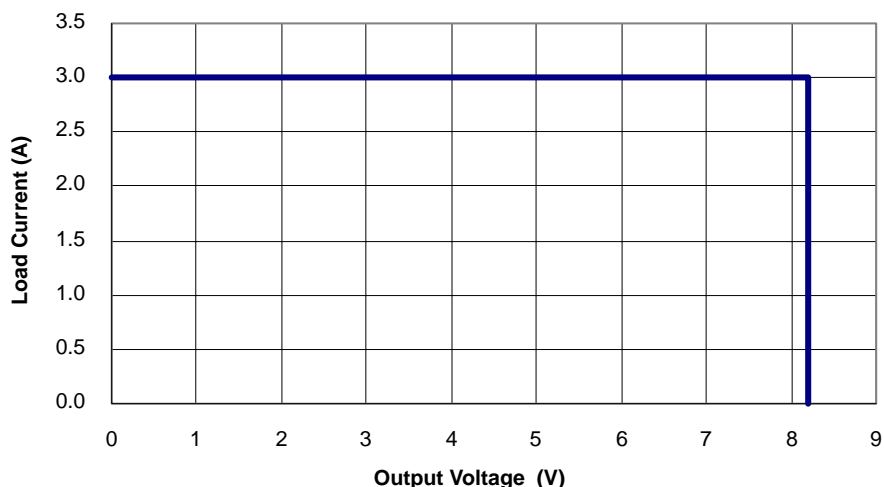


Figure 2. Square Voltage and Current Output Characteristics

Problems and Issues with the Blocking Oscillator

There are many issues associated with the blocking oscillator. The first issue is that it can only be designed for a single voltage input, such as 120 VAC or 220 VAC. This will not operate over the entire range from 85 VAC to 270 VAC input, due to the auxiliary voltage variation. The auxiliary voltage is proportional to the rectified DC line voltage across the input electrolytic capacitor C1. If the auxiliary voltage is 7 volts with the valley of voltage of C1 equal to 100 volts, this would mean 13 volts for 132 VAC input and 21.77 volts for a 220 VAC input. There are two problems with this. First, 7 volts is very near the threshold of the high voltage power FET for good saturation. The lowest voltage for a non-logic level device using “Engineering Rule of Thumb” is 8 volts. The highest gate voltage which should be applied using good engineering practice is 8 volts. Clearly, this is not a “Universal Input” candidate.

The second issue is the gate turn-off. The transistor Q1 has a limit to its ability to rapidly “turn-off” the power FET. The power FET therefore dissipates additional energy, requiring a large heat sink. The third issue occurs under a no load condition, where the frequency of operation becomes very high.

Problems and Issues with the Classic Secondary Side Control

The initial problem is operation under a short circuit condition. When the LED is connected to the +Output, there is no voltage to power the LED to cut back on the short circuit current. Therefore, the LED should be connected to the “Boosted Supply”.

The current should be limited through the LED to maintain a voltage on the “Boosted Supply”.

The second issue is the large number of components necessary to implement this circuit. Even though all of the components are available as surface mount components, it is important to note that quality, cost and space are usually impacted as component count increases.

THE IMPROVED APPROACH

Primary Side Integrated Circuit, MC33364

Today, a power supply is required have a universal input. Laptop computer, cellular phone, and various other pieces of equipment are required to be able to operate in any country or place on earth where AC or DC electrical energy is available. The requirement today is to only change the plug, which connects to power supply. The requirements are:

1. Universal Input Voltage
2. Circuit Short Operation
3. Open Circuit Operation
4. Power Limit or Square Loop Load Operation

There are various integrated circuits today that can perform this function; one of them is the MC33364. The MC33364 is labeled a critical conduction controller, which is the same as the traditional blocking oscillator shown in Figure 1. Therefore, the transformer design is identical to that of the blocking oscillator.

The advantages of this IC over the discrete blocking oscillator are:

1. Wide input voltage range from 40 VDC to 700 VDC. This IC can operate from the 48 volt telecom DC bus to the 381 VAC line-to-line voltage common in Europe
2. Full gate drive to properly drive high voltage power FET or IGBTs in a TO-220 package that only need 15 volts
3. Frequency clamp to limit the open circuit frequency
4. Reference to be able to perform primary side control

Low line is an 85 VAC, 50 Hz input with a 20 volt ripple on the electrolytic at this voltage. This defines the valley, from which the size of the electrolytic capacitor and the value of the inductor are determined. The value of the capacitor can be determined by several methods. Two will be given here. The first comes from a text by Savant et al [4] where:

$$C = \frac{V_{PEAK \text{ at LOWLINE}}}{\Delta V_{PEAK \text{ RIPPLE}} * FREQ * R_{LOAD}} \quad (4)$$

$$\frac{85 * \sqrt{2}}{20 * 100 * 500} = 120 \mu F \text{ for a 20 volt peak-to-peak ripple} \quad (5)$$

$$\frac{85 * \sqrt{2}}{25 * 100 * 500} = 96 \mu F \text{ for a 25 volt peak-to-peak ripple} \quad (6)$$

$$R_{Load} = \frac{V_{CAP \text{ AVERAGE}}^2}{\text{Watts}} \quad (7)$$

$$V_{CAP \text{ AVERAGE}} = V_{PEAK \text{ at LOWLINE}} - \frac{\Delta V_{PEAK \text{ RIPPLE}}}{2} \quad (8)$$

The second method uses the joules of energy to calculate the value of the capacitor. From engineering experience, the length of time the diodes conduct in a full wave bridge is approximately 2.5 milliseconds for a 50 Hz system and about 2.25 milliseconds for a 60 Hz system. This means the energy storage electrolytic capacitor must supply the energy during the non-conducting period. This is 7.5 milliseconds for 50 Hz and 6 milliseconds for a 60 Hz system.

$$\text{Joules} = \text{Watt} * \text{Seconds} \quad (9)$$

$$\text{Joules} = 30 * 7.5e - 3 = 0.225 \quad (10)$$

$$\text{Joules} = \frac{1}{2} CV^2_{PEAK} - \frac{1}{2} CV^2_{VALLEY} \quad (11)$$

$$C = \frac{2 * \text{JoulesLoad}}{V^2_{PEAK} - V^2_{VALLEY}} \quad (12)$$

$$C = \frac{2 * 0.225}{(85 * \sqrt{2})^2 - (85 * \sqrt{2} - 25)^2} = 83.5 \mu F \quad (13)$$

Both methods indicate a large electrolytic capacitance value is needed for operation at 85 VAC 50 Hz. The DC rating of the electrolytic capacitor is defined by the AC high line voltage, which is 270 volts. This means a 400 volt electrolytic capacitor is necessary. The typical embodiment is one 100 μF 400 VDC electrolytic, or two 47 μF 400 VDC electrolytics in parallel.

As an added note, if the supply were to be used in the US and Canada on a 120 volt, 60 Hz line, 2 times load is an "Engineering Rule of Thumb". This would be a 60 μF capacitor, or a 68 μF from manufacturers' catalogs. If in Europe, with its 220 VAC, 50 Hz line, the capacitor would be the 30 μF, or as a typical catalog value, 33 μF.

Power Factor Correction (PFC) and Hold Up Time

The design of a universal input from 85 VAC 50 Hz to 270 VAC 50 Hz can be difficult, as seen by the size of electrolytic capacitors. The above capacitor sizing does not include any "hold-up" time for missing AC line cycles. If a "hold-up" time is required along with a universal input, it is strongly suggested that an active PFC circuit be considered. This would reduce the capacitance value of the electrolytic capacitor and reduce the current rating of the flyback power MOSFET. The voltage ratings of both parts would remain nearly identical. Using an active PFC circuit like the MC33262 or the MC33261 could help reduce the physical size of the unit. The data sheets for the MC33262 and MC33261 contain design equations, and several reference designs are included with data.

Transformer or Coupled Inductor Design

Because the minimum voltage is defined, the value of the inductance can now be calculated. The minimum DC voltage across the electrolytic capacitor is 95 volts. At this point, the duty cycle is a maximum of 0.5, meaning that the on-time is equal to the off-time of the switch. The peak current for the switch and the inductance value are both calculated. This is developed by Chryssis [5]. The minimum frequency at full load is calculated to be 70 kHz.

$$I_{PEAK \text{ PRIMARY}} = \frac{2 * \text{Watts}}{V_{DC.MIN} * \delta_{MAX}} \quad (14)$$

$$\frac{2 * 30}{95 * 0.5} = 1.26 \text{ Amps} \quad (15)$$

$$E = L \frac{di}{dt} = L \frac{\frac{2 * \text{Watts}}{V_{DC.MIN} * \delta_{MAX}}}{\frac{\delta}{\text{Freq}}} \quad (16)$$

$$L = \frac{V^2_{DC.MIN} * \delta^2_{MAX}}{2 * \text{Watt} * \text{Freq}} = \frac{95^2 * 0.5^2}{2 * 30 * 70e3} = 537 \mu H \quad (17)$$

The core was chosen from parts readily available; Ferrite International (7070-30-15-07), Magnetic (P43007), Philips (E30/15/7-3C80). This core has the following parameters:

Cross Sectional Area, Ae or Ac = 0.49 cm² min. center leg
Magnetic Material Path Length, lm = 6.56 cm

The turns are calculated using Equation 19, which is developed from Equation 18.

$$E = N \frac{\partial \theta}{\partial t} = N A_C \frac{\partial B}{\partial t} \quad (18)$$

$$N = \frac{E \Delta t}{A_C \Delta B} \quad (19)$$

For the primary, there are 68 turns using AWG 25 wire. Next, the air gap is calculated to determine the edge space. The gap is calculated using equations 20 and 21. The gap is the total gap including the edge gap and the center gap. Since ungapped cores are being used, the gap length is divided by two, and the spacer is placed on the outer legs. The total gap is 2.05 e-5 meters, or 0.008 inches. This means a spacer of 0.004 inches, which is the thickness of sheet of copier paper.

$$L = \frac{N^2}{\mathcal{R}} = \frac{N^2}{\mathcal{R}_{CORE} + \mathcal{R}_{MATERIAL}} = \frac{N^2}{\frac{l_m}{\mu_0 \mu_R A_C} + \frac{l_{GAP}}{\mu_0 A_{GAP}}} \quad (20)$$

$$l_{GAP} = \frac{\mu_0 A_C N^2}{L} - \frac{l_m}{\mu_R} \quad (21)$$

L = Inductance in henries

l_m = core magnetic path length in meters

l_{gap} = gap length in meters

$A_C = A_e$ = Effective Cross Sectional Area in Meters²

$\mu_0 = 4\pi 10^{-7}$

μ_R = Core Permeability

N = Number of turns

The primary voltage divided by the primary turns defines the volts per turn, which is approximately 1.4 volts per turn. The secondary turns is calculated to be 6.35 turns. A value of 7 turns is chosen for the 8.3 volt secondary using two strands of 24 AWG magnet wire, and 10 turns is chosen for the auxiliary winding, using 30 AWG. If the power switch is an IGBT requiring 15 volts, the auxiliary winding would be 13 turns. All of this easily fits onto the single section bobbin. Additional information is available in the form of application notes from ON Semiconductor, see references [6], [7], and [8].

Transformer Sizing

It is beyond the intent of this application note to teach exact transformer and inductor design. The information given is used as a guide for background information. Choosing the size of the transformer or coupled inductor is easy, but there are rules of thumb. One of the easier methods is to use the "Area Product" method. The equations are developed in the Magnetics Ferrite Core catalog [9]. Another set of equations along with data is found in C. McLyman's books [10], [11], [12], which have become standards for transformer and inductor designers. The Area Product (A_P) equation is defined below for single transistor forward converter transformers and flyback transformers. This defines the smallest possible core.

A_P = Area product in cm⁴

P_O = Output power of all the windings

C = Inverse of current density $1/J = 3.55 * 10^{-3}$ cm² /Amp

$$A_P = \frac{P_O C * 10^8}{2eB^2FK} \quad (22)$$

This is similar to 500 circular mils per Amp.

e = Efficiency, often taken as 0.9 for a starting point

B = Peak flux density the core will see

F = Switching Frequency

K = Transformer utilization factor, typically 0.3

For a transformer this can never exceed 0.5

For an inductor this can be near 0.8

$$A_P = \frac{3 * 3.22 * 10^{-3} * 10^8}{2 * 0.9 * 2000 * 70 * 10^3 * 0.3} = 0.12778 \text{cm}^4 \quad (23)$$

The core chosen must be larger than 0.127 cm⁴. In order to meet many of the European regulator standards, the A_P may have to be increased by a factor between 2 and 3. This is where the art of transformer design begins to play an important part. The core chosen for this example has an $A_P = 0.55$ cm⁴.

Non-Dissipated Snubber Design For Quasi Resonant Mode Operation

The snubber circuit can be modified to make the circuit dissipate less energy and to lower the switching transitions. This is shown in Figure 4. The lossless snubber described in

Chapter 11 of the Rectifier Applications Handbook [13] reduces the turn-off losses of the power FET by limiting the dV/dt rise of the drain-source voltage. By starting with Equation 24 and rearranging into Equation 25, the turn-off energy to the power FET can be greatly reduced.

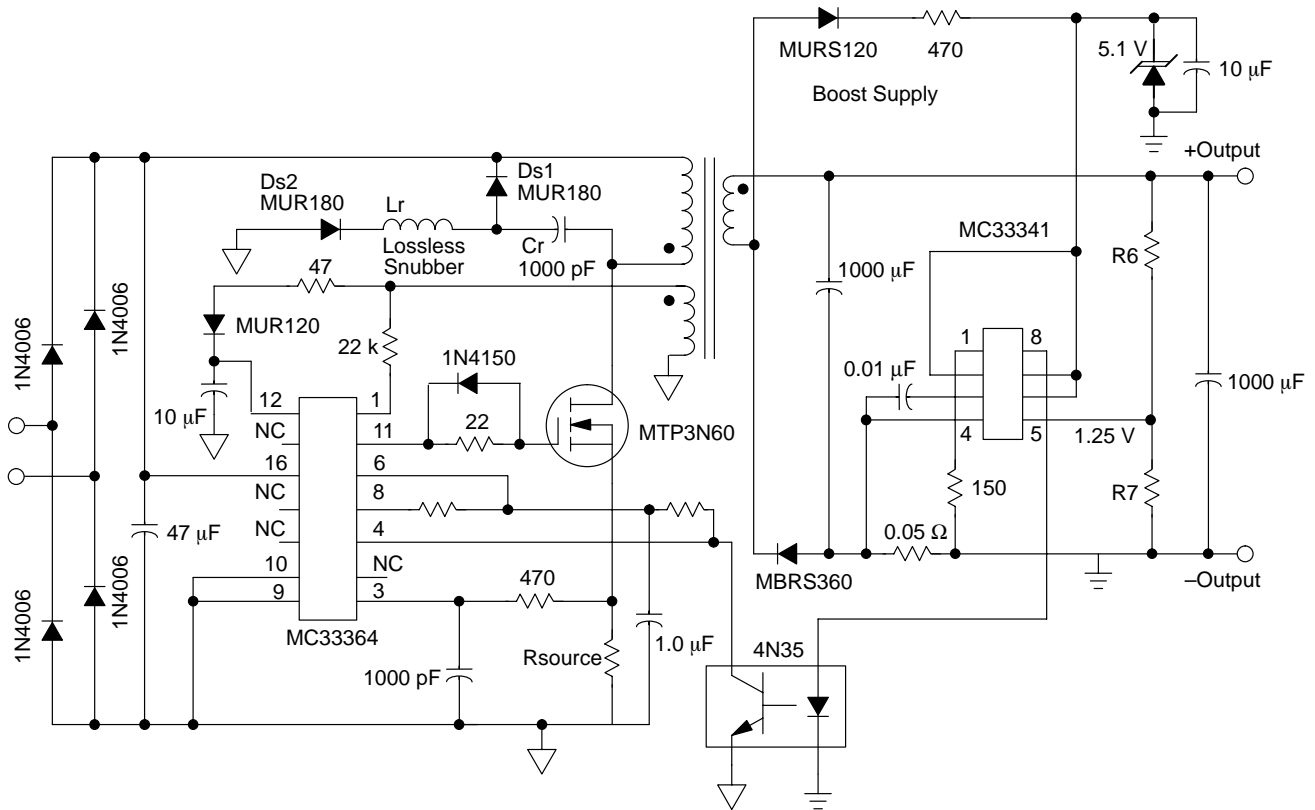


Figure 4. Lossless Snubber Circuit

During the beginning of the power FET “turn-off” period, the primary current wants to continue to flow, and forces the primary winding to change voltage direction. Instead of the primary current flowing through the FET, the current is directed through the capacitor, Cr, and diode, Ds1. The capacitor, Cr, charges to a voltage defined by Equation 26. The energy stored is given by Equation 27.

$$i = C \frac{\partial V}{\partial t} \tag{24}$$

$$\frac{i}{C} = C \frac{\partial V}{\partial t} \tag{25}$$

$$V_{Cr} = (V_{OUTPUT} + 0.7 V) \left(\frac{N_{PRIMARY}}{N_{SECONDARY}} \right) \tag{26}$$

$$86.4 = (8.2 + 0.7) \left(\frac{68}{7} \right)$$

$$J_{Cr} = \frac{1}{2} C V_{Cr}^2 \tag{27}$$

After all of the coupled energy is released to the secondary, the voltage on the auxiliary winding rings through zero and forces the MC33364 to start the next

energy storage cycle. When the Power FET turns on, the drain of the FET is at ground potential. There is a complete circuit consisting of the FET, diode (Ds2), inductor (Lr), and capacitor (Cr). In an ideal condition the voltage on the capacitor reverses its polarity, this is explained by Rashid in Chapter 2 of his text “Power Electronics” [14]. The time for this transition to occur is defined by Equation 28.

$$t = \pi \sqrt{C_r * L_r} \tag{28}$$

The value of the peak current is defined by Equation 29.

$$i_R = V_{Cr} \sqrt{\frac{C_r}{L_r}} \tag{29}$$

There are several limits that need to be considered. The time needs to be less than 1 microsecond. The value of the peak current needs to be less than the maximum peak current the power FET can handle. Table 1 shows this variation where Cr is 1000 picofarads and VCr = 86.4 volts using Equation 26.

The construction of the inductor Lr is somewhat critical. The inductor should be a toroid using a powdered iron material with a ur less than 100. The reason for a toroid is to

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confine the flux in small space and not radiate to the rest of the circuit. Using a MicroMetals [15] toroidal core, T38–26 or T38–52, with 14 turns, an 9.6 microhenry inductor can be constructed. This corresponds to a transition time of just over 0.3 microseconds and a peak current of 0.9 Amps. This is considerably under the peak current rating of the MTP3N60E device.

There is an RC filter between the FET source sense resistor, R_{source}, and the input to the IC, MC33364. The time constant of this RC network needs to be greater than the transition time of the snubber network. The purpose of this RC filter is to eliminate false triggering, and is often called leading edge blanking network.

Table 1. Lr and I_{peak} for Given Times

Time in μS	Lr in H	I _{peak}
0.2	4.05e – 06	1.357
0.3	9.12e – 06	0.905
0.4	1.62e – 05	0.679
0.5	2.53e – 05	0.543
0.6	3.65e – 05	0.452
0.7	4.96e – 05	0.388
0.8	6.48e – 05	0.339
0.9	8.21e – 05	0.302
1.0	1.01e – 04	0.271


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Notes

Notes

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