CY62138EV30 MoBL®

2 Mbit (256K x 8) MoBL® Static RAM

Features

- Very high speed: 45 ns
  - Wide voltage range: 2.20 V to 3.60 V
- Pin compatible with CY62138CV30
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 7 µA
- Ultra low active power
  - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconducor (CMOS) for optimum speed and power
- Offered in Pb-free 36-ball ball grid array (BGA) package

Functional Description

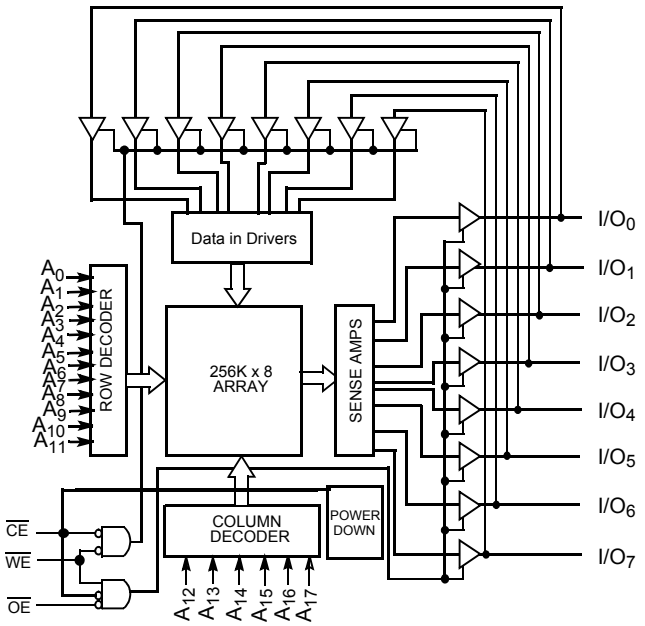
The CY62138EV30[1] is a high performance CMOS static RAM organized as 256K words by eight bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. The device can be put into standby mode reducing power consumption when deselected ($\overline{CE}$ HIGH).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

Logic Block Diagram

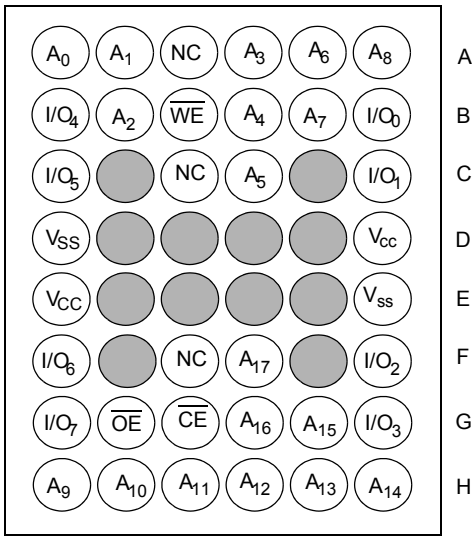


Note
1. For best practice recommendations, refer to the Cypress application note “SRAM System Design Guidelines” on http://www.cypress.com.

Contents

Pin Configuration[2]

FBGA
Top View



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (μA)	
					f = 1 MHz		f = f_{max}			
	Min	Typ[3]	Max		Typ[3]	Max	Typ[3]	Max	Typ[3]	Max
CY62138EV30LL	2.2	3.0	3.6	45	2	2.5	15	20	1	7

Notes
2. NC pins are not connected on the die.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, T_A = 25 °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature..... –65 °C to +150 °C

Ambient temperature with power applied ..... 55 °C to +125 °C

Supply voltage to ground potential.....–0.3 V to $V_{CC(MAX)}$ + 0.3 V

DC voltage applied to outputs in High Z state[4,5].....–0.3 V to $V_{CC(MAX)}$ + 0.3 V

DC input voltage[4,5].....–0.3 V to $V_{CC(MAX)}$ + 0.3 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage..... > 2001 V (per MIL-STD-883, Method 3015)

Latch-up current ..... > 200 mA

Product	Range	Ambient Temperature	V_{CC}[6]
CY62138EV30LL	Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62138EV30-45			Unit
				Min	Typ[7]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA	V_{CC} = 2.20 V	2.0	–	–	V
		I_{OH} = –1.0 mA	V_{CC} = 2.70 V	2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA	V_{CC} = 2.20 V	–	–	0.4	V
		I_{OL} = 2.1 mA	V_{CC} = 2.70 V	–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 2.2 V to 2.7 V		1.8	–	V_{CC} + 0.3V	V
		V_{CC}= 2.7 V to 3.6 V		2.2	–	V_{CC} + 0.3V	V
V_{IL}	Input LOW voltage	V_{CC} = 2.2 V to 2.7 V		–0.3	–	0.6	V
		V_{CC}= 2.7 V to 3.6 V		–0.3	–	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, Output disabled		–1	–	+1	µA
I_{CC}	V_{CC} Operating supply current	$f = f_{max} = 1/t_{RC}$	$V_{CC} = V_{CCmax}$ I_{OUT} = 0 mA CMOS levels	–	15	20	mA
		f = 1 MHz		–	2	2.5	mA
I_{SB1}[8]	Automatic CE power down current — CMOS inputs	$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V), f = f_{max} (Address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), V_{CC} = 3.60 V		–	1	7	µA
I_{SB2} [8]	Automatic CE power down current — CMOS inputs	$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = 3.60 V		–	1	7	µA

Notes

4. $V_{IL(min.)}$ = –2.0 V for pulse durations less than 20 ns.
5. $V_{IH(max)}$ = V_{CC}+0.75 V for pulse durations less than 20 ns.
6. Full device AC operation assumes a 100 µs ramp time from 0 to V_{CC}(min.) and 200 µs wait time after V_{CC} stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25 °C
8. Chip enable ($\overline{CE}$) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.

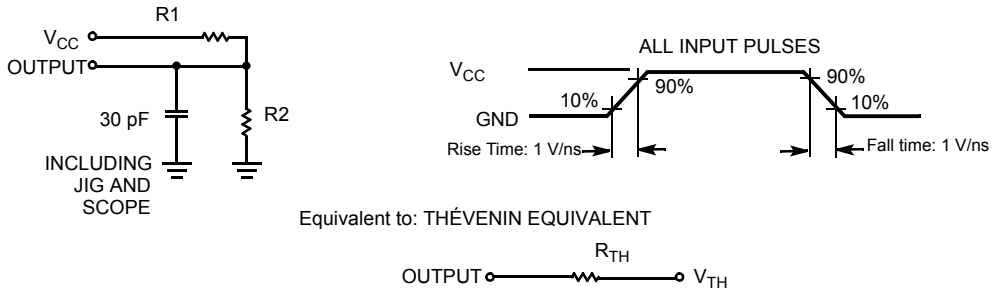
Capacitance

Parameter[9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ.)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter[9]	Description	Test Conditions	BGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	72	°C / W
Θ_{JC}	Thermal resistance (junction to case)		8.86	°C / W

Figure 1. AC Test Loads and Waveforms

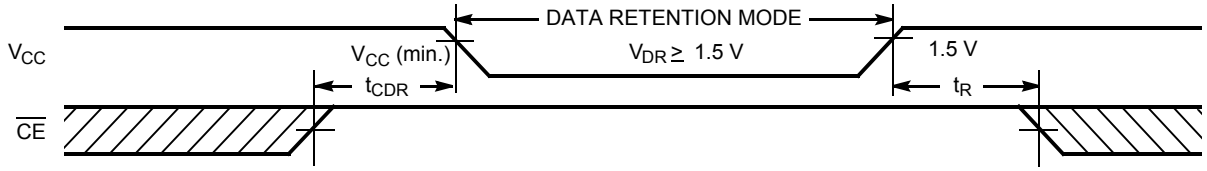


Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min	Typ[10]	Max	Unit
V_{DR}	V_{CC} for data retention		1	–	–	V
I_{CCDR} [11]	Data retention current	V_{CC} = 1V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	0.8	3	µA
t_{CDR}[9]	Chip deselect to data retention time		0	–	–	ns
t_R[12]	Operation recovery time		45	–	–	ns

Data Retention Waveform



Notes

9. Tested initially and after any design or process changes that may affect these parameters.
10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at VCC = VCC(typ), TA = 25 °C
11. Chip enable ($\overline{CE}$) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.
12. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.

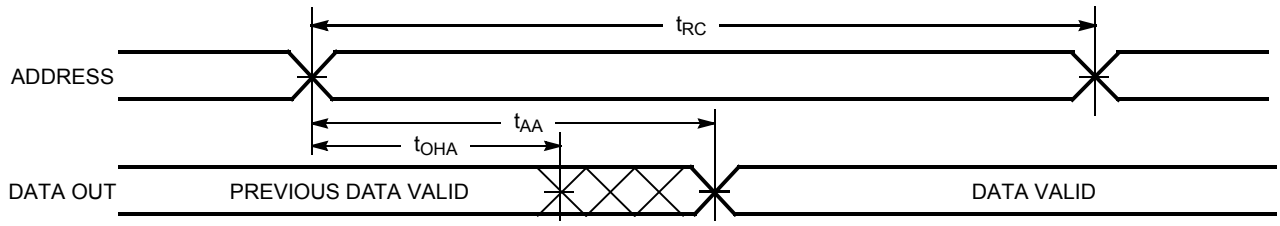
Switching Characteristics

Over the Operating Range

Parameter[13]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[14]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[14,15]	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[14]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[14,15]	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-up	–	45	ns
Write Cycle[16]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[14,15]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[14]	10	–	ns

Switching Waveforms

Figure 2. Read Cycle No. 1: Address Transition Controlled [17, 18]



Notes

13. Test conditions for all parameters other than three-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in AC Test Loads and Waveforms.
14. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
15. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the output enter a high impedance state.
16. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
17. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
18. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Figure 3. Read Cycle No. 2: $\overline{OE}$ Controlled [19, 20]

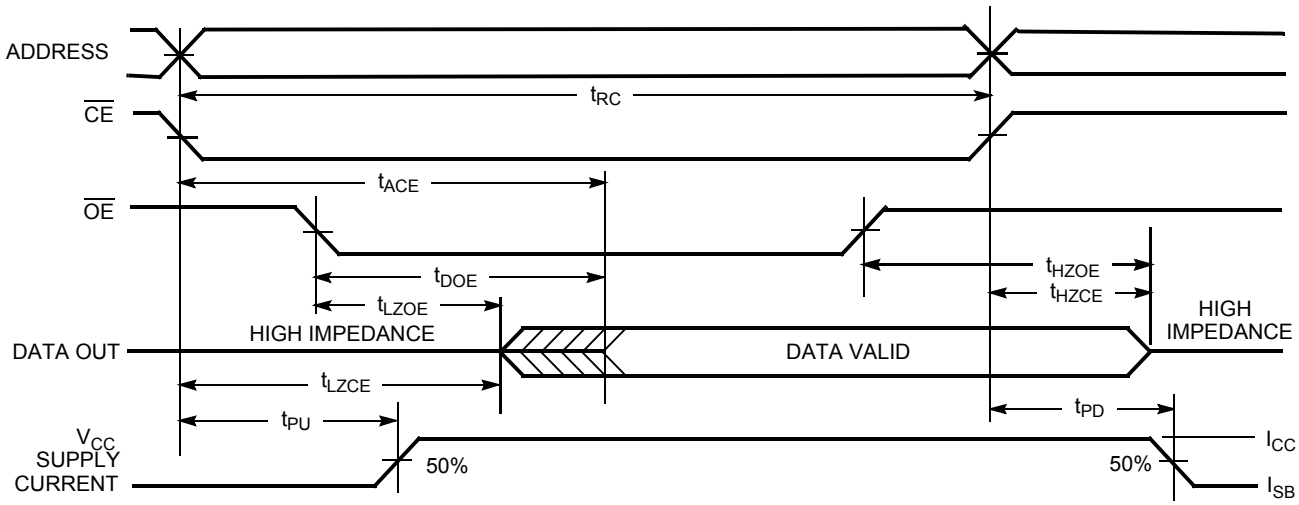
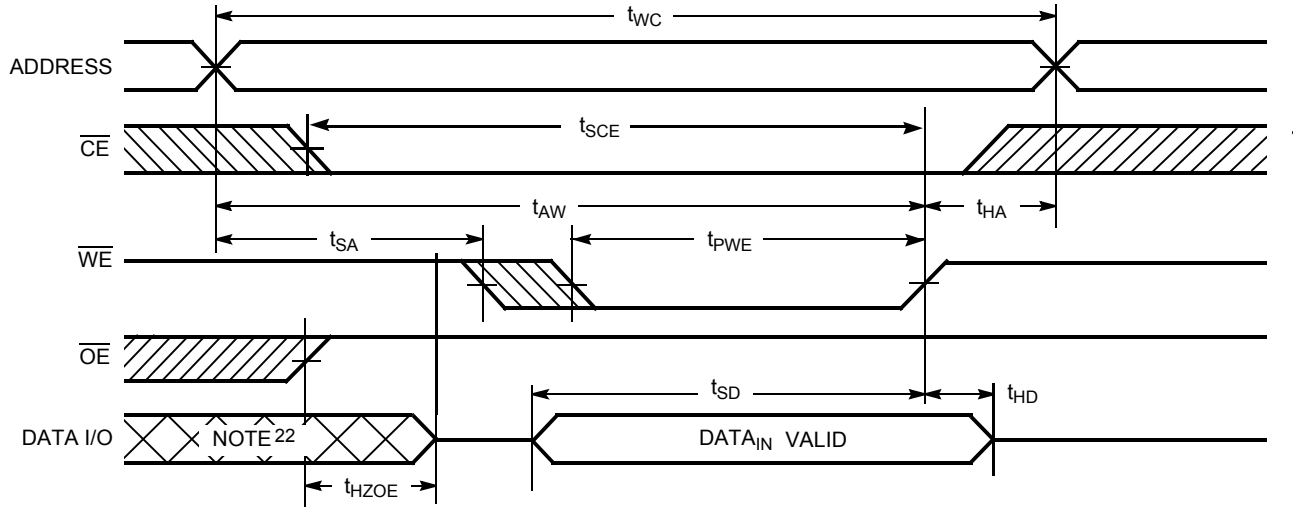


Figure 4. Write Cycle No. 1: $\overline{WE}$ Controlled [21, 23]



Notes
19. $\overline{WE}$ is HIGH for read cycle.
20. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
21. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
22. During this period, the I/Os are in output state and input signals should not be applied.
23. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 2 $\overline{CE}$ Controlled [24, 25]

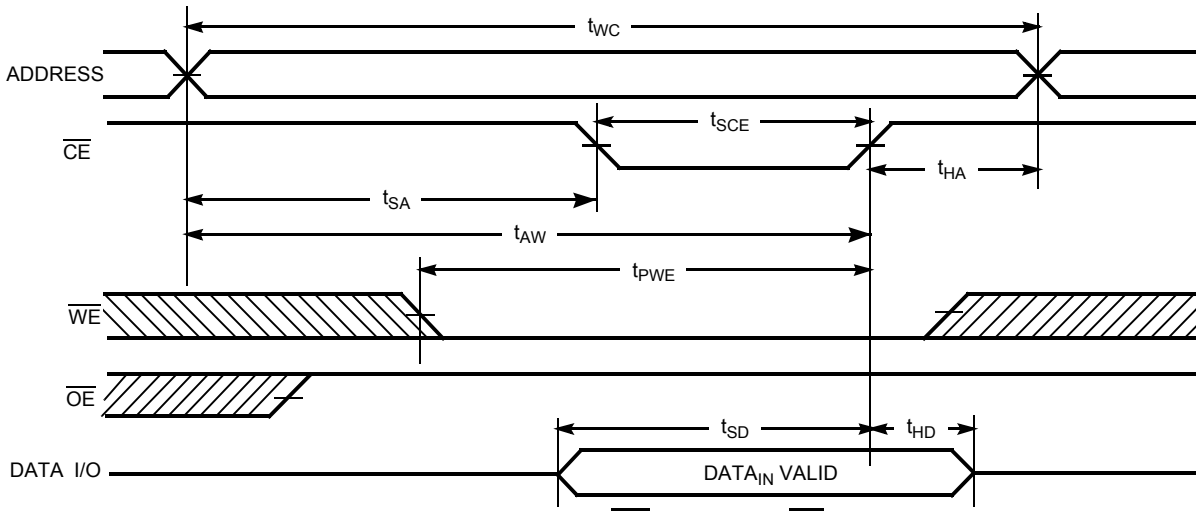
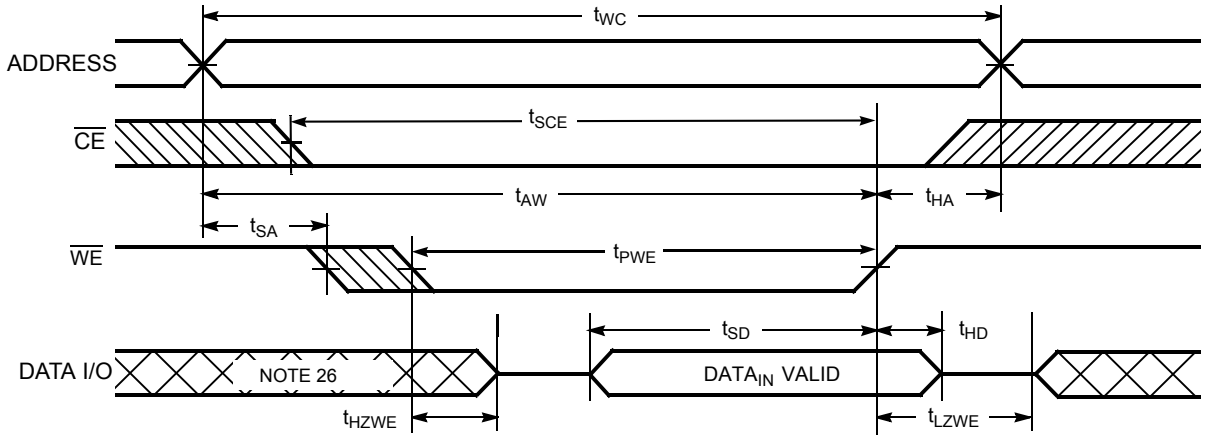


Figure 6. Write Cycle No. 3 : $\overline{WE}$ Controlled, $\overline{OE}$ LOW [25]



Truth Table

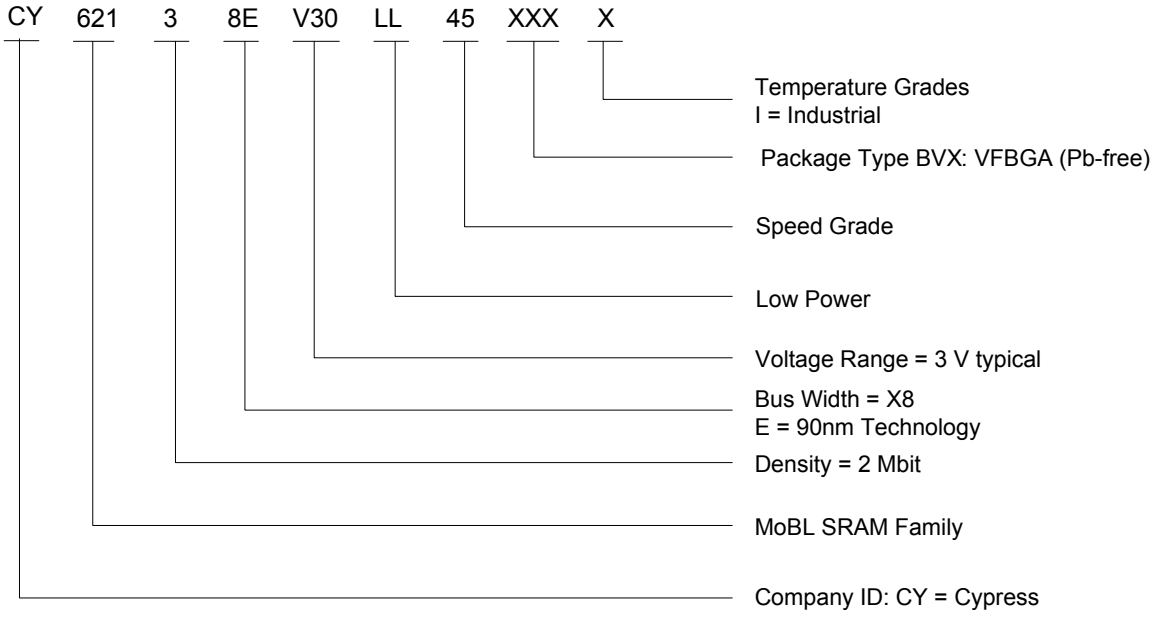
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H[27]	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	H	L	Data out (I/O_0–I/O_7)	Read	Active (I_{CC})
L	H	H	High Z	Output disabled	Active (I_{CC})
L	L	X	Data in (I/O_0–I/O_7)	Write	Active (I_{CC})

Notes
24. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
25. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
26. During this period, the I/Os are in output state and input signals should not be applied.
27. Chip enable ($\overline{CE}$) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.

Ordering Information

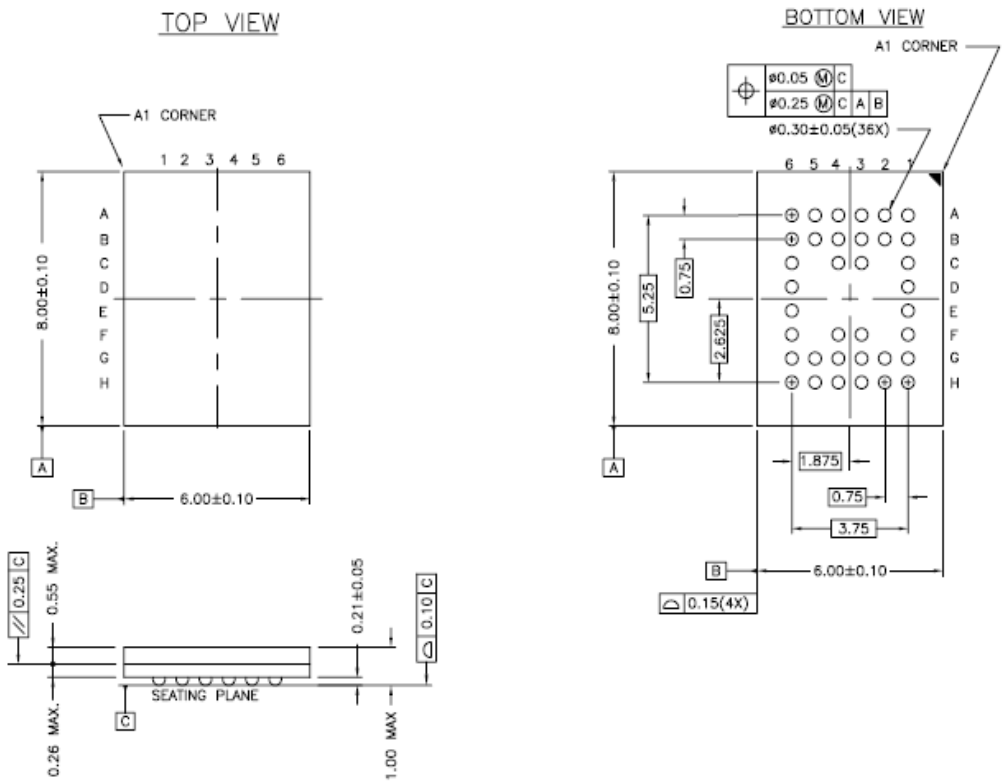
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62138EV30LL-45BVXI	51-85149	36-Ball Very Fine Pitch BGA (6 mm × 8 mm × 1 mm) (Pb-free)	Industrial

Ordering Code Definition



Package Diagram

Figure 7. 36-Ball VFBGA (6 x 8 x 1 mm) (51-85149)



51-85149-*D

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
SRAM	static random access memory
VFBGA	very fine ball gird array
TSOP	thin small outline package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
µA	microamperes
mA	milliampere
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

Document History Page

Document Title: CY62138EV30 MoBL® 2 Mbit (256K x 8) MoBL® Static RAM Document Number: 38-05577				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	237432	AJU	See ECN	New data sheet
*A	427817	NXR	See ECN	Removed 35 ns Speed Bin Removed “L” version Removed 32-pin TSOPII package from product Offering. Changed ball C3 from DNU to NC. Removed the redundant footnote on DNU. Moved Product Portfolio from Page # 3 to Page #2. Changed I_{CC} (Max) value from 2 mA to 2.5 mA and I_{CC} (Typ) value from 1.5 mA to 2 mA at f = 1 MHz Changed I_{CC} (Typ) value from 12 mA to 15 mA at f = f_{max}=1/t_{RC} Changed I_{SB1} and I_{SB2} Typ. values from 0.7 μA to 1 μA and Max. values from 2.5 μA to 7 μA. Changed V_{CC} stabilization time in footnote #7 from 100 μs to 200 μs Changed the AC test load capacitance from 50pF to 30pF on Page# 4 Changed V_{DR} from 1.5V to 1V on Page# 4. Changed I_{CCDR} from 1 μA to 3 μA in the Data Retention Characteristics table on Page # 4. Corrected t_R in Data Retention Characteristics from 100 μs to t_{RC} ns Changed t_{OHA}, t_{LZCE}, t_{LZWE} from 6 ns to 10 ns Changed t_{HZOE}, t_{HZCE}, t_{HZWE} from 15 ns to 18 ns Changed t_{LZOE} from 3 ns to 5 ns Changed t_{SCE} and t_{AW} from 40 ns to 35 ns Changed t_{SD} from 20 ns to 25 ns Changed t_{PWE} from 25 ns to 35 ns Updated the Ordering Information table and replaced Package Name column with Package Diagram.
*B	2604685	VKN/PYRS	11/12/08	Added footnote 7 related to I_{SB2} and I_{CCDR}
*C	3143896	RAME	01/17/2011	Updated Datasheet as per new template Added Ordering Code Definition Added Acronyms and Units of Measure table Converted all tablenotes to Footnote Updated Package Diagram 51-85149 from *C to *D

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