AND8020/D

Termination of ECL Logic Devices with EF (Emitter Follower) OUTPUT Structure

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APPLICATION NOTE

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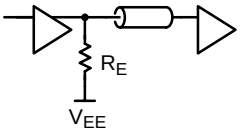

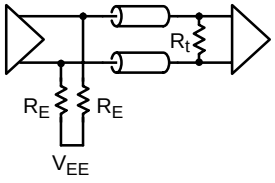

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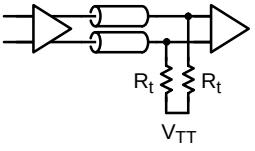

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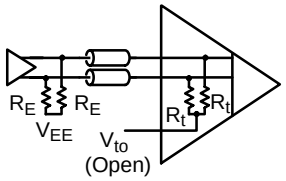

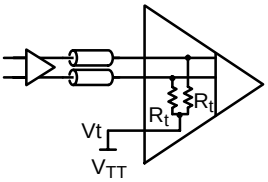

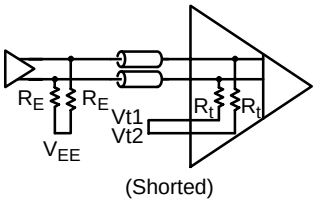

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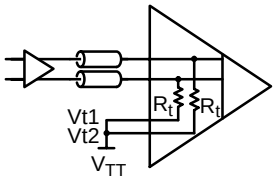

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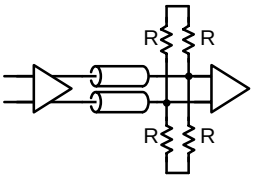
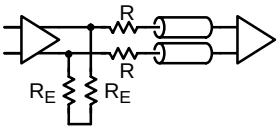
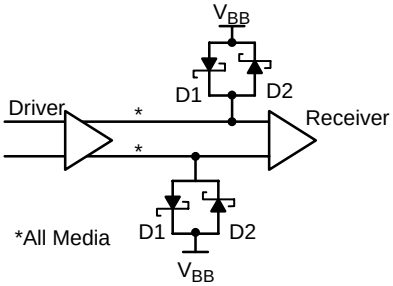
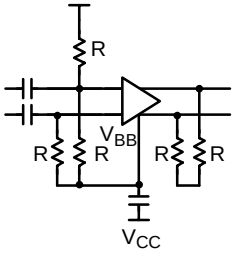








INTRODUCTION

Static DC Termination Analysis

A standard Emitter Coupled Logic (ECL) output driver typically uses a current switching differential with an emitter follower for level shifting the output and the internal CML levels to familiar ECL levels. This output driver architecture presents about 6−8 Ω internal impedance in both LOW and HIGH states when properly current biased. This results in a typical V_{PP} signal of 800 mV_{PP} (measured single−endedly on each line) swinging around a DC voltage point of $V_{CC} - 1.3$ V when properly terminated and operating correctly as shown in Figure 1.

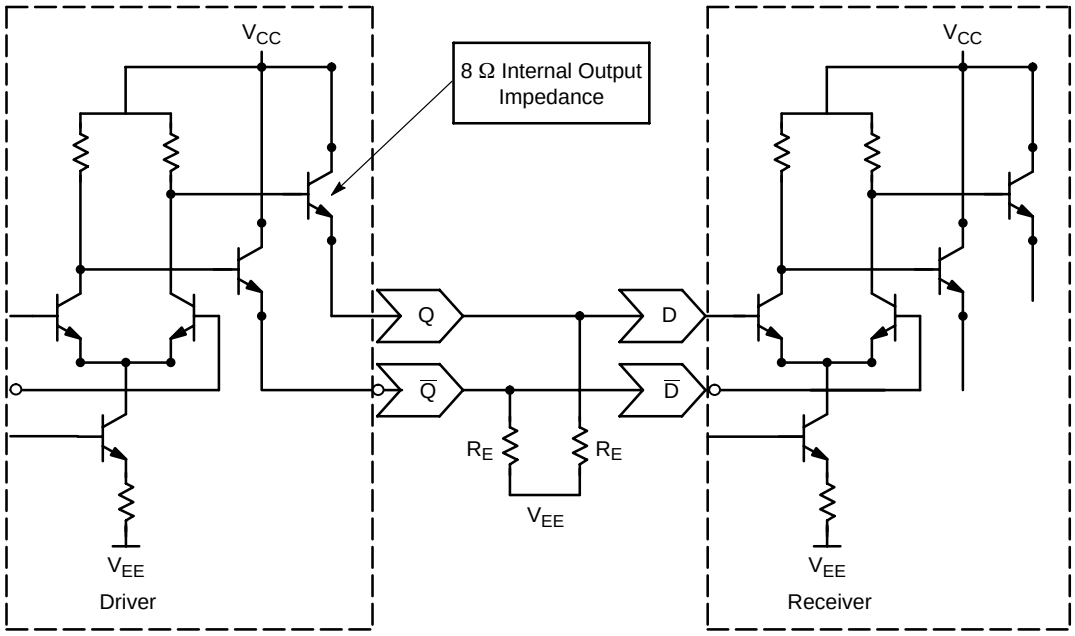


Figure 1. Typical ECL Output with Emitter Follower Output Structure, Typical Termination, and Typical ECL Input Interconnect

For proper static and dynamic operation, the output emitter follower transistor must remain in the active region of operation which requires an external resistive path be provided from the output pin to a voltage more negative than worst case V_{OL}, such as V_{EE}. The resistor, R_E, is considered a current bias for the Emitter Follower output structure.

When properly terminated and current biased (loaded), the outputs will generate both: (1) static state voltage levels V_{OL} (LOW) or V_{OH} (HIGH) and (2) a dynamic transition edge (tr or tf) between state levels.

Static State Voltage Levels

Figure 2 illustrates the typical relationship of static signal levels and dynamic transition edges between an Output Driver Signal and a Receiver Input Signal. Both outputs of a differential driver should always be terminated and loaded as identically as possible to preserve minimum skew and jitter operation of the device.

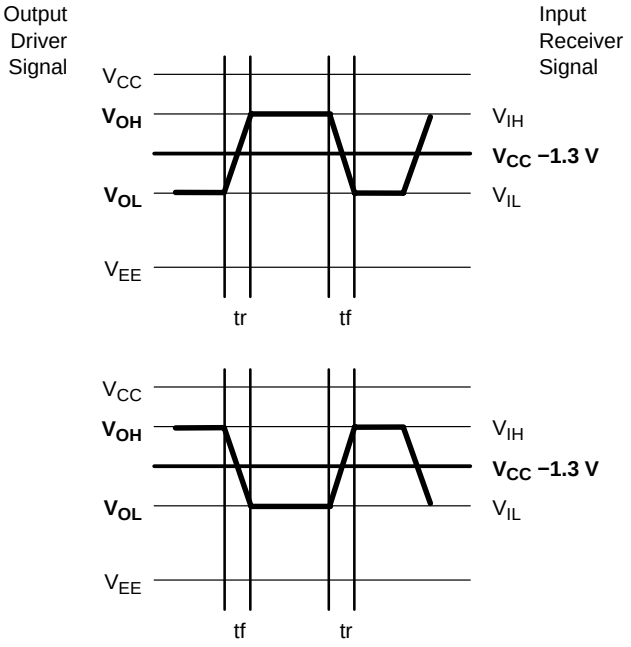


Figure 2. State Levels V_{OH}, V_{OL}, and Dynamic Transitions at Q or $\overline{Q}$ and D or $\overline{D}$

Output Open, Short, and Safe DC Current

Left open, an output will only swing a few millivolts due to parasitic “minimum current” leakage paths.

Shorted to V_{EE}, a maximum current will develop, limited only by the output transistor 8 Ω impedance, and *may cause damage to the output. Worst case short circuit current risks destruction of the devices*.

$$I_{SC} = \frac{V_{OH}}{R_{INT}} = \frac{4\ V}{8\ \Omega} \qquad \text{(eq. 1)}$$

= 500 mA!

Where:

V_{OH} = 4.0 V
V_{CC} = 5.0 V
V_{EE} = 0.0 V
R_{int} = 8 Ω

The continuous safe output current, I_{out} (continuous), maximum limit is 50 mA under all spec operating conditions. The continuous safe repetitive surge, I_{out} (surge), maximum current limit is 100 mA for 10 milliseconds per second duty cycle, provided the device’s total thermal limits are observed. Output current polarity will always be sinking into the termination scheme during proper operation.

Static Analysis of Termination Resistor R_E

The output continuous safe current limit, I_{out} (cont), determines R_E minimum DC termination scheme resistance to V_{EE} although this will not provide a practical AC signal termination as shown in Table A: Minimum R_E Values.

$$R_E = \frac{V_{OH}}{I_{max}} \qquad \text{(eq. 2)}$$

Table A. Minimum R_E Values

Line	V_{OH}	R_E(min)
PECL	4.0 V	80 Ω
LVPECL	2.4 V	48 Ω
LVEP PECL	1.6 V	32 Ω

A DC terminating resistor minimum, R_E (min), of 80 Ω, while sufficiently limiting the output load current to V_{EE}, may generate insufficient PECL output LOW and HIGH state transitions.

The R_E maximum is effectively determined by the application load capacitance, C_L, since an RC network is formed by R_E and C_L which limits the signal fall time, discharging the line to the LOW state voltage level. A sufficiently high value R_E or C_L can cause the signal fall time to the V_{OL} level to violate specification limits. Designed R_E or C_L values may selectively eliminate undesirable noise.

Dynamic Analysis of Termination Resistor R_E

The dynamic function of the termination resistor, R_E is to develop the voltage change, ΔV, during a high−to−low or low−to−high transition and present this to the transmission medium such as coax, twisted pair, microstrip or stripline. The ΔV signal propagates to the receiver and is either reflected, dissipated, or a combination.

Since the reflection coefficient at the load is of opposite polarity to that of the source, a reflection will travel back and forth over the transmission changing polarity after each reflection until critically damped by line impedance. Thus, steps may appear in the signal ΔV at the receiving gate input due to impedance mismatch and consequent partial reflections.

When R_E is too large, steps appear in the trailing edge of the propagating signal, ΔV, at the input to the receiving gate, slowing the edge speed and increasing the net propagation delay. A reasonable negative−going signal swing at the input of the receiving gate results when the value of R_E is selected to produce an initial step of 75% of the expected ΔV, or a 600 mV step for an 800 mV signal at the driving gate. For a RSECL expected ΔV swing of 400, a 300 mV initial step is desired. Hence for a 600 mV initial step:

$$I(init) * Z_0 > 0.6$$

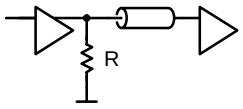
$$\frac{(V_{OH} - V_{EE})}{(R_t + Z_0)} * Z_0 \geqq 0.6 \qquad \text{(eq. 3)}$$

The value for R_E is found in Table B: Recommended Values of R_E in Dynamic Functional Application. This table lists recommended R_E values for the various ECL devices by Family Series according to the equation above. The table assumes operation with various data sheet V_{OH} values and various V_{CC} values driving a Z_0 = 50 Ω line. Lowering the value of R_E will increase the voltage change, ΔV, launched into the transmission media. Raising the value of R_E will decrease the voltage change, ΔV, launched into the transmission media.

Table B. Recommended Nominal Values of R_E in Dynamic Functional Application

Series	$\lvert V_{CC}-V_{EE}\rvert$	R_E (Ω)
NB	2.5	140
NB	3.3	250
10/100LVEP	2.5	50
10/100EP, 100LVEL	3.3	120
10/100EL, 10/100E	5.0	235

SECTION 1. UNTERMINATED LINES



From transmission line theory, when the driver R_E develops a ΔV swing, the signal propagates from point A arriving at point B at time Td later as shown in Figure 3. This configuration is also referred to as a stub or an open line.

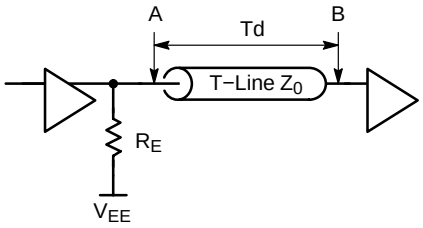


Figure 3. Unterminated Transmission Line Stub

At point B, the signal is reflected as a function of ρ_L. If the input impedance of the receiving gate is large relative to the line characteristic impedance, according to Equation 4:

$$\rho_L = \frac{(R_L - Z_0)}{(R_L + Z_0)} \qquad \text{(eq. 4)}$$

Where:

ρ_L = Load Reflection Coefficient
R_L = Load Impedance
Z_0 = Line Characteristic Impedance

A large positive reflection occurs resulting in overshoot. The reflected signal reaches point A at time 2Td , and a large negative reflection results because the output impedance of the driver gate is much less than the line characteristic impedance (i.e. $R_O << Z_0$).

When the reflected signal arrives at the source it is reflected back toward the load with a magnitude dictated by the source reflection coefficient:

$$\rho_S = \frac{(R_S - Z_0)}{(R_S + Z_0)} \qquad \text{(eq. 5)}$$

Where:

ρ_S = Source Reflection Coefficient
R_L = Source Impedance
Z_0 = Line Characteristic Impedance

The reflected signal continues to be reflected by the source and load impedances and is attenuated with each passage over the transmission line. The output response appears as a damped oscillation asymptotically approaching a steady state value. This phenomena is often referred to as “ringing.”

The importance of minimizing the reflected signals lies in their adverse affect on noise margin and the potential for driving the input transistors of the succeeding stage into saturation. Both of these phenomena can lead to less than ideal system performance. To maximize signal integrity on transmission lines, four basic techniques are available:

1. Minimizing Interconnect Line Lengths (Section 1)
2. Parallel Termination (Sections 2 and 3)
3. Series Termination (Section 4)
4. Diode Termination (Section 5)

Interconnect Line Lengths

The output signal Waveform rise (tr) and fall (tf) time are measured from the 20% and 80% levels of the static signal levels. This edge rate represents the waveforms highest harmonic and determines the maximum unterminated open line trace length, L_{max}, permissible without sustaining signal reflections.

The impetus in restricting interconnect lengths, L, is to mitigate the effects of overshoot and undershoot. A handy rule of thumb is that the undershoot can be limited to less than 15% of the logic swing if the two way line delay is less than the rise time of the pulse. With an undershoot of <15%, the physics of the situation will result in an overshoot which will not cause saturation problems at the receiving input. Thus, the maximum line length can be determined:

$$L_{max} < \frac{t_r}{2 * T_{pd}} \qquad \text{(eq. 6)}$$

Where:

L_{max} = Maximum Open Line Length
t_r = Signal Rise Time
T_{pd} = Length Pulse Delay per Unit Length

Further, the propagation delay increases with gate loading; thus, the effective delay per unit length (T_{pdEff}) is given as:

$$T_{pdEff} = T_{pd}\sqrt{1 + \frac{C_D}{L * C_O}} \qquad \text{(eq. 7)}$$

Where:

T_{pd} = Length Pulse Delay per Unit Length
C_D = Distributed Capacitance
C_O = Capacitance per Unit Length (Foot)
L = Line Length

Using the effective delay per unit length, $Tpd_{Eff,}$ yields:

$$t_r \geqq (2)\,(L)\,(T_{pd})\sqrt{1 + \frac{C_D}{L * C_O}} \qquad \text{(eq. 8)}$$

Solving for L_{max} line length produces:

$$L_{max} = 0.5\sqrt{\left(\frac{C_D}{C_O}\right)^2 + \left(\frac{t_r}{t_{pd}}\right)^2} - \frac{C_D}{C_O} \qquad \text{(eq. 9)}$$

Where:

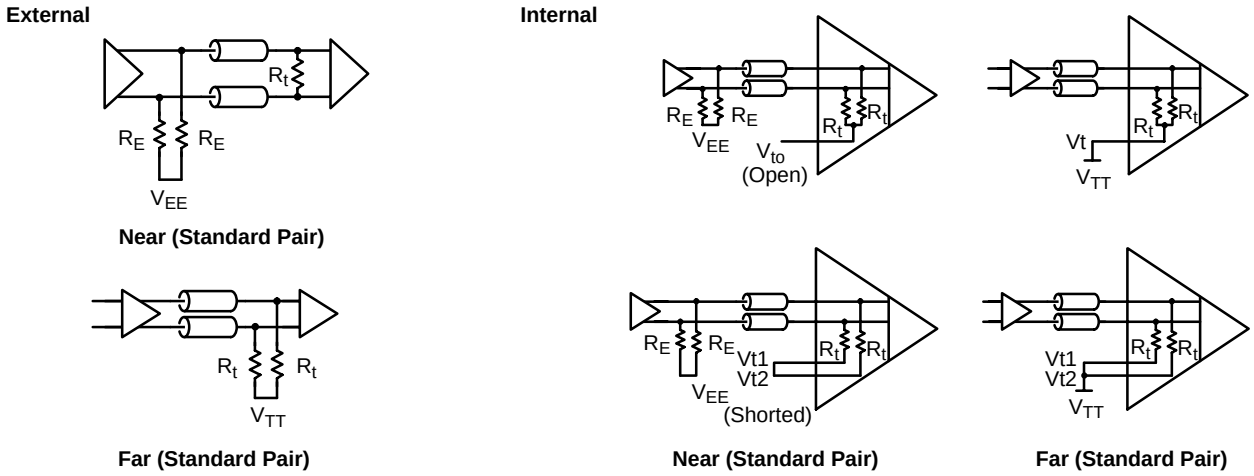
L_{max} = Line Length Maximum
C_D = Distributed Capacitance
C_O = Capacitance per Unit Length (Foot)
T_{pd} = Length Pulse Delay per Unit Length

Assuming a worst case capacitance of 2 pF and a rise time of 100 ps for EP gives a value of 0.03 inch for the maximum open line length. Maximum open line lengths derived from SPICE simulations for single and double gate loads, a maximum overshoot of 40% and undershoot of 20% was assumed. The simulation results indicate that for a 50 Ω line, a stub length of ≦ 0.03 inches will limit the overshoot to less than 40%, and the undershoot to within 20% of the logic swing. Signal traces will most assuredly be larger than 0.03 inch for most practical applications.

Therefore, it will be necessary to use controlled impedance environments for EP devices in general and devices with faster edges.

TERMINATION OF ECL LOGIC DEVICES

SECTION 2. PARALLEL TERMINATION − EXTERNAL AND INTERNAL



Parallel termination advantages:

- Method of choice for best circuit performance
- Particularly excellent for driving distributed loads
- Undistorted waveform along the full length of the line
- Decreased power consumption.

Far DC Current Return − V_{TT}

A parallel terminated line is one in which the receiving end is signal terminated internally or externally (usually to a voltage V_{TT}) through a resistor (R_t) with a value equal to the line characteristic impedance (Figure 4). This line also carries the biasing current for the drivers output far from the driver. Output current and power dissipation is decreased due to use of a V_{TT} termination supply. The V_{TT} supply must sustain the emitter follower output transistor in its active operating region under all operating conditions. A minimum continuous current occurs for the most negative V_{OL}, therefore the V_{TT} supply must remain more negative than the worst case V_{OLmin} and always sink current.

Standard V_{TT} is 2.0 V below V_{CC} supply. A parallel resistor, R_t, matching the controlled impedance transmission line, Z_0, connects the signal to the V_{TT} supply. The Parallel Termination to V_{TT} is shown in Figure 4. The termination resistors may be internal or external and either ganged into a Combo pin or offered as Singulated pins. Some devices may have each internal resistors independently pinned out, allowing further termination versatility.

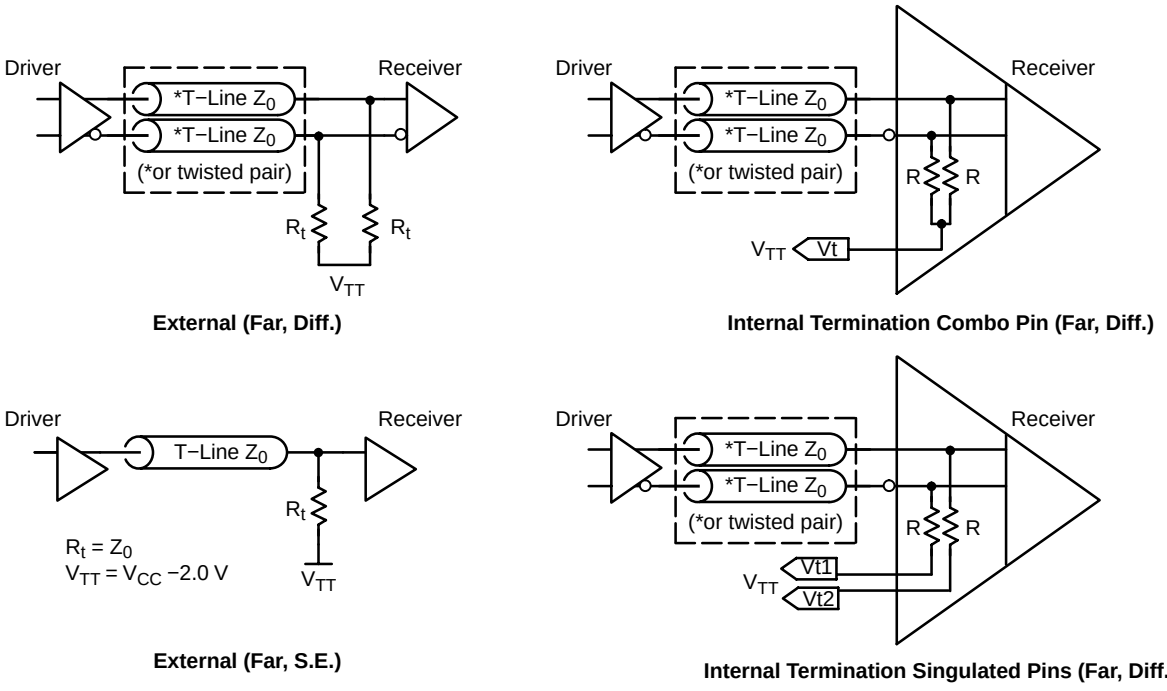


Figure 4. Parallel Termination to V_{TT} − Differential and Single−Ended with Combo or Singulated Vt Pins (Far Return)

Internal Termination Resistors

Internal termination conveniently uses 50 Ω values for R_t, with the most popular being Z_0. Note the internal termination allows the Combo Pin node, V_t, from the internal resistors to be connected to an external V_{TT} supply, typically at $V_{CC} - 2.0$ V, as shown in Figure 5. Alternatively, this Combo Pin may be pulled to V_{EE} through an external resistor to form a "Y" type termination variant, as shown in Figure 5. See the "Y Variance" topic and the "Y Term Table" for R_{t3} resistor values.

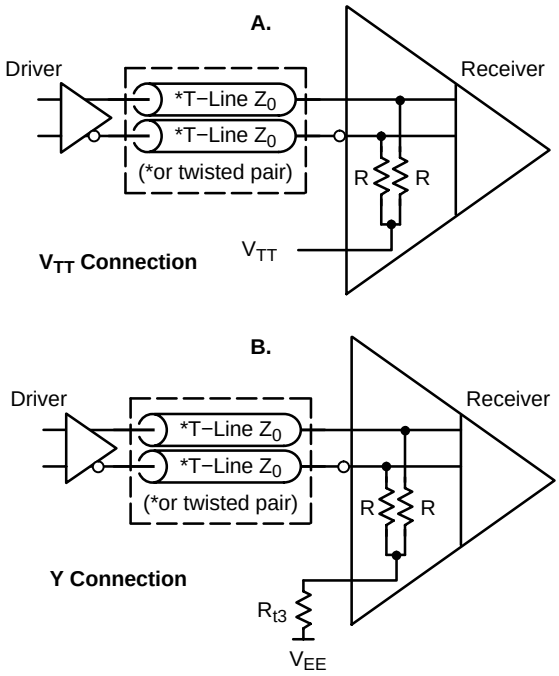


Figure 5. Combo Pin V_{TT} or "Y" Connection with Internal Parallel Termination

Example Calculations

Ideally, V_{TT} supply tracks 1:1 with V_{CC}; however, supply tolerances need to be considered. Assume for instance a MC10EP16, +85°C, nominal +3.3 V_{CC}, terminated 50 Ω (R_t) to V_{TT}, where V_{TT} is $V_{CC} - 2.0$ V, or 1.3 V:

$$I_{OHmax} \text{ of } (V_{CC}) - 0.885 \text{ V}$$

$$I_{OLmin} \text{ of } (V_{CC}) - 1.685 \text{ V}$$

resulting in the nominal case:

$$I_{OHmax} = \frac{(V_{OHmax} - V_{TT})}{R_t}$$

$$\frac{(3.3 - 0.885) - 1.3}{50} = 22.3 \text{ mA}$$

$$I_{OLmin} = \frac{(V_{OLmin} - V_{TT})}{R_t}$$

$$\frac{(3.3 - 1.685) - 1.3}{50} = 6.3 \text{ mA}$$

If +5% tolerances are assumed, two worst case conditions result.

Case #1: $V_{CC}min = V_{CC} - 5\%$, $V_{TT}max = V_{TT} + 5\%$

$$I_{OHmax} = \frac{(V_{OHmax} - V_{TT})}{R_t}$$

$$\frac{((3.135 - 0.885) - 1.365)}{50} = 17.7 \text{ mA}$$

$$I_{OLmin} = \frac{(V_{OLmin} - V_{TT})}{R_t}$$

$$\frac{((3.135 - 1.685) - 1.365)}{50} = 1.7 \text{ mA}$$

Case #2: $V_{CCmin} + 5\%$, $V_{TTmax} - 5\%$

$$I_{OHmax} = \frac{(V_{OHmax} - V_{TT})}{R_t}$$

$$\frac{((3.465 - 0.885) - 1.235)}{50} = 26.9 \text{ mA}$$

$$I_{OLmin} = \frac{(V_{OLmin} - V_{TT})}{R_t}$$

$$\frac{((3.465 - 1.685) - 1.235)}{50} = 1.09 \text{ mA}$$

Y Variance

The "Y" termination for a differential pair may be preferred when avoiding the use of a V_{TT} supply. The design is shown in Figure 6 and utilizes the following formulas for calculating resistor values which are found in the Y Term Table. The voltage at the Node where R_{t1}, R_{t2}, and R_{t3} connect remains at a static V_{TT} voltage of $V_{CC} - 2.0$ V, or 1.3 V.

$$R_{t1} = R_{t2} = Z_0 \quad \text{(eq. 10)}$$

$$R_{t3} = R_{t1}\left(\frac{V_{TT} - V_{EE}}{V_{OH} + V_{OL} - 2V_{TT}}\right) \quad \text{(eq. 11)}$$

$$V_{TT} = \frac{R_{t3}(V_{OH} + V_{OL}) + (R_{t1} * V_{EE})}{R_{t1} + 2R_{t3}} \quad \text{(eq. 12)}$$

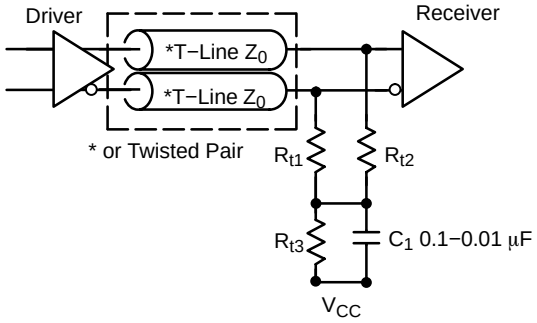


Figure 6. "Y" Variance

Table C. Y Term Table

$\lvert V_{CC}-V_{EE}\rvert$ = 5.0 V				$\lvert V_{CC}-V_{EE}\rvert$ = 3.3 V				$\lvert V_{CC}-V_{EE}\rvert$ = 2.5 V			
Z_0	R_{t1}	R_{t2}	R_{t3}	Z_0	R_{t1}	R_{t2}	R_{t3}	Z_0	R_{t1}	R_{t2}	R_{t3}
50	50	50	112	50	50	50	46	50	50	50	21.2
70	70	70	156	70	70	70	64	70	70	70	29.7
75	75	75	166	75	75	75	68	75	75	75	31.8
80	80	80	179	80	80	80	72	80	80	80	33.9
90	90	90	201	90	90	90	82	90	90	90	38.1
100	100	100	223	100	100	100	91	100	100	100	42.4
120	120	120	268	120	120	120	109	120	120	120	50.8
150	150	150	335	150	150	150	136	150	150	150	63.6

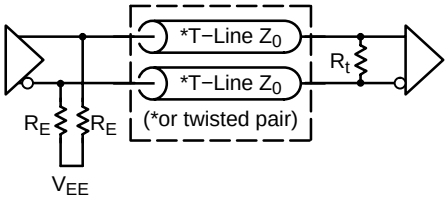


Figure 7. Standard Pair with External Parallel

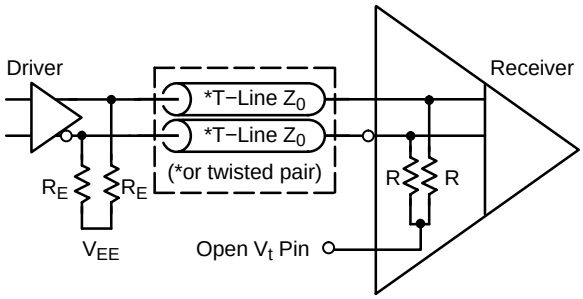
Near DC Current Return − Standard Pair Termination

The standard pair termination scheme uses a pull−down resistor, R_E, located at each driver pin to return the output transistor bias current near the driver, and an impedance matching parallel resistor, R_T, located at the receiver input pins (see Figure 7, standard pair with external parallel, and Figure 8, standard pair termination with internal termination, and Figure 9, standard pair termination with singulated internal termination resistors). The impedance matching parallel resistor may be internal or external depending on the receiver device. If internal to the receiver, the resistor may be singulated or combined (“combo”) for external pinout.

The diagram of Figure 7 shows a Standard Pair Termination with an R_E resistor for DC output current bias located nearby each driver pin: refer to Table B, for values of R_E. The differential transmission line AC impedance matching resistance, R_t, is located externally near the receiver input pins.

As a variation of a Standard Pair Termination, a receiver may provide the differential transmission line AC impedance matching resistance, R_t, internally. This internal impedance matching termination may be pinned out either combined into a Combo V_t pin or each resistor may be singulated and pinned out, such as V_{t1} and V_{t2}.

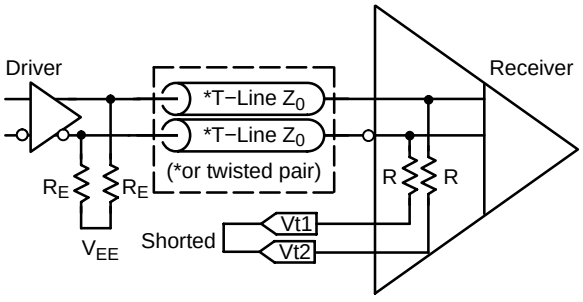
When left open, the Combo Pin still provides a passive 100 Ω termination across the nearby receiver’s differential signal line pair. This can compliment a pull−down resistor, R_E, located on each line of a differential at the driver pins. This is illustrated in Figure 8.



Internal Termination Combo Pin

Figure 8. Standard Pair Termination with Internal Termination

When the Internal Termination resistors are singulated, the two V_t pins must be shorted to create the 100 Ω value as shown in Figure 9.

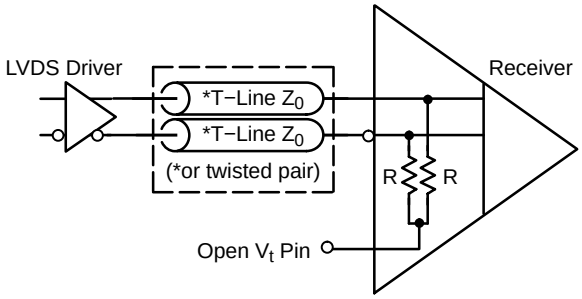


Internal Termination Singulated Pins

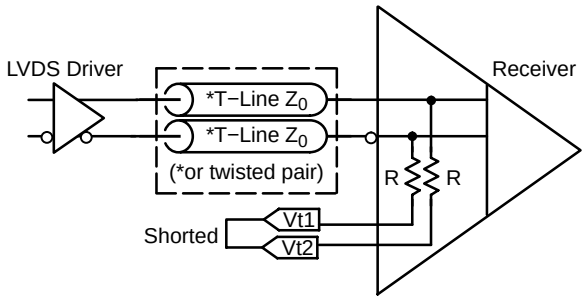
Figure 9. Standard Pair Termination with Singulated Internal Termination Resistors

Internal 100 Ω Termination (LVDS)

For some technologies, such as LVDS, this passive 100 Ω internal termination can provide sufficient termination for the driver as shown in Figure 10. Devices with a Combo Pin will require this pin to remain open, while devices with singulated internal resistors require the two pinned out V_t nodes for a differential pair to be shorted together to provide the 100 Ω termination.



Internal Termination Combo Pin



Internal Termination Singulated Pins

Figure 10. LVDS Interconnect with Internal Termination

Differential ECL outputs can be terminated as independent complimentary single−ended lines. Both sides of any differential pair must be terminated as identically as possible to minimize phase error and pulse width duty cycle skew.

The I_{OH} currents in these two cases will vary the DC V_{OH} levels by ± 40 mV. However in the vast majority of cases, DC levels are well centered in their specification windows, thus this variation will simply move the level within the valid specification window and no loss of worst case noise margin will be seen.

The I_{OL} situation on the other hand does pose a potential AC problem. In the worst Case #1 I_{OLmin} situation, the output emitter follower could move into the cutoff state (0 mA). The output emitter followers of ECL devices are designed to be in the conducting, active region of operation at all times. When forced into cutoff, the delay of the device will be increased due to the extra time required to pull the output emitter follower out of the cutoff state. Again, this situation will arise only under a number of simultaneous worst case situations and therefore, is highly unlikely to occur. But, because of the potential, it should not be overlooked.

Output Drive Characteristics

Figure 11 shows the nominal output characteristics for ECL devices operating in negative ECL mode, driving various load impedances (including the standard 50 Ω) returned to a negative two volt supply. The output resistances, RH (high state output resistance) and RL (low state output resistance), are obtained from the reciprocal of the slope at the desired operating point. Many applications require loads other than 50 Ω − the resulting V_{OH} and V_{OL} levels can be estimated using the following technique.

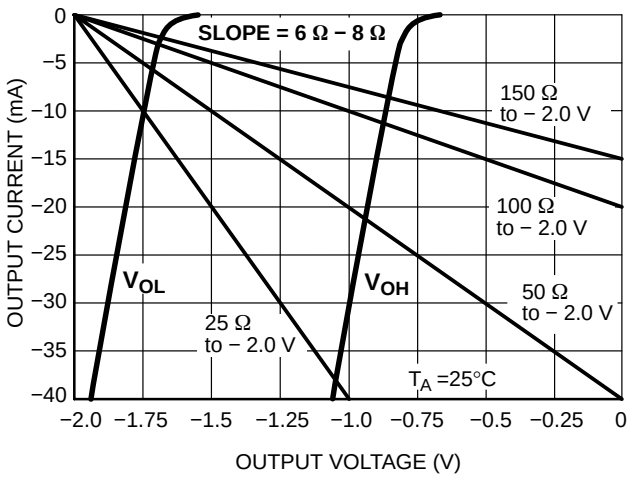
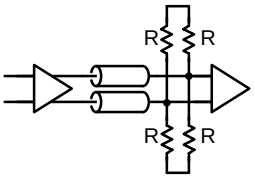
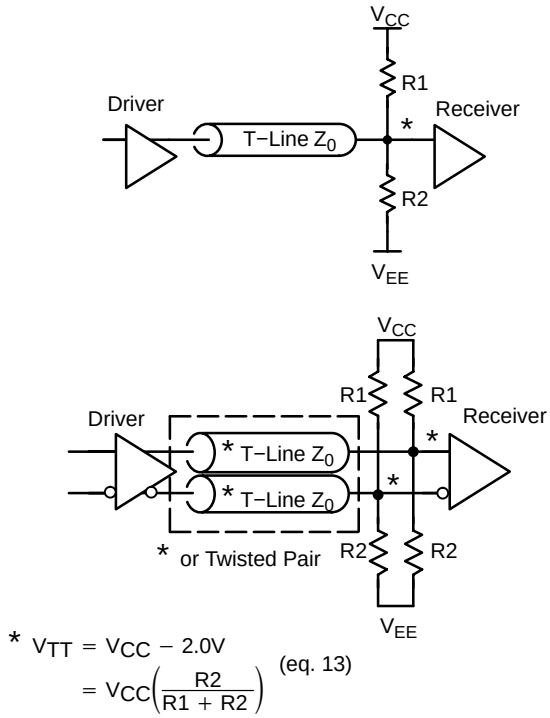


Figure 11. Normal Output Levels Driving Various Load Impedances

SECTION 3. THEVENIN EQUIVALENT PARALLEL TERMINATION



Although the single resistor termination to V_{TT} conserves power, it requires an additional supply voltage. An alternate approach to using a V_{TT} power supply is to use a resistor divider network as shown in Figure 12 to develop a Thevenin voltage, V_{TT}, and provide a parallel impedance matching AC termination, the Thevenin parallel termination.



* $V_{TT} = V_{CC} - 2.0V$
$= V_{CC}\left(\frac{R2}{R1 + R2}\right)$ (eq. 13)

Figure 12. Thevenin Equivalent Parallel Termination

Differential ECL outputs can be terminated as independent complimentary single−ended lines. Both sides of a differential pair must be terminated. Balanced, symmetrical loading of each line must be preserved.

While a Thevenin Parallel technique dissipates more termination power, it does not require the additional V_{TT} supply. This additional power is consumed entirely in the external resistor divider network and thus will not change the current being sourced by the device, hence it does not alter the IC reliability or lifetime. As with standard parallel termination, variance of V_{TT} and V_{CC} supplies must be considered.

The Thevenin equivalent of the two resistors needs to be equal to the characteristic impedance of the signal transmission line. Calculated values for resistors R1 and R2 may be obtained from the following relationships.

$$R2 = Z_0\left(\frac{V_{CC} - V_{EE}}{V_{CC} - V_{TT}}\right) \quad \text{(eq. 14)}$$

$$R1 = R2\left(\frac{V_{CC} - V_{TT}}{V_{TT} - V_{EE}}\right) \quad \text{(eq. 15)}$$

Where:

$V_{TT} = V_{CC} - 2.0$ V
Z_0 = Characteristic Impedance of the Signal Transmission Line

For a typical V_{CC} = 5.0 V PECL scheme, where V_{EE} = GND, V_{TT} = 3.0 V, and Z_0 = 50 Ω:

$$R2 = 50\left(\frac{5 - 0}{5 - 3}\right) = 125\ \Omega \quad \text{(eq. 16)}$$

$$R1 = 125\left(\frac{5 - 3}{3 - 0}\right) = 83.3\ \Omega \quad \text{(eq. 17)}$$

and cross−checking for V_{TT}:

$$V_{TT} = 5\left(\frac{125}{125 + 83.3}\right) = 3.0\ V \quad \text{(eq. 18)}$$

$$V_{TT} = V_{CC} - 2.0\ V = 3.0\ V \quad \text{(eq. 19)}$$

For the typical V_{CC} = 3.3 V LVPECL scheme, where V_{EE} = GND, V_{TT} = 1.3 V, and Z_0 = 50 Ω:

$$R2 = 50\left(\frac{3.3 - 0}{3.3 - 1.3}\right) = 82.5\ \Omega \quad \text{(eq. 20)}$$

$$R1 = 82.5\left(\frac{3.3 - 1.3}{1.3 - 0}\right) = 126\ \Omega \quad \text{(eq. 21)}$$

and cross−checking for V_{TT}:

$$V_{TT} = 3.3\left(\frac{82.5}{126 + 82.5}\right) = 1.3\ V \quad \text{(eq. 22)}$$

$$V_{TT} = V_{CC} - 2.0\ V = 1.3\ V \quad \text{(eq. 23)}$$

Table D. Thevenin Term Table

$\lvert V_{CC}-V_{EE}\rvert$ = 5.0 V			$\lvert V_{CC}-V_{EE}\rvert$ = 3.3 V			$\lvert V_{CC}-V_{EE}\rvert$ = 2.5 V		
Z_0	R1	R2	Z_0	R1	R2	Z_0	R1	R2
50	83	125	50	127	83	50	250	62.5
70	117	175	70	178	115	70	350	87.5
75	125	188	75	190	123	75	375	93.8
80	133	200	80	203	132	80	400	100
90	150	225	90	229	149	90	450	112.5
100	167	250	100	253	165	100	500	125.5
120	200	300	120	305	198	120	600	150
150	250	375	150	381	248	150	750	187.5

Because the resistor divider network of R1 and R2 is used to generate V_{TT}, the variation in V_{TT} will be intimately tied to the variation in V_{CC}. Differentiating the equation for V_{TT} with respect to V_{CC} yields:

$$\frac{\Delta V_{TT}}{\Delta V_{CC}} = \frac{R2}{(R1 + R2)} \Delta V_{CC} \quad \text{(eq. 24)}$$

For the nominal case, this equation reduces to:

$$\Delta V_{TT} = 0.6\, \Delta V_{CC} \quad \text{(eq. 25)}$$

If $\Delta V_{CC} = \pm 5\% = \pm 0.25$ V, then $\Delta V_{TT} = \pm 0.15$ V.

As mentioned previously, the real potential for problems will be if the V_{OL} level can potentially put the output emitter follower out of the active operating region and into cutoff. Because of the relationship between the V_{CC} and V_{TT} levels, the only cutoff risk condition occurs at V_{CCmin}, the lowest value of V_{CC}. Applying the equation for I_{OLmin} under this −5% V_{CC} condition yields:

$$I_{OLmin} = \frac{(V_{OLmin} - V_{TT})}{R_t} \quad \text{(eq. 26)}$$

$$I_{OLmin} = \frac{(4.75 - 1.85) - 2.85}{50} = 1.0\ \text{mA} \quad \text{(eq. 27)}$$

The results of this cutoff risk analysis show there is no potential for the output emitter follower to be in cutoff. This would indicate a Thevenin equivalent termination scheme is more robust to variation in V_{CC}. Since the designer has the flexibility of choosing the V_{TT} level via the selection of the R1 and R2 resistors, the following procedure can be used.

At −5% minimal variation case for V_{CC}:

$V_{CC} = 4.75$ V

$V_{TT} = V_{CC} - 2.0$ V = 2.75 V

R2 = 119 Ω

R1 = 86 Ω

Thus:

$I_{OHmax} = 23$ mA

$I_{OLmin} = 3.0$ mA

At +5% minimal variation case for V_{CC}:

$V_{CC} = 5.25$ V

$V_{TT} = 3.05$ V

Thus:

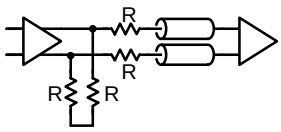
$I_{OHmax} = 28$ mA

$I_{OLmin} = 5.2$ mA

Although the output currents are slightly higher than nominal, the elimination of emitter follower cutoff risk is well justified.

When the equivalent termination resistance matches the line impedance, no reflection occurs because all the energy in the signal is dissipated by the termination. Hence, in comparing properly terminated schemes parallel and Thevenin, a primary consideration is the power supply requirements. As mentioned earlier, the parallel V_{TT} scheme requires an extra power supply; however, the Thevenin termination dissipates 10 times more DC power. Fortunately, this extra power dissipation cannot be seen on the die; therefore, either technique results in similar die junction temperatures.

SECTION 4. SERIES TERMINATION



Series Damping is a technique in which a termination resistance is placed between the driver and the transmission line with no termination resistance placed at the receiving end of the line (Figure 13).

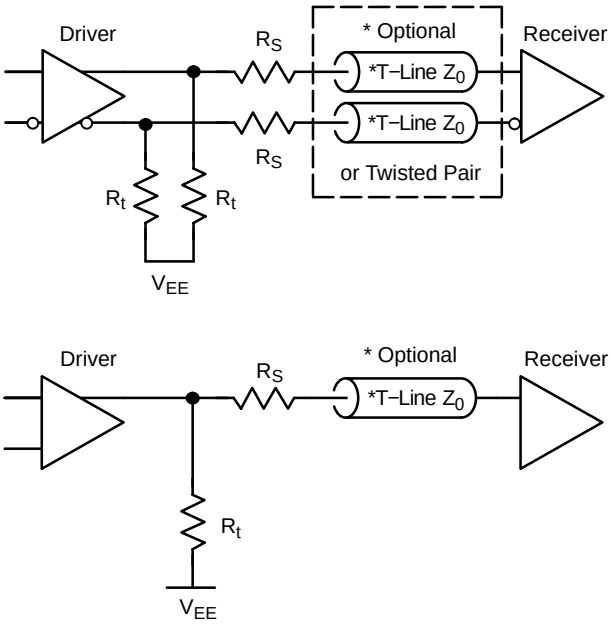


Figure 13. Series Termination

Differential ECL outputs can be terminated as independent complimentary single−ended lines. Both sides of any differential pair must be terminated as identically as possible to minimize phase error and pulse width duty cycle skew.

Series Termination is a special case of series damping in which the sum of the termination resistor (R_S) and the output impedance of the Driver gate (R_O) is equal to the line characteristic impedance (Figure 14).

$$R_S + R_O = Z_0 \qquad \text{(eq. 28)}$$

Where:

R_S = Series Termination Resistor
R_O = Output Impedance
Z_0 = Line Characteristic Impedance

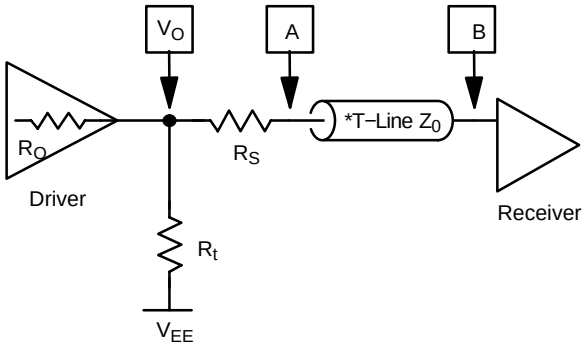


Figure 14. Series Termination

Series termination techniques are useful when the interconnect lengths are long or impedance discontinuities exist on the line. Additionally, the signal travels down the line at half amplitude minimizing problems associated with crosstalk. Unfortunately, a drawback with this technique is the possibility of a two−step signal appearing when the driven inputs are far from the end of the transmission line. To avoid this problem, the distance between the end of the transmission line and input gates should adhere to the guidelines specified from the section on unterminated lines.

Series Termination Theory

When the output of the series terminated driver gate switches levels, this driver output voltage change, ΔV_O, is impressed on the input to the transmission line (Point A) as a change in voltage (ΔV_A) and propagates to the Receiver at the output of the transmission line (Point B) as a change in voltage (ΔV_B) in Figure 14.

$$\Delta V_A = \Delta V_O * \left(\frac{Z_0}{R_S + R_O + Z_0}\right) \qquad \text{(eq. 29)}$$

Where:

ΔV_A = Input to the Transmission Line Voltage Change
ΔV_B = Receiver Input Voltage Change
ΔV_O = Driver Output Voltage Change
Z_0 = Line Characteristic Impedance
R_O = Output Impedance of the Driver Gate
R_S = Termination Resistance

Since $Z_0 = R_S + R_O$, substitution into the above equations yields:

$$\Delta V_A = \frac{\Delta V_O}{2} \qquad \text{(eq. 30)}$$

From this relationship, $\Delta V_A = \Delta V_O / 2$, an incident wave of half amplitude propagates down the transmission line. At the Receivers input Point B, typically high impedance, the transmission line sees an unterminated open line and the signal reflection coefficient at the Receiver load is approximately unity. The reflection causes the voltage to double at the receiving end. When the reflected wave arrives back at the source end, its energy is dissipated by the series resistor. When the sum of the source and series impedance is equal to the characteristic impedance of the line, no further reflections occur.

Calculation of R_t

The Emitter Pull−Down Resistor, R_t, functions to establish V_{OH} and V_{OL} levels. Voltage transitions imposed on R_t propagate through R_S and Z_0 to a receiver. Negative voltage transition are current limited by R_t, R_S, and Z_0 when the driver output switches to the low state. The R_t value must maximize the negative voltage transition and prevent the output transistor from entering the cutoff operating region in a low state (Figure 15).

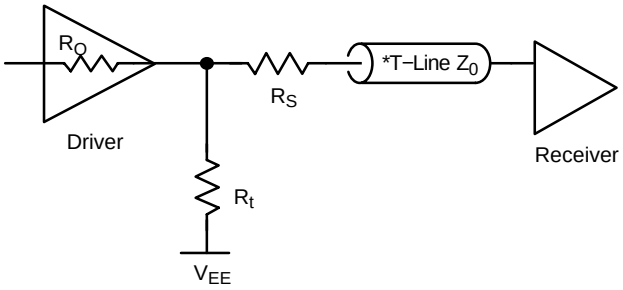


Figure 15. Equivalent Circuit for RE Determination

The worst case scenario occurs when the driver output emitter follower enters into cutoff during a negative going transition. When this happens, the driver can be considered opened and, at the instant it opens, the line characteristic impedance behaves as a linear resistor returned to V_{OH}. The model becomes a simple series resistive network as shown in Figure 16.

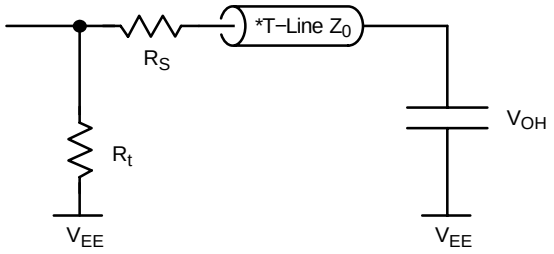


Figure 16. Equivalent Circuit with Output Cutoff

The maximum current, I_{max}, occurs at the instant the switch opens and is calculated by:

$$I_{max} = \frac{(V_{OH} - V_{EE})}{(R_t + R_S + Z_0)} \qquad \text{(eq. 31)}$$

An initial current, I_{init}, must be sufficient to generate a transient voltage equal to half of the logic swing since the voltage at the receiver will double due the reflection coefficient approaching 1.0 for series termination. To accommodate reflections caused by discontinuities and load capacitances the transient voltage should be increased by 25%. Thus, I_{init} is defined as:

$$I_{init} = \frac{\left(1.25 * \frac{V_{pp}}{2}\right)}{Z_0} \qquad \text{(eq. 32)}$$

To satisfy the initial constraints of $I_{max} > I_{init}$:

$$\frac{(V_{OH} - V_{EE})}{(R_t + R_S + Z_0)} > \frac{\left(1.25 * \frac{VSWING}{2}\right)}{Z_0} \qquad \text{(eq. 33)}$$

Solving for R_t, gives the inequality:

$$R_t \leq (KZ_0)\, Z_0 - R_S \qquad \text{(eq. 34)}$$

Where:

Z_0 = Line Characteristic Impedance
R_O = Output Impedance of the Driver Gate
R_S = Termination Resistance
KZ_0 = Coefficient to Z_0

For various series, the coefficient to Z_0, KZ_0, is presented in Table E: Coefficient to Z_0.

Table E. Coefficient to Z_0

Series	KZ_0
10EP	4.0
100LVEL	4.01
10EL	5.99
10E	7.10
100E	6.57

For the 10EP series (LVPECL mode operation), where V_{OH} = 2.4 V, V_{SWING} = 0.8 V, and V_{EE} = 0.0 V:

$$\frac{(2.4 - 0.0)}{(R_t + R_S + Z_0)} \geqq \frac{0.5}{Z_0} \qquad \text{(eq. 35)}$$

$$\mathbf{4.0} * Z_0 - R_S \geqq R_t$$

For the 100LVEL series (LVPECL mode operation), where: V_{OH} = 2.345 V, V_{SWING} = 0.750 V, V_{EE} = 0.0 V:

$$\frac{(2.345 - 0.0)}{(R_t + R_S + Z_0)} \geqq \frac{0.468}{Z_0} \qquad \text{(eq. 36)}$$

$$\mathbf{4.01} * Z_0 - R_S \geqq R_t$$

For the 10EL series (PECL mode operation), where: V_{OH} = 4.185 V, V_{SWING} = 0.958 V, V_{EE} = 0.0 V:

$$\frac{(4.185 - 0.0)}{(R_t + R_S + Z_0)} \geqq \frac{0.599}{Z_0} \qquad \text{(eq. 37)}$$

$$\mathbf{5.99} * Z_0 - R_S \geqq R_t$$

For the 10E series (ECL mode operation),
where: V_{OH} = −0.9 V, V_{SWING} = 0.85 V, V_{EE} = −5.2 V:

$$\frac{(-0.9)-(-5.2)}{R_t + R_S + Z_0} \geqq \frac{0.531}{Z_0} \quad \text{(eq. 38)}$$

$$\mathbf{7.10} * Z_0 - R_S \geqq R_t$$

For the 100E series (ECL mode operation),
where: V_{OH} = −0.955 V, V_{SWING} = 0.75 V, V_{EE} = −4.5 V:

$$\frac{(-0.955)-(-4.5)}{R_t + R_S + Z_0} \geqq \frac{0.468}{Z_0} \quad \text{(eq. 39)}$$

$$\mathbf{6.57} * Z_0 - R_S \geqq R_t$$

Parallel Fanout of Series Termination

An extension of the series termination technique, using parallel fanout, eliminates the problem of lumped loading at the expense of extra transmission lines (Figure 17).

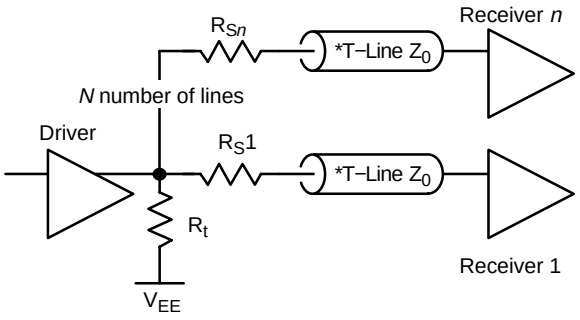


Figure 17. Parallel Fanout Using Series Termination

Figure 17 shows a modification of the series termination scheme in which several series terminated lines in parallel fanout are driven using a single ECL gate. The principle concern when applying this technique is to maintain the current in the output emitter follower below the maximum rated value. The value for R_t can be calculated by viewing the circuit in terms of conductances.

$$G_{output} > G1 + G2n + G \quad \text{(eq. 40)}$$

From Table B, for each of the series:

$$\frac{1}{(R_t)} \geqq \frac{1}{(\mathbf{KZ_0} * Z_01 - R_S1)} + \frac{1}{(\mathbf{KZ_0} * Z_02 - R_S2)} + \frac{1}{(\mathbf{KZ_0} * Z_0n - R_S)} \quad \text{(eq. 41)}$$

Where:

n = Number of Parallel Circuits

When:

$$Z_01 = Z_02 = Z_0 n, \text{ and } R_S1 = R_S2 = R_S n \quad \text{(eq. 42)}$$

Then R_t is calculated as:

$$R_t \geqq \frac{(KZ_0 * Z_0 - R_S)}{n} \quad \text{(eq. 43)}$$

When a single series terminated line is driving more than a single receiver, the maximum number of loads must be addressed. The factor limiting the number of loads is the DC voltage drop across the series termination resistor caused by the summary input currents I_T during the receivers quiescent high state. Noise margin loss, NM_{loss}, will probably determine the acceptable DC voltage drop limit across R_s.

$$NM_{loss} = I_T * (R_S = R_O) \quad \text{(eq. 44)}$$

Where:

I_T = Sum of IINH Currents
R_O = Output Impedance of the Driver Gate
R_S = Termination Resistance

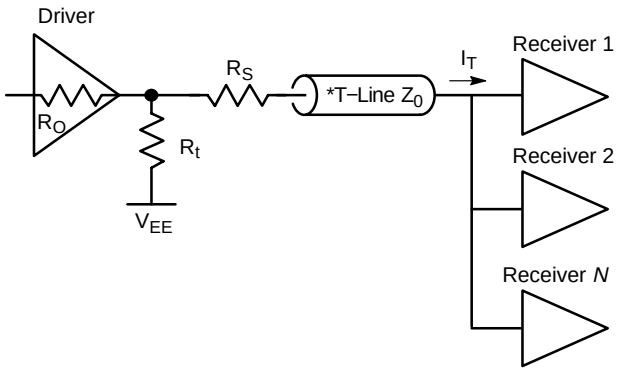


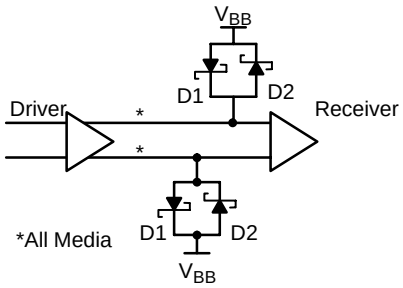
Figure 18. Noise Margin Loss Example

For the majority of ECL devices typical maximum value for quiescent high state input current is 150 uA. Thus, for the circuit shown in Figure 18, in which three gate loads are present in a 50 Ω environment, the loss in high state noise margin is calculated as:

$$NM_{loss} = 3 * -150\ mA * 50\ \Omega = -22.5\ mV \quad \text{(eq. 45)}$$

This represents a potential shift in the V_{OH} level of −22.5 mV.

SECTION 5. DIODE TERMINATION



Alternative to the resistor network termination schemes, a Diode method shown in Figure 19 may afford certain advantages when a design has the following constraints.

1. Impedance controlled media line is not required (coax, twisted pair, striplines, etc.)
2. Impedance matched termination network is not required.
3. Overshoot and Noise need to be clamped to logic HIGH/LOW levels.

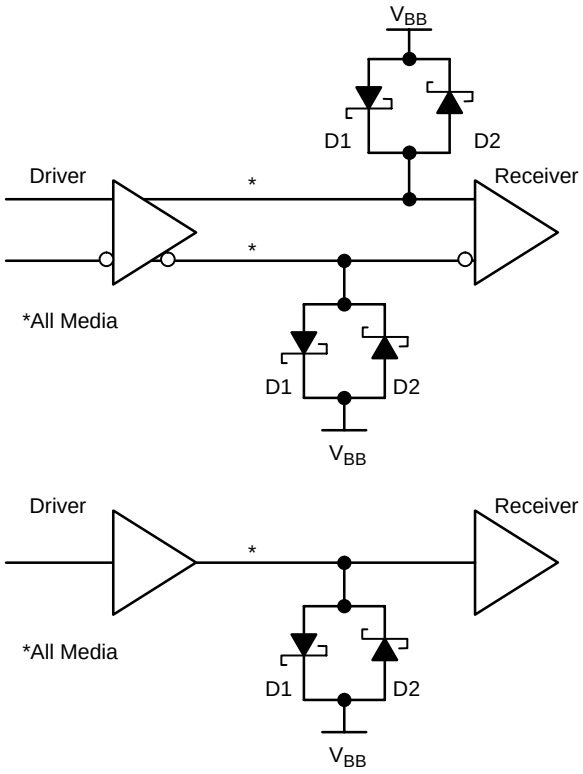


Figure 19. Diode Termination

D1 and D2 diodes may be an MBD301, MMBD301, MBD701, MMBD701LT1, or a dual package MMBD452LT1. Diode forward voltage curves from a data sheet, such as shown in Figure 20, will determine specific current and voltage operation range. Frequency limitations may be a consideration when selecting the diodes. The Silicon Hot−Carrier Schottky Barrier diode MBD701, for example, displays a forward V_f of about 0.55 V and an I_f of about 11 mA (at 25°C) to match a 50 Ω impedance line. At higher temperatures, the current decreases.

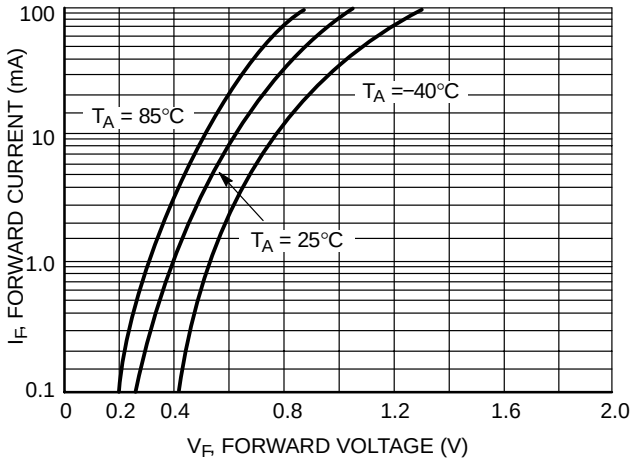
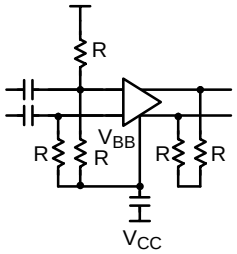


Figure 20. MMBD701 Diode Forward Voltage

SECTION 6. CAPACITIVE COUPLING



Although not strictly a termination, AC or capacitive coupling is often used to provide features in conjunction with proper termination. Such capabilities as hot swapping capability, DC isolation to a receiver, and level shifting are possible with capacitive coupling.

Data stream characteristics may impose restriction on both termination and capacitive coupling. AC coupled signals have the line DC blocked and will require a DC restoration voltage, V_{BIAS}, for the receiver input. Data in unencoded Non−Return−to−Zero (NRZ) format will require DC restoration prior to AC coupling into a ECL receiver input.

A sinusoidal waveform clock signal may be cap coupled for conversion to a square wave with 50% duty cycle and sharp rise and fall edges.

The capacitor used to couple the signal must have a impedance rating of < 50 Ω over the frequency range of the input signal. Because large capacitors appear somewhat inductive at high frequencies, it may be necessary to use a small capacitor in parallel with a larger one to achieve satisfactory operation.

A coupling capacitor and the signal load impedance form an RC network which will boundary the duration of a pulse. Values for the R (load and leakage total resistance) and C (coupling capacitor) should be selected to provide a time constant, T_C, of at least 10x the pulse width. Data streams may require larger T_C values to retain logic levels.

Hot Swapping

The desire often arises to remove or install a receiver or daughter card without powering down the driver or motherboard. This is termed “Hot Swapping”.

Powered Driver and an Unpowered Receiver Damage Risk

Hot swapping presents a potential risk to an unpowered or powered down ECL device receiver and driver in either the Negative or Positive mode when driven by a typical signal level.

When a receiver PECL receiver V_{CC} is off or powered down, the V_{CC} Power Supply typically appears as a low impedance source at 0.0 V capable of sinking considerable current. Typical driver signal levels present voltages that forward bias the input ESD protection diode structure and the input base collector junction. Potentially lethal current paths may develop through forwarded junctions to V_{CC}.

There is also a risk for a powered down or off NECL or LVNECL receiver and driver. A V_{EE} supply will typically appear as a low impedance path to 0.0 V (GND). Typical negative levels present signal voltages that will forward bias the input ESD protection diode structure and the input base collector junction to this low impedance path. Potentially lethal current paths may develop through the forwarded junctions and V_{EE} to 0.0 V.

Powered down receiver risk may be managed in several ways.

1. Physical Sequencing − the supplies for V_{EE} (Ground) and V_{CC} (Power) may be physically connected prior to signal lines by altering the daughter board edge connection geometry, making V_{EE} and V_{CC} connectors protrude and engage or sequence first. V_{EE} connectors could even be sequenced prior to V_{CC}. This insures the supplies are powered prior to input signal voltages.
2. Switching − a relay (or analog switch) could be used to open or close the supply lines insuring the power supply line is opened when powered off.
3. Cap Coupling − DC isolation of potentially damaging current.
4. Series R − an additional series impedance matching resistor, R_S, will act as power splitter with an existing parallel termination resistor, R_T, to accomplish some current limiting to help manage the risk. This will also attenuate the amplitude 50%, easily tolerated by most high gain, high input sensitivity devices.

Using V_{BB} Pin for V_{BIAS}

Some devices provide a convenient V_{BB} pin for use as a VBIAS reference supply to rebias a DC level. A DC rebias level must be at the common mode voltage of the input signal to properly preserve a 50% output duty cycle (see AND8066). A package V_{BB} pin may provide an internally generated DC switching reference voltage for the device inputs, and is available only to the package input pins. Do not port one package V_{BB} pin directly to another device without current amplification. When used, decouple V_{BB} to V_{CC} (or V_{TT}) via a 0.01 to 0.001 μF capacitor to suppress noise injection. Limit current to less than 0.5 mA (Absolute Maximum Rating source or sink) as shown in Figure 21. When not used, V_{BB} should be left open.

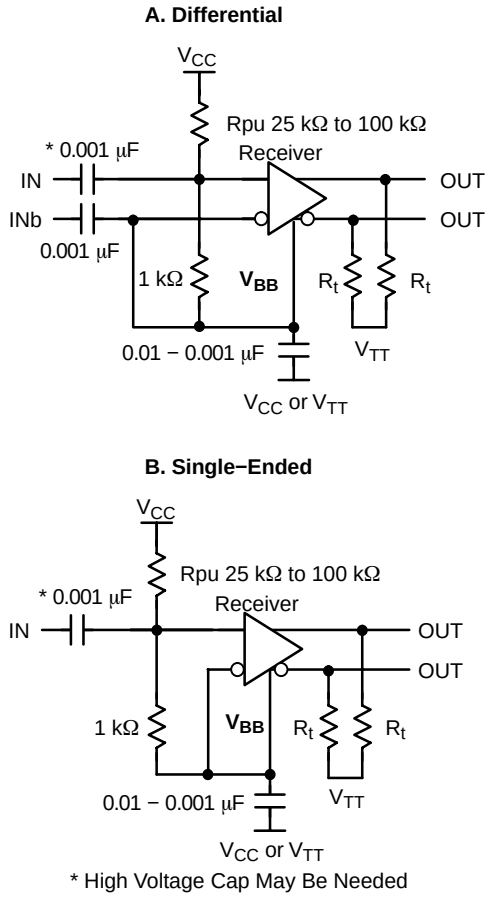


Figure 21. Differential and Single−Ended AC Configurations Using V_{BB} Reference

In Figure 21A, the IN line has a 1 kΩ resistor to V_{BB}, presenting a 1 KΩ impedance across the differential signal lines. This assumes the signal impedance matching has been accomplished prior to the cap coupling, on the driver side of cap. Locate the coupling capacitor as physically close to the input pin as possible to minimize the trace length and diminish potential reflections due to the impedance mismatch.

If signal impedance matching has not been accomplished prior to the cap coupling, then a characteristic impedance resistor, $2Z_0$, would be used across the input lines, on the receiver side of the cap. The value of the Rpu resistor would be adjusted to produce an acceptable null signal default voltage drop.

Auto−Oscillation Suppression with V_{BB}

If the differential inputs to the AC coupled device are left open or if the driving signals are lost, both receiver input pin voltages converge toward the VBIAS reference voltage V_{BB} value. Sustained oscillation may autonomously result from a combination of ambient environmental noise, the device small signal gain, and feedback from the output to the input through parasitic capacitive and inductive paths.

As a differential receiver input voltage diverges, the output responds by transitioning toward a state voltage. A sufficient voltage Δ across the receiver inputs will force the output to state level. Depending on conditions, about 10 to 50 mV is sufficient to suppress instability oscillation and force a determined state on the output.

For the configuration using the V_{BB} reference, Figure 21, this input voltage Δ may be accomplished by injecting a minimum current from V_{CC} through an external pullup resistor, Rpu, on ONE input line. The value of Rpu could range from 25 kΩ to 100 kΩ. As Rpu increases, the phase error is diminished and the susceptibility to oscillation increases.

Generally, an internal pull−down resistor ranging in value from 52 kΩ to 75 kΩ is deployed on an input pin. On some D−bar (Invert) input pins an additional 36 kΩ to 75 kΩ resistor is deployed to suppress oscillation by forcing a determined state on the output under open input or null voltage conditions. A minimum input voltage Δ of 20 to 30 mV may be effective depending on noise, gain, and layout.

Generating V_{BB} for VBIAS

When V_{BB} voltages are desired, but not available within a device, the reference level may be ported from a generator as illustrated in Figure 22. Any of the “16” type buffers are recommended for use in a high current gain V_{BB} Generator buffer. For example, the E416, EL16, LVEL16, EP16, LVEP16, EL17, LVEL17, etc. type devices have a V_{BB} pin available for constructing a V_{BB} Generator buffer.

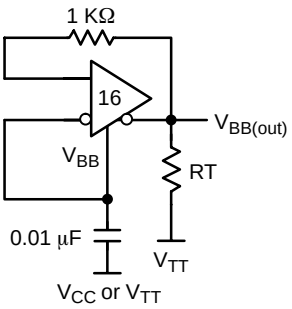


Figure 22. V_{BB} Voltage Reference Generator

Non−V_{BB} Biasing

Alternative to a device supplied V_{BB}, any voltage source may be supplied to bias receiver inputs to provide an acceptable V_{IHCMR} (Voltage Input HIGH Common Mode Range) DC reference to the receiver (see specific device data sheet). Signal impedance matching may be accomplished prior to cap coupling, allowing a wide range values for a rebiasing resistor network.

When the coupling capacitor is physically located near enough to the receiver input pins to prohibit reflections on the connecting trace length or signal impedance matching has been accomplished prior to cap coupling, then a simple high value resistor divider network from V_{CC} to V_{EE} is recommended as shown in Figure 23. Differential and Single−Ended AC Configurations Using Non−V_{BB} Biasing (A and B). This network total resistance may be from 1 KΩ to 10 KΩ. For 50 Ω impedance traces, the typical value for the voltage divider resistors are given in Table F. Typical Rebias and Impedance Matching Resistor Network Values @ Z_0 = 50. Note the impedance presented to a signal is > 5 KΩ.

Table F. Typical Rebias and Impedance Matching Resistor Network Values @ Z_0 = 50

Resistor	$\|V_{CC}-V_{EE}\|$ = 5.0 V	$\|V_{CC}-V_{EE}\|$ = 3.3 V	$\|V_{CC}-V_{EE}\|$ = 2.5 V	Units
R1 (R1′)	4	4	4	KΩ
R2 (R2′)	6	6	6	KΩ
V_{rebias}	3.3	2.2	1.7	V

When the coupling capacitor is physically located at a distance from receiver over a trace or cable length capable of sustaining reflections, a Thevenin parallel network matching the line of impedance is recommended for their suppression. This is shown in Figure 23. Differential and Single−Ended AC Configurations Using Non−V_{BB} Biasing (A and B). The rebias voltage may always be safely set at V_{CC}−1.3. For 50 Ω impedance traces, the typical value for the voltage divider resistors are given in Table G. Typical Rebias and Impedance Matching Resistor Network Values @ Z_0 = 50.

Table G. Typical Rebias and Impedance Matching Resistor Network Values @ Z_0 = 50

Resistor	$\|V_{CC}-V_{EE}\|$ = 5.0 V	$\|V_{CC}-V_{EE}\|$ = 3.3 V	$\|V_{CC}-V_{EE}\|$ = 2.5 V	Units
R1 (R1′)	68	83	96.15	Ω
R2 (R2′)	192	127	104.16	Ω
V_{rebias}	3.7	2.0	1.2	V

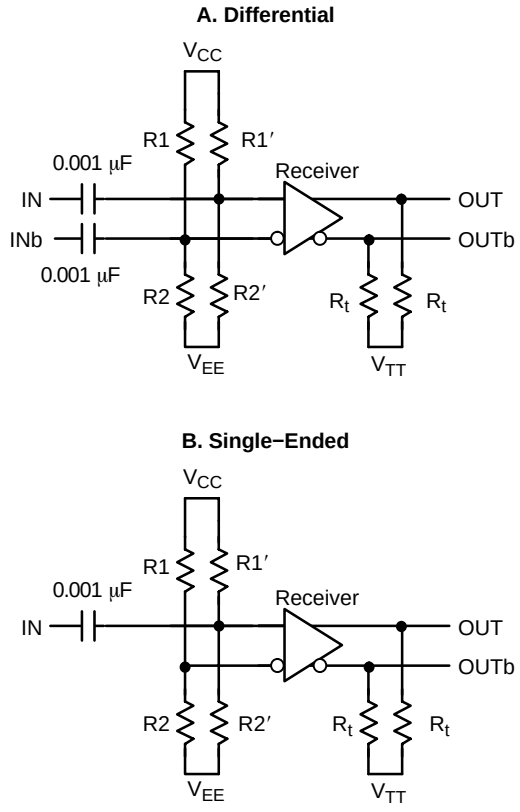


Figure 23. Differential and Single−Ended AC Configurations Using Non−V_{BB} Biasing

The characterized V_{BB} reference voltage bias, VBIAS, is V_{CC} − 1.33 V, but a device is not restricted to this VBIAS value. The VBIAS range is determined by the Vpp amplitude and the signal HIGH level, V_{IH}. Input HIGH level, V_{IH}, is constrained by the data sheet specification of common mode range, V_{IHCMR} or V_{CMR}. Thus, the VBIAS range is constrained:

$$VBIAS_{max} = V_{IHCMRmax} - (0.5)(Vpp)$$
$$VBIAS_{min} = V_{IHCMRmin} - (0.5)(Vpp)$$

A single−ended source into a differential type input signal amplitude swing, V_{pp}, is typically constrained from V_{ppmin} = 300 mV to V_{ppmax} = 1000 mV.

An input signal must swing symmetrically above and below VBIAS to preserve a 50% duty cycle out of the receiver. Differential signals must have identical crosspoint voltages to preserve minimum phase error and duty cycle error. Crosspoint voltages are determined by the matched precision of the resistor divider network from V_{CC} to V_{EE}.

Auto−Oscillation Suppression without V_{BB}

For a configuration without a V_{BB} reference pin, such as illustrated in Figure 23, the resistor network may be modified to have an input voltage Δ of 20 to 30 mV offset between the input pins. Either a high resistor value divider or a Thevenin parallel network may be modified to accomplish this input voltage Δ. This is accomplished by altering the values of R1, R1′, R2, and R2′.

Combining the high impedance and impedance matching networks results in an input voltage scheme shown in Figure 24. This creates the proper input voltage Δ, VBIAS, using fewer components.

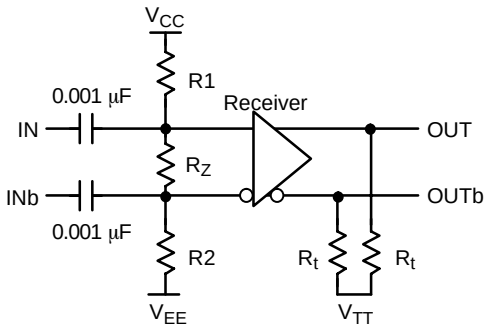


Figure 24. VBIAS and Auto−Oscillation Suppression with Thevenin Parallel Network

For a 3.3 V V_{CC}, the values of R1 and R2 provide a Thevenin parallel network divider voltage with V_{IH} in the V_{IHCMR} of the receiver. Current through the divider develops the default offset across R_z and can be adjusted as needed. For example, in Z_0 = 50 traces, a 30 mV default offset difference will be created if V_{CC} = 3.3 V and the DC bias voltage is 2.0 V (typical V_{BB}) when:

$R1 = 4.22\ k\Omega$
$R2 = 6.34\ k\Omega$
$R_Z = 100\ \Omega$

The 0.001 coupling cap may need to be adjusted to frequency and Vpp amplitude of the receiver input signal.

A similar single−ended network may be used with only one coupling cap and sufficient bypass capacitance on the non−driven resistor to preserve a DC level.

Output Level Shifting

Receiver inputs may be level shifted using capacitive coupling and adjusting VBIAS within the acceptable common mode range for V_{IH}. Output levels may also be changed independent of input levels. The driver device may be operated with both V_{CC} and V_{EE} at shifted values. This is used at the factory to evaluate devices and conveniently port signals directly into standard 50 Ω impedance equipment modules. The V_{CC} is fixed to +2.0 V above Test System chassis ground and the test equipment internal 50 Ω impedance constitutes a proper signal termination. Thus, the split V_{EE} supply is adjusted to a negative value.

$\lvert V_{CC} - V_{EE} \rvert$	Split V_{CC}	Split V_{EE}	Unit
3.0	+2.0	−1.0	V
3.3	+2.0	−1.3	V
5.0	+2.0	−3.0	V
5.5	+2.0	−3.5	V

Output levels may be shifted to symmetrically cross 0.0 V by a similar method although the advantage of conveniently directly connecting into standard test equipment is no longer available.

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