3000 SERIES FAMILY OF PROGRAMMABLE GATE ARRAYS

T-46-13-47

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Second generation user-programmable gate array
- Flexible array architecture
- High performance (50, 70 MHz)
- Improved interconnection resources
- Density of up to 9000 gates
- 100% factory pre-tested
- Selectable configuration modes
- 100% compatibility with AMD PGA development tools
- Standard PROM file interface
- Off the shelf availability

GENERAL DESCRIPTION

The AM 3000 Series Logic Cell™ Array (LCA) is a high-performance, second generation user-programmable gate array. The array contains three types of configurable elements that are customized in accordance with the user-defined system design; a perimeter of Input/Output Blocks (IOBs), a core array of Configurable Logic Blocks (CLBs), and interconnection resources.

The final configuration of the three main programmable elements is determined by the user and easily implemented by AMD user-programmable gate array design tools.

AMD's development tools let users produce a complete design, from schematic capture through device customization, on an IBM PC-AT or compatible computer. LCA macro libraries and interface software are also available to support schematic capture and simulation on popular CAE workstations.

4

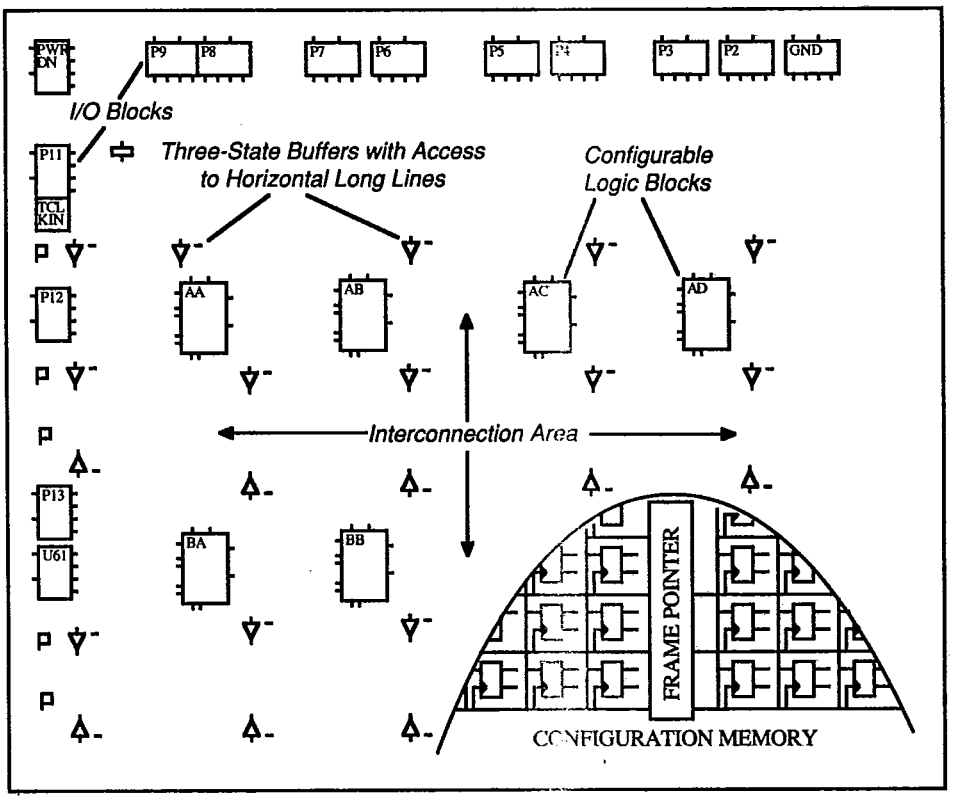
PRODUCT SELECTOR GUIDE

Basic Array	Logic Capacity (usable gates)	Configurable Logic Blocks	User I/Os	Program Data (bits)
M3020	2000	64	64	14779
M3090	9000	320	144	64160

Publication #	Rev.	Amendment
10642	A	/0

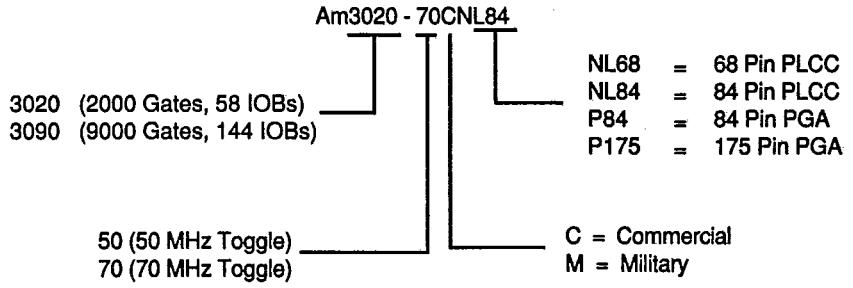
Issue Date: June 1988

BLOCK DIAGRAM



ORDERING INFORMATION

Further information is available from AMD franchised distributors or from the nearest AMD sales representative. Part numbers are composed as follows:



ARCHITECTURE

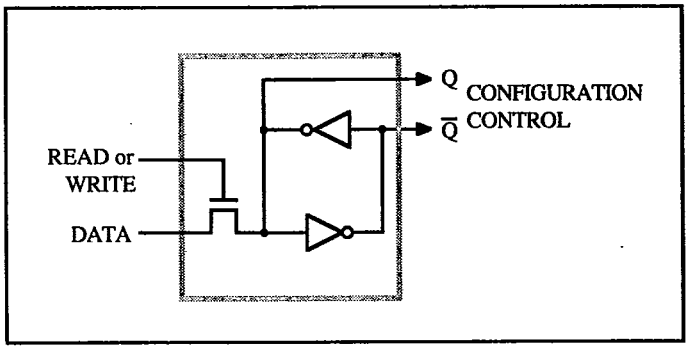
Functional Description

The perimeter of configurable IOBs provides a programmable interface between the internal logic array and the device package pins. The array of CLBs performs user-specified logic functions. The interconnection are programmed to form networks, carrying logic signals among blocks. This is analogous to printed circuit board traces connecting MSI/SSI packages.

The logic functions of these blocks are determined by programmed look-up tables. Functional options are performed by program-controlled multiplexers. Interconnecting networks between blocks are composed of metal segments joined by program-controlled pass transistors. These LCA functions are activated by a configuration bit stream that is loaded into an internal, distributed array of configuration memory cells. The configuration bit stream is loaded into the LCA device at power-up and can be reloaded on command. The LCA device includes logic and control signals for automatic or passive configuration. Configuration data can be either bit serial or byte parallel. The XACT LCA Development System generates the configuration bit stream used to configure the LCA device. The memory loading process is independent of the user logic functions.

Configuration Memory

The static memory cell used for the LCA's configuration memory has been designed specifically for high reliability and noise immunity, ensuring integrity even under adverse conditions. Static memory provides the best combination of high density, high performance, high reliability, and comprehensive testability. As shown below, the basic memory cell consists of two CMOS inverters and a pass transistor, which is used for writing and reading cell data. The cell is only written during configuration and only read during readback. During normal operation, the pass transistor is off and does not affect the stability of the cell. This is quite different from the operation of conventional memory devices, in which the cells are frequently read and re-written.



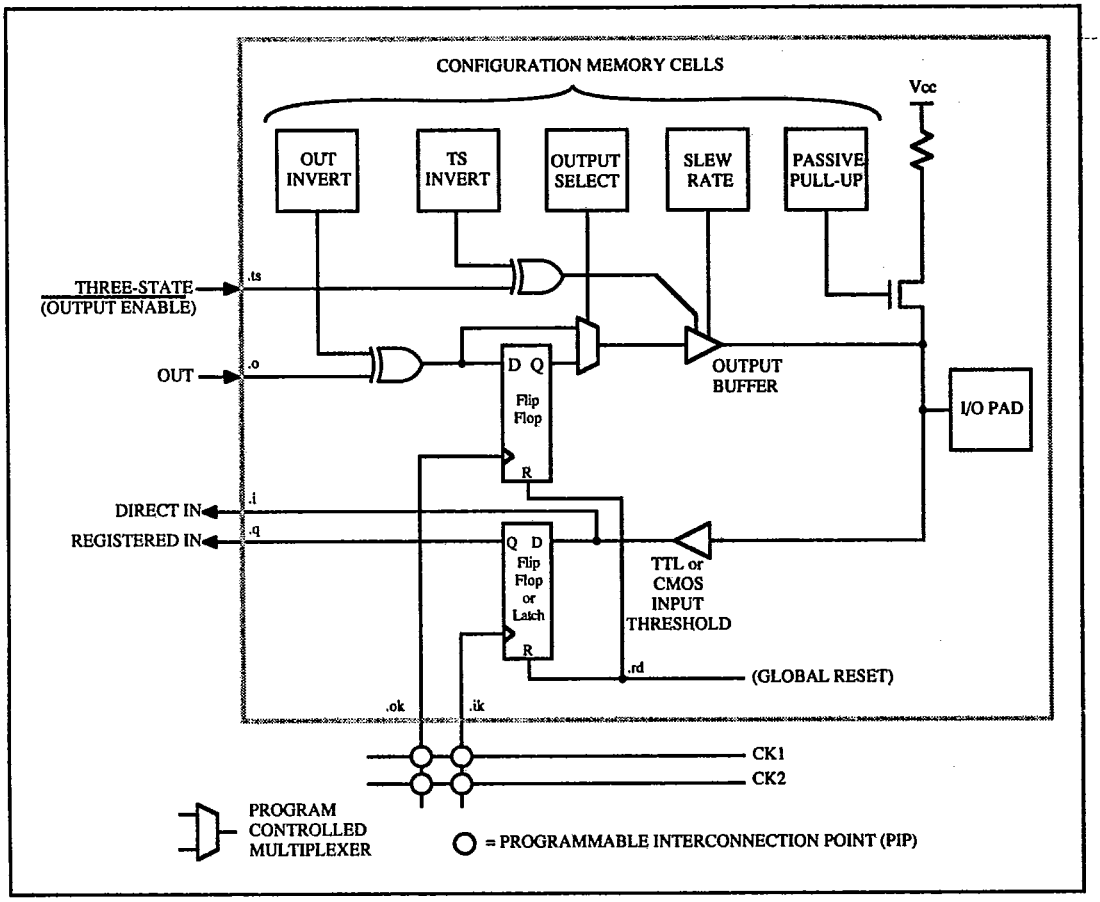
A static configuration memory cell is loaded with one bit of the configuration bit stream and controls one data selection in the LCA device. The memory cell outputs Q and ~Q use full Ground and Vcc levels and provide continuous, direct control. The additional capacitive load, together with the absence of address decoding and sense amplifiers, gives the cell high stability.

Due to the structure of the configuration memory cells, they are not affected by extreme power supply excursions or very high levels of alpha particle radiation. No soft errors have been observed in reliability testing, even in the presence of very high doses of alpha radiation.

The method of loading the configuration data is selectable. Two methods use serial data, while three use byte-wide data. The internal configuration logic uses framing information, which is embedded in the configuration data by the XACT LCA Development System, to direct memory cell loading. The serial data framing and length count preamble provide synchronous, serial, or daisy-chained compatibility with various AMD programmable gate arrays.

Input/Output BlockS

Each user-configurable IOB, shown below, provides an interface between the device's external package pin and the internal user logic. Each IOB includes both registered and direct input paths and each provides a programmable three-state output buffer that can be driven by a registered or direct output signal. Configuration options allow a choice of polarity on the output and three-state control signals, a controlled slew rate, and a high impedance pull-up. Each input circuit provides input clamping diodes for electrostatic protection, and circuits to inhibit latch-up produced by input currents.



The input buffer portion of each IOB provides threshold detection to translate external signals applied to the package pin to internal logic levels. The global input-buffer threshold of the IOBs can be programmed for TTL or CMOS voltage levels. The buffered input signal drives the data input of a storage element that can be configured as a positive edge-triggered D flip-flop, or a level-transparent latch. Clock/load signals, IOB pin .ik, can be chosen from either of two available metal lines along each die edge. I/O storage elements are reset during configuration or by the active low chip ~RESET input. Both direct input signals, from IOB pin.q, are available.

For reliable operation, inputs should have transition times less than 100 ns and should not be left undriven, or floating. Unused CMOS input-pin circuits can be at threshold and produce oscillations. This produces additional power dissipation and system noise. A typical hysteresis of about 50 mV reduces input noise sensitivity . Each user IOB includes a programmable high impedance pull-up resistor that

can be selected by the bit stream and which provides a constant HIGH for undriven pins. Although the LCA device provides circuitry for input protection against electrostatic discharge, normal CMOS handling precautions should be observed.

Loop delays for the IOB and logic block flip-flops are about 3 ns. This increases reliability, especially for asynchronous clock and data conditions. Short loop delays minimize the probability of a metastable condition, which can result from assertion of the clock during data transitions. Because of the short loop delay in LCA devices, the flip-flops can be used to synchronize external signals applied to the device. Once synchronized in the IOB, the signals can be used internally without regard to their clock-relative timing, except as it applies to the internal logic and routing path delays.

Output buffers of the IOBs provide CMOS-compatible 4 mA source-or-sink drive for high fan-out CMOS or TTL compatible signal levels. The network driving IOB pin .o becomes the registered or direct data source for the output buffer. The three-state control signal, IOB pin .ts, can control output activity. An open-drain type output can be obtained by using the same signal for driving the output and three-state signal nets, so that the buffer output is enabled only for a LOW.

The configuration memory cells, shown in the figure above, control the optional output register and logical signal inversion, as well as the three-state and slew rate configuration bits. A choice of two clocks is available on each die edge. All user inputs are programmed for TTL or CMOS thresholds.

The IOB includes input and output storage elements and the following I/O options selected by configuration memory cells.

- Logical **inversion of the output** is controlled by one configuration bit per IOB.
- Logical **three-state control** of each IOB output buffer is determined by the states of the configuration data bits that turn the buffer on/off or select the output buffer three-state control interconnection, pin .ts. When this IOB output control signal is HIGH, or logic 1, the buffer is disabled and the package pin is high impedance. Inversion of the buffer three-state control logic sense, output enable, is controlled by an additional configuration data bit.
- **Direct or registered output** is selectable for each IOB . The register uses a positive-edge, clocked flip-flop. The clock source, IOB pin .ok, can be supplied by either of two metal lines, which are available along each die edge. Each of these lines is driven by an invertible buffer.
- Increased **output transition speed** can be selected to satisfy critical nets. Slower transitions reduce capacitive load peak currents of non-critical outputs and minimize system noise.
- A high impedance **pull-up resistor** can be used to prevent floating, unused inputs.

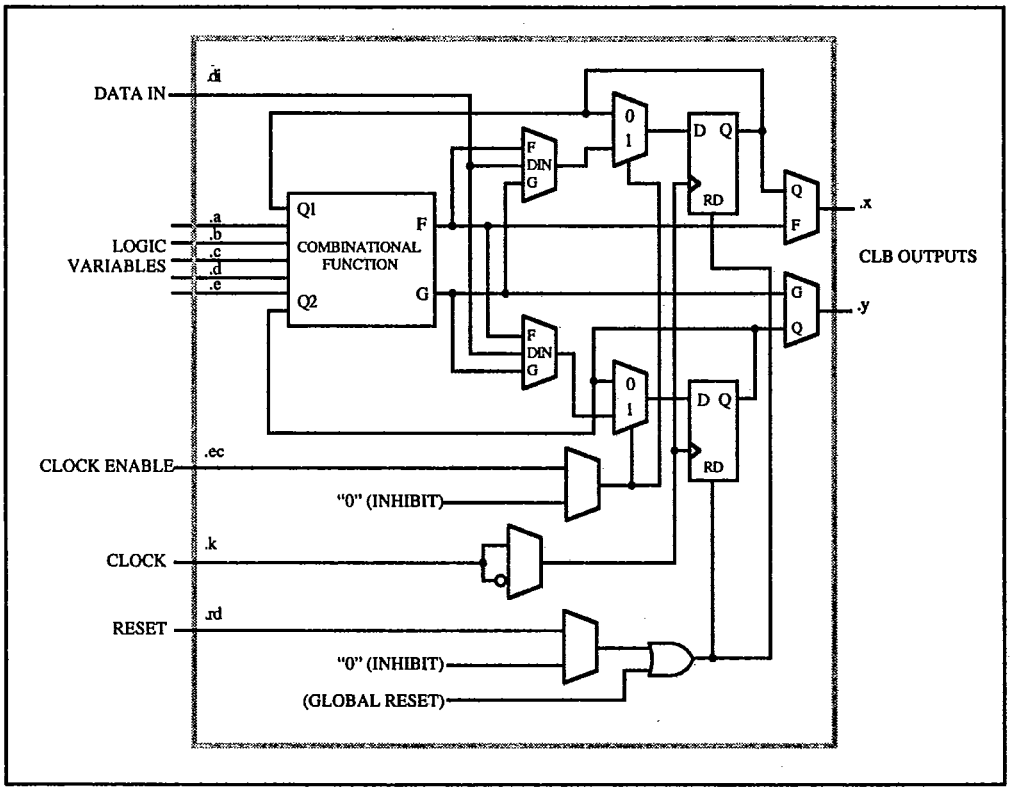
The following table is summarizes the I/O options.

INPUTS	OUTPUTS
Direct	Direct/registered
Flip-flop/latch	Inverted/true
CMOS/TTL threshold (chip inputs)	Full speed/slew limited
Pull-up resistor	Optional three-state control

Configurable Logic Blocks

CLBs are the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of IOBs. The 3020 has 64 such blocks arranged in eight rows and eight columns. The XACT LCA Development System compiles the configuration data, which defines the operation and interconnection of each block. Users can define CLBs and their interconnecting networks by automatic translation from a schematic capture logic diagram or, optionally, by installing library or user macros.

Each CLB has a combinational logic section, two flip-flops, and an internal control section. As shown in the following figure, there are five logic inputs (.a, .b, .c, .d, and .e), a common clock input (.k), an asynchronous direct reset input (.rd), and a clock enable (.ec). All can be driven from the interconnection resources adjacent to the blocks. Each CLB also has two outputs (.x and .y) that can drive interconnection networks.

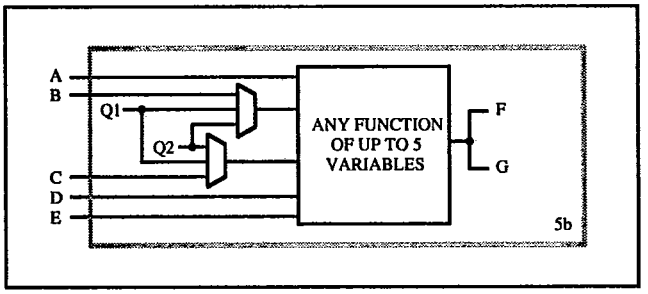


Data input for either flip-flop within a CLB is supplied from the F or G function outputs of the combinational logic, or the direct data input, .di. Both flip-flops in each CLB share the active HIGH

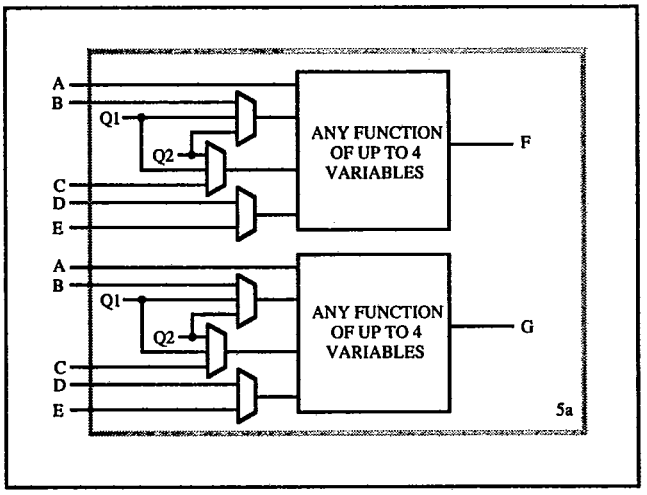
asynchronous reset (.rd), which is dominant over clocked inputs. All flip-flops are reset by the active LOW chip input, ~RESET, or during the configuration process. The flip-flops share the clock enable (.ec), which, when LOW, recirculates the present states of the flip-flops and inhibits response to the data-in or combinational function inputs on a CLB. The user can enable these control inputs and select their sources. The user also can select the clock net input (.k) and its active sense in each logic block. This programmable inversion eliminates the need to route both phases of a clock signal throughout the device. Flexible routing allows use of common or individual CLB clocking.

The combinational logic portion of the CLB uses a 32-by-1 look-up table to perform Boolean functions. Variables selected from the five logic inputs and two internal block flip-flops are used as table address inputs. The combinational propagation delay through the network is independent of the logic function generated and is spike free for changes in single input variables.

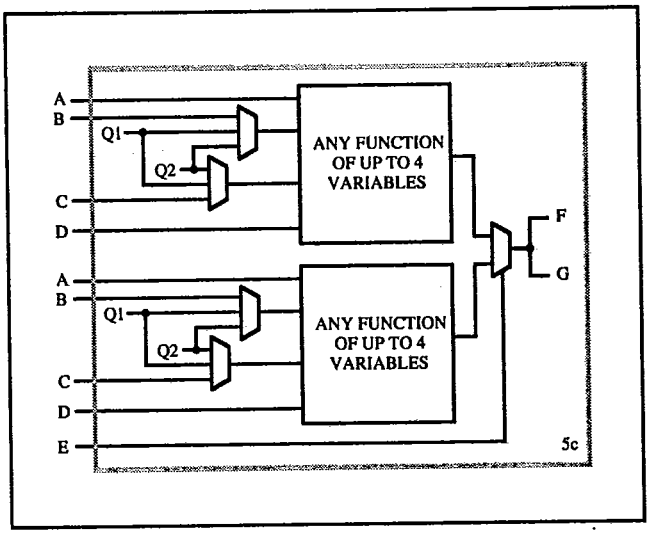
This technique can generate a single function of five variables, as shown below.



It can also generate any two logic functions of up to four variables each.

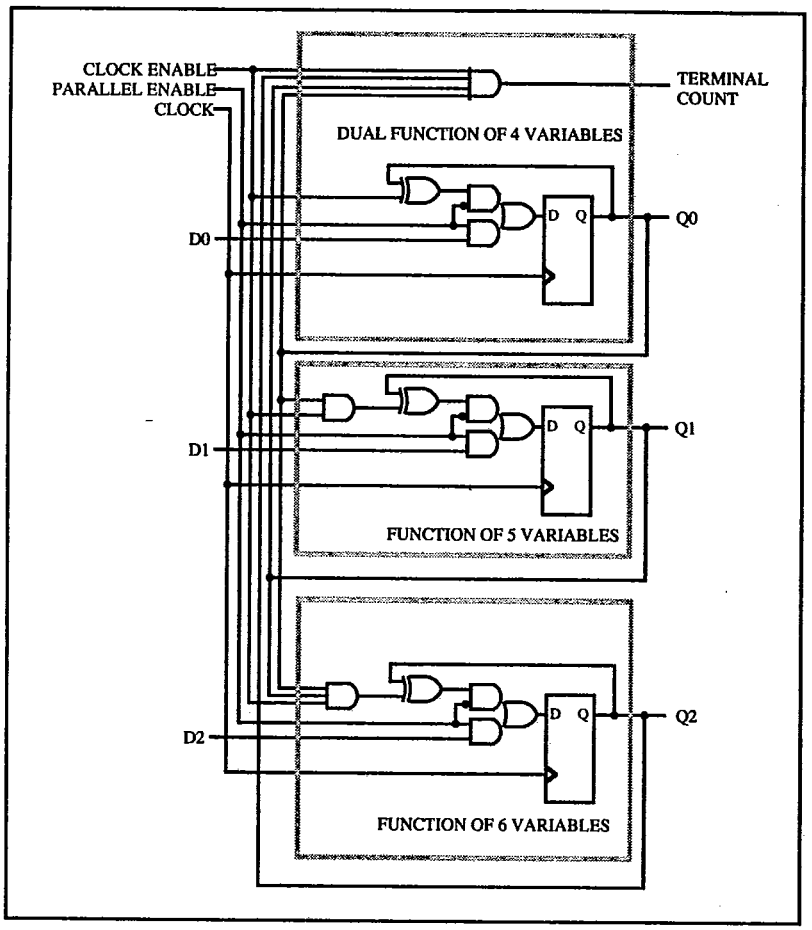


It can also generate some functions of seven variables, as shown in the next figure.



The partial functions of six or seven variables are generated by the input variable,.e, which dynamically selects between two functions of four different variables. For the two functions of four variables each, the independent results,F and G, can be used as data inputs to either flip-flop or either logic block output. For the single function of five variables and merged functions of six or seven variables, the F and G outputs are identical. Symmetry of the F and G functions and the flip-flops helps optimize the routing of the networks connecting the logic blocks and IOBs.

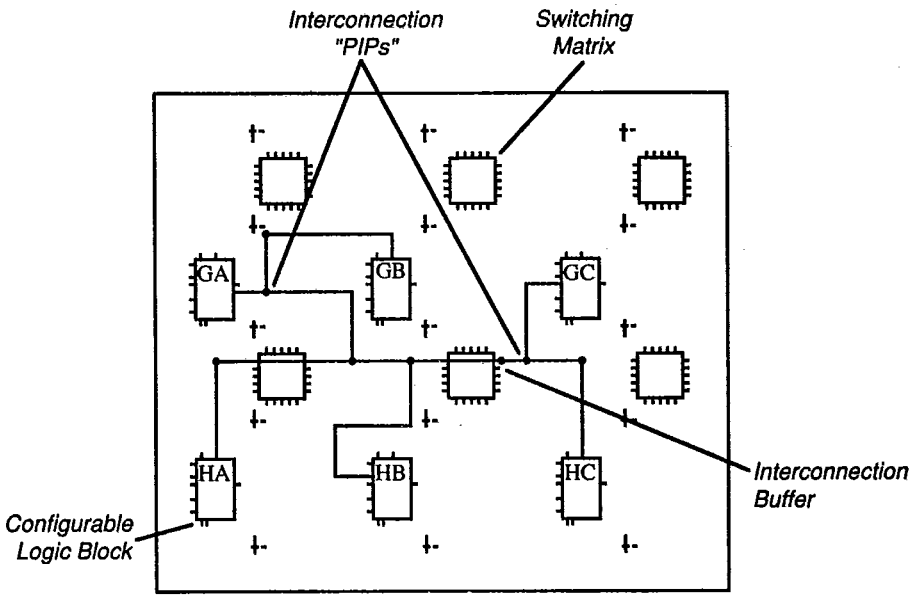
The next figure shows a modulo 8 binary counter with parallel enable. It uses one CLB of each type.



INTERCONNECTIONS

Programmable Interconnections

Programmable interconnection resources in the LCA device provide routing paths to connect inputs and outputs of the I/O and logic blocks into logical networks. Interconnections between blocks are composed of two-layer grid of metal segments. Specially designed pass transistors, each controlled by a configuration bit, form programmable interconnect points (PIPs) and switching matrices used to implement the necessary connections between selected metal segments and block pins. The figure below provides an example of a routed net.

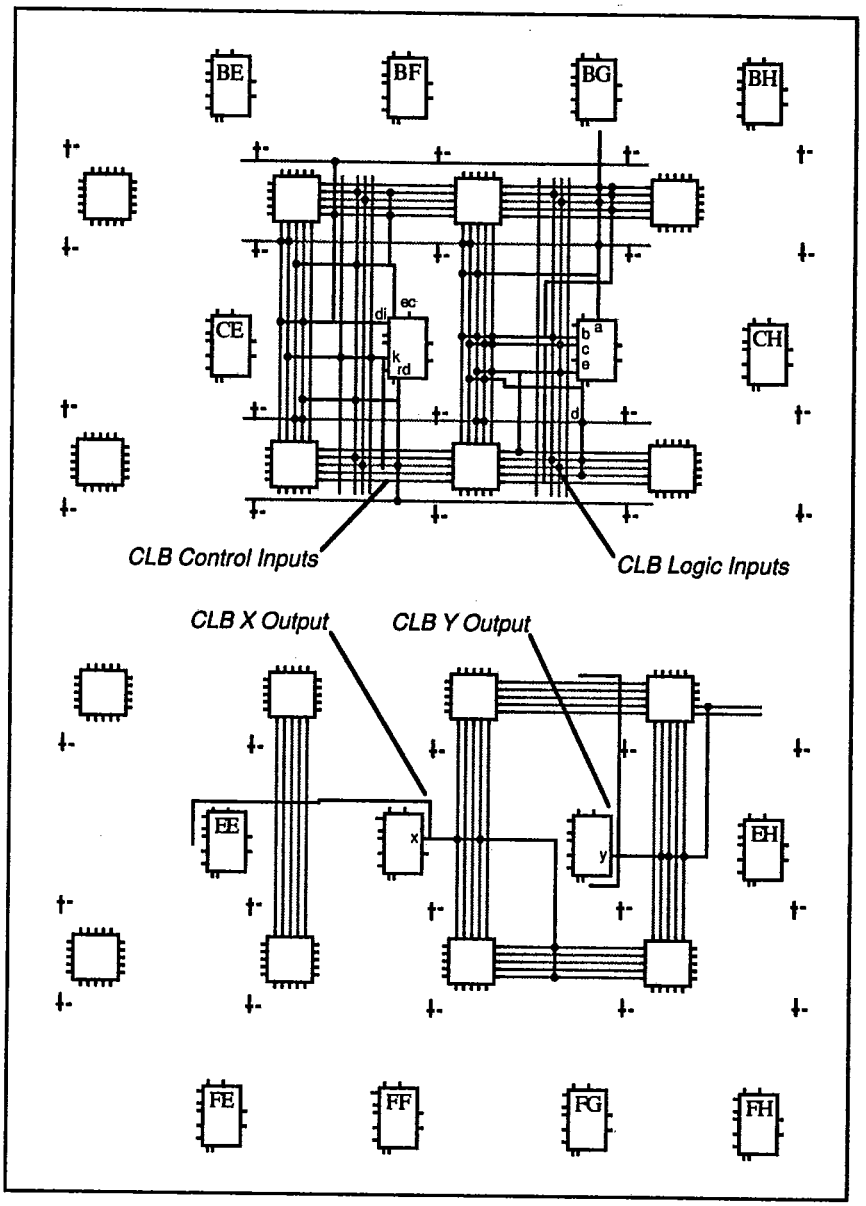


The XACT LCA Development System automatically routes these interconnections. Interactive routing using Editnet can also be done to optimize the design. The inputs of the logic or IOB are multiplexers that can be programmed to select an input network from the adjacent interconnection segments.

4

Note: The switch connections to block inputs are usable only for input connection, and not for routing, because they are unidirectional (as are block outputs).

The following figure illustrates routing access to logic block input variables, control inputs, and block outputs.

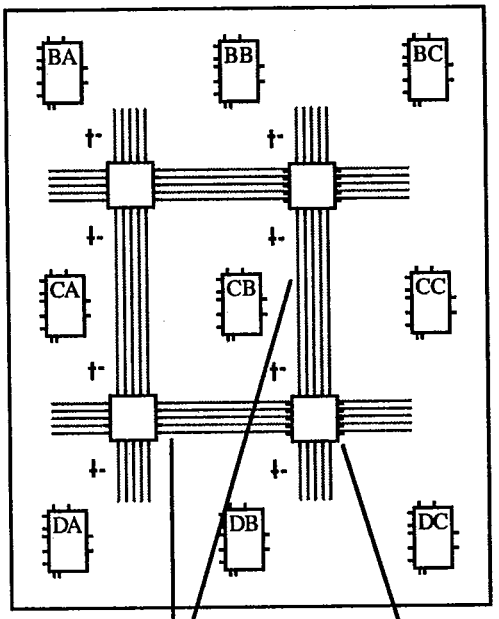

BE
BF
BG
BH
CE
CH
EE
EH
FE
FF
FG
FH
CLB Control Inputs
CLB Logic Inputs
CLB X Output
CLB Y Output

Three types of metal resources are available for network interconnections.

- General Purpose Interconnection
- Direct Connection
- Long Lines

General Purpose Interconnections

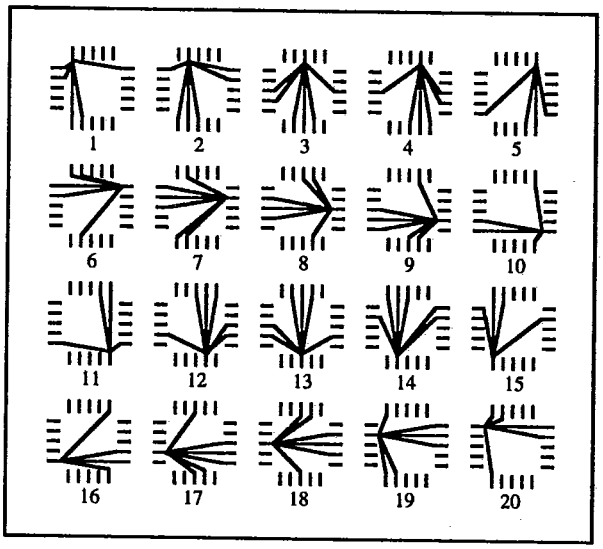
A general purpose interconnection, as shown below, consists of a grid of five horizontal and five vertical metal segments located between the rows and columns of logic and I/O Blocks. These segments can be connected through switch matrices to form networks for CLB and IOB inputs and outputs.



Grid Of General Interconnection Metal Segments

Switching Matrix

Each segment is the height or width of a logic block. Switching matrices join the ends of these segments and allow programmed interconnections between the metal grid segments of adjoining rows and columns. The switches of an unprogrammed device are all non-conducting. The connections through the switch matrix can be made by automatic routing, or by using Editnet to select the desired pairs of matrix pins that are to be connected or disconnected. The legitimate switching matrix combinations for each pin are shown in the next figure.

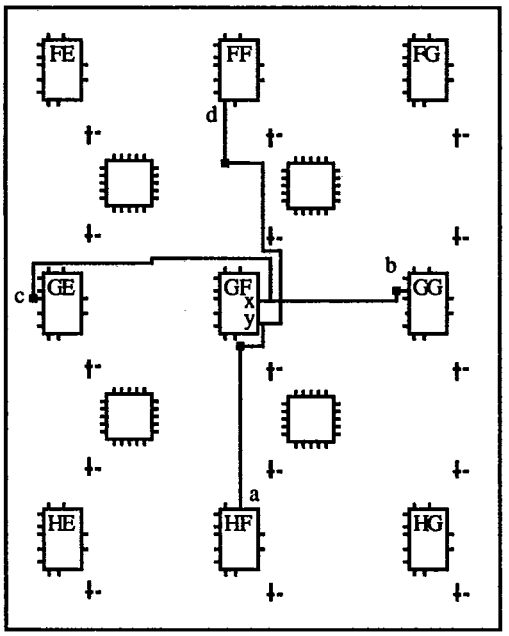


Special buffers in the general interconnection areas provide periodic signal isolation and restoration, thus improving performance of lengthy nets. The interconnection buffers can propagate signals in either direction on a general interconnection segment. These bidirectional buffers are above and to the right of the switching matrices. The other PIPs adjacent to the matrices are gateways to and from long lines.

The XACT LCA Development System automatically defines the buffer direction based on the location of the interconnection network source. The delay calculator of the XACT LCA Development System automatically calculates and displays the block, interconnection, and buffer delays for the selected paths. It can also generate the simulation net list with a worst-case delay model.

Direct Interconnections

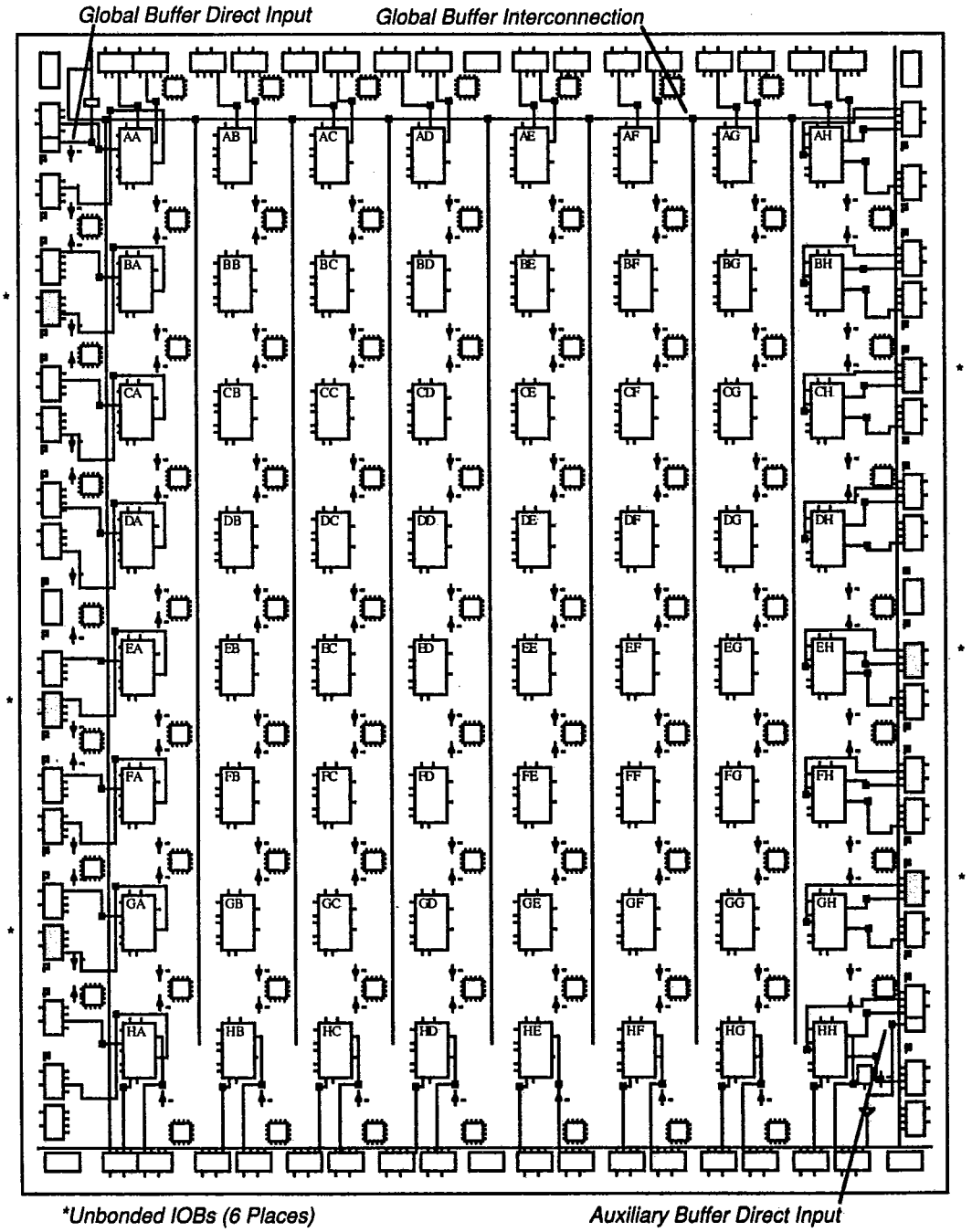
A direct interconnection, shown below, provides the most efficient implementation of networks between adjacent logic or IOBs. The .x and .y outputs of each CLB have single contact, direct access to inputs of adjacent CLBs.



4

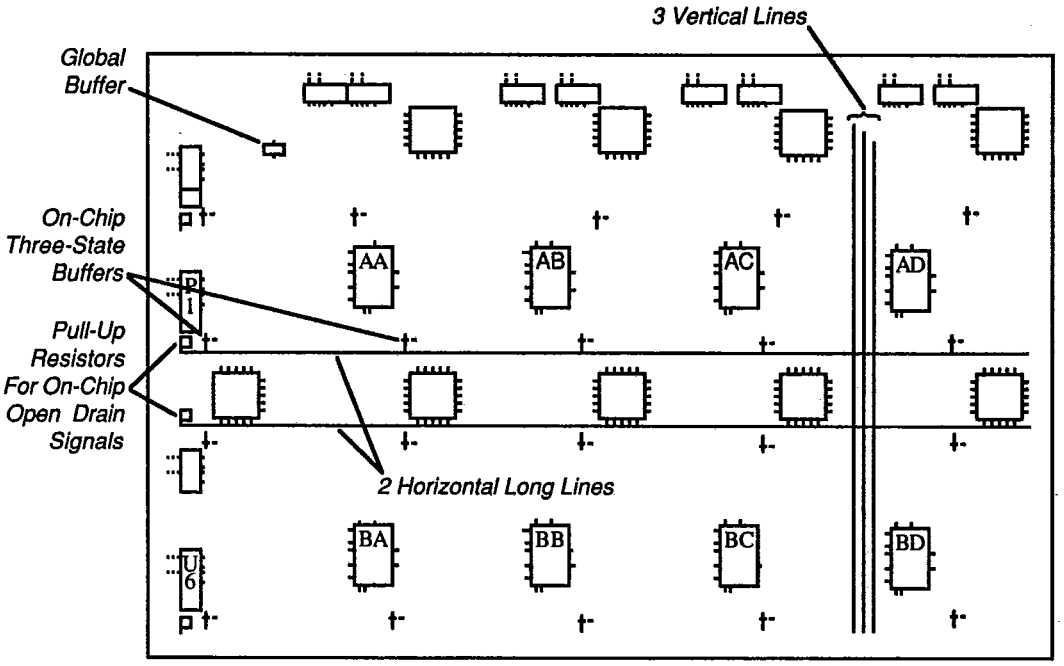
Signals routed from block to block by direct interconnection show minimum interconnection propagation and use no general interconnection resources. For each CLB, the .x output can be connected directly to the .b input of the CLB to its right, and to the .c input of the CLB to its left. The .y output can use a direct interconnection to drive the .d input of the block above, and the .a input of the block below.

Direct interconnection should be used to maximize the speed of high performance portions of logic. Where logic blocks are adjacent to IOBs, a direct connection is provided alternately to the IOB inputs (.i) and outputs (.o) of the left, top, and bottom edges of the die. The right edge provides alternate direct input and output of CLBs and IOBs. Direct interconnections of IOBs and CLBs are shown in the next figure.

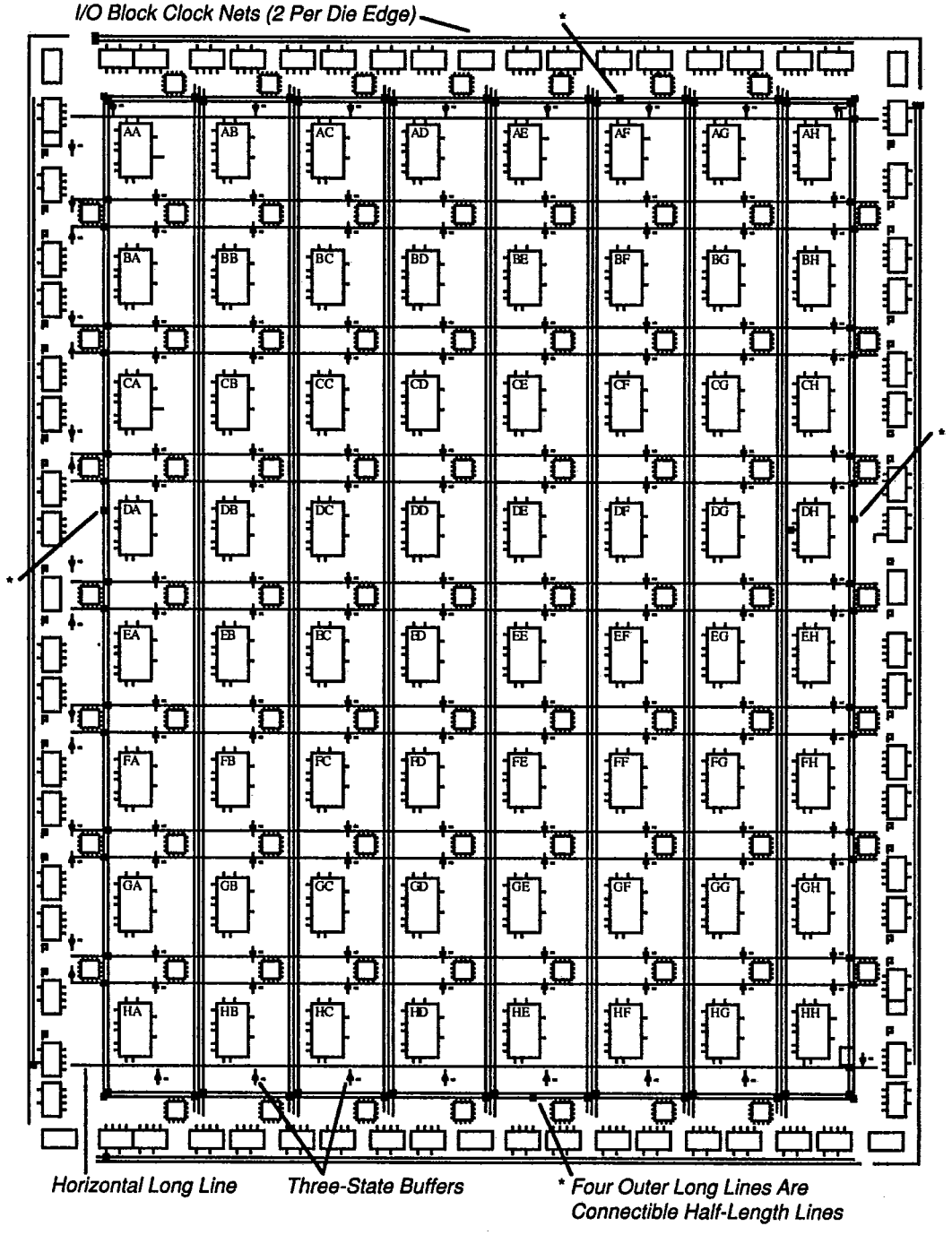

Global Buffer Direct Input
Global Buffer Interconnection
AA
AB
AC
AD
AE
AF
AG
AH
BA
BB
BC
BD
BE
BF
BG
BH
CA
CB
CC
CD
CE
CF
CG
CH
DA
DB
DC
DD
DE
DF
DG
DH
EA
EB
EC
ED
EE
EF
EG
EH
FA
FB
FC
FD
FE
FF
FG
FH
GA
GB
GC
GD
GE
GF
GG
GH
HA
HB
HC
HD
HE
HF
HG
HH
*Unbonded IOBs (6 Places)
Auxiliary Buffer Direct Input

Long Lines

Long lines, which bypass the switch matrices, are intended primarily for signals that must travel a long distance, or that must have minimum skew among multiple destinations. Long lines, shown below, run the height or width of the interconnection area. Each interconnection column has three vertical long lines, and each interconnection row has two horizontal long lines. Two additional long lines are adjacent to the outer sets of switching matrices. The outermost are connectible half-length lines.



Horizontal and vertical long lines provide high fan-out, low-skew signal distribution in each row and column. The global buffer in the upper left die corner drives a common line throughout the LCA device. The programmable interconnection of long lines is provided at the edges of the routing area. Long lines can be driven by a CLB or IOB output on a column-by-column basis. This provides a common low skew control or clock line within each column of logic blocks. Interconnections of these long lines are shown in the following figure. Isolation buffers are provided at each input to a long line and are enabled automatically by the XACT LCA Development System when a connection is made.

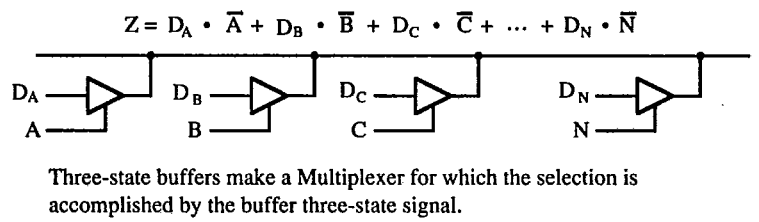

I/O Block Clock Nets (2 Per Die Edge)
AA
AB
AC
AD
AE
AF
AG
AH
BA
BB
BC
BD
BE
BF
BG
BH
CA
CB
CC
CD
CE
CF
CG
CH
DA
DB
DC
DD
DE
DF
DG
DH
EA
EB
EC
ED
EE
EF
EG
EH
FA
FB
FC
FD
FE
FF
FG
FH
GA
GB
GC
GD
GE
GF
GG
GH
HA
HB
HC
HD
HE
HF
HG
HH
Horizontal Long Line
Three-State Buffers
* Four Outer Long Lines Are Connectible Half-Length Lines

A buffer in the upper left corner of the LCA chip drives a global net available to all .k inputs of logic blocks. Using the global buffer for a clock signal provides a skew free, high fan-out, synchronized clock for use at any, or all, of the I/O and logic blocks. Three-state buffers let you use horizontal long lines to form wired-AND and multiplexed busses. Configuration bits for the .k input to each logic block can select this global line or another routing resource as the clock source for its flip-flops. This net can also be programmed to drive the die edge clock lines for IOB use. An enhanced speed, CMOS threshold direct access to this buffer is available at the second pad from the top of the left die edge.

A buffer in the lower right corner of the array drives a horizontal long line, which can drive programmed connections to a vertical long line in each interconnection column. This alternate buffer also is low skew and high fan-out. The network formed by this alternate buffer's long lines can be selected to drive the .k inputs of the logic blocks. The CMOS threshold, high-speed access to this buffer is at the third pad from the bottom of the right die edge.

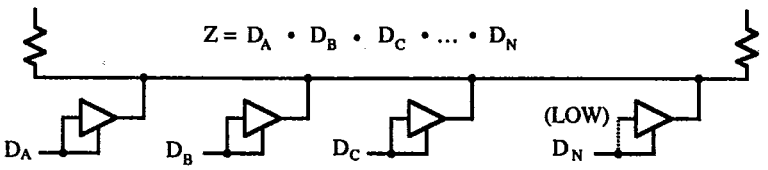
Internal Busses

A pair of three-state buffers are located adjacent to each CLB. These let logic drive the horizontal long lines. Logical operation of the three-state buffer controls lets them implement wide multiplexing functions. Any three-state buffer input can be selected to drive the horizontal long line bus by applying a low logic level on its three-state control line, as shown in the next figure.



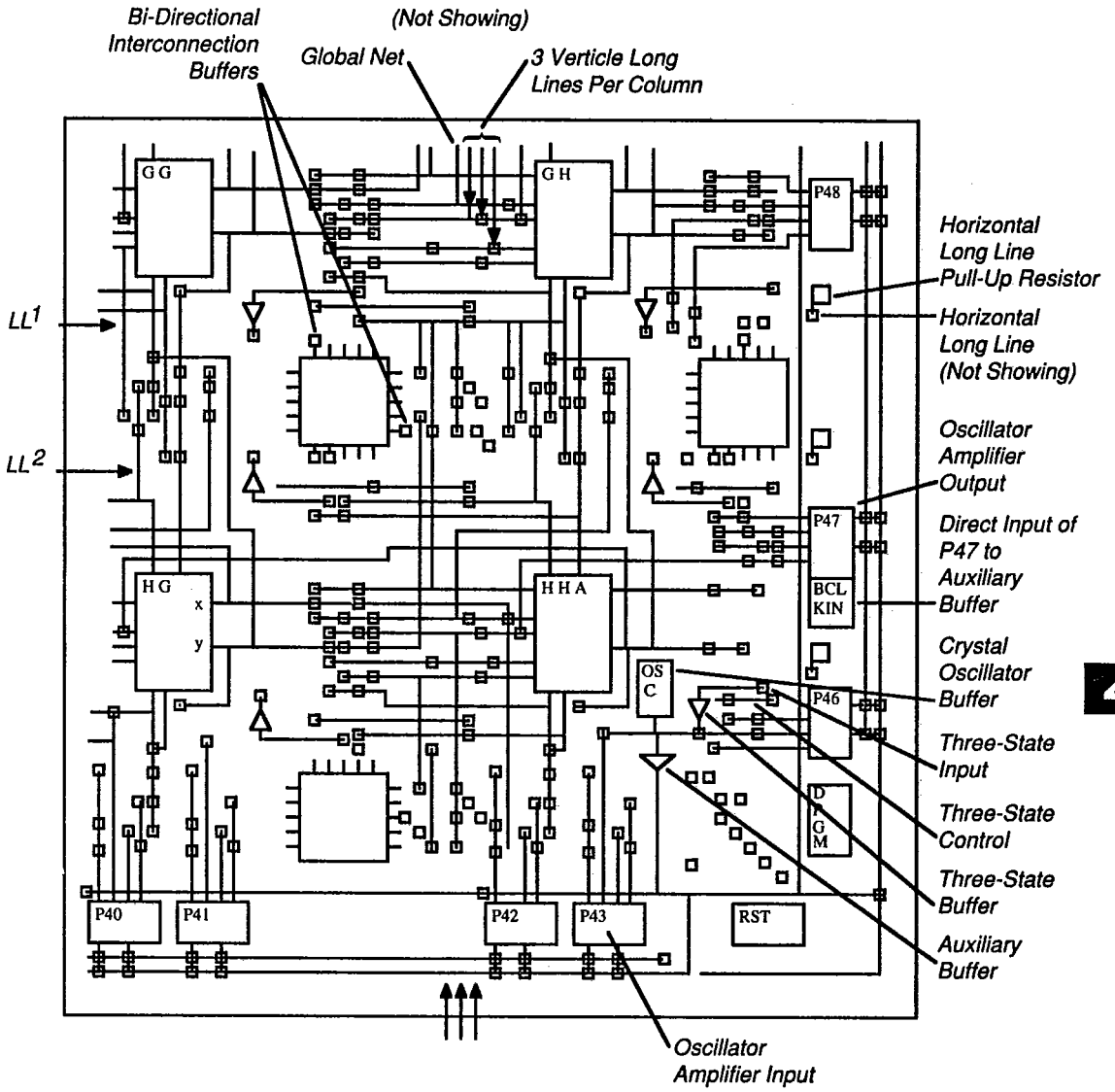
Three-state buffers make a Multiplexer for which the selection is accomplished by the buffer three-state signal.

The user must avoid contention resulting from multiple drivers with opposing logic levels. Control of the three-state input by the same signal that drives the buffer input creates an open drain wired-AND function. A logical HIGH on both buffer inputs creates a high impedance with no contention. A logical LOW enables the buffer to drive the long line low, as shown below.



Three-state buffers make a Wired-AND function. When all the three-state lines are HIGH (high impedance), the pull-up resistor(s) provide the HIGH output. The buffer inputs are driven by the control signals or a LOW.

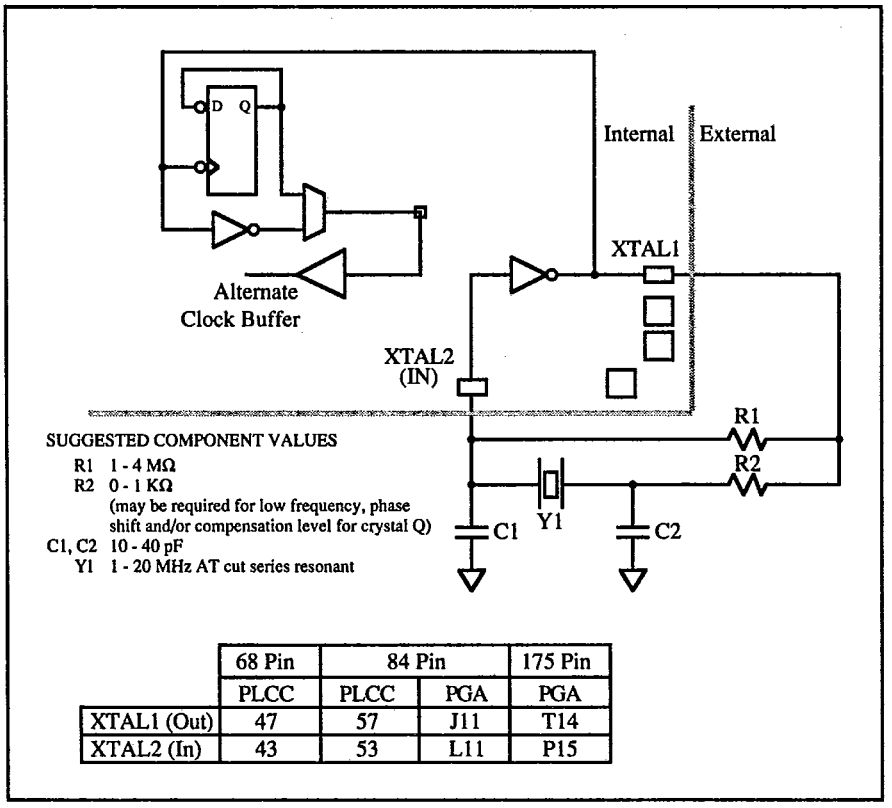
Pull-up resistors are available at each end of the long line to provide a HIGH output when all connected buffers are non-conducting. These buffers allow fast, wide gating, optimum speed, and efficient routing of high fan-out signals. The following figure shows three-state buffers, long lines, and pull-up resistors.


Bi-Directional Interconnection Buffers
(Not Showing)
Global Net
3 Verticle Long Lines Per Column
GG
GH
P48
Horizontal Long Line Pull-Up Resistor
LL1
Horizontal Long Line (Not Showing)
LL2
Oscillator Amplifier Output
P47
Direct Input of P47 to Auxiliary Buffer
HG
x
y
HHA
BCL KIN
Crystal Oscillator Buffer
OS C
P46
Three-State Input
D M G M
Three-State Control
Three-State Buffer
Auxiliary Buffer
P40
P41
P42
P43
RST
Oscillator Amplifier Input

Crystal Oscillator

The previous figure also shows the location of an internal high-speed inverting amplifier that can be used as an on-chip crystal oscillator. It is associated with the auxiliary buffer in the lower right corner of the die. When the oscillator is configured as a signal source, two special user IOBs are also configured to connect the oscillator amplifier with external crystal oscillator components, as shown below.

When activated by selecting an output network for its buffer, the crystal oscillator inverter uses two of the package pins and external components to make an oscillator. An optional divide-by-two mode is available to ensure symmetry.



	68 Pin	84 Pin		175 Pin
	PLCC	PLCC	PGA	PGA
XTAL1 (Out)	47	57	J11	T14
XTAL2 (In)	43	53	L11	P15

A divide-by-two option is available to assure symmetry. The oscillator circuit becomes active before configuration is complete so the oscillator can stabilize. Actual internal connection is delayed until completion of configuration. In the preceding figure the feedback resistor, R1, between output and input biases the amplifier at threshold. The value should be as large as practical to minimize loading the

crystal. The inversion of the amplifier, together with the R-C networks and an AT cut series resonant crystal, produce the 360 degree phase shift of the Pierce oscillator. A series resistor, R2, can be included to increase the amplifier output impedance. This may be needed for phase shift control or crystal resistance matching, or to limit the amplifier input swing to control clipping at large amplitudes.

Excess feedback voltage can be corrected by the ratio of C2/C1. The amplifier can be used from 1 MHz to one-half the specified CLB toggle frequency. Used at frequencies below 1 MHz, the amplifier may require individual characterization with respect to a series resistance. Crystal oscillators operating at frequencies above 20 MHz usually require a crystal that operates in a third overtone mode, in which the fundamental frequency must be suppressed by the R-C networks. When the oscillator inverter is not used, these IOBs and their package pins are available for general user I/O.

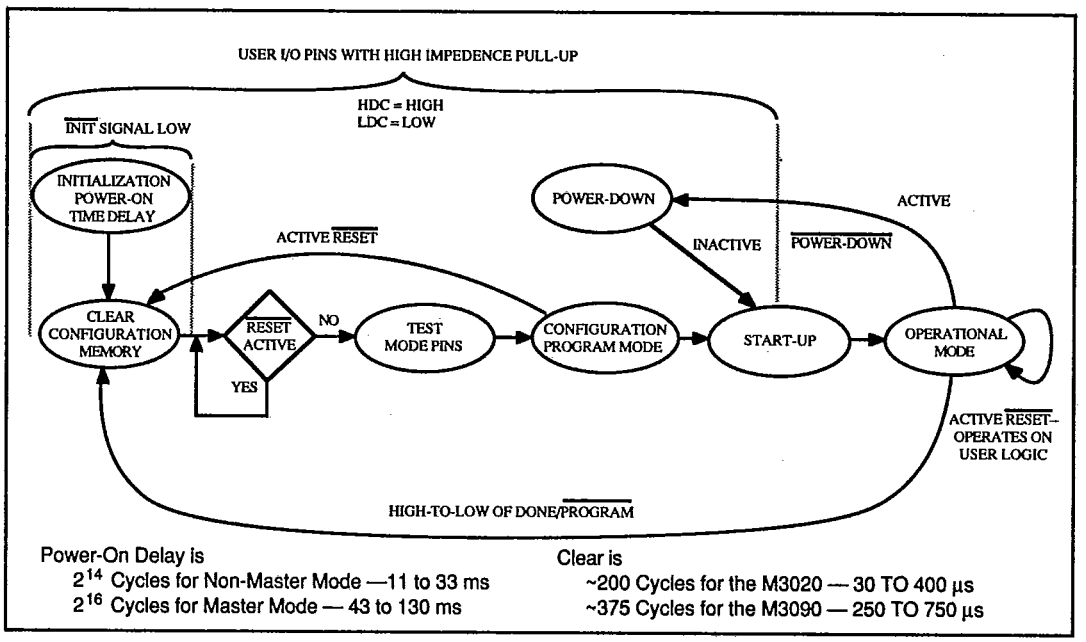
PROGRAMMING

Initialization

An internal power-on reset circuit is triggered when power is applied. When Vcc reaches the voltage at which portions of the LCA device begin to operate (2.5 to 3 V), the programmable I/O output buffers are disabled and a high impedance pull-up resistor is provided for the user I/O pins. A time-out delay is initiated to let the power supply voltage stabilize. During this time, the power-down mode is inhibited. The initialization state time-out (about 20 to 30 ms) is determined by a 14-bit counter driven by a self-generated, internal timer. This nominal 1 MHz timer is subject to variations as a result of process, temperature, and power supply from 0.5 to 1.5 MHz. As shown in the following table, five configuration modes are available, as determined by the input levels of three mode pins M0, M1, and M2.

M0	M1	M2	CLOCK	MODE	DATA
0	0	0	output	Master	Bit Serial
0	0	1	output	Master	Byte Wide (0000 up)
0	1	0	—	—	—
0	1	1	output	Master	Byte Wide (FFFF down)
1	0	0	—	—	—
1	0	1	input	Peripheral	Byte Wide
1	1	0	—	—	—
1	1	1	input	Slave	Bit Serial

In master configuration modes, the LCA device becomes the source of the configuration clock (CCLK). The beginning of configuration of devices using peripheral or slave modes must be delayed until they are initialized. An LCA device with mode lines selecting a master configuration mode extends its initialization state using four times the delay (80 to 120 ms). This ensures that all daisy-chained slave devices it may be driving will be ready. The next figure shows the sequence of states.

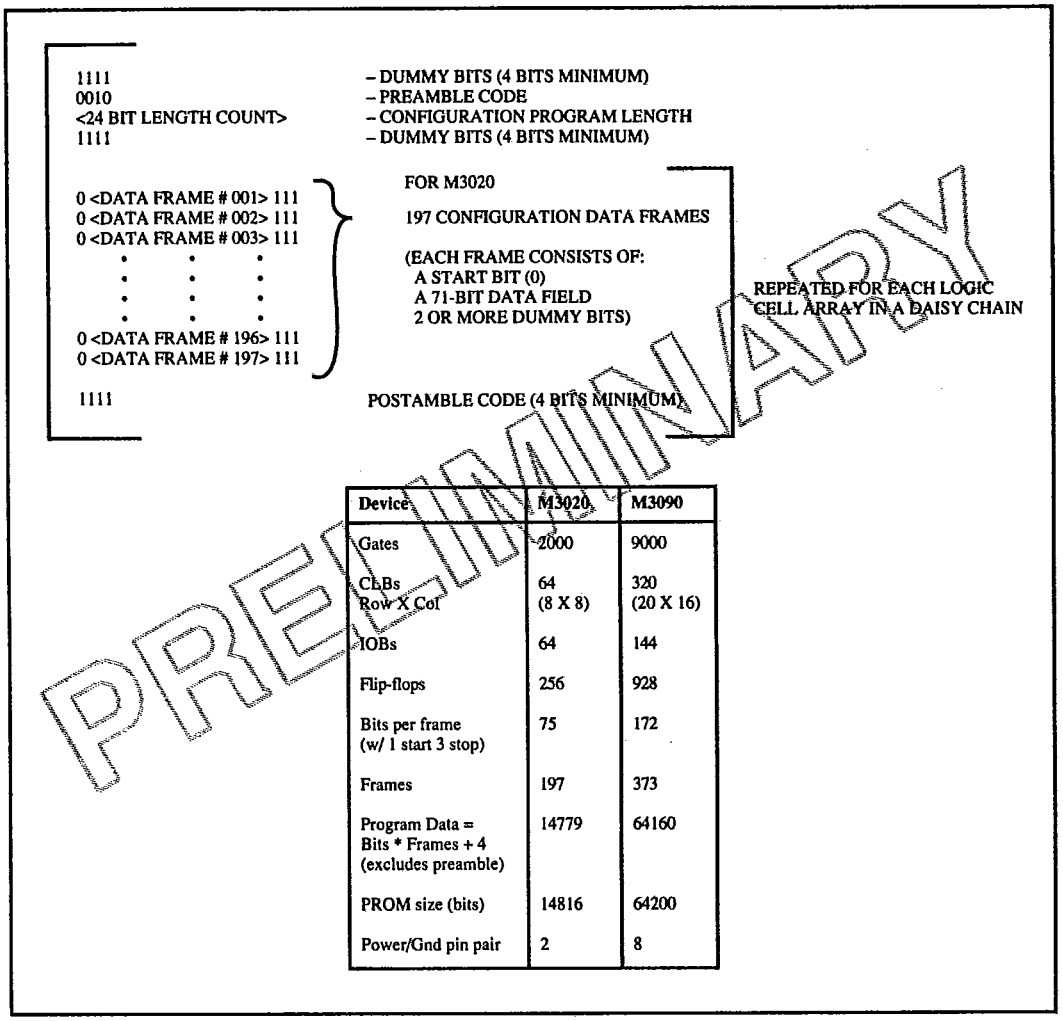


At the end of initialization, the LCA device enters the clear state, in which it clears the configuration memory. The active LOW, open-drain initialization signal, RDY/~INIT, indicates completion of the initialization and clear states. The LCA device tests for the absence of an external active LOW ~RESET before it makes a final sample of the mode lines and enters the configuration state. An external wired-AND of one or more ~INIT pins can be used to control configuration by the assertion of the active LOW ~RESET of a master mode device or to signal a processor that the LCA devices are not yet initialized.

If a configuration has begun, re-asserting ~RESET for at least three internal timer cycles is recognized, and the LCA device will abort the program, clearing the partially loaded configuration memory words. The LCA device will then re-sample ~RESET and the mode lines before re-entering the configuration state.

The configuration bit stream is initiated again when a configured LCA device senses a HIGH to LOW transition on the DONE/~PROG package pin. The LCA device returns to the clear state, in which the configuration memory is cleared and mode lines re-sampled, as for an aborted configuration. The complete configuration bit stream is cleared and loaded during each configuration cycle.

Length count control lets a system of multiple LCA devices, of various sizes, begin synchronized operation. The configuration bit stream generated by the MakePROM software of the XACT LCA Development System begins with a preamble of 11110010. This is followed by a 24-bit length count representing the total number of configuration clocks needed to complete loading of the configuration program(s). The data framing is shown in the following figure.

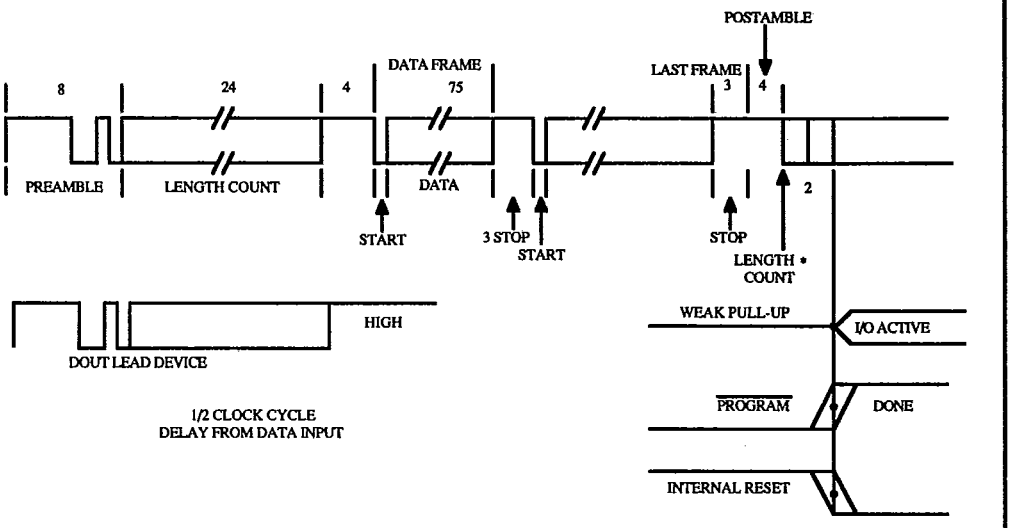


Device	M3020	M3090
Gates	2000	9000
CLBs Row X Col	64 (8 X 8)	320 (20 X 16)
IOBs	64	144
Flip-flops	256	928
Bits per frame (w/ 1 start 3 stop)	75	172
Frames	197	373
Program Data = Bits * Frames + 4 (excludes preamble)	14779	64160
PROM size (bits)	14816	64200
Power/Gnd pin pair	2	8

4

All LCA devices connected in series read and shift preamble and length count in on positive, and out on negative, configuration clock edges. An LCA device that has received the preamble and length count then presents a HIGH Data Out until it has intercepted the appropriate number of data frames. When the configuration memory of an LCA device is full and the length count does not compare, the LCA device shifts any additional data through in the same way it did for preamble and length count.

When the LCA configuration memory is full and the length count compares, the LCA device executes a synchronous start-up sequence and becomes operational, as shown below.



* THE CONFIGURATION DATA CONSISTS OF A COMPOSITE 36-BIT PREAMBLE/LENGTH-COUNT, FOLLOWED BY ONE OR CONCATENATED LCA PROGRAMS, SEPARATED BY 4-BIT POSTAMBLES. AN ADDITIONAL FINAL POSTAMBLE BIT IS ADDED FOR EACH SLAVE DEVICE AND THE RESULT ROUNDED UP TO A BYTE BOUNDARY. THE LENGTH COUNT IS TWO LESS THAN THE NUMBER OF RESULTING BITS.

TIMING OF THE ASSERTION OF DONE AND TERMINATION OF THE INTERNAL RESET MAY EACH BE PROGRAMMED TO OCCUR ONE CYCLE BEFORE OR AFTER THE I/O OUTPUTS BECOME ACTIVE.

Two CCLK cycles after the completion of loading configuration data, the user I/O pins are enabled as configured. As selected in MAKEBITS, the internal user-logic reset is released either one clock cycle before, or one clock cycle after the I/O pins become active. A similar timing selection is programmable for the DONE/~PROG output signal. DONE/~PROG can also be programmed to be an open drain or to include a pull-up resistor to accommodate wired ANDing. High During Configuration (HDC) and Low During Configuration (LDC) are two user I/O pins driven active when an LCA is initializing, clearing, or configuring. These pins and the DONE/~PROG commands provide signals for control of external logic signals such as reset, bus enable, or PROM enable during configuration. For parallel master configuration modes, these signals provide PROM enable control and let the data pins be shared with user logic signals.

User I/O inputs can be programmed for either TTL or CMOS compatible thresholds. At power-up, all inputs have TTL thresholds and can change to CMOS thresholds at the completion of configuration, if the user has selected CMOS thresholds. The threshold of ~PWRDWN and the direct clock inputs are fixed at the CMOS level.

If the crystal oscillator is used, it will begin operation before configuration is completed; this allows time for stabilization before the oscillator is connected to the internal circuitry.

Configuration Data

Configuration data to define the function and interconnection within an LCA device are loaded from an external storage at power-up and, if not inhibited, on a reprogram signal. Several methods of automatic and controlled loading of the required data are designed into the LCA device. Logic levels applied to mode selection pins at the start of configuration determine the method to be used. See the mode selection table above.

The format of the data can be either bit-serial or byte-parallel, depending on the configuration mode. Various AMD programmable gate arrays will have different sizes and numbers of data frames. To maintain compatibility between various device types of the AMD product line, the 3000 series LCA devices use formats compatible with the 2000 series. For the 3020, configuration requires 14779 bits, arranged in 197 data frames, for each device. An additional 36 bits are used in header, as shown in the previous figure. The specific data format for each device is produced by the MAKEBITS command of the XACT LCA Development System.

One or more of these files can then be combined and appended to a length count preamble and be transformed into a PROM format file by the MAKE PROM command of the XACT LCA Development System. An exception to the compatibility of the devices is that a 2000 series device cannot be used as the master for a 3000 series device if their DONE or RESET are programmed to occur after their outputs become active. The TIE option of MAKEBITS causes the unused block outputs to be defined as constant LOW levels that are used to drive the unused routing and block resources. Resources that might not be accessible to unused block outputs will then be added to FLAGNET, non-critical user nets. NORESTORE will retain the results of TIE for timing analysis with QUERYNET, before RESTORE returns the design to the untied condition. TIE can be omitted for quick breadboard iterations where a few additional mA of Icc are acceptable.

The configuration bit stream begins with HIGH preamble bits, a four-bit preamble code, and a 24-bit length count. When configuration is initiated, a counter in the LCA device is set to 0 and begins to count the total number of configuration clock cycles applied to the device. As each configuration data frame is supplied to the LCA device, it is internally assembled into a data word. As each data word is completely assembled, it is loaded in parallel into one word of the internal configuration memory array. The configuration loading process is completed when the current length count equals the loaded length count, and the required configuration bit stream data frames have been written. Internal user flip-flops are held reset during configuration.

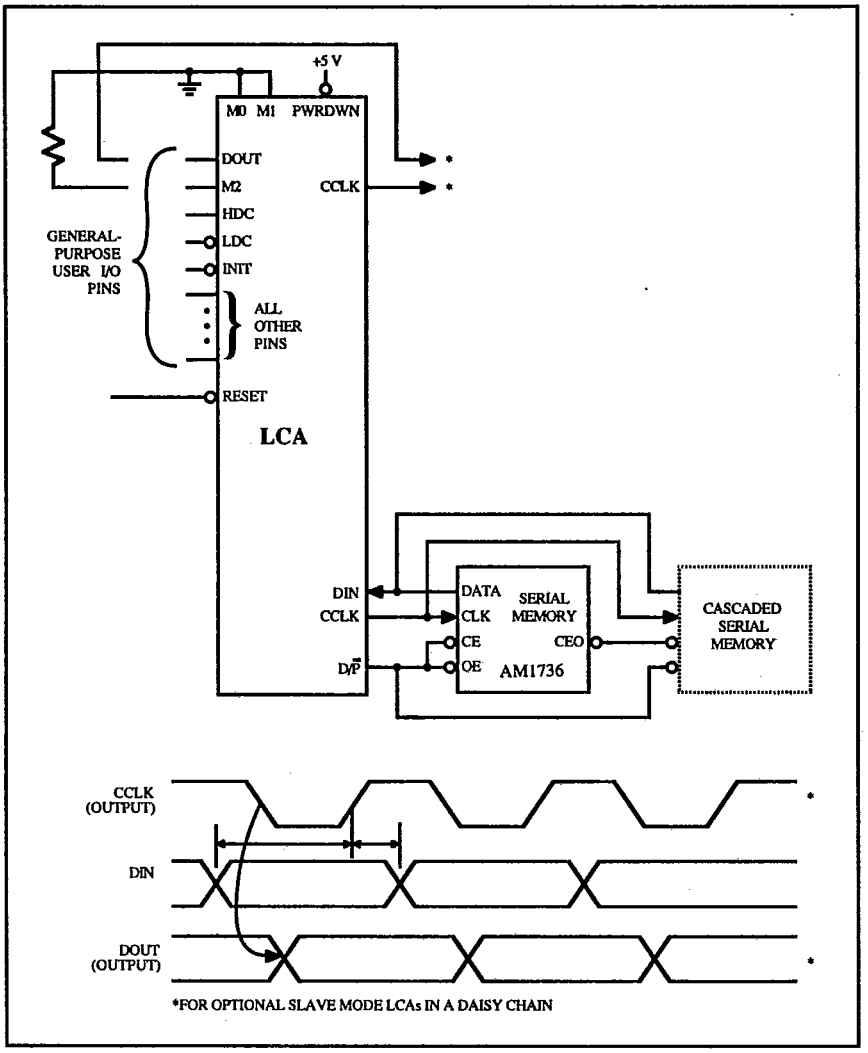
Two user-programmable pins are defined in the unconfigured LCA device. HDC and LDC, as well as DONE/~PROG, can be used as external control signals during configuration. In master mode configurations it is convenient to use LDC as an active-LOW EPROM Chip Enable. After the last configuration data-bit is loaded and the length count compares, the user I/O pins become active. Options in the MAKEBITS software allow timing choices of one clock earlier or later for the timing of the end of the internal logic reset and the assertion of the DONE signal. The open-drain DONE/~PROG output can be AND-tied with multiple LCA devices and used as an active HIGH READY, an active LOW PROM enable, or a RESET to other portions of the system.

Master Mode

In master mode, the LCA device automatically loads configuration data from an external memory device. There are three master modes that use the internal timing source to time the incoming data supplying the

configuration clock (CCLK). Serial master mode uses serial configuration data supplied to data-in (DIN) from a synchronous serial source such as the AMD Serial Configuration PROM (Am1736) shown below.

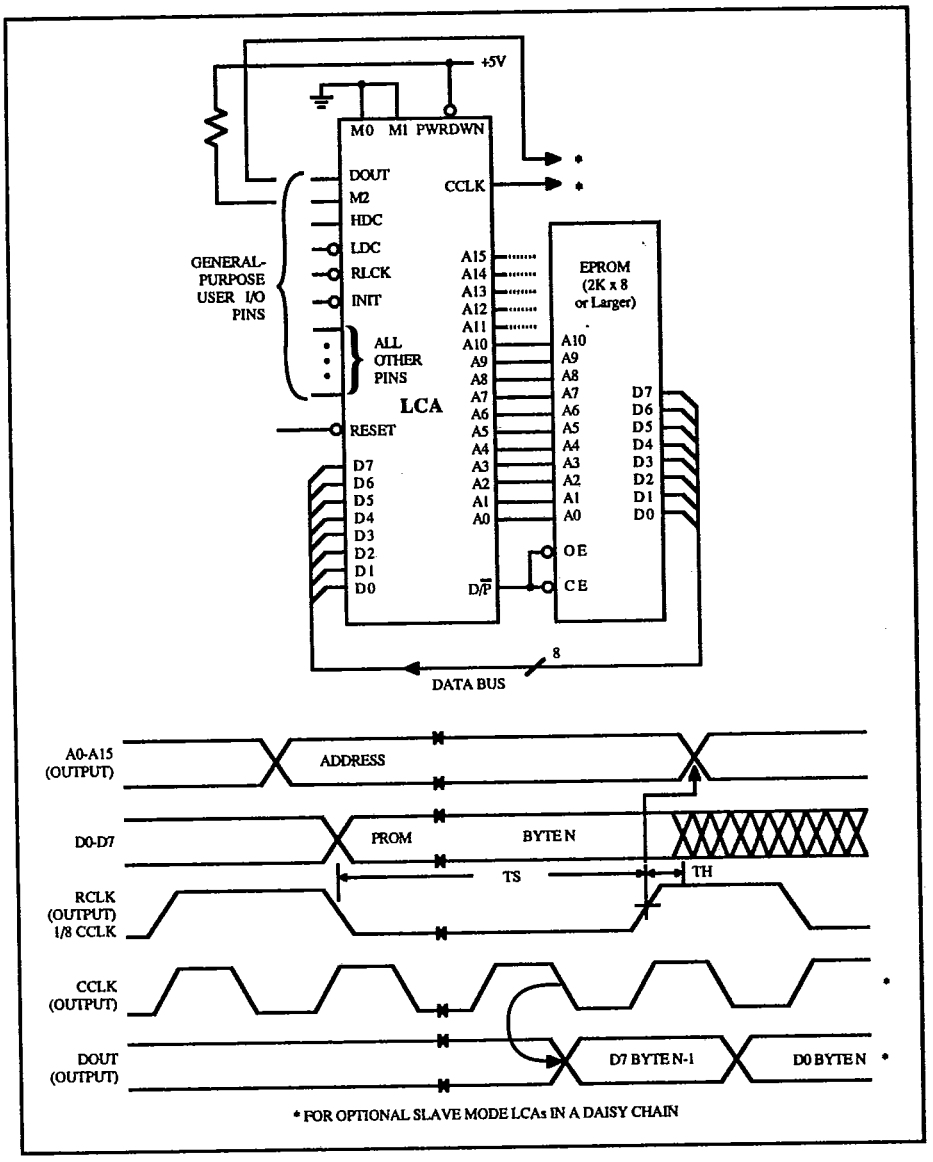
The one-time-programmable Am1736 Serial Configuration PROM supports automatic loading of configuration programs up to 36K bits. Multiple devices can be cascaded to support additional LCA devices. An early DONE inhibits the Am1736 data output one CCLK cycle before the LCA I/O becomes active.



Master LOW and master HIGH modes automatically use parallel data supplied to the D0-D7 pins in response to the 16-bit address generated by the LCA device. The next figure shows an example of the parallel master mode connections required. The LCA HEX starting address is 0000 and increments for master LOW mode. It is FFFF and decrements for master HIGH mode. These two modes provide address compatibility with microprocessors beginning execution from opposite ends of memory.

For master HIGH or LOW, data bytes are read in parallel by each read clock (RCLK) and internally serialized by the configuration clock. As each data byte is read, the least significant bit of the next byte, D0, becomes the next bit in the internal serial configuration word. One master mode LCA device can be used to interface the configuration program-store and pass additional concatenated configuration data to additional LCA devices in a serial daisy-chain fashion. CCLK is provided for the slaved devices and their serialized data is supplied from DOUT to DIN - DOUT to DIN, etc.

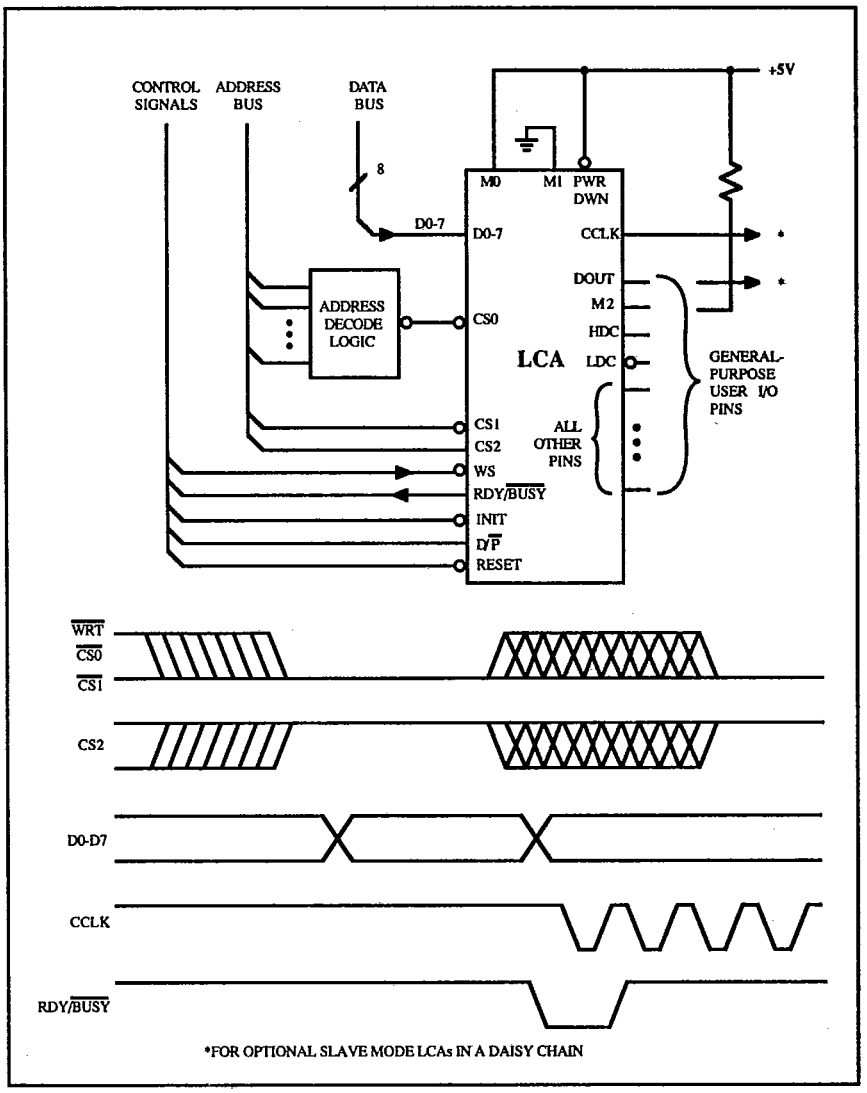
Configuration data are loaded automatically from an external byte wide PROM. An early DONE inhibits the PROM outputs a CCLK before the LCA I/O becomes active.


+5V
M0 M1 PWRDWN
DOUT
M2
HDC
LDC
RLCK
INIT
CCLK
GENERAL-PURPOSE USER I/O PINS
ALL OTHER PINS
LCA
RESET
D7 D6 D5 D4 D3 D2 D1 D0
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
D/P
EPROM (2K x 8 or Larger)
A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
D7 D6 D5 D4 D3 D2 D1 D0
OE
CE
8
DATA BUS
A0-A15 (OUTPUT)
ADDRESS
D0-D7
PROM
BYTE N
TS
TH
RCLK (OUTPUT) 1/8 CCLK
CCLK (OUTPUT)
DOUT (OUTPUT)
D7 BYTE N-1
D0 BYTE N
* FOR OPTIONAL SLAVE MODE LCAs IN A DAISY CHAIN

Peripheral Mode

Peripheral mode provides a simplified interface through which the device can be loaded byte-wide, as a processor peripheral. The next figure shows the peripheral mode connections. Processor write cycles are decoded from the common assertion of the active LOW Write Strobe (~WRT), and two active LOW and one active HIGH Chip Selects (~CS0, ~CS1, CS2). If all these signals are not available, the unused inputs should be driven to their respective active levels. The LCA device accepts one byte of configuration data on the D0-D7 inputs for each selected processor write cycle. Each byte of data is loaded into a buffer register.

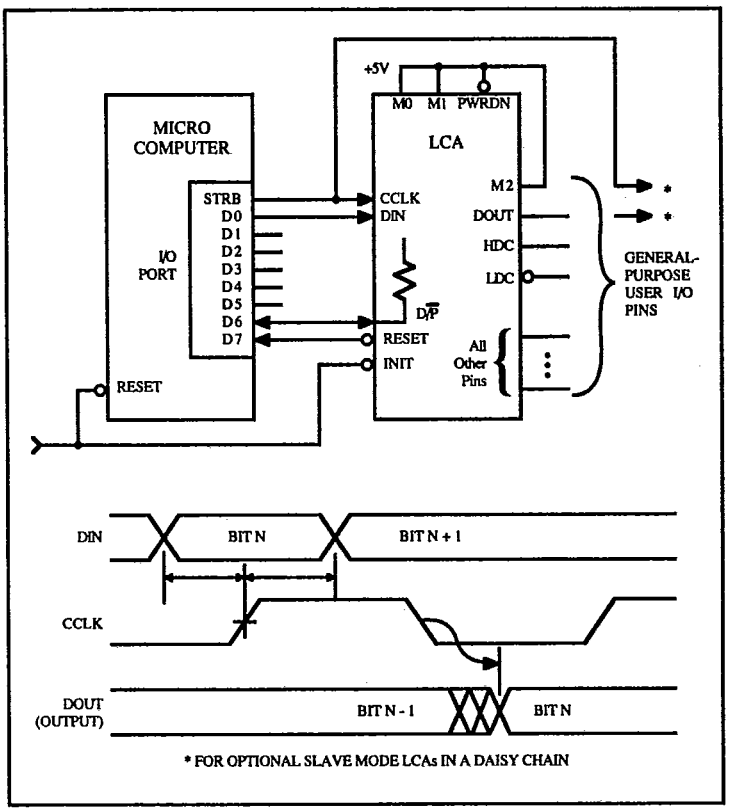
The LCA device generates a configuration clock from the internal timing generator and serializes the parallel input data for internal framing or for succeeding slaves on Data Out (DOUT). An output HIGH on the READY/~BUSY pin indicates completion of loading for each byte and that the input register is ready for a new byte. As with master modes, peripheral mode can also be used as a lead device for a daisy-chain of slave devices.


CONTROL SIGNALS
ADDRESS BUS
DATA BUS
8
D0-7
+5V
M0
M1
PWR DWN
D0-7
CCLK
DOUT
M2
HDC
LDC
ADDRESS DECODE LOGIC
CS0
LCA
GENERAL-PURPOSE USER I/O PINS
ALL OTHER PINS
CS1
CS2
WS
RDY/BUSY
INIT
D/P
RESET
WRT
CS0
CS1
CS2
D0-D7
CCLK
RDY/BUSY
*FOR OPTIONAL SLAVE MODE LCAs IN A DAISY CHAIN

Slave Mode

Slave mode provides a simple interface for loading the LCA device configuration, as shown below. Data are supplied in conjunction with a synchronizing input clock. Bit-serial data configuration are read at rising edge of the CCLK. Data on DOUT are provided on the falling edge of CCLK.

Most slave mode applications are in daisy-chain configurations in which the data input are supplied by the previous LCA's data out, while the clock is supplied by a lead device in master or peripheral mode. Data can also be supplied by a processor or other special circuits.

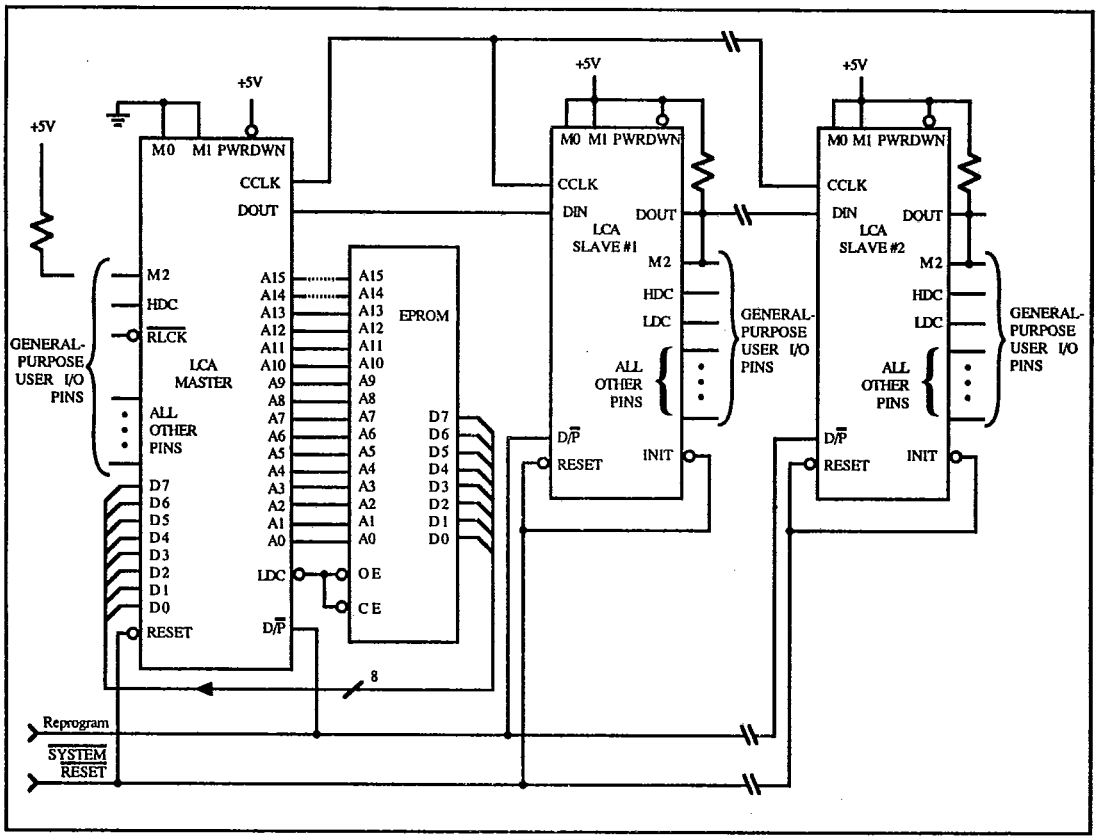


Daisy-Chain

The AMD XACT LCA Development System is used to create a composite configuration bit stream for selected LCA devices. This configuration includes the following:

- A preamble
- A length count for the total bit stream
- Multiple concatenated data programs
- A postamble
- An additional fill bit per device in the serial chain

After loading and passing on the preamble and length count to a possible daisy-chain, a lead device will load its configuration data frames while providing a HIGH DOUT to possible down-stream devices as shown below. In this figure, all are configured from the common EPROM source. The slave mode device ~INIT signals delay the master device configuration until they are initialized. A well defined termination of SYSTEM RESET is needed when controlling multiple LCA devices.



Loading continues until the current length count has reached the full value. The additional data are passed through the lead device and appear on the DOUT pin in serial form. The lead device also

generates the CCLK to synchronize the serial output data and data in of LCA devices further attached. Data are read in on DIN of slave devices by the positive edge of CCLK and shifted out the DOUT on the negative edge of CCLK. A parallel master mode device uses its internal timing generator to produce an internal CCLK of eight times its EPROM address rate, while a peripheral mode device produces a burst of eight CCLKs for each chip select and write-strobe cycle. The internal timing generator continues to operate for general timing and synchronization of inputs in all modes.

SPECIAL CONFIGURATION FUNCTIONS

The configuration data include control over several special functions, in addition to the normal user logic functions and interconnections.

- Input thresholds
- Readback enable
- DONE pull-up resistor
- DONE timing
- RESET timing
- Oscillator frequency divided-by-two

Each of these functions is controlled by configuration data bits selected as part of the normal XACT LCA Development System bit-stream generation process.

Input Thresholds

Prior to the completion of configuration, all LCA input thresholds are TTL compatible. Upon completion of configuration, the input thresholds become either TTL or CMOS compatible, as programmed. The use of the TTL threshold option requires some additional supply current for threshold shifting. The exception is the threshold of the ~PWRDWN input and direct clocks that always have a CMOS input. Prior to the completion of configuration, the user I/O pins have a high impedance pull-up. The configuration bit stream can be used to enable the IOB pull-up resistors in the operational mode to act either as an input load or to avoid a floating input on an otherwise unused pin.

Readback

The contents of an LCA device can be read back if it has been programmed with a bit stream in which the Readback option has been enabled. Readback can be used for verification of configuration, as well as a method of determining the state of internal logic nodes during debugging with the XACTOR In-Circuit debugger. There are three options in generating the configuration bit stream.

- **Never** inhibits the Readback capability.
- **One-time** inhibits Readback after one Readback has been executed to verify the configuration.
- **On-command** permits unrestricted use of Readback.

Readback is done without the use of any of the user I/O pins; only M0, M1, and CCLK are used. The initiation of readback is produced by a LOW to HIGH transition of the M0/RTRIG (Read Trigger) pin. Once the READBACK command has been given, the input CCLK is driven by external logic to read back each data bit in a format similar to loading. After two dummy bits, the first data frame is shifted out, in inverted sense, on the M1/~RDATA (Read Data) pin. All data frames must be read back to complete the process and return the mode select and CCLK pins to their normal functions.

The readback data includes the current state of each internal logic block storage element, and the state of the .i and .ri connection pins on each IOB. These data are imbedded into unused configuration bit positions during readback. This state information is used by the XACT LCA Development System In-Circuit Verifier to provide visibility into the internal operation of the logic while the system is operating. To readback a uniform time-sample of all storage elements it may be necessary to inhibit the system clock.

Reprogram

To initiate a reprogramming cycle, the dual function package pin DONE/~PROG must transition from HIGH to LOW . To reduce noise sensitivity, the input signal is filtered for two cycles of the LCA's internal timing generator. When reprogram begins, the user programmable I/O output buffers are disabled, and high impedance pull-ups are provided for the package pins. The device returns to the clear state and clears the configuration memory before it is initialized.

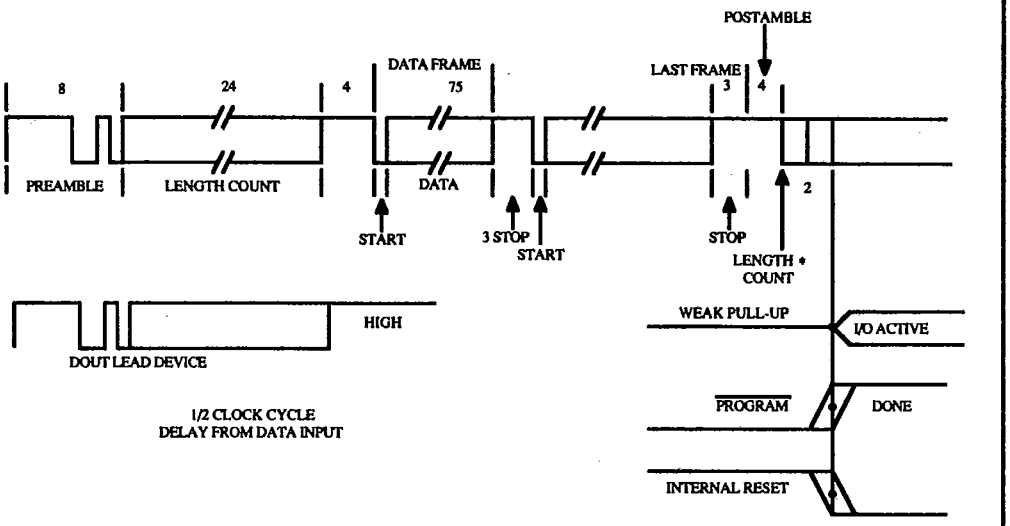
Reprogram control is often exercised using an external open collector driver that pulls DONE/~PROG LOW. Once it recognizes a stable request, the LCA device holds a LOW until the new configuration has been completed. Even if the reprogram request is externally held LOW beyond the configuration period, the LCA device will begin operation upon completion of configuration.

DONE Pull-up

DONE/~PROG is an open drain I/O pin indicating that the LCA device is operational. An optional internal pull-up resistor can be enabled by the user of the XACT LCA Development System when MakeBits is executed. The DONE/~PROG pins of multiple LCA devices in a daisy-chain can be connected to indicate all are DONE or to direct them to reprogram.

DONE Timing

By a selection in the MakeBits program, the timing of the DONE status signal can be controlled to occur one CCLK cycle before, or one cycle after, the timing of outputs are activated. This is shown below. This facilitates control of external functions such as a PROM enable or holding a system in a wait state.



* THE CONFIGURATION DATA CONSISTS OF A COMPOSITE 36-BIT PREAMBLE/LENGTH-COUNT, FOLLOWED BY ONE OR CONCATENATED LCA PROGRAMS, SEPARATED BY 4-BIT POSTAMBLES. AN ADDITIONAL FINAL POSTAMBLE BIT IS ADDED FOR EACH SLAVE DEVICE AND THE RESULT ROUNDED UP TO A BYTE BOUNDARY. THE LENGTH COUNT IS TWO LESS THAN THE NUMBER OF RESULTING BITS.

TIMING OF THE ASSERTION OF DONE AND TERMINATION OF THE INTERNAL RESET MAY EACH BE PROGRAMMED TO OCCUR ONE CYCLE BEFORE OR AFTER THE I/O OUTPUTS BECOME ACTIVE.

4

RESET Timing

As with DONE timing, the timing of the release of the internal RESET can be controlled by a selection in the MakeBits program. It then occurs one CCLK cycle before, or one cycle after, the timing of outputs are enabled, as shown above. This reset maintains all user-programmable flip-flops and latches in a zero state during configuration.

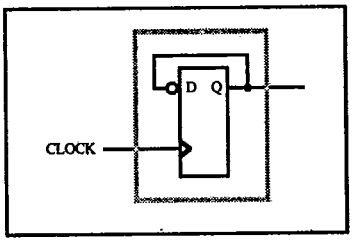
Crystal Oscillator Division

A selection in the MakeBits software lets the user incorporate a dedicated divide-by-two flip-flop in the crystal oscillator function. This helps ensure a symmetrical timing signal. Although the frequency stability of crystal oscillators is high, the symmetry of the waveform can be affected by bias or feedback drive.

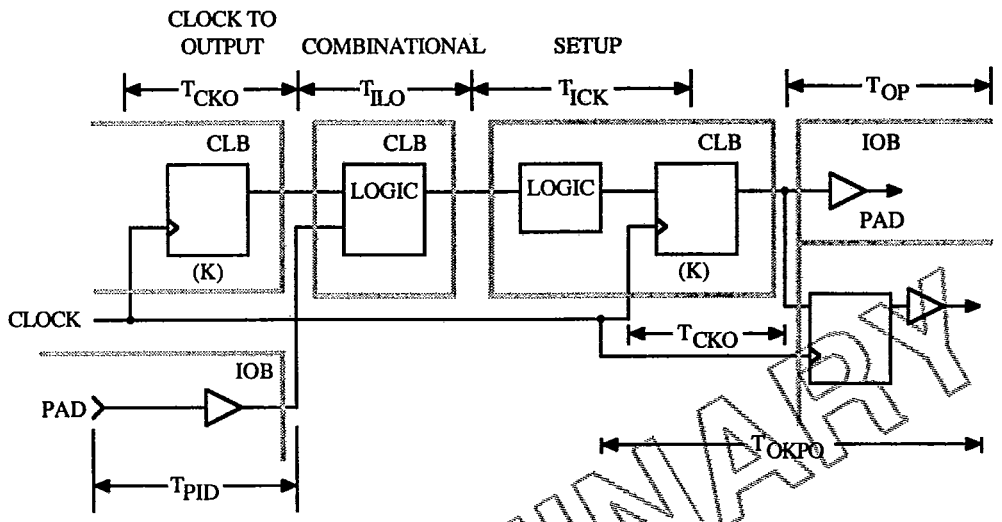
PERFORMANCE

Device Performance

The high performance of the LCA device is due in part to the manufacturing process, which is similar to that used for high-speed CMOS static memories. Performance can be measured in terms of minimum propagation times for logic elements. The parameter that traditionally describes the overall performance of a gate array is the toggle frequency of a flip-flop. The configuration for determining the toggle performance of the LCA device is shown below. The flip-flop output Q is fed back through the combinational logic as ~Q to form the toggle flip-flop.



Actual LCA device performance is determined by the timing of critical paths, including both the fixed timing for the logic and storage elements in that path, as well as the timing associated with the network routing. Examples of internal worst-case timing are included in the performance data to let the user to make the best use of the device's capabilities. The XACT LCA Development System timing calculator, or LCA generated simulation models, should be used to calculate worst-case paths by using actual impedance and loading information. The following figure shows a variety of elements used involved in determining system performance.



		Speed Grade	-50		-70			Units
	Description	Symbol	Min	Max	Min	Max		
Logic input to Output	Combinational	T_{ILO}		14		9		ns
K Clock	To output	T_{CKO}		12		8		ns
	Logic-input setup	T_{ICK}	12		8			ns
	Logic-input hold	T_{CKI}	0		0			ns
Input/Output	Pad to input (direct)	T_{PID}		10		7		ns
	Output to pad (enabled)	T_{OP}		14		10		ns
	I/O clock to pad	T_{OKPO}		18		13		ns
FF toggle frequency		F_{CLK}		50		70		MHz

The speed of internal elements is determined by differential measurements of package pins. The performance of a user's design can be predicted by the XACT LCA Development System delay calculator.

Actual measurement of internal timing is not practical; often only the sum of component timing is relevant, as in the case of input to output. The relationship between input and output timing is arbitrary; only the total determines performance. Timing components of internal functions can be determined by measuring the differences at the pins of the package. A synchronous logic function with a clock-to-block output, and a block-input to clock set-up, is capable of higher speed operation than a logic configuration of two synchronous blocks with an extra combinational block level between them. System clock rates to 60% of the toggle frequency are practical for logic in which there is an extra combinational level located between synchronized blocks. This permits implementation of functions of up to 25 variables. The use of the wired-AND is also available for wide, high-speed functions.

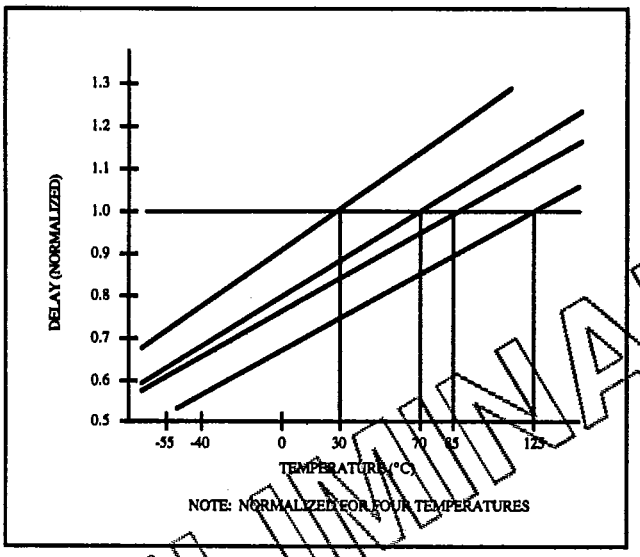
Logic Block Performance

Logic block performance is expressed as the propagation time from the interconnection point at the input of the combinational logic, to the output of the block in the interconnection area. Combinational performance is independent of the specific logic function, which is based on look-up tables.

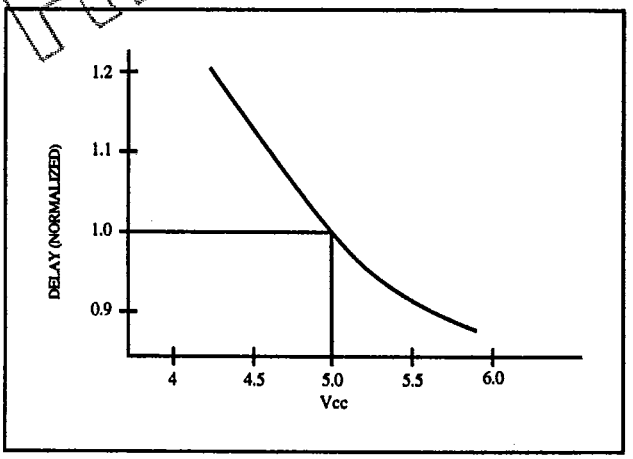
The only parameter for all logic functions is the Logic Input to Output delay. For combinational logic used in conjunction with the storage element, however, there are two critical parameters. First, for the combinational logic function driving the data input of the storage element, the critical timing is data setup relative to the clock edge provided to the flip-flop. Second, for the signals then produced by the storage elements, the critical timing is the Clock to Output delay. These parameters are shown in the previous figure.

Loading of a logic block output is limited only by the resulting propagation delay of the larger interconnection network. Speed performance of the logic block is a function of the supply voltage and the temperature, as shown in the next two figures.

The following figure shows the change in speed performance as a function of temperature. The variation is normalized for 30° C, 70° C, 85° C, and 125° C.



The following figure shows how the speed performance of a CMOS device increases with Vcc within the operating range.



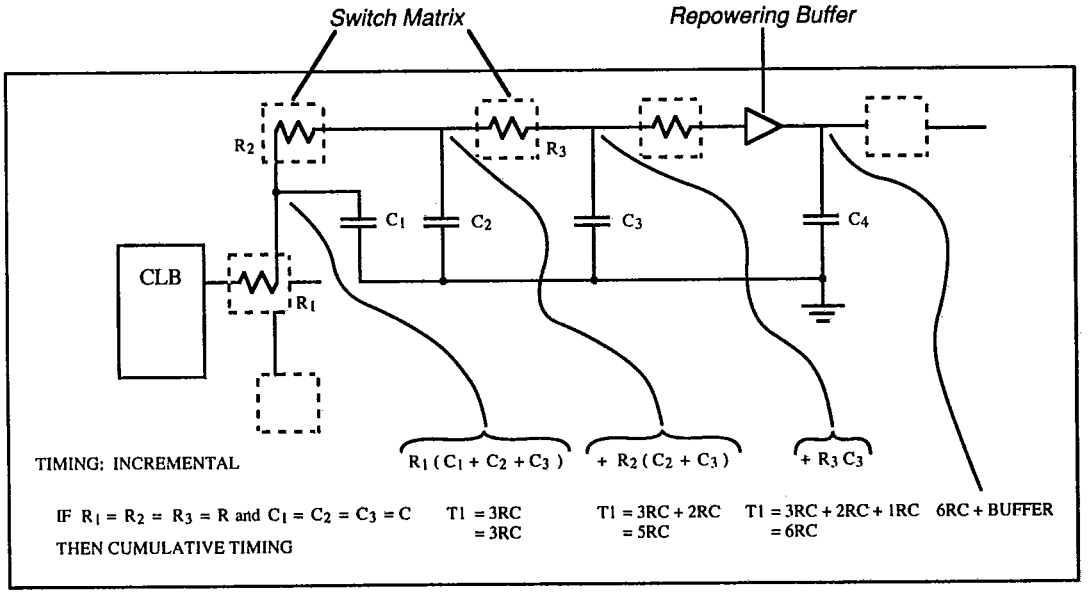
Interconnection Performance

Interconnection performance depends on the routing resource used for the signal path. As discussed earlier, direct interconnection from block to block provides a fast path for a signal. The single metal segment used for long lines exhibits low resistance from end to end, but relatively high capacitance. Signals driven through a programmable switch will have the additional impedance of the switch added to their normal drive impedance.

General purpose interconnection performance depends on the number of switches and segments used, the presence of the bidirectional re-powering buffers, and the loading at all points on the signal path. In calculating the worst-case timing for a general interconnection path, the timing calculator portion of the XACT LCA Development System takes all of these elements into account.

As an approximation, interconnection timing is proportional to the summation of totals of local metal segments beyond each programmable switch. In effect, the time is a sum of R-C time, each approximated by an R times the total C it drives. The R of the switch and the C of the interconnection are functions of the particular device performance grade.

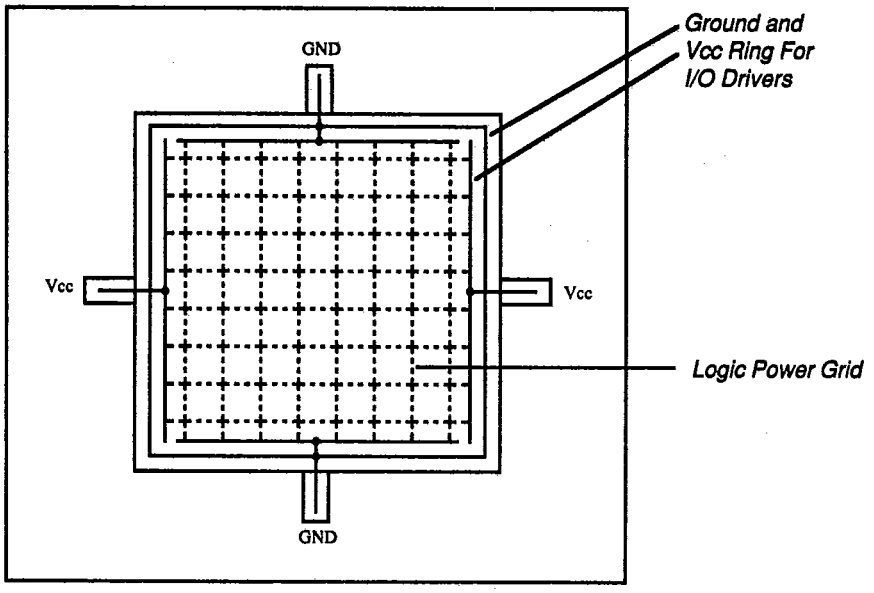
For a string of three local interconnections, the approximate time at the first segment (after the first switch resistance) would be three units; after the next switch there are an additional two units; and there is an additional unit after the last switch in the chain. The interconnection R-C chain terminates at each re-powering buffer. The capacitance of the block inputs is not significant; the capacitance is in the interconnection metal and switches, as shown in the following figure.



POWER

Power Distribution

Power for the LCA device is distributed through a grid to achieve high noise immunity and isolation between the logic and I/O. Inside the LCA device, a dedicated Vcc and ground ring surrounding the logic array provide power to the I/O drivers, as shown below. An independent matrix of Vcc and ground lines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic; this assumes that the external package power pins are all connected and appropriately decoupled. Usually, a 0.1 µF capacitor connected near the Vcc and ground pins of the package will provide adequate decoupling.

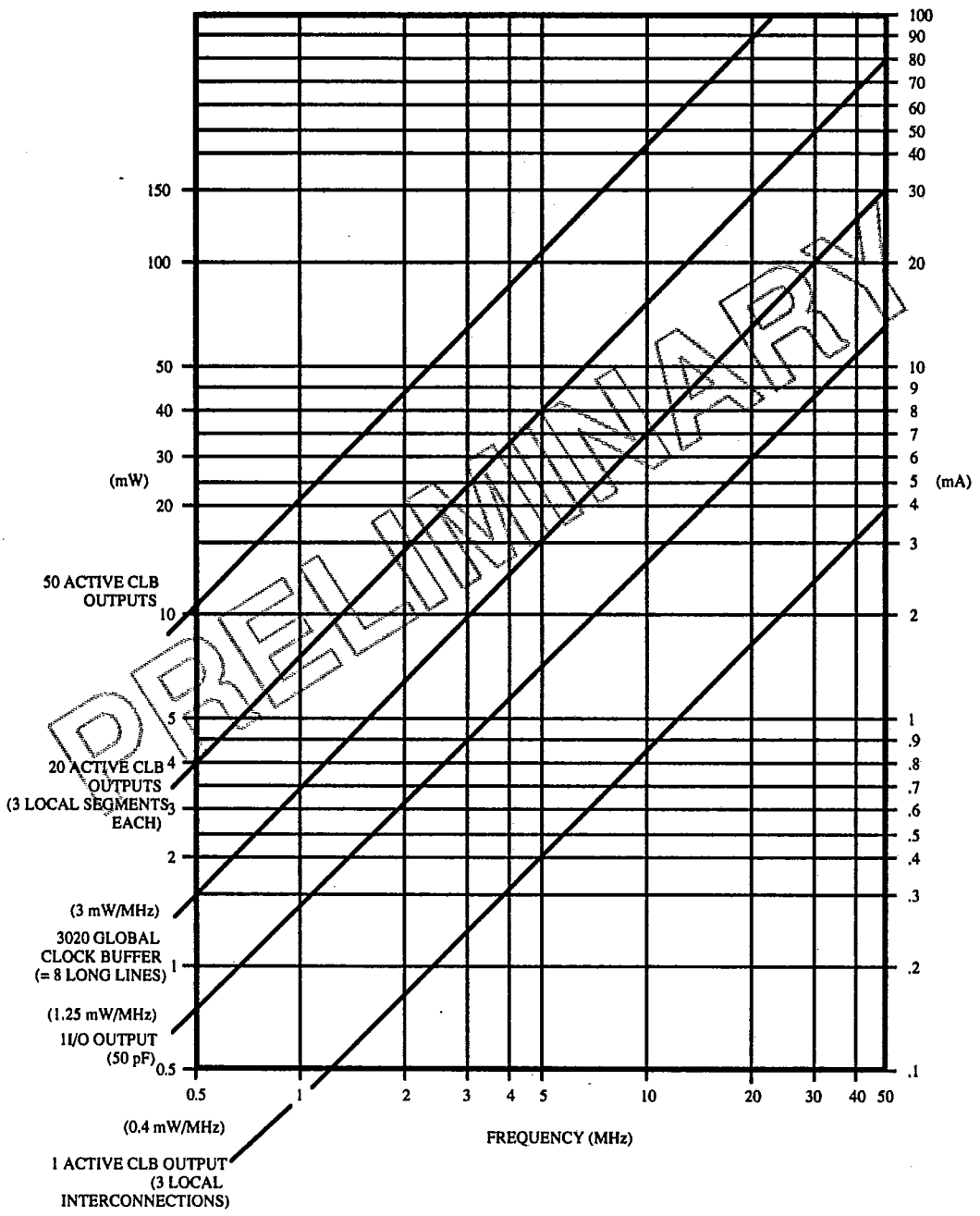


Output buffers capable of driving the specified 4 mA loads under worst-case conditions can be capable of driving 25 to 30 times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. Also, it may be beneficial to locate heavily loaded output buffers near the ground pads. The IOB output buffers have a slew-limited mode that should be used where output rise and fall times are not speed critical. A lower AC drive current reduces transition and supply noise without a corresponding reduction in DC drive. A maximum of 32 simultaneously switching outputs is allowed.

Power Dissipation

The LCA device exhibits the low power consumption characteristic of CMOS ICs. For any design, the user can use the figure below to calculate the total power requirement based on the sum of the external and internal capacitive and DC loads. The total chip power is the sum of Vcc•Icco, plus internal and external values of capacitive charging currents and resistive loads.

The configuration options of TTL chip input threshold requires power for the threshold reference. The power required by the static memory cells holding the configuration data is very low and can be maintained in a power-down mode.


150
100
50
40
30
(mW)
20
10
5
4
3
2
1
0.5
50 ACTIVE CLB OUTPUTS
20 ACTIVE CLB OUTPUTS (3 LOCAL SEGMENTS EACH)
(3 mW/MHz)
3020 GLOBAL CLOCK BUFFER (= 8 LONG LINES)
(1.25 mW/MHz)
1I/O OUTPUT (50 pF)
(0.4 mW/MHz)
1 ACTIVE CLB OUTPUT (3 LOCAL INTERCONNECTIONS)
0.5
1
2
3
4
5
10
20
30
40
50
FREQUENCY (MHz)
100
90
80
70
60
50
40
30
20
10
9
8
7
6
5
4
3
2
1
.9
.8
.7
.6
.5
.4
.3
.2
.1
(mA)
PRELIMINARY

Usually, most power dissipation is produced by external capacitive loads on the output buffers. The load- and frequency-dependent power is 25 µW/pF/MHz per output. Another component of I/O power is the DC loading on each output pin by LCA-driven devices.

Internal power dissipation is a function of the number and size of the nodes, and the frequency at which they change. In an LCA device, the fraction of nodes changing on a given clock is typically low (10-20%). For example, in a large binary counter, the average clock cycle produces changes equal to one CLB output at the clock frequency. In a 4-input AND gate, there will be two transitions in 16 states. Typical global clock buffer power is about 3 mW/MHz. The internal capacitive load is more a function of interconnection than fanout. With typical load of three general interconnection segments, each CLB output requires about 0.4 mW/MHz of its output frequency.

Total power = Vcc • Icco + external (DC + capacitive) + internal (CLB + IOB+ Long Line+ pull-up)

Because the control storage of the LCA device is CMOS static memory, its cells require a very low standby current for data retention. In some systems, this characteristic can be used as a method of preserving configurations in the event of a primary power loss. The LCA device has built in power-down logic that, when activated, will disable normal operation of the device and retain only the configuration data. All internal operation is suspended and output buffers are placed in a high impedance state with no pull-ups. Power-down data retention is possible with a simple battery-backup circuit because the power requirement is extremely low. For retention at 2.4 V, the required current is typically on the order of 50 nA.

To force the LCA device into the power-down state, the user must pull the ~PWRDWN pin LOW and continue to supply a retention voltage to the Vcc pins of the package. When normal power is restored, Vcc is increased to its normal operating voltage and ~PWRDWN is returned to HIGH. The LCA device resumes operation with the same internal sequence that occurs at the conclusion of configuration. Internal I/O and logic block storage elements will be reset, the outputs will become enabled, and the DONE/~PROG pin will be released. No configuration programming is required.

When the power supply is removed from a CMOS device, it is possible to supply some power from an input signal. The conventional electrostatic input protection is provided by diodes to the supply and ground. A positive voltage applied to an input or output will cause the positive protection diode to conduct and drive the power pin. This condition can produce invalid power conditions and should be avoided. A large series resistor can be used to limit the current, or a bi-polar buffer can be used to isolate the input signal.

DEVELOPMENT SYSTEMS

To implement your system application on the LCA device, AMD provides a wide host of software packages. These packages are primarily IBM-PC/AT based and allow the entire programmable gate array design cycle to be completed inexpensively and quickly at the system designer's desk. The packages provide the following capabilities.

- Schematic capture
- PALASM™ Boolean entry
- Large number of predefined macro library elements
- Automatic logic conversion and reduction
- Logic and electrical rule checking

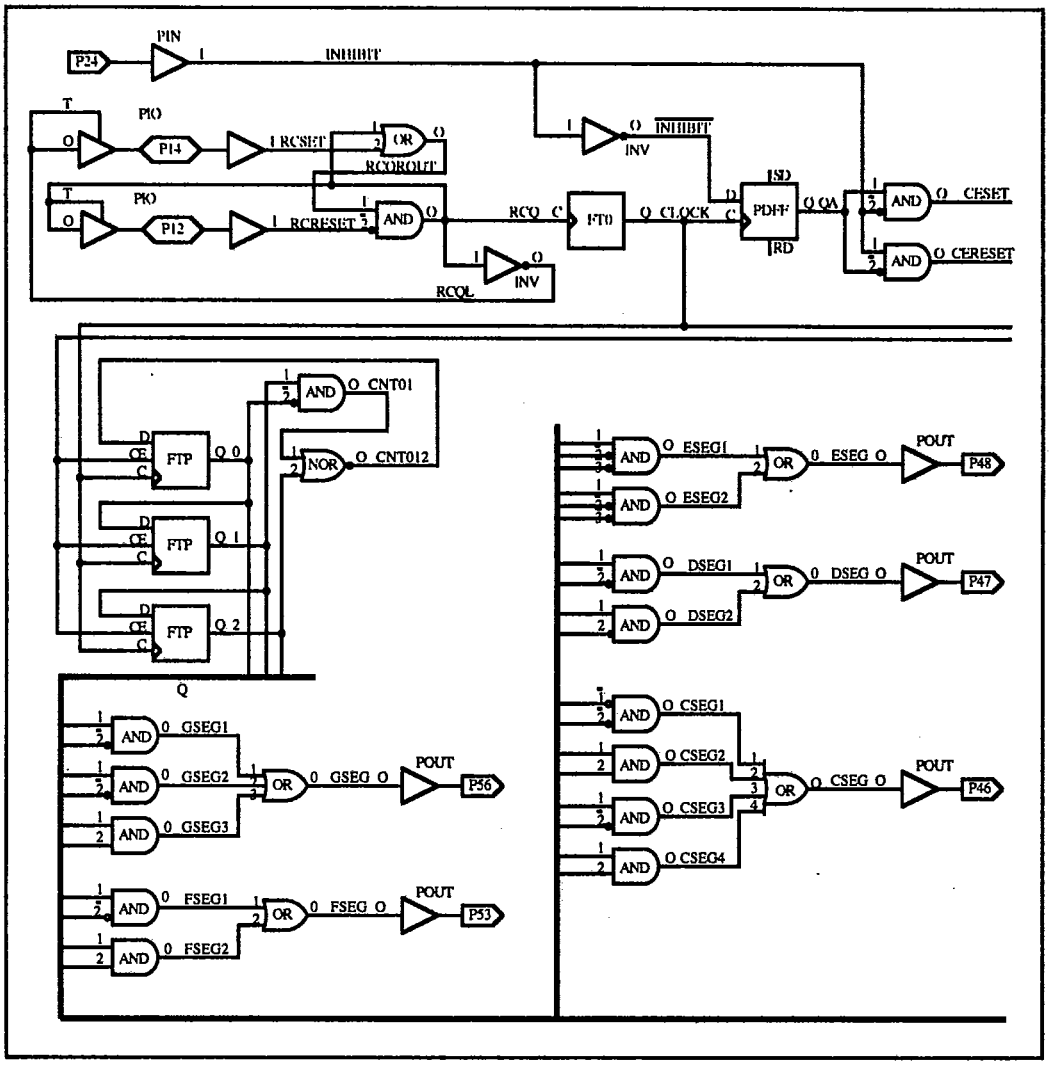
- Logic partitioning
- Automatic placement and routing
- Interactive timing calculator
- Logic and timing simulation interfaces
- Automatic design documentation
- Interactive design editing and optimization
- PROM programmer format output capabilities
- In-system design verification for multiple arrays

The XACT LCA Design Editor is hosted on an IBM-PC/AT system with DOS 3.0 or higher. The system requires 640K bytes of internal RAM, 1.5 MBytes of extended memory, color graphics, and a mouse. The complete system requires one parallel I/O port and two serial ports for the mouse and in-system emulator.

Design Entry

Design entry can be accomplished with popular schematic editors. Popular engineering workstations such as Daisy or Mentor are also supported. Additionally, designs can be entered and configured manually with the XACT Design Editor, or through Boolean expressions via PALASM programmable logic language.

The following figure shows a partial sample of a entering a design via schematic capture.



Design Implementation

Following design entry, logic designs can be automatically converted, reduced, partitioned, placed, and routed with the Automatic Design Implementation (ADI) software packages. For those designs that are not completely automatic, the XACT Design Editor can be used to manually complete or optimize the design. Following layout, various design and electrical rules are checked automatically by the software, producing a valid design file. This file contains all the programming data used to download directly into

an LCA device in the user's target system. The programming information can be used to program PROM, EPROM, or ROM devices, or stored in other media, as needed by the final system.

Design Verification

Design verification can be accomplished by using the AMD XACTOR In-System Emulator directly in the target system. Also, the ADI packages provide output data that can be accepted by popular simulators such as P-SILOS for complete logic and timing simulation. If design changes are required, the changes can be implemented in minutes at the designer's desk.

PIN DESCRIPTIONS

~PWRDWN

An active LOW power down input stops all internal activity to minimize Vcc power and puts all output buffers in a high impedance state. Configuration is retained, however, internal storage elements are Reset. When the ~PWRDWN pin returns HIGH, the device returns to operation with the same sequence of Reset, buffer enable, and DONE/~PROGRAM as at the completion of configuration.

M0

As Mode 0, this input and M1 M2 are sampled before the start of configuration to establish the configuration mode to be used.

or

RTRIG

As a Read Trigger, after configuration is complete, an input transition to a HIGH will initiate a Readback of configuration and storage element data by CCLK. This operation can be limited to a single request, or can be inhibited altogether, by selecting the appropriate readback option when generating the bit stream.

M1

As Mode 1, this input, M0, and M2 are sampled before the start of configuration to establish the configuration mode.

or

~RDATA

As an active LOW Read Data, this pin is the output of the readback data after configuration is complete.

M 2

As Mode 2 this input, M0, and M1 are sampled before the start of configuration to establish the configuration mode. After configuration, this pin becomes a user-programmable I/O pin.

HDC

High During Configuration is held at a HIGH level by the LCA device until after configuration. It is intended to be available as a control indication that configuration is not completed. After configuration, this pin is a user I/O pin.

LDC

Low During Configuration is held at a LOW level by the LCA device until after configuration. It is intended to be available as a control indication that configuration is not completed. It is particularly useful in master mode as a LOW enable for an EPROM. After configuration, this pin is a user I/O pin. If used as a LOW EPROM enable, it would need to be programmed as a HIGH after configuration.

~INIT

This is active LOW open collector output is held LOW during the power stabilization and internal clearing of the configuration memory. It can be used to indicate status to a configuring microprocessor or, as a wired-AND of several slave mode devices, a hold-off signal for a master mode device. After configuration, this pin becomes a user programmable I/O pin.

~RESET

This active LOW input has three functions. Prior to the start of configuration, a LOW input will delay the start of configuration. An internal circuit senses the application of power and begins a minimal time-out cycle. When the time-out and ~RESET are complete, the levels of the M lines are sampled and configuration begins. If ~RESET is asserted during a configuration , the LCA device is re-initialized and will restart the configuration at the termination of ~RESET. If ~RESET is asserted after configuration is complete, it will provide an asynchronous reset of all IOB and CLB storage elements of the LCA device.

DONE

The DONE output is configurable as an open drain with or without a pull-up resistor. At the completion of configuration, the circuitry of the LCA device becomes active in a synchronous order, and DONE can be programmed to occur one cycle before or after.

~PROG

Once configuration is completed, a HIGH-to-LOW transition of this pin will cause an initialization of the LCA device and start a reconfiguration.

XTL1

This user I/O pin can be configured to operate as the output of an amplifier usable with an external crystal and bias circuitry.

XTL2

This user I/O pin can be configured to operate as the input of an amplifier usable with an external crystal and bias circuity.

CCLK

During configuration, Configuration Clock is an output of an LCA device in master mode or peripheral mode. LCA devices in slave mode use it as a clock input. During a Readback operation, it is an input clock for the configuration data being output.

DOUT

This user I/O pin is used during configuration to output serial configuration data for the Data In of daisy-chained slaves.

DIN

This user I/O pin is used as serial Data In during slave or master serial configuration. This pin is D0 in master or peripheral configuration mode.

~CS0, ~CS1, CS2, ~WRT

These four inputs represent a set of signals, three active LOW and one active HIGH, which are used in peripheral mode to control configuration data entry. The assertion of all four generates a write to the internal data buffer. The removal of any assertion results in the present data of D0-D7 being clocked in.

~RCLK

During master parallel mode configuration, this pin represents a read of an external memory device.

RDY/~BUSY

During peripheral parallel mode configuration, this pin indicates when the chip is ready for another byte of data to be written to it. After configuration is complete, this pin becomes a user-programmed I/O pin.

D0-D7

This set of eight pins represents the parallel configuration byte for the parallel master and peripheral modes. After configuration is complete, they are user-programmable I/O pins.

A0-A15

This set of 16 pins presents an address output for a configuration EPROM during master parallel mode. After configuration is complete, they are user-programmable I/O pins.

I/O

A pin that, after configuration, can be programmed by the user to be an input and/or output pin. Some of these pins present a high impedance pull-up or perform other functions before configuration is complete.

APPENDIX A: TABLES AND DIAGRAMS

Table 2a. 3000 Family Configuration Pin Assignments

CONFIGURATION MODE: <M2:M1:M0>					68 PLCC	84 PLCC	84 PGA	175 PGA	USER OPERATION
SLAVE <1:1:1>	MASTER-SER <0:0:0>	PERIPHERAL <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>					
PWR DWN (I)	PWR DWN (I)	PWR DWN (I)	PWR DWN (I)	PWR DWN (I)	10	12	B2	B2	PWR DWN (I)
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	25	31	J2	B14	RDATA (O)
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	M0 (LOW) (I)	26	32	L1	B15	RTRIG (I)
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	27	33	K2	C15	I/O
HDC (HIGH)	HDC (LOW)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	28	34	K3	E14	I/O
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	30	36	L3	D16	I/O
INIT*	INIT*	INIT*	INIT*	INIT*	34	42	K6	H15	I/O
					43	53	L11	P15	XTL2 OR I/O
RESET (I)	RESET (I)	RESET (I)	RESET (I)	RESET (I)	44	54	K10	R15	RESET (I)
DONE	DONE	DONE	DONE	DONE	45	55	J10	R14	PROGRAM (I)
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	46	56	K11	N13	I/O
					47	57	J11	T14	XTL1 OR I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	48	58	H10	P12	I/O
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	49	60	F10	T11	I/O
		CS0 (I)			50	61	G10	R10	I/O
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	51	62	G11	R9	I/O
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	53	65	F11	R8	I/O
		CS1 (I)			54	66	E11	P8	I/O
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	55	67	E10	R8	I/O
		DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	56	70	D10	R7	I/O
		RDY/BUSY (I)	RCLK	RCLK	57	71	C11	R5	I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	58	72	B11	P5	I/O
DOUT (O)	DOUT (O)	DOUT	DOUT	DOUT	59	73	C10	R3	I/O
CCLK	CCLK	CCLK	CCLK	CCLK	60	74	A11	N4	I/O
		WS (I)	A0	A0	61	75	B10	R2	CCLK (I)
		CS2 (I)	A1	A1	62	76	B9	P2	I/O
			A2	A2	63	77	A10	M3	I/O
			A3	A3	64	78	A9	P1	I/O
			A15	A15	65	81	B6	N1	I/O
			A4	A4	66	82	B7	M1	I/O
			A14	A14	67	83	A7	L2	I/O
			A5	A5	68	84	C7	K2	I/O
			A13	A13	2	2	A6	K1	I/O
			A6	A6	3	3	A5	H2	I/O
			A12	A12	4	4	B5	H1	I/O
			A7	A7	5	5	C5	F2	I/O
			A11	A11	6	8	A3	E1	I/O
			A8	A8	7	9	A2	D1	I/O
			A10	A10	8	10	B3	E3	I/O
			A9	A9	9	11	A1	C2	I/O

REPRESENTS A 50K TO 100K OHM PULL-UP DURING CONFIGURATION
* INIT IS AN OPEN DRAIN OUTPUT DURING CONFIGURATION

Note: Pin assignments of "PGA Footprint" PLCC sockets and PGA packages are not electrically identical.

Table 2b. 3000 Family 68-Pin PLCC Pinouts

PLCC Pin Numbers	3020	PLCC Pin Numbers	3020
10	~PWRDN	44	~RESET
11	I/O	45	DONT-~PG
12	I/O	46	D7-I/O
13	I/O*	47	XTL1-I/O
14	I/O	48	D6-I/O*
15	I/O	49	D5-I/O
16	I/O	50	~CS0-I/O
17	I/O	51	D4-I/O*
18	VCC	52	VCC
19	I/O*	53	D3-I/O
20	I/O	54	~CS1-I/O
21	I/O*	55	D2-I/O*
22	I/O	56	D1-I/O
23	I/O	57	RDY/~BUSY-~RCLK-I/O
24	I/O	58	D0-DIN-I/O
25	M1-~RDATA	59	DOUT-I/O
26	M0-RTRIG	60	CCLK
27	M2-I/O	61	A0-~WS-I/O
28	HDC-I/O	62	A1-CS2-I/O
29	I/O	63	A2-I/O
30	~LDC-I/O	64	A3-I/O
31	I/O	65	A15-I/O
32	I/O	66	A4-I/O
33	I/O	67	A14-I/O
34	~INIT-I/O	68	A5-I/O
35	GND	1	GND
36	I/O	2	A13-I/O
37	I/O	3	A6-I/O
38	I/O	4	A12-I/O
39	I/O	5	A7-I/O
40	I/O	6	A11-I/O
41	I/O	7	A8-I/O
42	I/O	8	A10-I/O
43	XTL2-I/O	9	A9-I/O

*6 Unbonded IOBS 3020

The default configuration of IOBs is input with pull-up. This can be used to prevent an undefined pad level for unbonded or unused IOBs.

Table 2c. 3000 Family 84-Pin PLCC and PGA Pinouts

PLCC Pin Number	PGA Pin Number	3020	3030	PLCC Pin Number	PGA Pin Number	3020	3030
12	B2	~PWRDN	~PWRDN	54	K10	~RESET	~RESET
13	C2	I/O	I/O	55	J10	DONE-~PG	DONE-~PG
14	B1	N/C	I/O	56	K11	D7-I/O	D7-I/O
15	C1	I/O	I/O	57	J11	XTL1-I/O	XTL1-I/O
16	D2	I/O	I/O	58	H10	D6-I/O	D6-I/O
17	D1	I/O	I/O	59	H11	I/O	I/O
18	E3	I/O	I/O	60	F10	D5-I/O	D5-I/O
19	E2	I/O	I/O	61	G10	~CS0-I/O	~CS0-I/O
20	E1	I/O	I/O	62	G11	D4-I/O	D4-I/O
21	F2	I/O	I/O	63	G9	I/O	I/O
22	F3	VCC	VCC	64	F9	VCC	VCC
23	G3	I/O	I/O	65	F11	D3-I/O	D3-I/O
24	G1	I/O	I/O	66	E11	~CS1-I/O	~CS1-I/O
25	G2	I/O	I/O	67	E10	D2-I/O	D2-I/O
26	F1	I/O	I/O	68	E9	I/O	I/O
27	H1	I/O	I/O	69	D11	N/C	I/O
28	H2	I/O	I/O	70	D10	D1-I/O	D1-I/O
29	J1	I/O	I/O	71	C11	RDY/~BUSY-~RCLK-I/O	RDY/~BUSY-~RCLK I/O
30	K1	I/O	I/O	72	B11	D0-DIN-I/O	D0-DIN-I/O
31	J2	M1-~RDATA	M1-~RDATA	73	C10	DOUT-I/O	DOUT-I/O
32	L1	M0-~RTRIG	M0-~RTRIG	74	A11	CCLK	CCLK
33	K2	M2-I/O	M2-I/O	75	B10	A0-~WS-I/O	A0-~WS-I/O
34	K3	HDC-I/O	HDC-I/O	76	B9	A1-CS2-I/O	A1-CS2-I/O
35	L2	I/O	I/O	77	A10	A2-I/O	A2-I/O
36	L3	~LDC-I/O	~LDC-I/O	78	A9	A3-I/O	A3-I/O
37	K4	I/O	I/O	79	B8	N/C	I/O
38	L4	N/C	I/O	80	A8	N/C	I/O
39	J5	I/O	I/O	81	B6	A15-I/O	A15-I/O
40	K5	I/O	I/O	82	B7	A4-I/O	A4-I/O
41	L5	N/C	I/O	83	A7	A14-I/O	A14-I/O
42	K6	~INIT-I/O	~INIT-I/O	84	C7	A5-I/O	A5-I/O
43	J6	GND	GND	1	C6	GND	GND
44	J7	I/O	I/O	2	A6	A13-I/O	A13-I/O
45	L7	I/O	I/O	3	A5	A6-I/O	A6-I/O
46	K7	I/O	I/O	4	B5	A12-I/O	A12-I/O
47	L6	I/O	I/O	5	C5	A7-I/O	A7-I/O
48	L8	I/O	I/O	6	A4	N/C	I/O
49	K8	I/O	I/O	7	B4	N/C	I/O
50	L9	N/C	I/O	8	A3	A11-I/O	A11-I/O
51	L10	N/C	I/O	9	A2	A8-I/O	A8-I/O
52	K9	I/O	I/O	10	B3	A10-I/O	A10-I/O
53	L11	XTL2-I/O	XTL2-I/O	11	A1	A9-I/O	A9-I/O

The default configuration of IOBs is input with pull-up. This can be used to prevent an undefined pad level for unbonded or unused IOBs.

Table 2d. SC3000 Family 175-Pin PGA Pinouts

PGA Pin Number	3090	PGA Pin Number	3090	PGA Pin Number	3090	PGA Pin Number	3090
B2	~PWRDN	D13	I/O	R14	DONE-~PG	R3	D0-DIN-I/O
D4	I/O	B14	M1-~RDATA	N13	D7-I/O	N4	DOUT-I/O
B3	I/O	C14	VSS	T14	XTAL1-I/O	R2	CCLK
C4	I/O	B15	M0-~RTRIG	P13	I/O	P3	VCC
B4	I/O	D14	VCC	R13	I/O	N3	VSS
A4	I/O	C15	M2-I/O	T13	I/O	P2	A0-~WS-I/O
D5	I/O	E14	HDC-I/O	N12	I/O	M3	A1-CS2-I/O
C5	I/O	B16	I/O	P12	D6-I/O	R1	I/O
B5	I/O	D15	I/O	R12	I/O	N2	I/O
A5	I/O	C16	I/O	T12	I/O	P1	A2-I/O
C6	I/O	D16	~LDC-I/O	P11	I/O	N1	A3-I/O
D6	I/O	F14	I/O	N11	I/O	L3	I/O
B6	I/O	E15	I/O	R11	I/O	M2	I/O
A6	I/O	E16	I/O	T11	D5-I/O	M1	A15-I/O
B7	I/O	F15	I/O	R10	~CS0-I/O	L2	A4-I/O
C7	I/O	F16	I/O	P10	I/O	L1	I/O
D7	I/O	G14	I/O	N10	I/O	K3	I/O
A7	I/O	G15	I/O	T10	I/O	K2	A14-I/O
A8	I/O	G16	I/O	T9	I/O	K1	A5-I/O
B8	I/O	H16	I/O	R9	D4-I/O	J1	I/O
C8	I/O	H15	~INIT-I/O	P9	I/O	J2	I/O
D8	VSS	H14	VCC	N9	VCC	J3	VSS
D9	VCC	J14	VSS	N8	VSS	H3	VCC
C9	I/O	J15	I/O	P8	D3-I/O	H2	A13-I/O
B9	I/O	J16	I/O	R8	~CS1-I/O	H1	A6-I/O
A9	I/O	K16	I/O	T8	I/O	G1	I/O
A10	I/O	K15	I/O	T7	I/O	G2	I/O
D10	I/O	K14	I/O	N7	I/O	G3	I/O
C10	I/O	L16	I/O	P7	I/O	F1	I/O
B10	I/O	L15	I/O	R7	D2-I/O	F2	A12-I/O
A11	I/O	M16	I/O	T6	I/O	E1	A7-I/O
B11	I/O	M15	I/O	R6	I/O	E2	I/O
D11	I/O	L14	I/O	N6	I/O	F3	I/O
C11	I/O	N16	I/O	P6	I/O	D1	A11-I/O
A12	I/O	P16	I/O	T5	I/O	C1	A8-I/O
B12	I/O	N15	I/O	R5	D1-I/O	D2	I/O
C12	I/O	R16	I/O	P5	RDY/~BUSY-~RCLK-I/O	B1	I/O
D12	I/O	M14	I/O	N5	I/O	E3	A10-I/O
A13	I/O	P15	XTAL2-I/O	T4	I/O	C2	A9-I/O
B13	I/O	N14	VSS	R4	I/O	D3	VCC
C13	I/O	R15	~RESET	P4	I/O	C3	VSS
A14	I/O	P14	VCC				

The default configuration of IOBs is input with pull-up. This can be used to prevent an undefined pad level for unbonded or unused IOBs. Pins A2, A3, A15, A16, T1, T2, T3, T15 and T16 are not connected. Pin A1 does not exist.

PARAMETRICS

Absolute Maximum Ratings			Units
V_{CC}	Supply voltage relative to GND	–0.5 to 7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to three-state output	–0.5 to V_{CC} + 0.5	V
V_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 sec @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

*Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

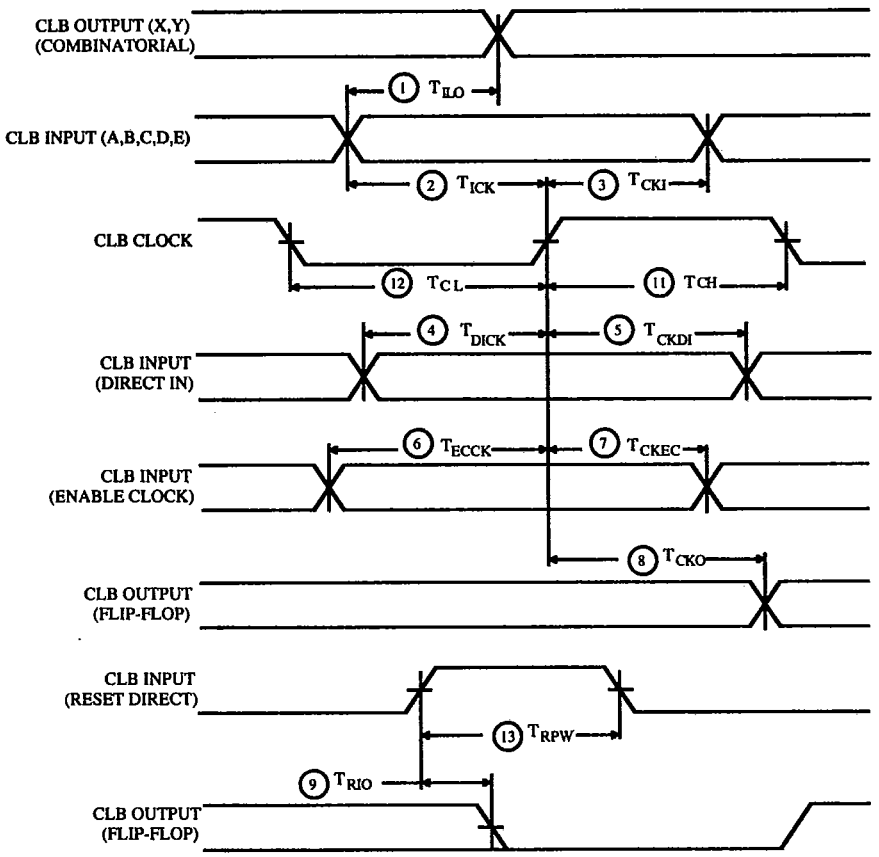
Recommended Operating Conditions				Min	Max	Units
V_{CC}	Supply voltage relative to GND	Commercial	0° C to 70° C	4.75	5.25	V
	Supply voltage relative to GND	Industrial	–40° C to 85° C	4.5	5.5	V
	Supply voltage relative to GND	Military	–55° C to 125° C	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration			2.0	V_{CC}	V
V_{ILT}	Low-level input voltage — TTL configuration			0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration			.7 V_{CC}	V_{CC}	V
V_{ILC}	Low-level input voltage — CMOS configuration			0	.2 V_{CC}	V
T_{IN}	Input signal transition time				250	ns

ELECTRICAL CHARACTERISTICS OVER OPERATING CONDITIONS			MIN	MAX	UNITS
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 ma V_{CC} min)	Commercial	3.86		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 ma V_{CC} min)			0.32	V
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 ma V_{CC})	Industrial	3.76		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 ma V_{CC})			0.37	V
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 ma V_{CC})	Military	3.7		V
V_{OL}	Low-level output voltage (@ I_{OH} = 4.0 ma V_{CC})			0.4	V
I_{CCPD}	Power-down supply current (V_{CC} = 5.0 V @ 70°C)[1]			500	µA
I_{CCO}	Quiescent LCA supply current in addition to I_{CCPD}[2]				
	CMOS chip thresholds			500	µA
	TTL chip thresholds			10	mA
I_{IL}	Leakage Current Commercial/Industrial Temperature		–10	+10	µA
	Leakage Current Military –55° C to 125° C		–20	+20	µA
C_{IN}	Input capacitance (sample tested)			10	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	0.17	mA
I_{RLL}	Horizontal long line pull-up (when selected) @ logic LOW		0.4	3.4	mA

Notes: 1. Based on a 3020, I_{CCPD} ratio for 3090, 5.0

2. With no output current loads, no active input or long line pull-up resistors, all package pins at V_{CC} or GND, and the LCA configured with a MAKEBITS "tie" option. See LCA power chart for additional activity dependent operating component.

CLB SWITCHING CHARACTERISTIC GUIDELINES



CLB SWITCHING CHARACTERISTIC GUIDELINES (Continued)

Testing of the switching characteristic guidelines is modeled after testing specified by MIL-M-38510/605. Devices are 100% functionally tested. Benchmark timing patterns are used to provide correlation to the switching characteristic guideline values. Actual worst-case timing is provided by the XACT Timing calculator or Simulation modeling.

Speed Grade				-50		-70		Units
	Description	Symbol		Min	Max	Min	Max	
CLB Logic Input	Combinatorial	1	T_{ILO}		14		9	ns
Reset direct	CLB output	9	T_{RIO}		15		10	ns
	Reset Direct width*	13	T_{RPW}		10		7	ns
	Master Rest pin to CLB out		T_{MRQ}		35		25	ns
CLB K Clock input	To CLB output	8	T_{CKO}		12		8	ns
	Additional for Q returning through F or G to CLB out		T_{QLO}		11		7	ns
	Logic-input setup	2	T_{ICK}	12		8		ns
	Logic-input hold	3	T_{CKI}	0		0		ns
	Data In setup	4	T_{DICK}	8		5		ns
	Data In hold	5	T_{CKDI}	6		4		ns
	Enable Clock setup	6	T_{EGCK}	10		7		ns
	Enable Clock hold	7	T_{CKEC}	0		0		ns
	Clock (high)*	11	T_{CH}	9		7		ns
	Clock (low)*	12	T_{CL}	9		7		ns
Flip-flop Toggle rate	Q through F/G to flip-flop in*		F_{CLK}	50		70		MHz

* These timing limits are based on calculations.

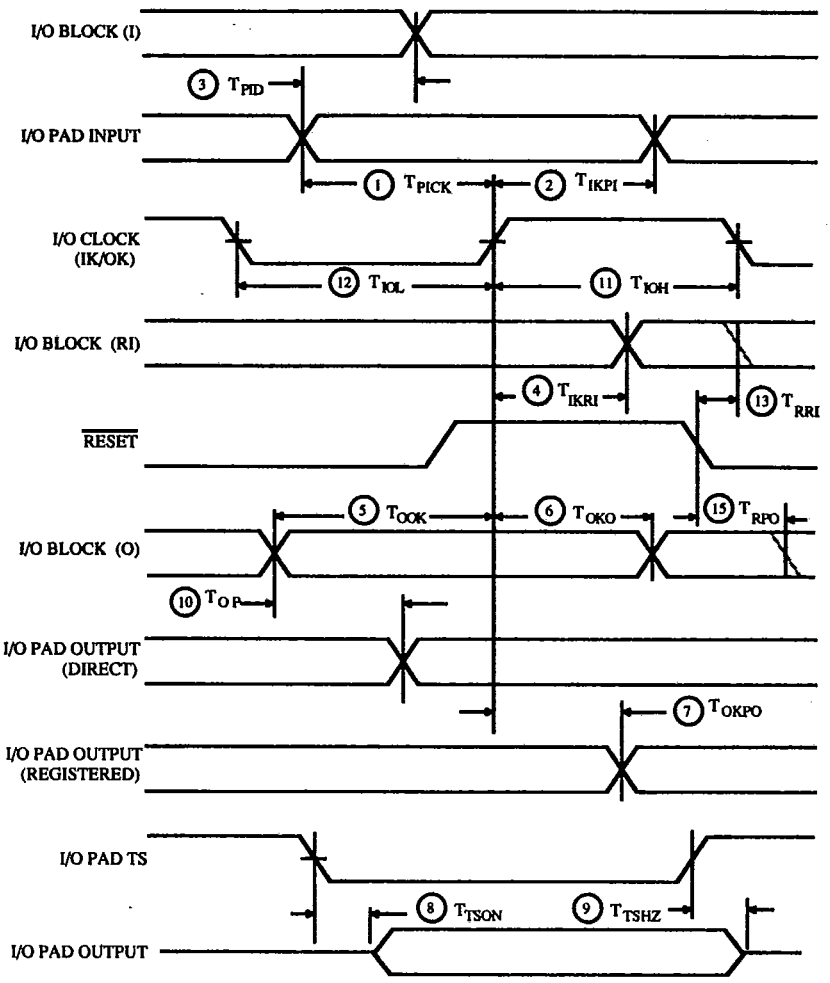
The speed of block inputs is a function of interconnect.

BUFFER (Internal) SWITCHING CHARACTERISTIC GUIDELINES

Speed Grade		-50		-70		Units
	Description	Min	Max	Min	Max	
Clock Buffer**	GCLK, ACLK		9		6	ns
TBUF**	Data to Output (Long line buffer)		8		5	ns
	Three-state to Output					
	Single pull-up resistor		34		22	ns
	Pair of pull-up resistors		17		11	ns
Bi-directional	BIDI		6		4	ns

** Timing is based on the 3020, for other devices see XACT timing calculator.

IOB SWITCHING CHARACTERISTIC GUIDELINES



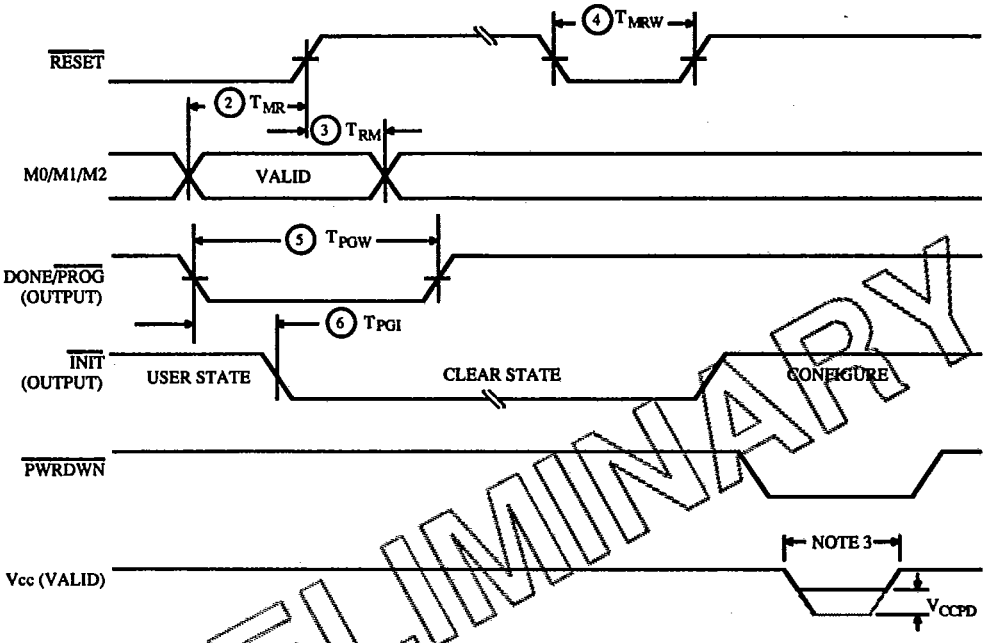
IOB SWITCHING CHARACTERISTIC GUIDELINES (Continued)

Testing of the switching characteristic guidelines is modeled after testing specified by MIL-M-38510/605. Devices are 100% functionally tested. Benchmark timing patterns are used to provide correlation to the switching characteristic guideline values. Actual worst-case timing is provided by the XACT Timing calculator or Simulation modeling.

Speed Grade				-50		-70		Units
	Description	Symbol		Min	Max	Min	Max	
Pad (package pin)	To input (direct CLKIN)		T_{PIDC}		6		3	ns
	To input (direct)	3	T_{PID}		10		7	ns
I/O Clock	To I/O RI input (FF)	4	T_{IKRI}		10		7	ns
	I/O pad-input setup	1	T_{RICK}	30		20		ns
	I/O pad-input hold	2	T_{IKPI}	0		0		ns
	To I/O pad (fast)	7	T_{OKPC}		18		13	ns
	I/O pad output setup	5	T_{OOK}	15		10		ns
	I/O pad output hold	6	T_{OKO}	0		0		ns
	Clock (high)	11	T_{IOH}	9		7		ns
	Clock (low)	12	T_{IOL}	9		7		ns
Output	To pad (enabled fast)	10	T_{OPF}		14		10	ns
	To pad (enabled slow)	10	T_{OPS}		33		25	ns
Three-state	To pad begin hi-Z (fast)	9	T_{TSHZ}		12		8	ns
	To pad valid (fast)	8	T_{TSON}		20		14	ns
Master Reset (Package Pin)	To input RI	13	T_{RRI}		45		30	ns
	To output (FF)	15	T_{RPO}		55		37	ns

Notes:
1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical fast mode output rise/fall times are 5 ns and will increase approximately 2%/pF. A maximum total external capacitive load for simultaneous fast mode switching in the same direction is 500 pF per power/ground pin pair.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.

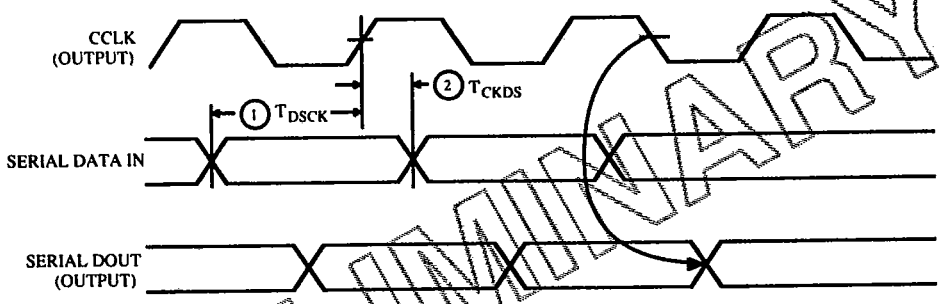
GENERAL LCA SWITCHING CHARACTERISTICS



				-50		-70		Units
	Description	Symbol		Min	Max	Min	Max	
~RESET (2)	M2, M1, M0 setup	2	T_{MR}	1		1		µs
	M2, M1, M0 hold	3	T_{RM}	1		1		µs
	Width (low) Abort	4	T_{MRW}	6		6		µs
DONE/~PROG	Program width (low)	5	T_{PGW}	6		6		µs
	Start ~INIT	6	T_{PGI}		7		7	µs
~PWRDWN (3)	Power Down V_{CC}		V_{CCPD}		2.0		2.0	V

Notes:
1. V_{CC} must rise from 2.0 Volts to V_{CC} minimum in less than 10 ms for master modes.
2. RESET timing relative to valid mode lines (M0, M1, M2) is relevant when ~RESET is used to delay configuration.
3. ~PWEDWN transitions must occur during operational V_{CC} levels.

MASTER SERIAL MODE SWITCHING CHARACTERISTICS GUIDELINES

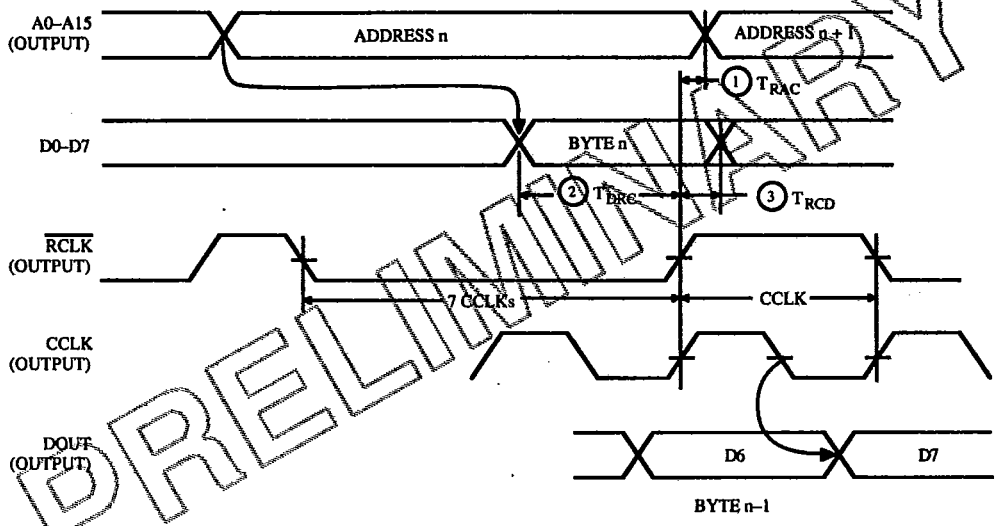


				-50		-70		Units
	Description	Symbol		Min	Max	Min	Max	
CCLK[3]	Data In setup	1	T_{DSCK}	60		60		ns
	Data In hold	2	T_{CKDS}	0		0		ns

Notes:
1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min. in less than 10 ms, otherwise delay configuration using ~RESET until VCC is valid.
2. Configuration can be controlled by holding ~RESET low with or until after the ~INIT of all daisy-chain slave mode devices is HIGH.
3. Master serial mode timing is based on slave mode testing.

MASTER PARALLEL MODE PROGRAMMING SWITCHING CHARACTERISTIC GUIDELINES

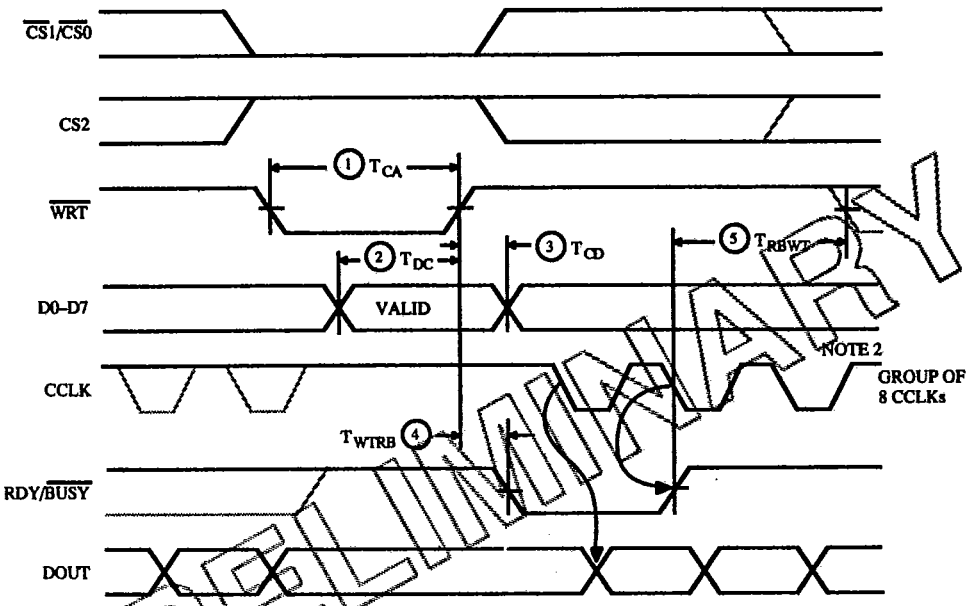
Testing of the switching characteristic guidelines is modeled after testing specified by MIL-M-38510/605. Devices are 100% functionally tested. Benchmark timing patterns are used to provide correlation to the switching characteristic guideline values. Actual worst-case timing is provided by the XACT Timing calculator or Simulation modeling.



				–50		–70		Units
	Description	Symbol		Min	Max	Min	Max	
RCLK	To address valid	1	T_{RAC}	0	200	0	200	ns
	To data setup	2	T_{DRC}	60		60		ns
	To data hold	3	T_{RCD}	0		0		ns
	RCLK high		T_{RCH}	600		600		ns
	RCLK low		T_{RCL}	4.0		4.0		µs

Notes: 1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min. in less than 10 ms, otherwise delay configuration using ~RESET until V_{CC} is valid.
2. Configuration can be controlled by holding ~RESET low with or until after the ~INIT of all daisy-chain slave mode devices is HIGH.

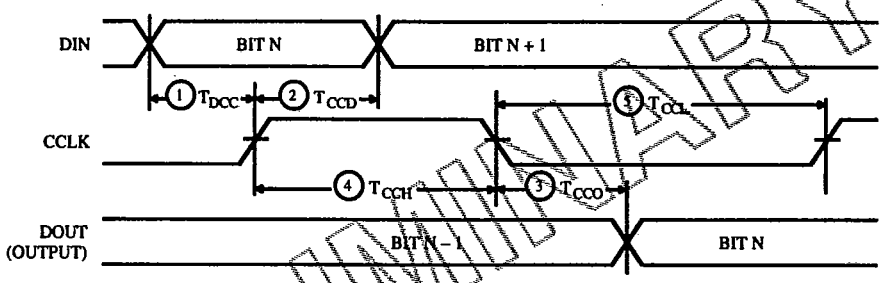
PERIPHERAL MODE PROGRAMMING SWITCHING CHARACTERISTICS



				-50		-70		Units
	Description	Symbol		Min	Max	Min	Max	
Write	WRT Low	1	T_{CA}	0.5		0.5		µs
	DIN setup	2	T_{DC}	60		60		ns
	DIN hold	3	T_{CD}	0		0		ns
	Ready/Busy	4	T_{WTRB}		60		60	ns
RDY	WRT Active	5	T_{RBWT}	0		0		ns

Notes:
1. Configuration must be delayed until the ~INIT of all LCAs is HIGH.
2. Time from end of WRT to CCLK cycle for the new byte of data depends on completion of previous byte processing and the phase of the internal timing generator for CCLK.
3. CCLK and DOUT timing is tested in slave mode.

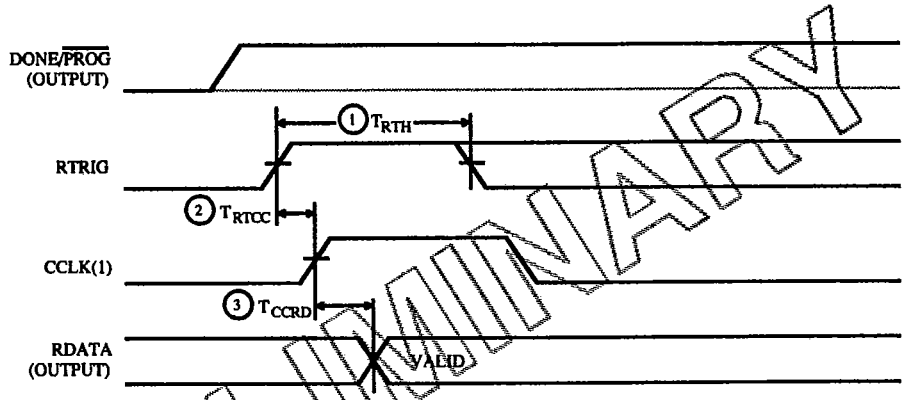
SLAVE MODE PROGRAMMING SWITCHING CHARACTERISTICS



				–50		–70		Units
	Description	Symbol		Min	Max	Min	Max	
CCLK	To DOUT	3	T_{CCO}		100		100	ns
	DIN setup	1	T_{DCC}	60		60		ns
	DIN hold	2	T_{CCD}	0		0		ns
	High time	4	T_{CCH}	0.5		0.5		µs
	Low time	5	T_{CCL}	0.5	5.0	0.5	5.0	µs
	Frequency		F_{CC}		1		1	MHz

Note: Configuration must be delayed until the INIT of all LCAs is HIGH.

PROGRAM READBACK SWITCHING CHARACTERISTICS



		Symbol		-50		-70		Units
	Description			Min	Max	Min	Max	
RTRIG	RTRIG high	1	T_{RTH}	250		250		ns
CCLK	RTRIG setup	2	T_{RTCC}	10		10		µs
	~RDATA delay	3	T_{CCRD}		100		100	ns

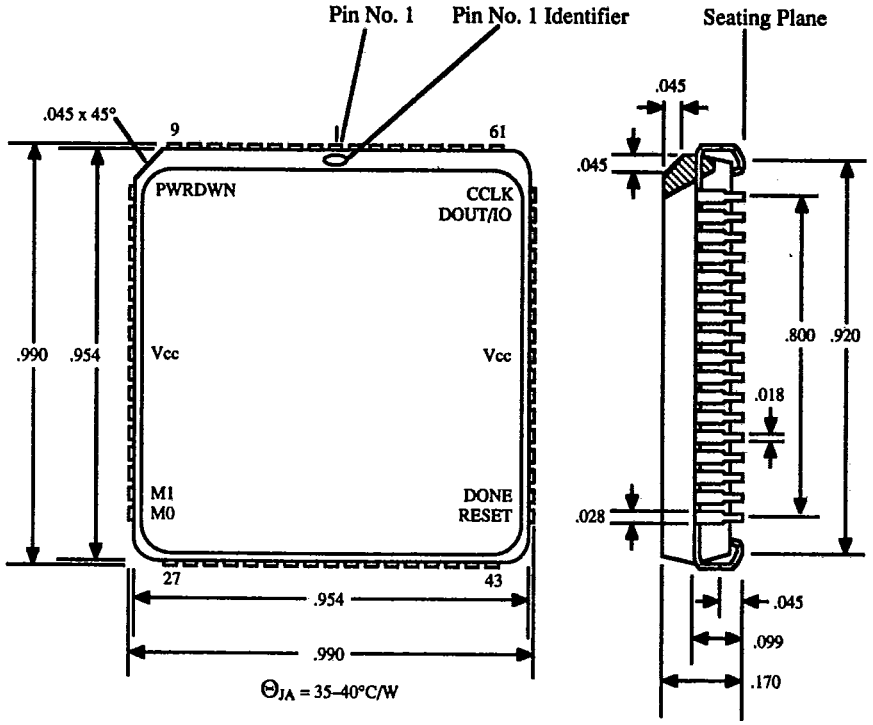
Notes: 1. CCLK and DOUT timing are the same as for slave mode.
2. RETRIG (M0 positive transition) shall not be done until after one clock following active I/O pins.
3. Readback should not be initiated until configuration is complete.

SOCKET INFORMATION

The following sockets, with matching hole patterns, are available for PLCC devices.

DESCRIPTION 68 PIN	VENDOR	PART NUMBER
PCB solder tail, tin plate	AMP	821574-1
Surface mount, tin plate	AMP	821542-1
PCB solder tail, tin plate*	Burndy	QILE68P-410T
PCB solder tail, tin plate*	Midland-Ross	709-2000-068-4-1-1
PCB solder tail, tin plate*	Methode	213-068-001
Surface mount, tin plate	Methode	213-068-002

*Sockets will plug into pin-grid array wire-wrap sockets for breadboard use. However, the physical translation of pins in a PLCC socket does not result in electrical equivalence to the pin locations of a PGA package.

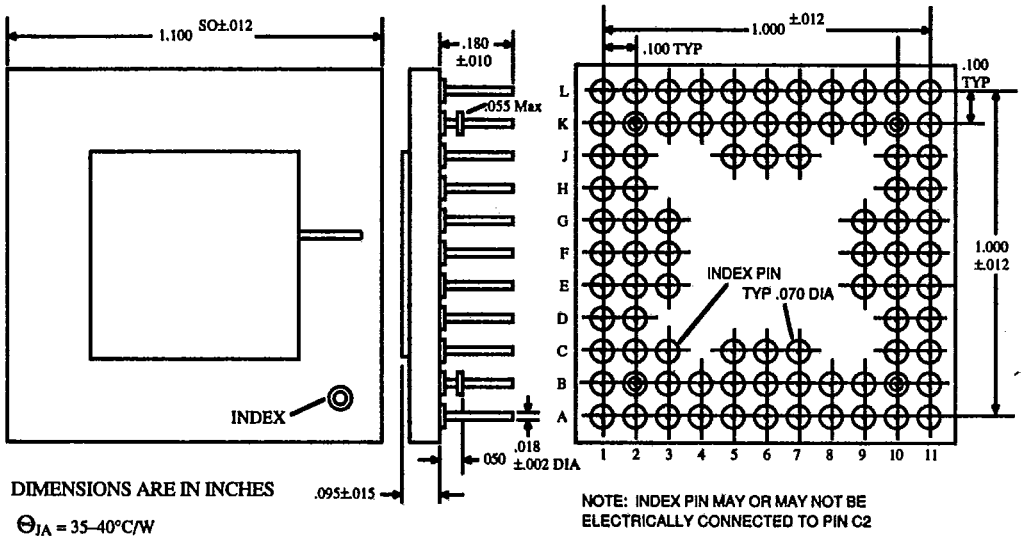


PIN SPACING
.050 TYPICAL

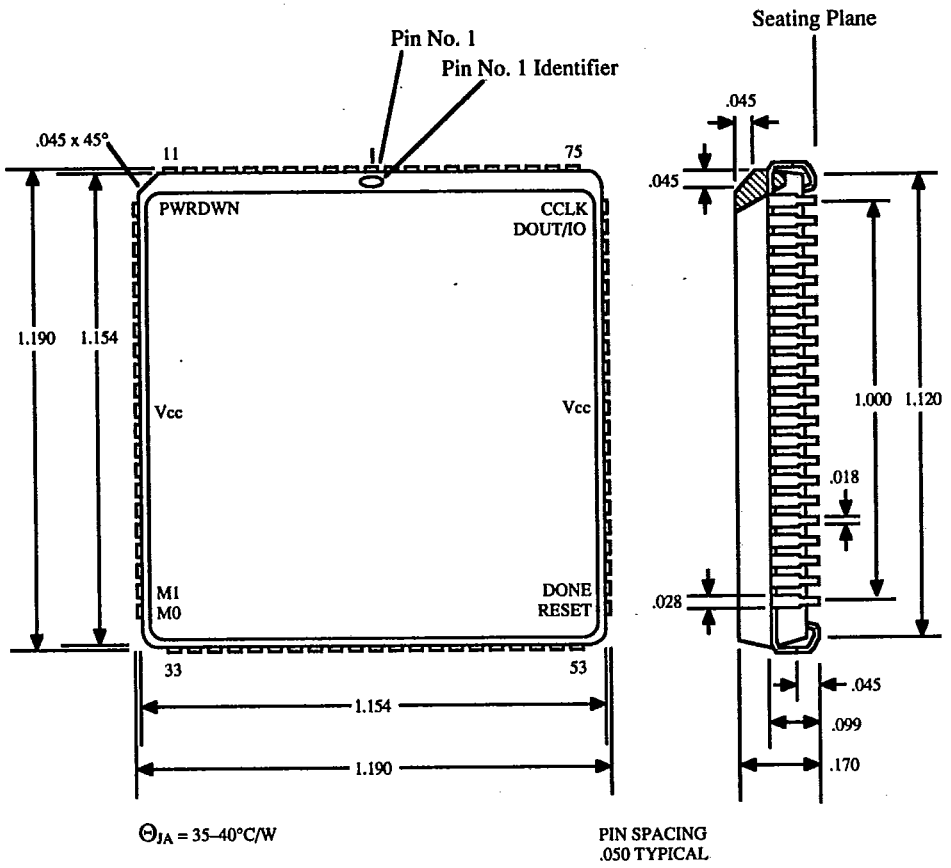
LEAD CO-PLANARITY ± 0.002 IN

ALL OTHER DIMENSIONS ARE
IN INCHES ± 0.005

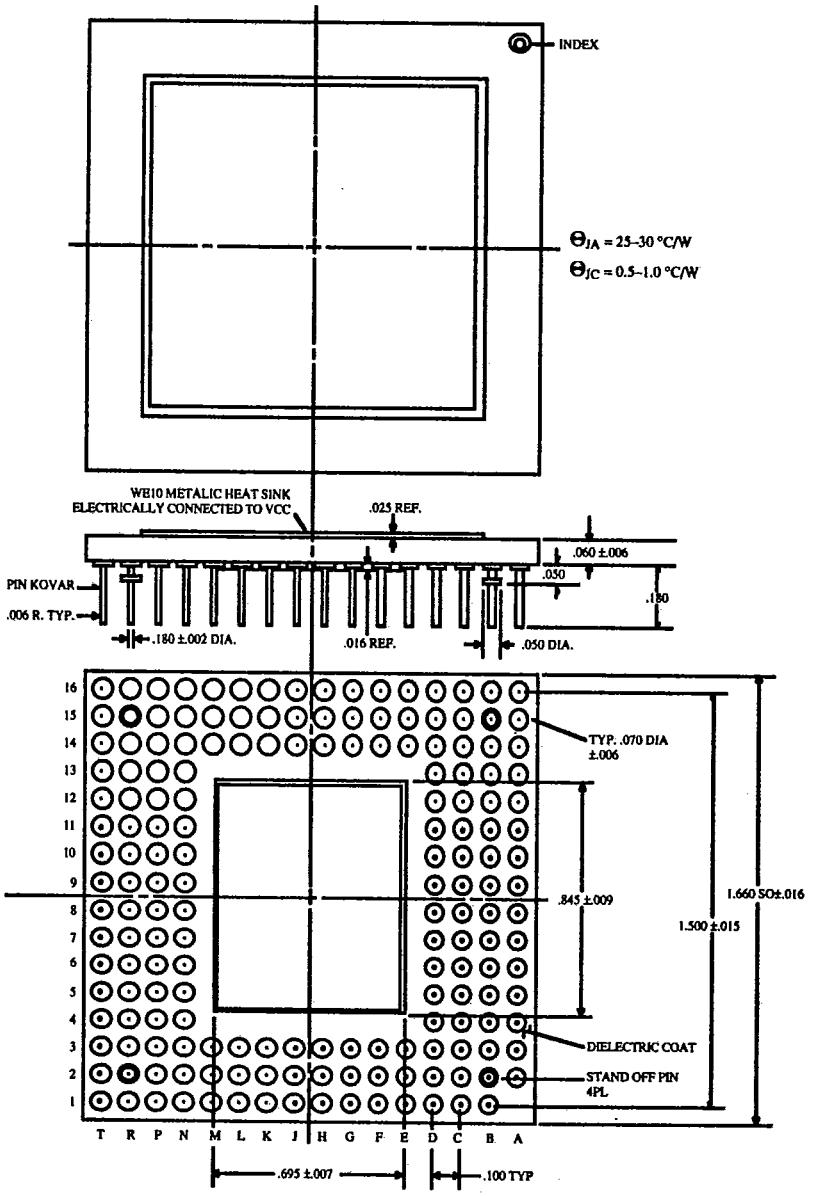
68-Pin PLCC Package



84-Pin PGA Package



84-Pin PLCC Package



175-Pin PGA Package