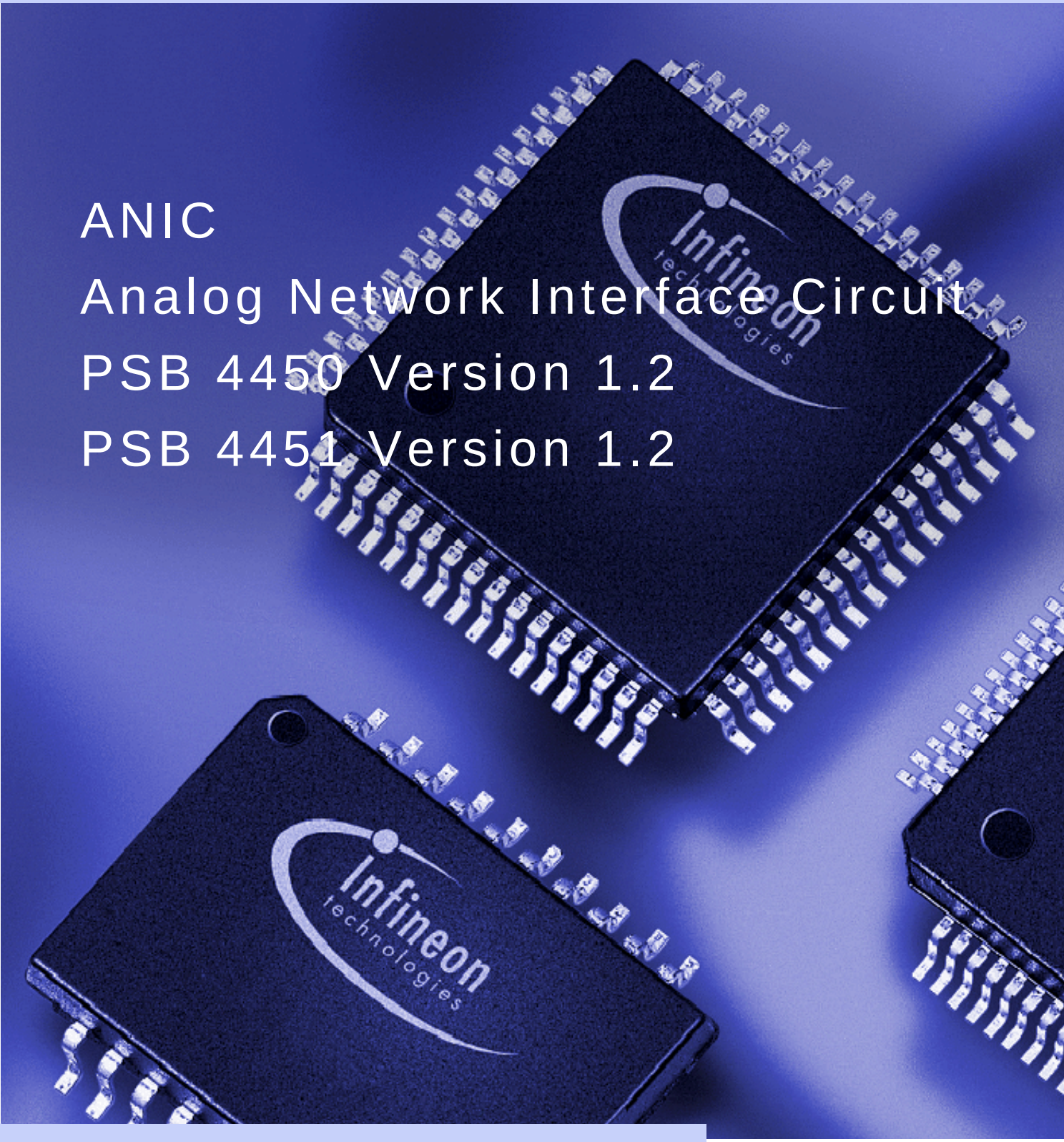
Data Sheet, DS8, September 2000

ANIC
Analog Network Interface Circuit
PSB 4450 Version 1.2
PSB 4451 Version 1.2



Wired Communications

Infineon technologies

Never stop thinking.

Edition 2000.09.04

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München, Germany

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

ANIC
Analog Network Interface Circuit
PSB 4450 Version 1.2
PSB 4451 Version 1.2

Wired Communications

Infineon technologies

Never stop thinking.

ANIC
Preliminary
Revision History: 2000.09.04 DS8

Previous Version: Data Sheet DS7

Page	Subjects (major changes since last revision)
Page 15	Table **"Pin Descriptions PSB 4450" on Page 15**: "LINE-" connected to pin 1, "LINE+" connected to pin 2
Page 17	Table **"Pin Descriptions PSB 4451" on Page 17**: $t_{RESET,min}$ changed from 500 ns to 300 ns, f_{DATCLK} min. changed from 256 kHz to 512 kHz
Page 22	Figure **"Voice Path" on Page 22**: ANIC-D loop removed
Page 36	Chapter **"Data Loops" on Page 36**: ANIC-D loop removed, description changes
Page 51	Table **"Register Overview" on Page 51**: register index 0, offset 10: bit 2 CIF_LOOP renamed to ANIC-A_LOOP
Page 92	Chapter **"RESET (Basic Setting Mode)" on Page 92** : $t_{RESET,min}$ changed from 500 ns to 300 ns. Chapter **"IDLE Mode" on Page 92**: note added
Page 94	Chapter **"CONVERSATION Mode" on Page 94**: description added
Page 96	Table **"Selectable Values for R" on Page 96**: values modified
Page 98	Table **"Ringer Impedance" on Page 98**: values modified
Page 102	Table **"DC Characteristics PSB 4450" on Page 102**: conditions for supply current changed
Page 104	Table **"DC Characteristics PSB 4451" on Page 104**: condition on 5 V tolerance added, values and conditions for supply current changed, internal pull-up resistor ranges added (footnote)
Page 106	Test conditions partially modified
Page 122	Chapter **"Input/ Output Waveform for AC Tests" on Page 122**: figure and description changes
Page 122	Chapter **"Reset Timing" on Page 122**: figure and description changes
Page 123	Figure **"Serial Control Interface Timing" on Page 123**: minor changes
Page 124	Table **"Serial Control Interface Switching Characteristics" on Page 124**: value and description for $t_{D(DOUT\_Z)}$ and other parameters changed, parameter DCLK frequency added, note on pull-up resistor added, sentence about DCLK in header added
Page 125	Figure **"PCM Interface Timing" on Page 125**: minor changes, note added
Page 126	Table **"PCM Interface Switching Characteristics" on Page 126**: values and description for $t_{SU(DATIN)}$, $t_{HD(DATIN)}$ and $t_{D(DATOUT\_Z)}$ changed, note on pull-up resistor added, parameters DATCLK clock frequency and FSC frequency added, $t_{SU(FSC)}$ min. changed to $4*T_{MCLK}$

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at http://www.infineon.com

Table of Contents **Page**

Table of Contents **Page**

Table of Contents **Page**

List of Figures

Page

List of Figures

Page

List of Tables

1 Overview

ANIC is a chip set to interface analog voice signals to digital terminals such as DSL transceivers. Its technology and design make it especially suitable for the use throughout the world for applications such as

- DAML (Digital Added Main Line) interface between a central office and digital line transceivers,
- PBX trunks,
- Universal DLC (Digital Loop Carrier) systems.

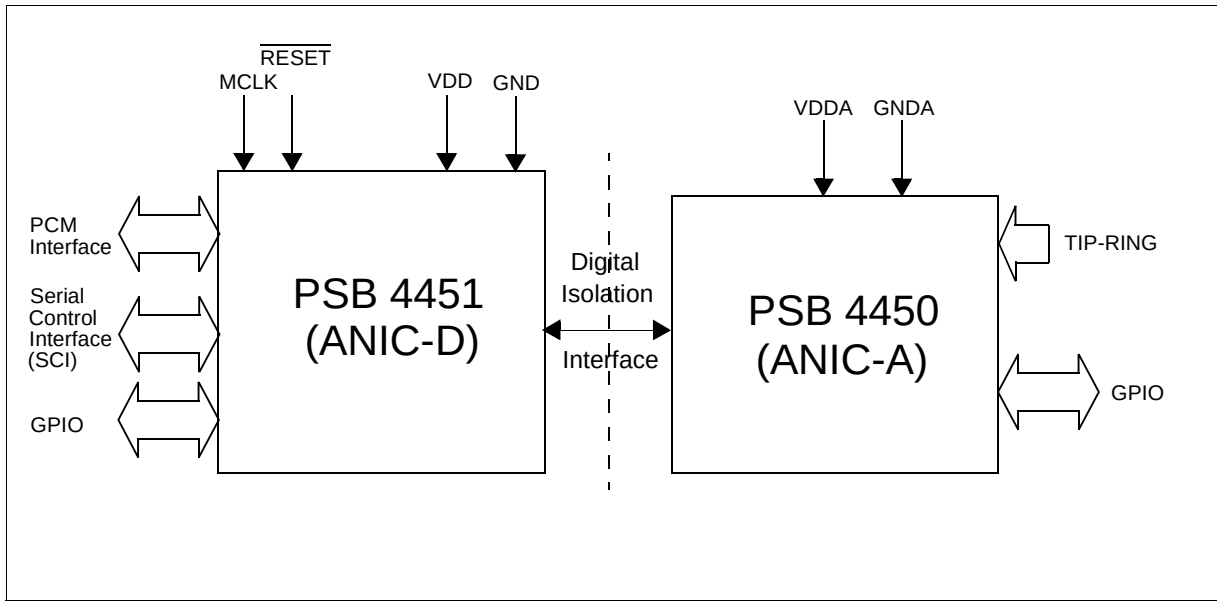


Figure 1 Block Diagram of the ANIC Chip Set

Note: The block diagram is described in more detail in the section ***"Functional Description" on Page 20****.*

The ANIC chip set is an ideal analog front end to convert digital information into analog signals and vice versa for communication via telephone lines.

Reliability in digital processing is much better than in analog communications. The new design of the ANIC chip set has transferred processing that was previously done on the analog side to the digital part. Digital filters ensure great precision and virtually no fluctuation.

The use of digital filter processing in combination with software algorithms ensures excellent transmission performance and adaptability. The ANIC chip set is programmable to adapt to different countries' requirements. Coefficient sets can be downloaded to the ANIC chip set to comply with specifications throughout the world.

Preliminary

Overview

The ANIC chip set replaces the traditional Data Access Arrangement (DAA) with voice band transformer and discrete components. The use of digital signal processing and filtering approaches provides the user not only more features and programmability, but also better system performance.

As a result of the Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) technology used, the linearity of the ANIC chip set is limited only by second-order parasitic effects.

The main functional blocks of the ANIC are:

- Data Access Arrangement (DAA)
- Selectable A-law, µ-law, and 16-bit linear coder/decoder (codec)
- TIP-RING-GROUND voltage measurements to identify, e.g., polarity reversal
- Time slot assignment for PCM-highway interface

The technology used for the two chips is:

- PSB 4450 (analog) low-power 0.8 µm BiCMOS
- PSB 4451 (digital) 0.35 µm CMOS

Infineon Technologies offers a range of reference and evaluation tools for the ANIC chip set. For appropriate tools, please contact your nearest Infineon Technologies representative.

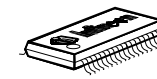
Preliminary

Analog Network Interface Circuit ANIC

PSB 4450
PSB 4451

Version 1.2

1.1 Features



P-TSSOP-38-1

P-TSSOP-28-1

- The ANIC chip set replaces the traditional Data Access Arrangement (DAA), codec and hybrid components.
- On-hook transmission.
- DC measurements of TIP-RING, RING-GROUND and TIP-GROUND voltage.
- General purpose I/O pins.
- Works with a large range of clock frequencies from 16.384 MHz to 33 MHz.
- Supports sample rates from 6 kHz up to 24 kHz
- 3 V technology for the PSB 4451.
  - Output pins are TTL and CMOS compatible.
  - Input pins are 5 V tolerant.
- On chip VDD control for the PSB 4450.

International features:

- Programmable ring detection: country-specific frequencies and levels. Coefficients for frequencies and levels are downloadable.
- Programmable country-specific DC characteristics.
- Detection of metering signals.
- PCM encoded digital voice transmission (A-Law or µ-Law) according G.711.

Type	Package
PSB 4450	P-TSSOP38
PSB 4451	P-TSSOP28

2 Pin Descriptions

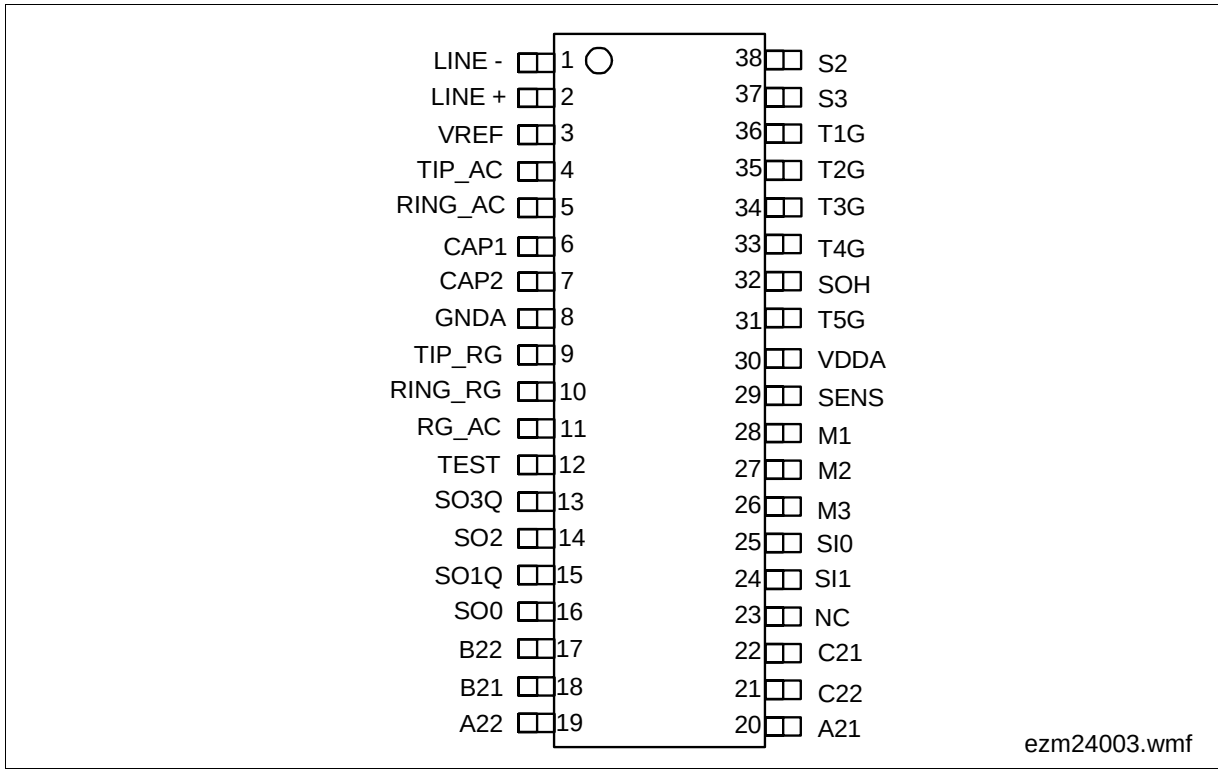


Figure 2 Pinning Diagram PSB 4450 (ANIC-A)

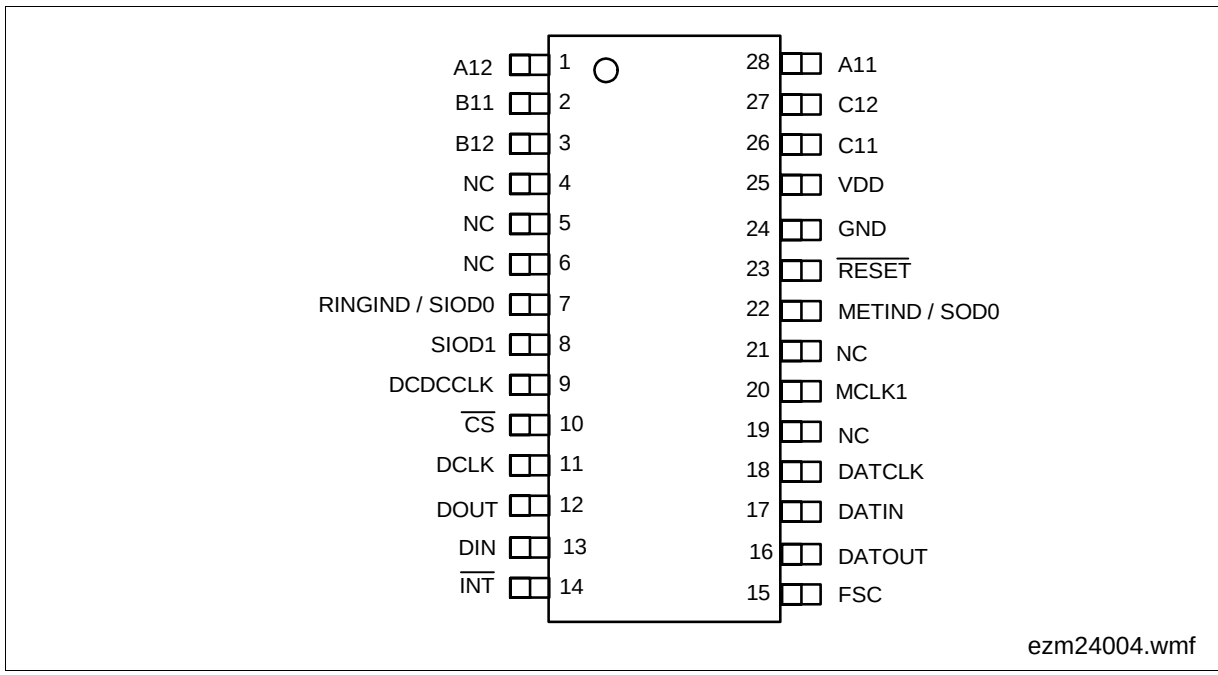


Figure 3 Pinning Diagram PSB 4451 (ANIC-D)

2.1 Pin Descriptions PSB 4450

Table 1 Pin Descriptions PSB 4450

Pin No.	Symbol	Function	Description
30	VDDA	Power	+ 5 V supply for analog circuitry
3	VREF		Filtering reference voltage
8	GNDA	Power	Ground analog. All signals are referenced to this pin.
1	LINE-	I	Voltage sense input from TIP
2	LINE+	I	Voltage sense input from RING
9	TIP_RG	I	Voltage sense input for ringing
10	RING_RG	I	Voltage sense input for ringing
4	TIP_AC	I	Voltage sense input for AC signals
5	RING_AC	I	Voltage sense input for AC signals
11	RG_AC	I	Voltage sense input for AC signals in ON-HOOK CONVERSATION mode
38	S2	I	Sense inputs for ringer impedance loop
37	S3	I	Sense inputs for ringer impedance loop
16	SO0	O	General purpose output
15	SO1Q	O	General purpose output
14	SO2	O	General purpose output
13	SO3Q	O	General purpose output
12	TEST	I	Must be connected to GND
25	SI0	I	General purpose input
24	SI1	I	General purpose input
36	T1G	O	Control pin for transistor T1
35	T2G	O	Control pin for transistor T2
34	T3G	O	Control pin for transistor T3
33	T4G	O	Control pin for transistor T4
31	T5G	O	Control pin for transistor T5
11	NC	-	unused
29	SENS	I	Voltage sense for VDD control
32	SOH	I	Current sensing for on-hook transmission

Table 1 Pin Descriptions PSB 4450 (Continued)

Pin No.	Symbol	Function	Description
28	M1	I	Measurement input GROUND
27	M2	I	Measurement input TIP
26	M3	I	Measurement input RING
6	CAP1	O	External low pass filter
7	CAP2	O	External low pass filter
20	A21	I	Digital isolation interface to PSB 4451: Must be connected to pin A11 of PSB 4451 (see **Page 50**)
19	A22	I	Digital isolation interface to PSB 4451: Must be connected to pin A12 of PSB 4451 (see **Page 50**)
18	B21	O	Digital isolation interface to PSB 4451: Must be connected to pin B11 of PSB 4451 (see **Page 50**)
17	B22	O	Digital isolation interface to PSB 4451: Must be connected to pin B12 of PSB 4451 (see **Page 50**)
22	C21	I	Digital isolation interface to PSB 4451: Must be connected to pin C11 of PSB 4451 (see **Page 50**)
21	C22	I	Digital isolation interface to PSB 4451: Must be connected to pin C12 of PSB 4451 (see **Page 50**)
23	NC	–	unused

Note: For further details see Application Note "Understanding the External Components of the ANIC Chip Set".

2.2 Pin Descriptions PSB 4451

Table 2 Pin Descriptions PSB 4451

Pin No.	Symbol	Function	Description
25	VDD	Power	+ 3.3 Volt supply for the digital & analog circuitry.
24	GND	Power	Ground digital. All signals are referenced to this pin.
20	MCLK1	I	Master Clock1: this pin must be driven by an external clock of e.g. 16.384 MHz
23	$\overline{\text{RESET}}$	I	Reset input: resets the device (low active) Reset is considered valid if asserted active longer than $t_{RESET,min}$ = 300 ns .
15	FSC	I	Frame Synchronization Clock
17	DATIN	I	PCM Interface: receive data 8-bit timeslots.
16	DATOUT	O	PCM Interface: transmit data, tristate if not active
18	DATCLK	I	Data clock 512 to 2048 kHz: determines the rate at which data is transferred to and from the PCM Interface.
14	$\overline{\text{INT}}$	O	Interrupt output pin (open drain, low active, internal pull up with 32 kOhm).
11	DCLK	I	Serial Control Interface: clock for control data.
10	$\overline{\text{CS}}$	I	Serial Control Interface: chip select
13	DIN	I	Serial Control Interface: receive control data from the µC / DSP
12	DOUT	O	Serial Control Interface: transmit control data to the µC / DSP
9	DCDCCLK	O	Output for DCDC switching clock
28	A11	O	Digital isolation interface to PSB 4450: Must be connected to pin A21 of PSB 4450 (see **Page 50**)
1	A12	O	Digital isolation interface to PSB 4450: Must be connected to pin A22 of PSB 4450 (see **Page 50**)

Table 2 Pin Descriptions PSB 4451 (Continued)

Pin No.	Symbol	Function	Description
2	B11	I	Digital isolation interface to PSB 4450: Must be connected to pin B21 of PSB 4450 (see **Page 50**)
3	B12	I	Digital isolation interface to PSB 4450: Must be connected to pin B22 of PSB 4450 (see **Page 50**)
26	C11	O	Digital isolation interface to PSB 4450: Must be connected to pin C21 of PSB 4450 (see **Page 50**)
27	C12	O	Digital isolation interface to PSB 4450: Must be connected to pin C22 of PSB 4450 (see **Page 50**)
22	METIND / SOD0	O	Metering indication or general purpose output pin (active high).
8	SIOD1	IO	General purpose I/O pin.
7	RINGIND / SIOD0	IO	Ring indication or general purpose I/O pin (active high).
6	NC	–	Unused
21	NC	–	Unused
19	NC	–	Unused
4	NC	–	Unused
5	NC	–	Unused

3 Typical Applications

As mentioned in the overview, one of the ANIC applications is in central office terminals (COT) serving as interface between voice signals of the CO's analog line card and the digital line transceivers connected to the network.

In typical implementations, the innovative digital isolation interface renders a transformer redundant, reducing weight and space requirements.

3.1 ANIC Chip Set in the Central Office Terminal (COT)

The ANIC chip set forms the front end between a MDSL chip set and the TIP-RING line.

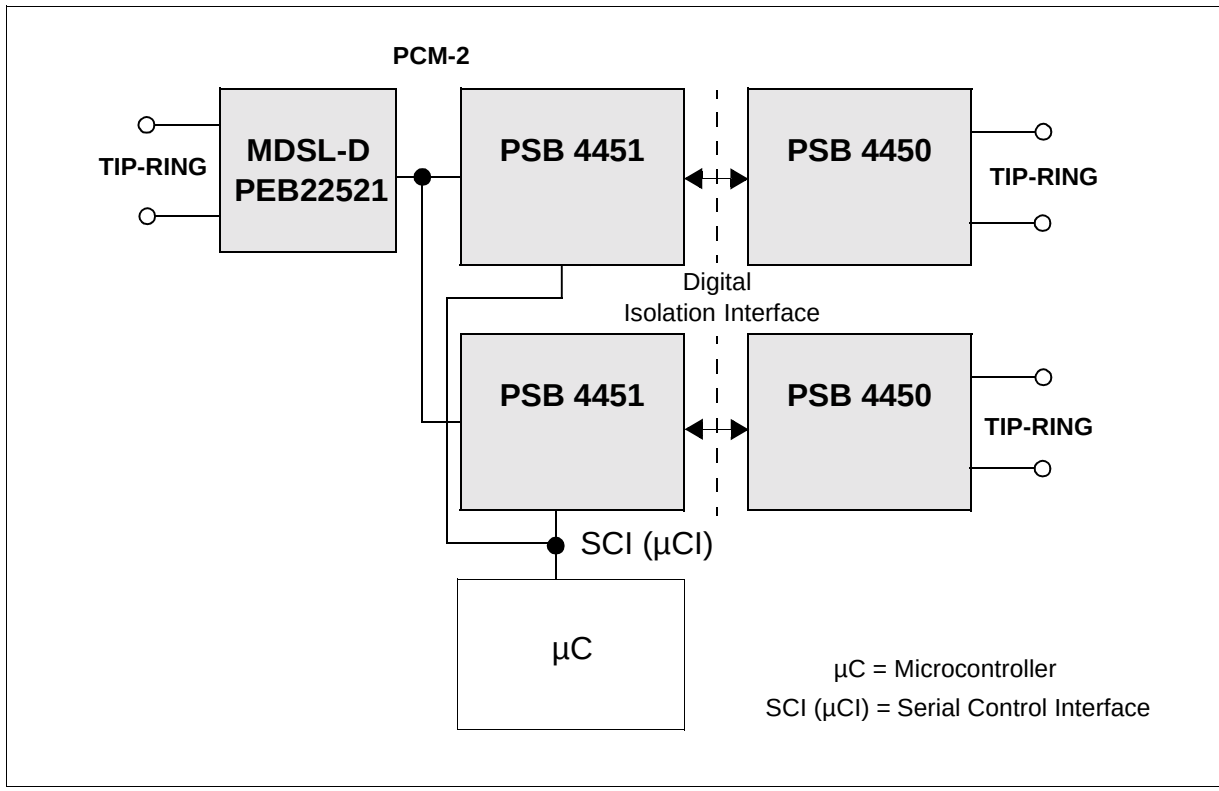


Figure 4 ANIC Application in a COT

The MDSL chip set is both source and destination of digital signals which are transferred to and from the digital chip PSB 4451 via the PCM Interface. The Serial Control Interface (SCI) enables external control of the ANIC chip set. The SCI gives transparent access to ANIC commands and signalling pins so that precalculated coefficient sets can be downloaded from the system to the on-chip coefficient RAM (CRAM) to program the filters.

4 Functional Description

The functional description consists of a block diagram with explanation of the building blocks followed by a description of the chip set's basic principles of operation.

4.1 Functional Block Diagram

The chip set consists of two chips, PSB 4450 and PSB 4451. **Figure 5** shows the main building blocks:

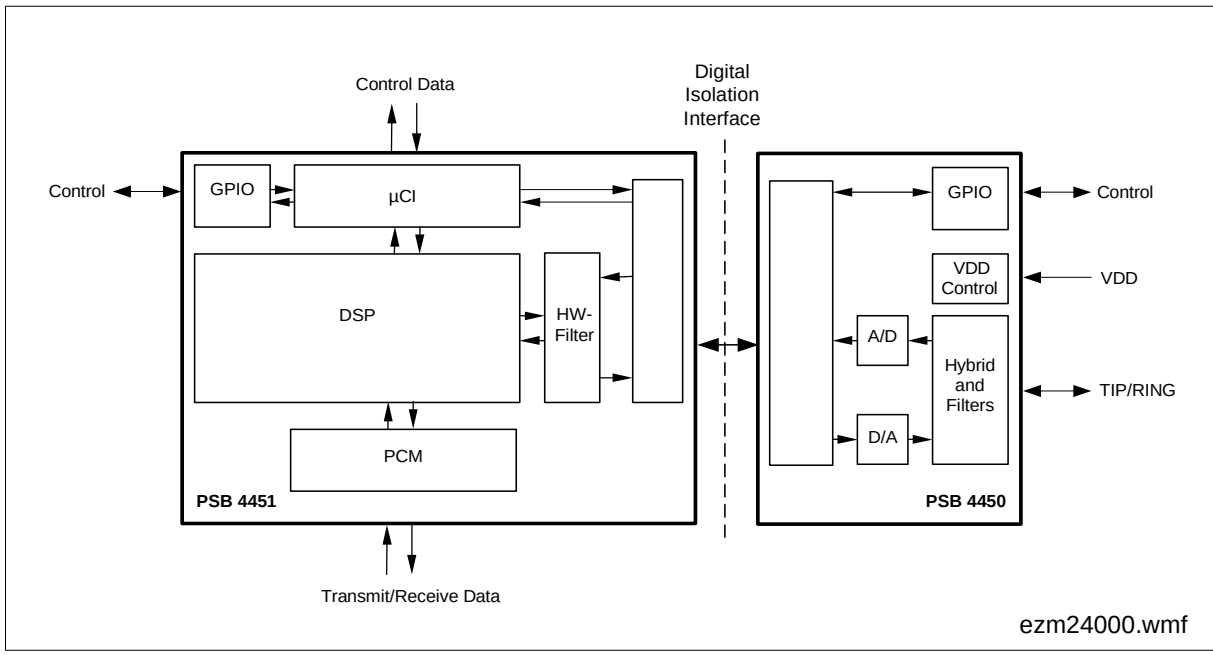


Figure 5 Functional Block Diagram of the PSB 4450/PSB 4451 Chip Set

PSB 4450:

VDD Control: regulates the supply voltage for the PSB 4450 and can be connected to an isolated 5 V or by the use of an external transistor to an unregulated DC voltage (VDD).

Hybrid and Filters: the hybrid provides two-wire to four-wire conversion, and the analog anti-aliasing pre-filters and smoothing post-filters provide signal conditioning.
The voice data path is routed from the filters to the digital isolation interface through the **Analog-to-Digital** (A/D) or the **Digital-to-Analog** (D/A) converters: These are oversampling converters based on a Δ–Σ modulation approach. The oversampling technique provides signals with low signal-to-noise ratio and high conversion resolution.
Digital Isolation Interface: Used for isolation of PSB 4451 from PSB 4450.
General **P**urpose **I/Os (GPIOs):** PSB 4450 has 2 inputs (SI0, SI1) and 2 outputs (SO2, SO3Q). The inputs can be used as interrupt sources. The outputs can be used to control external switches for the connection of terminal impedance.

PSB 4451:

Hardware filters: The HW filters are interpolating transmit and decimating receive digital filters. See also **Figure 6** for details.

Digital Signal Processing Unit (DSP): The DSP does equalization, gain adjustment, impedance matching, and other DAA functions, in accordance with the downloaded coefficient set.

PCM Interface: Via the PCM Interface transmit and receive data are transferred between the PSB 4451 and the digital transceiver (e.g. MDSL chip set).

Serial Control Interface (SCI): The Serial Control Interface allows external control of the ANIC features and provides transparent access to ANIC commands and signalling pins, so that pre-calculated coefficient sets can be downloaded from the system to the on-chip Coefficient RAM (CRAM) to program the filters.

General **P**urpose **I/Os (GPIOs):** PSB 4451 has two input/output pins (SIOD1, RINGIND/ SIOD0) and one output pin (METIND/SOD0) to control external components.

4.2 General Description

4.2.1 Impedance

ANIC requires an external transistor T1 to control the DC and AC loop current. T1 must be able to handle 100 mA of continous current.

On the TIP/RING side, ANIC applies voltage sensing and current feeding. There is a feedback loop between the receive and the transmit path to synthesize input impedance. This means the voltage is multiplied by a transfer function and fed back as a current to the line. This transfer function synthesizes the ANIC input impedance for AC, DC and RING. Within that functionallity, the ANIC acts as the required passive network.

4.3 Voice Path

These filters are programmable according to the selected specification by downloading the appropriate sets of coefficients. The converted signal is available at the PCM output every 125 µs. Decoding can be either selected according G.711 (A- / µ-law) or 16-bit linear 2´s complement. Similarly, digital data in the transmit direction are shifted in and processed by programmable filters for the selected specification. The results are sent to the interpolating transmit filter and are converted to an analog signal by the oversampling D/A converter.

Figure 6 shows the voice path through the digital filter structure. Some filters are fixed while others are user programmable.

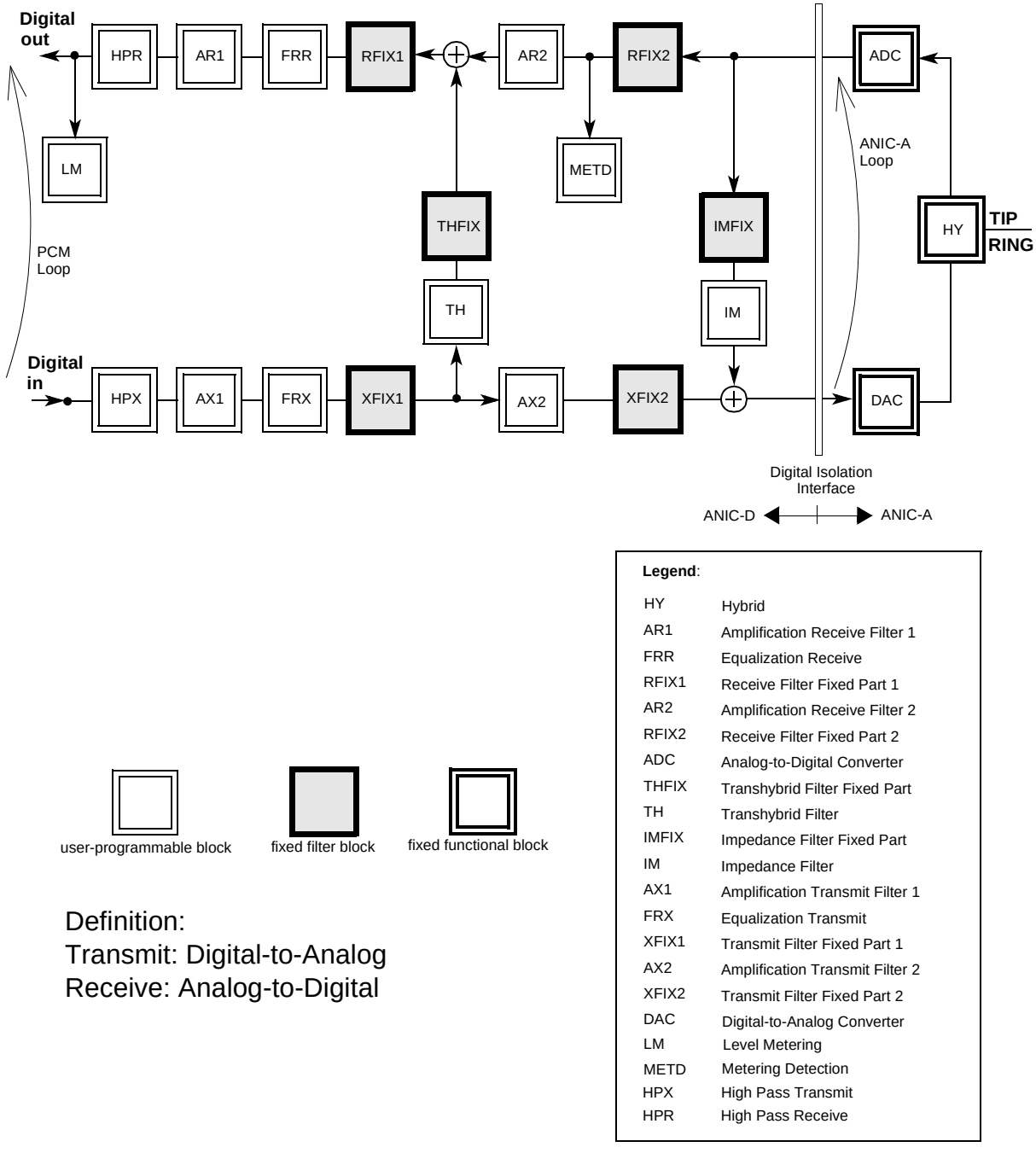


Figure 6 Voice Path

4.3.1 Receive Path

The analog signal proceeds from TIP/RING to PSB 4450 with an anti-aliasing pre-filter. The Analog-to-Digital Converter (ADC) is a sigma-delta converter, which converts the signal to a 1-bit digital data stream. The signal is then passed to the PSB 4451 where the first stage of down-sampling is performed in hardware, for better performance, in the digital filter RFIX2.

Subsequent stages of processing are done by microcode in the digital filter structure, to allow adaptability. Gain adjustment is provided in the two stages AR1 and AR2. The switchable high pass HPR is used to suppress low frequent noise.

A decimation stage is located inbetween to reduce the sampling rate to the 8/16 kHz PCM rate, and a low-pass filter to band-limit the signal in accordance with ITU-T G.714 and Q.552 recommendations; and an equalization stage (in FRR).

Finally, the signal will be A–law or µ–law coded and transferred out to the PCM Interface.

The ANIC meets or exceeds all ITU and ETSI recommendations on attenuation, distortion and group delay.

A metering function is included on the receive path.

4.3.2 Transmit Path

The digital input signal is received from the PCM Interface and decoded from A–law or µ–law. Most processing steps are done in microcode in the digital filter structure, which is programmable and therefore flexible.

There are two gain adjustment stages, in AX1 and AX2. The switchable high pass HPX is used to suppress low frequent noise.

Located inbetween, there is an equalization stage (in FRX), a high-pass filter and a low-pass filter to band-limit the signal (in XFIX1); and a first stage of interpolation.

Further up-sampling is done by hardware (in XFIX2), and the 1-bit data stream is converted to analog in the DAC and smoothed by a post-filter, followed by an analog gain stage before the signal is converted to a two-wire signal.

4.3.3 Loops

ANIC implementation includes two loops. One is used to generate the AC-termination impedance (IM, IMFIX), the ring impedance and the AC impedance for on-hook transmission and the other is used to perform accurate hybrid balancing (TH, THFIX).

4.4 Ring Path

The ringer impedance is synthesized in the same way as the AC impedance using a feedback loop.

4.5 DC Measurement Path

To measure the DC voltage between TIP-RING, TIP-GROUND and RING-GROUND, a filter structure similar to that of the voice receive path is used. Each voltage is measured for an interval of 375 µs (3 times 1/8000 Hz) and stored in the corresponding register (2´s complements, see register 7 to register 9). These registers are updated every 1.125 milliseconds. The voltage is measured in four selectable ranges with 8 bit resolution (see register 25)

Each measurement provides individual programmable thresholds (registers 19 & 20 for RING-GROUND, registers 21 & 22 for TIP-GROUND and registers 15 to 18 for TIP-RING). Any voltage exceeding these thresholds will trigger a maskable interrupt. The measured value can be used to detect line reversal and disconnection of the line.

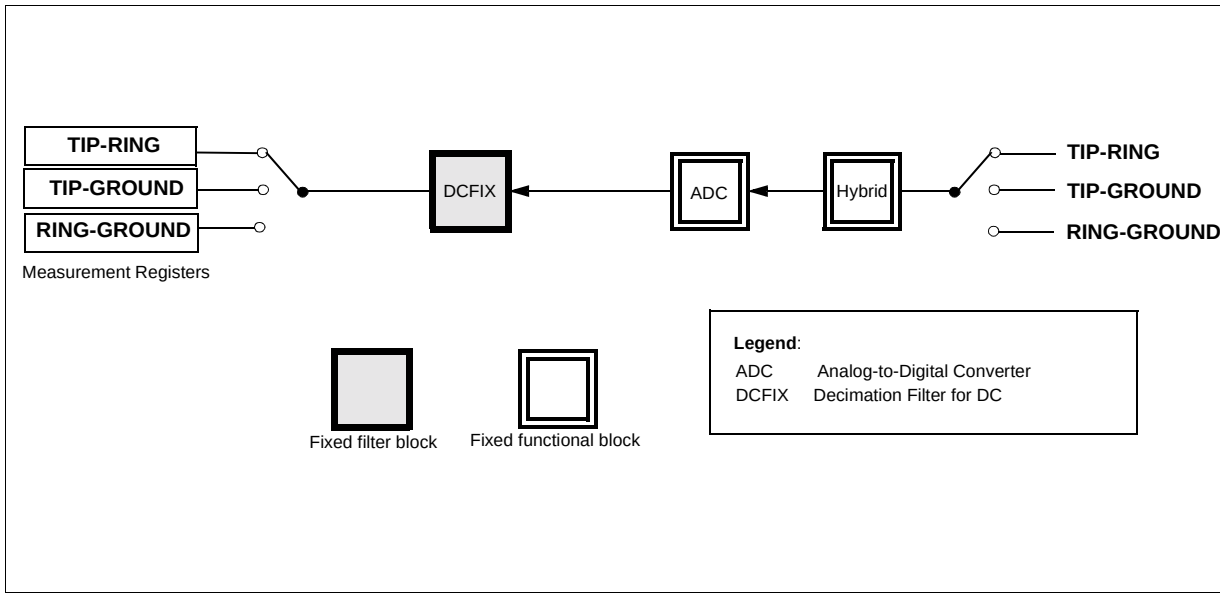


Figure 7 DC Measurement Path

4.6 Tone Detection[1)]

ANIC is equipped with two programmable tone detectors to detect modem and CALLER ID alert tones. Both of them can generate an interrupt.

1) Coefficients will be computed by the ANICOS Software. By downloading these coefficients to the ANIC using the ANICON software, the desired functionality will be provided.

4.7 Metering[1)]

Metering frequencies of 12 and 16 kHz are filtered out by the PSB 4451. Signals with level less than 2.5 Vrms can be applied directly to ANIC. However, an external notch filter is necessary to attenuate metering signals that exceed 2.5 Vrms.

ANIC is capable of signalling metering information via interrupt. Longitudinal 50 Hz metering can be realized usings ANICs measurement cabability.

4.8 Ring Detect[2)]

ANIC can be programmed to detect ring signals and will indicate them with an interrupt. The ring threshold as well as the ring frequency can be programmed.

1) Coefficients will be computed by the ANICOS Software. By downloading these coefficients to the ANIC using the ANICON software, the desired functionality will be provided.

2) Coefficients will be computed by the ANICOS Software. By downloading these coefficients to the ANIC using the ANICON software, the desired functionality will be provided.

4.9 Interrupt Structure

4.9.1 Interrupt-Handling

All interrupt sources are polled at a time intervall of at least t_{FSC} = 125 µs for FSC = 8 kHz (depending on the load of the controller). That means that an interrupt source must be stable for a minimum of this period to be detected.

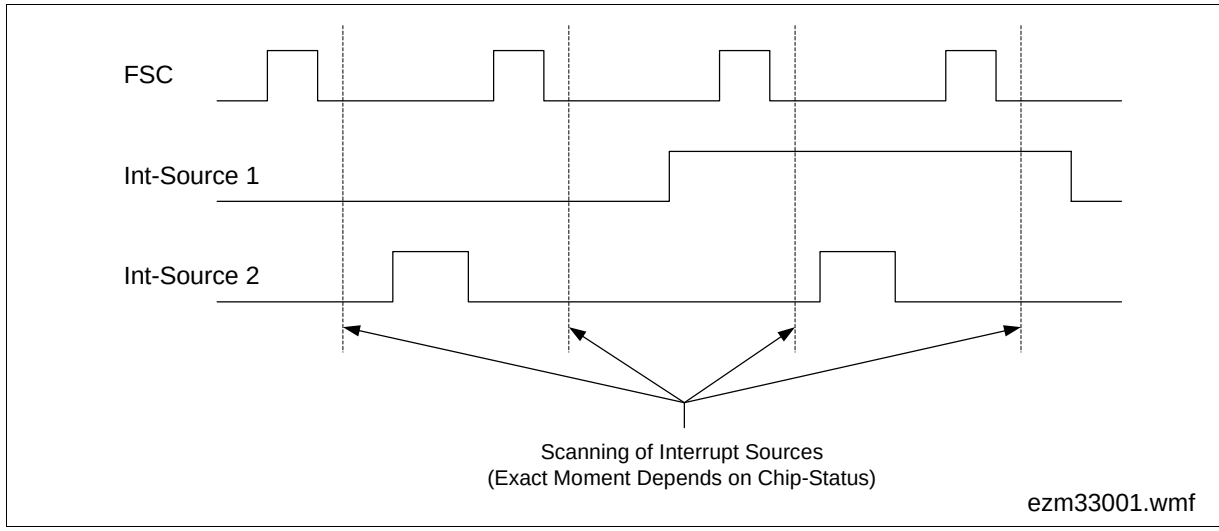


Figure 8 Interrupt Structure

In the above example the change of the Int-Source 1 is detected. Int-Source 2 is not detected by the Interrupt-controller and therefore will be ignored.

The host can enable the $\overline{INT}$ output by setting register 2. Following power-up, register 2 is cleared, i.e., all interrupt sources are disabled and $\overline{INT}$ is in high impedance state.

$\overline{INT}$, when asserted low, indicates an interrupt. The host reads the register 1 to determine the source of the interrupt. Reading the interrupt status register 1 clears the register content. All interrupt sources have equal priority.

4.9.2 Interrupt Sources

TYPE	NAME	MEANING
Static	SI0, SI1	Detection of changes on this GPI´s of ANIC-A via the digital isolation interface
Static	RINGIND/ SIOD0, SIOD1	Detection of changes on this GPIO´s of ANIC-D, when they are configured as inputs
Static	RING	Detection of ring signal
Static	MET	Detection of metering signals by ANIC DSP software
Dynamic	TONE	Detection of programmed tone
Dynamic	THRESHOLD	Detection if actual programmed threshold value on TIP-RING, RING-GROUND or TIP-GROUND has been exceeded.

Polling:

If all interrupts are disabled in register 2 there is still a possibility to poll the events that otherwise would have caused an indication at the $\overline{\text{INT}}$ pin. The occurence of an interrupt can always be detected by reading the register 1.

There are two types of interrupts:

4.9.2.1 Static Interrupts

Static interrupts take place on signal changes of the following signals:

- Static interrupt sources on pins SI0, SI1, RINGIND / SIOD0 and SIOD1
- Detection of ring signals
- Detection of metering signals

Every detected signal change is reflected by an logic 1 in the corresponding bit in the register 1. Unlike dynamic interrupts there is also an interrupt produced at the end of the event or signal.

Interrupts on the pins SI0, SI1, RINGIND/SIOD0 and SIOD1:

Interrupts on the GPI pins SI0 and SI1 use the following bits:

- Bits SIA0 and SIA1 in register 5 indicate the value of the pins SI0 and SI1.
- Bits SIA0 and SIA1 in register 1 show that a signal on the pins SI0 and SI1 was the cause for an interrupt indication on the $\overline{\text{INT}}$ pin. Reading register 1 sets the $\overline{\text{INT}}$ pin back to inactive (high).

For detecting interrupts on the GPIO pins RINGIND/SIOD0 and SIOD1 it is necessary to configure them as inputs in register 10. The following bits are used:

- Bits SIOD0_I and SIOD1_I in register 5 indicate the value of the pins RINGIND/SIOD0 and SIOD1.
- Bits SIOD0 and SIOD1 in register 1 show that a signal on the pins RINGIND/SIOD0 and SIOD1 was the cause for an interrupt indication on the $\overline{\text{INT}}$ pin. Reading register 1 sets the $\overline{\text{INT}}$ pin back to inactive (high).

Figure 9 shows the status of the $\overline{\text{INT}}$ output in relation to the static interrupt sources SI_X input pins.

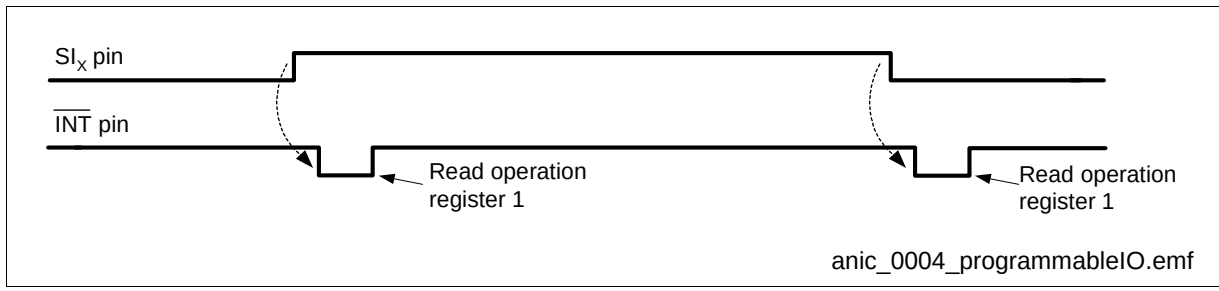


Figure 9 Interrupts on the pins SI0, SI1, RINGIND/SIOD0 and SIOD1

Ring Interrupt:

There are two possibilities for ring detection on TIP/RING:

1. Ring interrupt by detection of a voltage above the ring threshold

Since only a voltage detection takes place, the validation according to amplitude and frequency of the ring signal has still to be done by the host.
The ring interrupt indication on the RINGIND/SIOD0 pin derives from internal signals which allow checking for spike rejection (ring deglitch time, see register 27), suppression of short rings (ring persistance time, see register 26) and ring interruptions (ring timeout, see register 103) as shown in **Figure 10**.

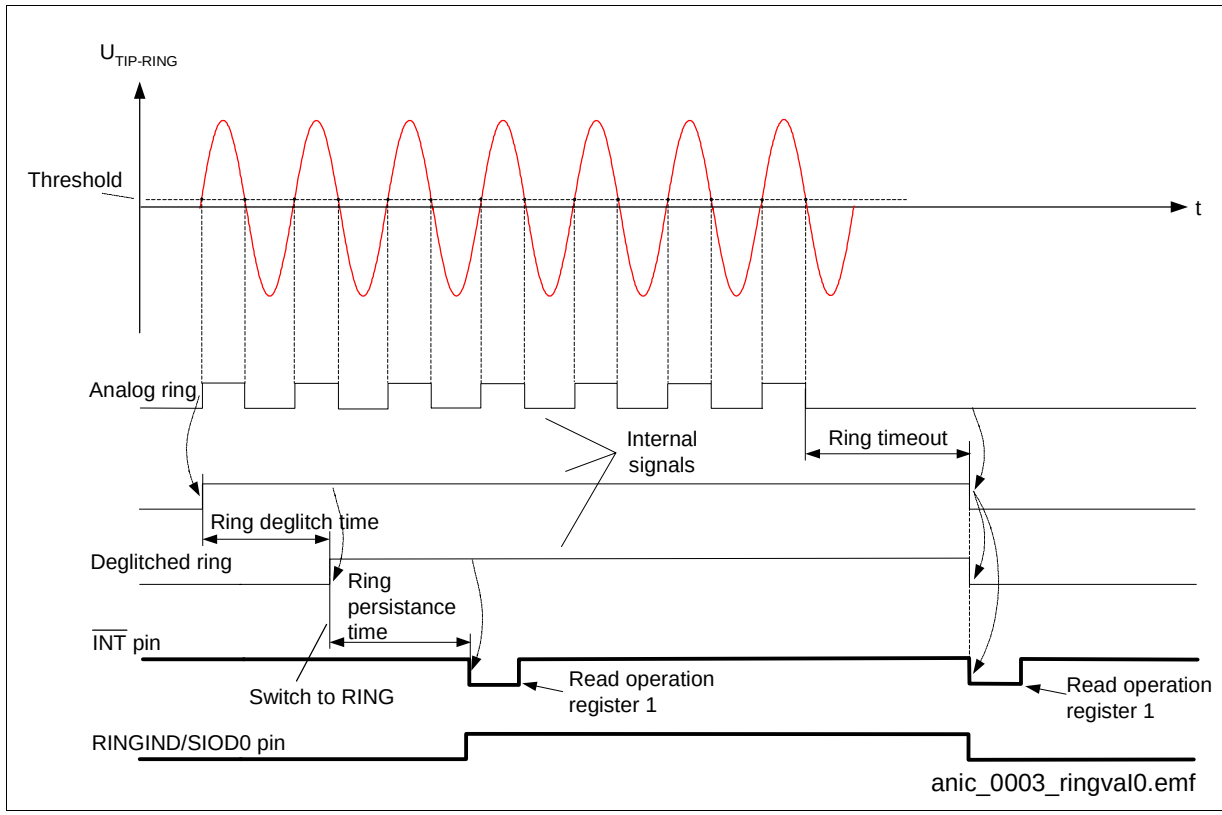


Figure 10 Ring Interrupt by Detection of a Voltage above a Threshold

2. Ring interrupt by detection of valid ring

Figure 11 shows a ring interrupt with internal validation in the ANIC according to amplitude and frequency defined by programmed CRAM coefficients.

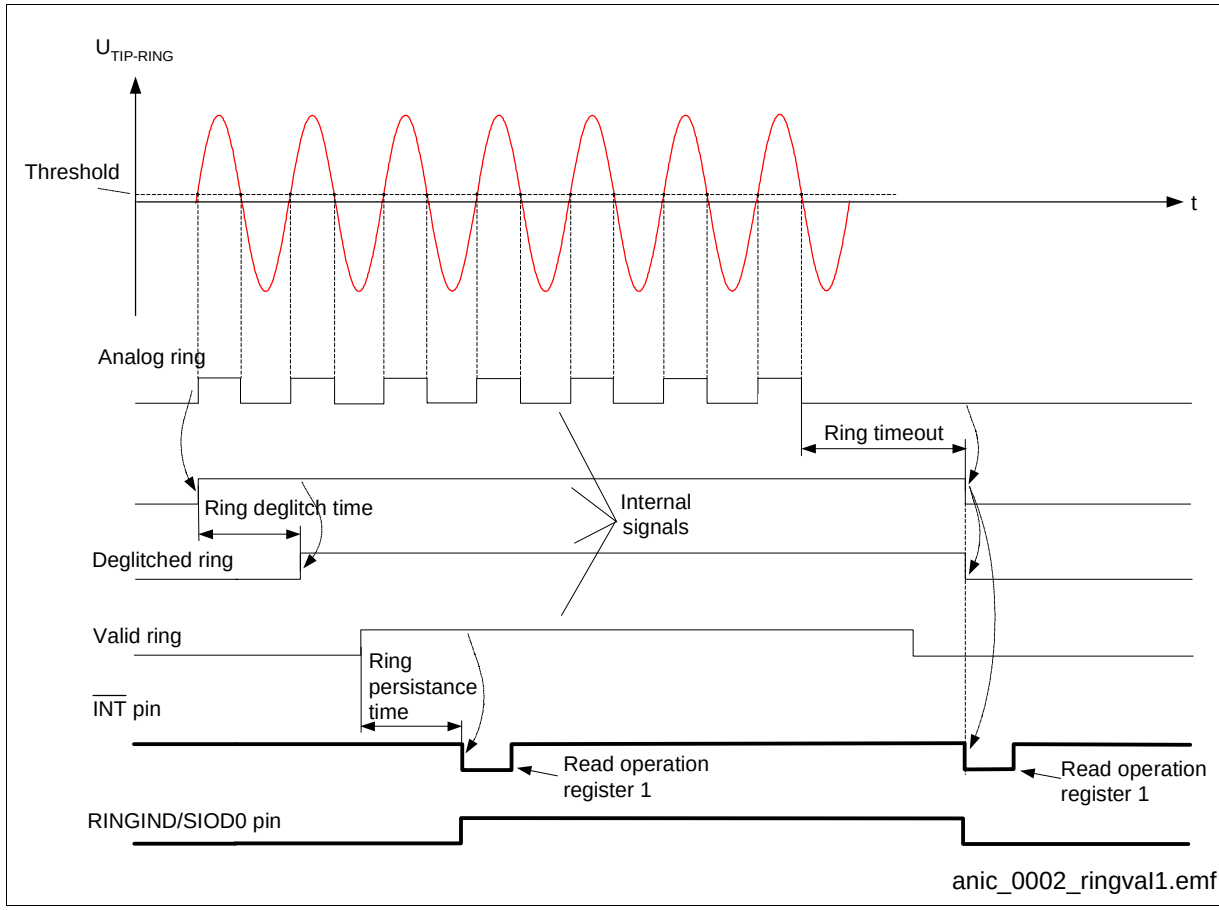


Figure 11 Ring Interrupt by Detection of Valid Ring

According to **Figure 12**, ring signal detection in ANIC-A causes an automatic transition from the ON-HOOK CONVERSATION or ON-HOOK RECEIVE to the RING state (see register 5).

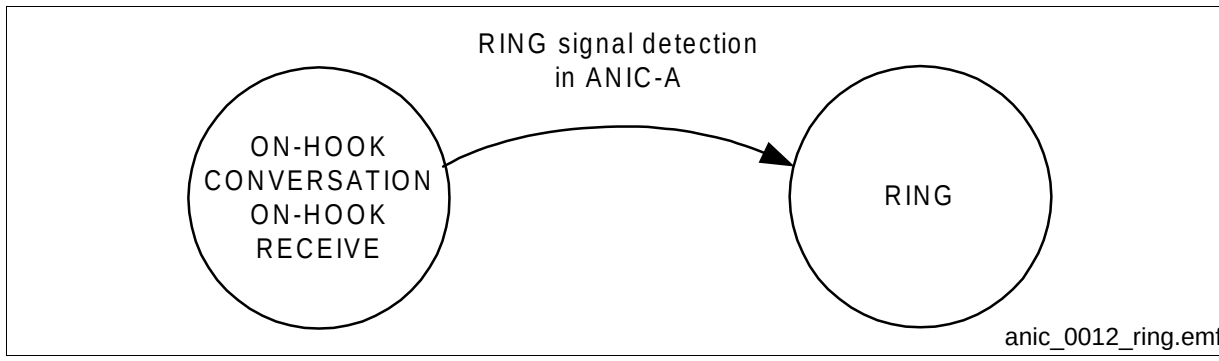


Figure 12 Ring Signal Detection in ANIC-A

Both possiblities for ring detection use the following bits:

- Bit SHOW_RING in register 24 enables the indication of the ring status on pin RINGIND/SIOD0, if this pin is configured as output (register 10).
- Bit RING in register 5 indicates if either a voltage above a ring threshold or a valid ring was detected or finished (depending of bit RING_VAL in register 10).
- Bit RING in register 1 shows that a ring detection was the cause for an interrupt indication on the $\overline{\text{INT}}$ pin. Reading register 1 sets the $\overline{\text{INT}}$ pin back to inactive (high).

Metering Interrupt:

Metering interrupts use the following bits:

- Bit SHOW_MET in register 24 enables indication of metering signals on pin METIND/SOD0.
- Bit MET in register 1 shows that a metering detection was the cause for an interrupt indication on the $\overline{\text{INT}}$ pin. Reading register 1 sets the $\overline{\text{INT}}$ pin back to inactive (high).

The metering interrupt indication on the METIND/SOD0 pin derives from internal signals which allow checking for suppression of short metering signals (metering persistance time, see register 28) and metering signal interruptions (metering timeout, see register 104) as shown in **Figure 13**. The filter transient ON and OFF times are defined by CRAM settings.

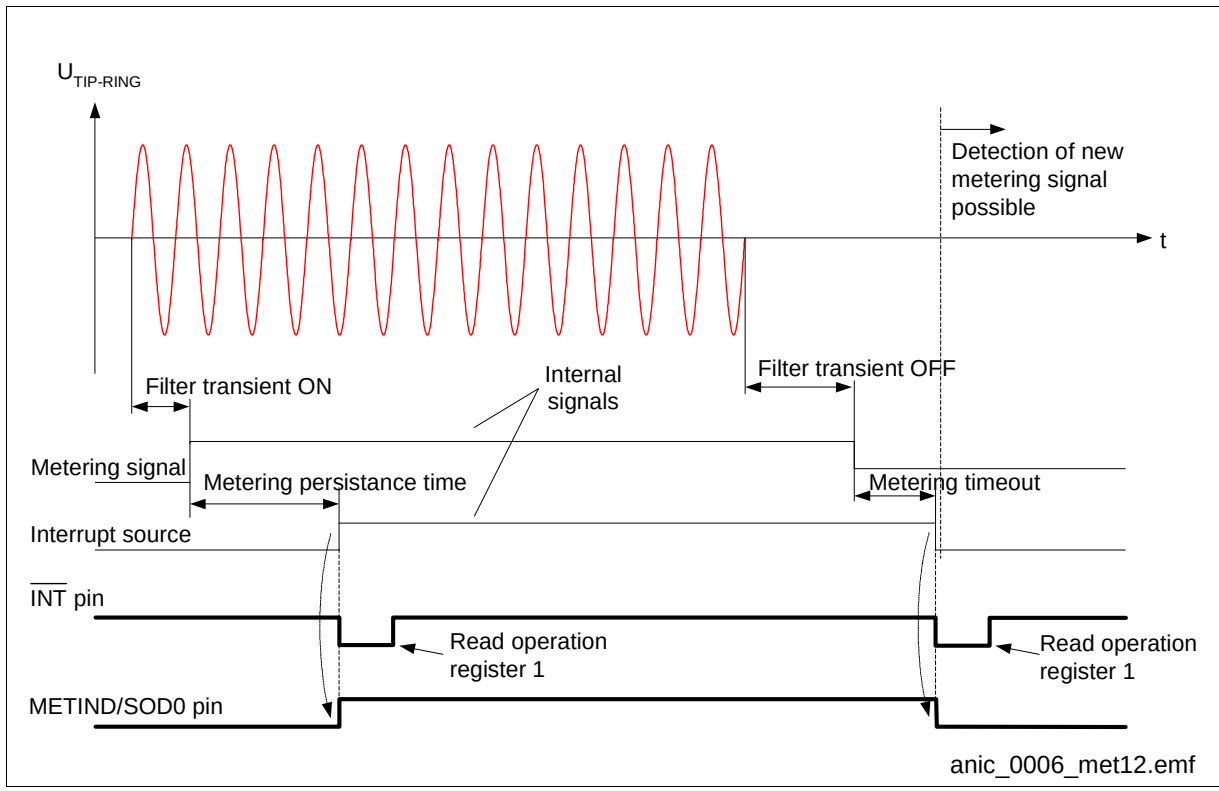


Figure 13 Metering Interrupt

4.9.2.2 Dynamic Interrupts

Dynamic interrupts are caused by the following events:

- Detection of tone signals
- Passing of programmed threshold voltages at TIP-RING, RING-GROUND and TIP-GROUND.

Unlike static interrupts there is no interrupt produced at the end of the event.
Every detected event is reflected by a logic 1 in the corresponding bit of register 1 (details in register 2 and register 5).

Tone Interrupt:

Tone interrupts can be used for fax or modem alert tone detection.

The following bits are used:

- Bits E_TONE(0) and E_TONE(1) in register 24 enable the detection of the tone sources tone 0 or tone 1.
- Bits TONE(0) and TONE(1) in register 5 indicate the detection of the tone sources tone 0 or tone 1. Reading register 5 clears the bits TONE(0) and TONE(1).
- Bit TONE in register 1 shows that a tone detection was the cause for an interrupt indication on the $\overline{\text{INT}}$ pin. Reading register 1 sets the $\overline{\text{INT}}$ pin back to inactive (high).

The tone interrupt indication on the $\overline{\text{INT}}$ pin derives from internal signals which allow checking for suppression of short metering signals (tone persistance time, see register 28) and tone signal interruptions (tone timeout, see register 104) as shown in **Figure 14**. The filter transient ON and OFF times are defined by CRAM settings.

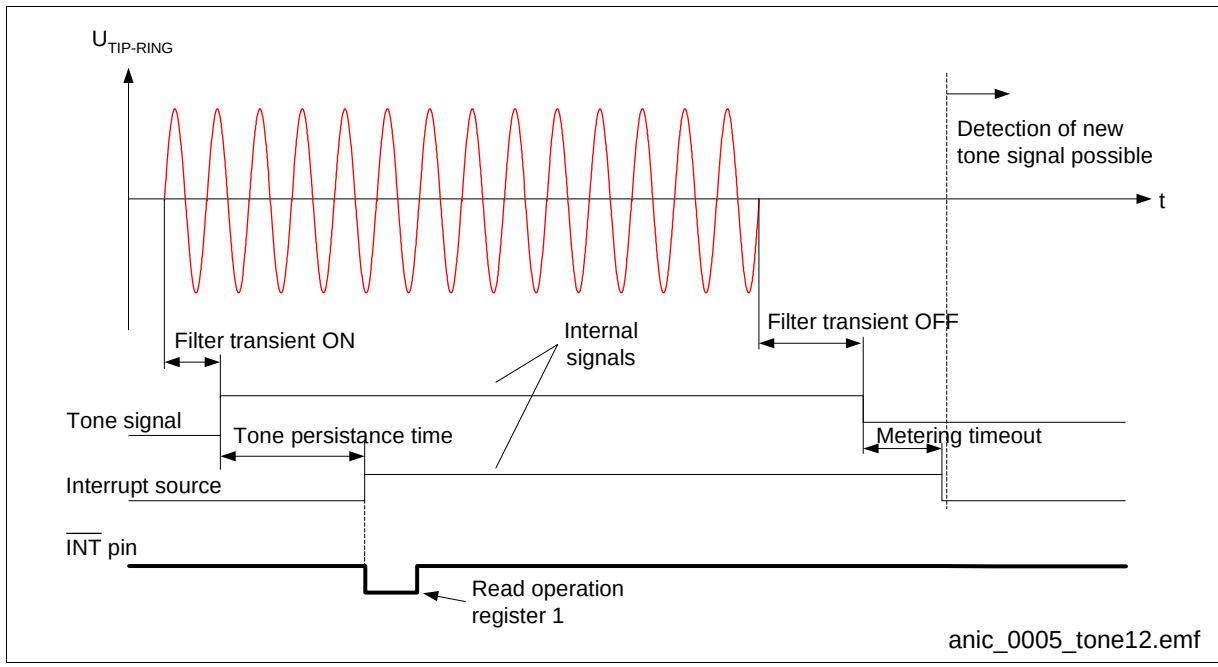


Figure 14 Tone Interrupt

When there are two consecutive tone interrupts (e.g. "INT-A" followed by "INT-B", see **Figure 15**) and INT-B happens before the interrupt service routine of INT-A could read register 5, the source of INT-B will be read together with the source of INT-A in register 5 (Bits TONE(0) = TONE(1) = 1). As reading register 5 clears the bits TONE(0) and TONE(1), the later starting interrupt service routine of INT-B can´t find a source for this interrupt in register 5 (Bits TONE(0) = TONE(1) = 0). Therefore, the host must ignore the interrupt service routine of INT-B and use the values of the former routine.

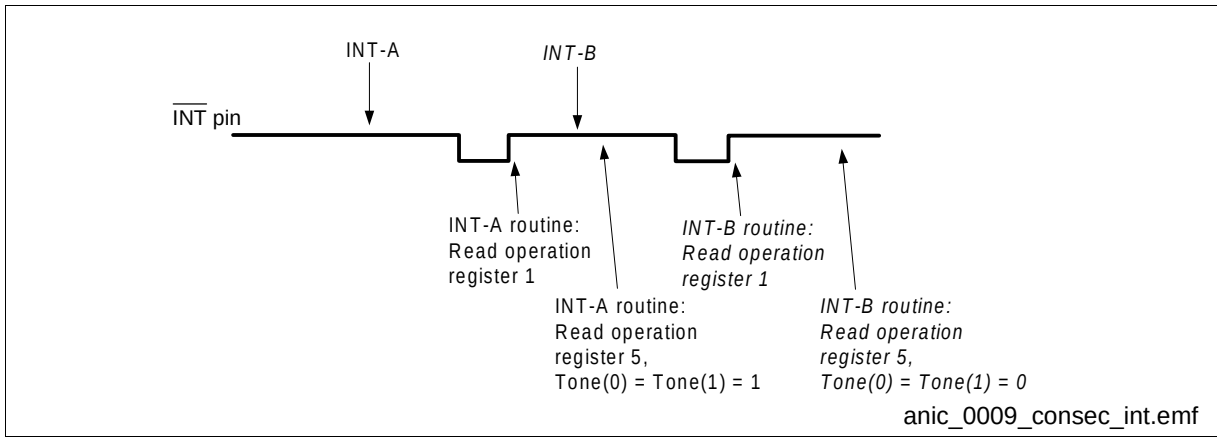


Figure 15 Example for Consecutive Tone Interrupts

Threshold Interrupt:

Threshold interrupts can be used to detect line reversal, disconnect or 50 Hz metering signals on TIP-RING, RING-GROUND or TIP-GROUND line voltages. An interrupt is detected, when the line voltage passes a programmable threshold voltage (see registers 15 to 22).

TIP-RING, RING-GROUND and TIP-GROUND threshold interrupts use the following bits:

- Bits E_TR(x), E_RG(x) and E_TG(x) in register 23 enable the detection of TIP-RING, RING-GROUND or TIP-GROUND line voltage threshold indications.
- Bits TR(x), RG(x) and TG(x) in register 4 indicate the TIP-RING, RING-GROUND and TIP-GROUND voltages passing a programmed threshold value. Reading register 4 clears the bits TR(x), RG(x) and TG(x).
- Bit THR in register 1 shows that passing a voltage threshold was the cause for an interrupt indication on the $\overline{\text{INT}}$ pin. Reading register 1 sets the $\overline{\text{INT}}$ pin back to inactive (high).

Figure 16 shows an example for a TIP-RING threshold interrupt with the threshold voltages TR0 to TR3 (registers 15 to 18). A programmable measurement persistance time (see register 29) helps to avoid threshold indications caused by spikes. $U_{M2\text{-}M3}$ is the voltage between the pins M2 and M3 which derives from TIP and RING.

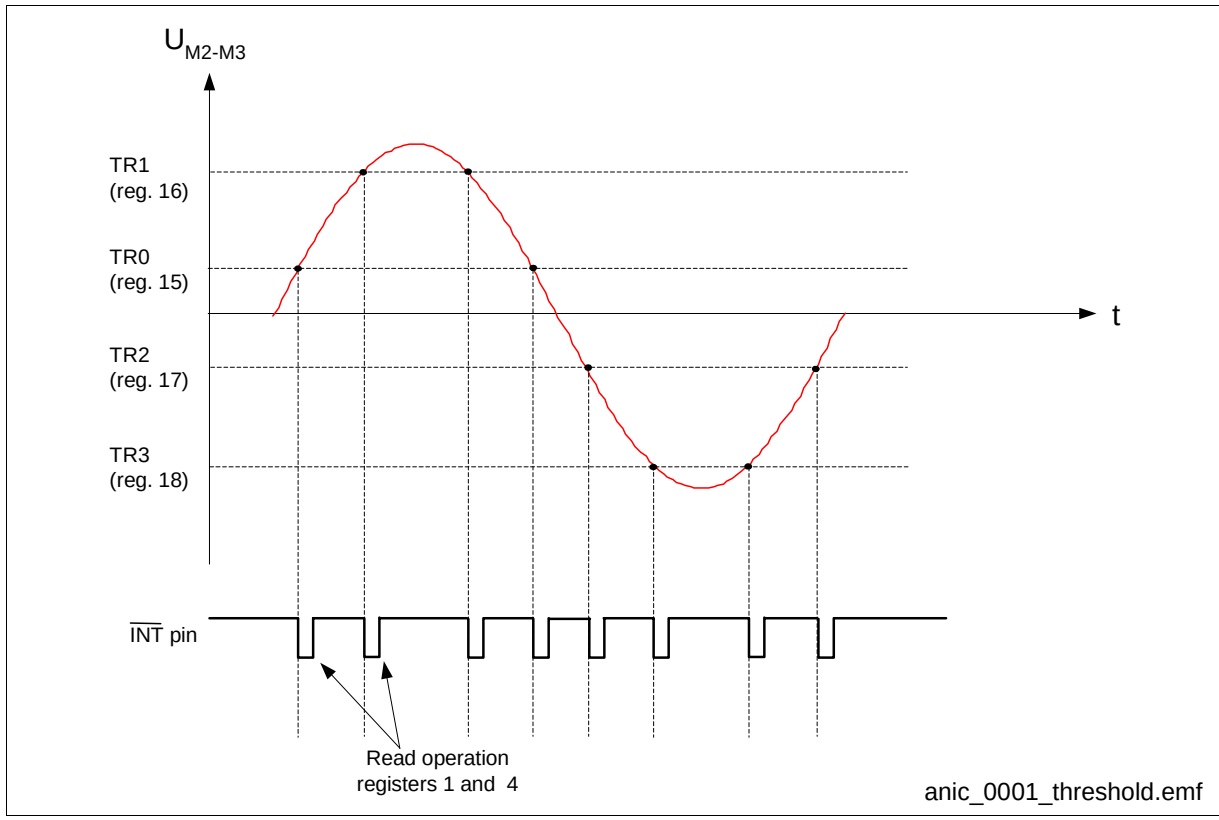


Figure 16 Threshold Interrupt: TIP-RING

When there are two consecutive threshold interrupts (e.g. "INT-A" followed by "INT-B", see **Figure 17**) and INT-B happens before the interrupt service routine of INT-A could read register 4, the source of INT-B will be read together with the source of INT-A in register 4 (Bits TR(x), RG(x) and TG(x)). As reading register 4 clears the bits TONE(0) and TONE(1), the later starting interrupt service routine of INT-B can´t find a source for this interrupt in register 4 (Bits TR(x) = RG(x) = TG(x) = 0). Therefore, the host must ignore the interrupt service routine of INT-B and use the values of the former routine.

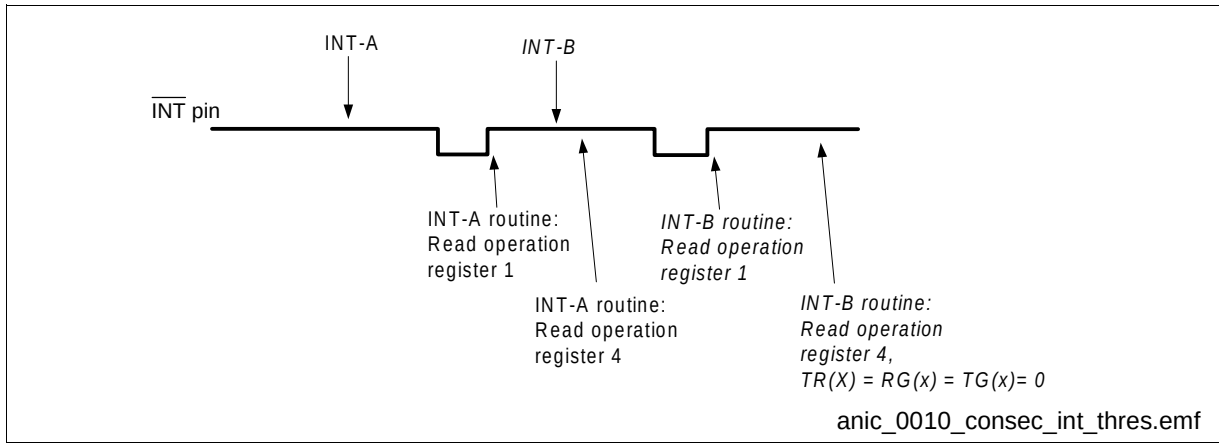


Figure 17 Example for Consecutive Threshold Interrupts

4.10 ANIC Clocking

Any master clock frequency between 16.384 MHz and 33 MHz can be used as the ANIC synchronizes to the incoming frame sync (FSC).

The DCDCCLK or a synchronous clock should be used to clock a DCDC converter to supply the ANIC-A. This will prevent intermodulation in between the VDDA and the A/D or D/A converters of the ANIC-A.

4.11 Test Modes

4.11.1 Data Loops

To test the chip datapath the following digital loops are available (see **Figure 6**):

- PCM loop to test the correct connection to the PCM Interface (see bit **PCM_LOOP** in register 10). The PCM input data will be send back exactly in the next PCM frame.
- ANIC-A loop to test the ANIC-A and ANIC-D (see bit **ANIC-A_LOOP** in register 10). Functional test loop. The functionallity of the ANIC-D and the digital isolation interface of the ANIC-A can be checked.

4.12 Support Package

The ANIC can be programmed to pass individual country specific requirements. This can be done by downloading different coefficients into the CRAM using the ANICON control software. For the calculation of these coefficients a coefficent computing program called ANICOS will be provided.

The ANICOS software is a project-oriented Windows-based program. On-line help is available and the validity of user inputs checked automatically, enabling users to obtain optimized sets of coefficients to program the ANIC quickly and easily.

ANICOS calculates coefficients for the following filters.

AC Filters:

- Impedance matching to adapt the system to the required line impedance of the local loop (return loss calculation),
- Frequency response correction for both receive and transmit paths,
- Level adjustment for both receive and transmit paths,
- Transhybrid balancing

DC Filters:

- DC characteristic

Ringing:

- Ringer impedance
- Ring detect (level and frequency)

Miscellaneous:

- Ringing signal
- Level Metering
- Metering signals detection (level and frequency)

After defining the required inputs for ANICOS, the user can start calculating the filter coefficients. All calculation results are stored in the result file which can be displayed in the ANICOS program. Some of the calculations are also displayed graphically to enable the product designer to verify the required behaviour quickly, and make any additional optimization manually.

The following calculations are displayed graphically:

- Return loss,
- Input impedance,
- Frequency response in receive and transmit path (locus diagram),
- Transhybrid loss.

ANICOS produces both a result file and a byte file. The byte file contains the programming bytes, including the filter coefficients. An important feature of the ANICOS software is the automatic verification of the calculated coefficients against criteria necessary to maintain overall system stability.

5 Digital Interfaces

The digital interfaces consist of a Serial Control Interface (SCI) and a PCM Interface. Both interfaces operate up to 2048 kHz.

As described in **Chapter 4.10**, ANIC uses master clock frequencies from 16.384 up to 33 MHz. In this document, functionality is described for f_{MCLK} = 24.576 MHz.

5.1 Sample Rates

The internal datapath clock is synchronized to the frame synchronization (FSC) signal. For PCM frame based systems this clock is 8 kHz.

In this document, functionalitiy is described using this 8 kHz FSC.

However, the ANIC can be synchronized to all frame synchronization (FSC) signals between 6 and 12 kHz, although the used FSC frequencies are in a range between 8 and 12 kHz as shown in **Table 6**. The FSC limits can be computed:

Example: f_{MCLK} = 24.576 MHz, no predivider is used

$f_{FSC} = f_{FRAC} / 2048$

with

$f_{FRAC,min} = f_{MCLK} / [1+32767/32768] > f_{MCLK} / 2$

$f_{FRAC,max} = f_{MCLK} / [1+1/65536)] < f_{MCLK}$

Therefore:

Frame sync lower limit: $f_{FSC,min} > f_{MCLK} / 4096 = 6$ kHz

Frame sync upper limit: $f_{FSC,max} < f_{MCLK} / 2048 = 12$ kHz

Within one frame the ANIC can be programmed to provide one (8 k sampling mode) ore two (16 k sampling mode) samples (see register 14, bit 16k).

Following power-up ANIC is programmed to the 16-bit linear mode and 8 k sampling mode. If the companding mode is switched on (register 14, bit COMP = 1), ANIC sends and receives the 8 bit A-law companded data on one PCM slot.

Using the 16 kHz mode, the PCM decimation filter from 16 to 8 kHz is switched off and four consecutive time slots are used to provide these two samples. Within that mode, **only** the 16 bit linear data transmission is possible.

5.2 PCM Interface

A serial PCM Interface is used for voice transfer. The PCM Interface consists of 4 pins:

Table 3 PCM Interface Pins

DATCLK	PCM-Clock, 512 kHz to 2048 kHz
FSC	Frame Synchronization Clock
DATIN	Receive Voice input for PCM Highway
DATOUT	Transmit Voice output for PCM Highway

The data rate of the interface can vary from 512 kb/s to 2048 kb/s. A frame may consist of up to 32 time slots of 8 bits each. Receive and transmit time slots can be programmed individually in normal mode (PCM) and in linear mode. An extra delay of up to 7 clocks, valid for all channels, as well as the sampling slope[1)] may be programmed. In order to provide high bandwith for modem and fax application also a sample rate of 16 kHz can be programmed. In this mode the ANIC will use four consecutive timeslots for the two 16 kHz linear coded samples within one frame.

The frame sync (FSC) input determines the beginning of the receive and transmit time slots. The FSC must have a minimum duration of one DATCLK cycle (see **Chapter 9.5.4**). The DATCLK clock is the signal to synchronize the voice transfer on both lines DATOUT and DATIN. Bytes in all channels are serialized to 8 bit width (normal mode) or 16 bit width (linear mode) and MSB first. For configuration of the PCM Interface see register 14.

Note: In order to avoid bus contention, bit 0 (LSB) at DATOUT is only asserted during the positive half-cycle of DATCLK, and is high-impedance during the negative half-cycle of DATCLK. At power up, the PCM interface is inactive (tri-state condition) until the relevant registers are programmed.

Table 4 and **Table 5** list the possible clock rates for the PCM Interface at f_{FSC} = 8 kHz. Clock rates such as 768 kHz and 1536 kHz are also supported.

Table 6 shows the FSC frequency and number of time slots per PCM frame for a given SCI-clock f_{DCLK} and the 8 k or 16 k sampling mode. **Figure 18** to **Figure 21** are graphical illustrations of the values in **Table 6**.

Figure 22, **Table 4** and **Table 5** illustrate the PCM Interface timing and time slots mapping, respectively.

Figure 25 shows examples of time slot offset referenced to FSC. The recieve and transmit time slots are offset by the same amount of DATCLK periods.

1) Data can be sampled at the rising or falling edge of the clock.

Table 4 8 kHz Sampling Rate (8 k sampling mode, f_{FSC} = 8 kHz)

	PCM-Clock Frequency (kHz)	Time Slots (per highway)	Datarate (kbits/s per highway)
	512	8	512
	1024	16	1024
	2048	32	2048
Formula	f	f/64	f

Table 5 16 kHz Sampling Rate (16 k sampling mode, f_{FSC} = 8 kHz)

	PCM-Clock Frequency (kHz)	Time Slots (per highway)	Datarate (kbits/s per highway)
	512	4	512
	1024	8	1024
	2048	16	2048
Formula	f	f/128	f

Table 6 SCI-Clock, FSC, Sampling Mode and Time Slot Interdependency[1)]

SCI-Clock[2)] f_{DCLK} (kHz) / Sampling Mode	maximum FSC Frequency f_{FSC} (kHz)	Time Slots per Frame	Figure
2048 / 8 k	8	32	see **Figure 18**
	10	16	
	12	8	
2048 / 16 k	10	8	see **Figure 19**
1024 / 16 k	8	16	see **Figure 20**
	11	8	
512 / 16 k	10	16	see **Figure 21**
	11	8	

1) for f_{MCLK} = 24.576 MHz

2) Serial Control Interface SCI-Clock on pin DCLK (f_{DCLK})

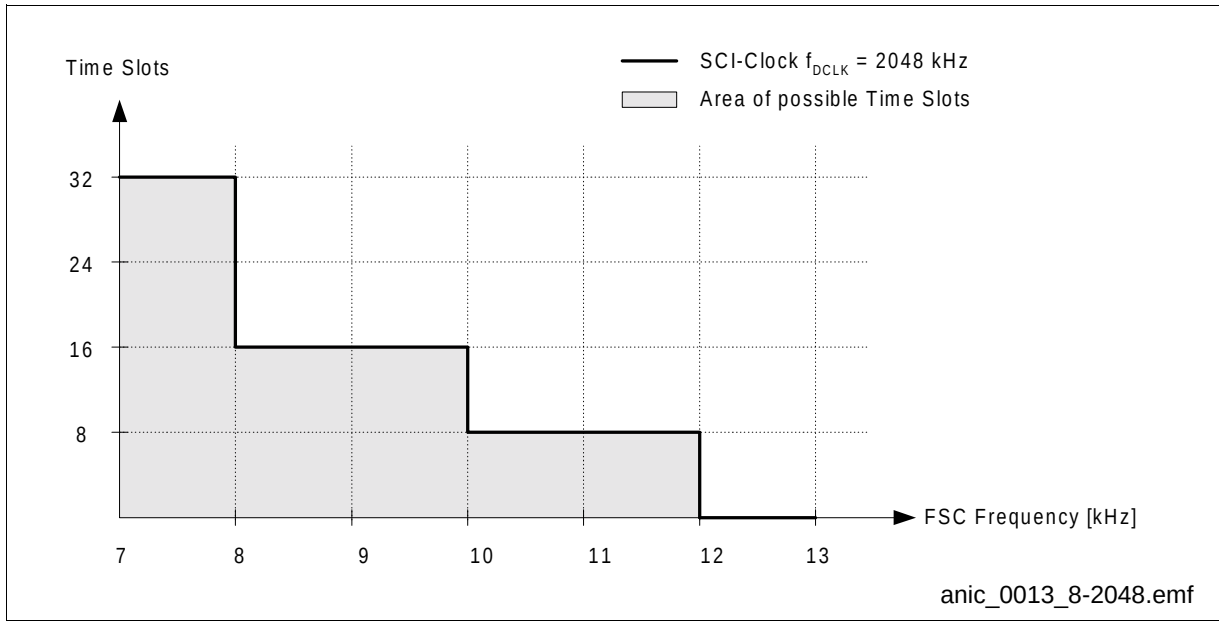


Figure 18 Time Slots for 8 k Sampling Mode and SCI-Clock 2048 kHz

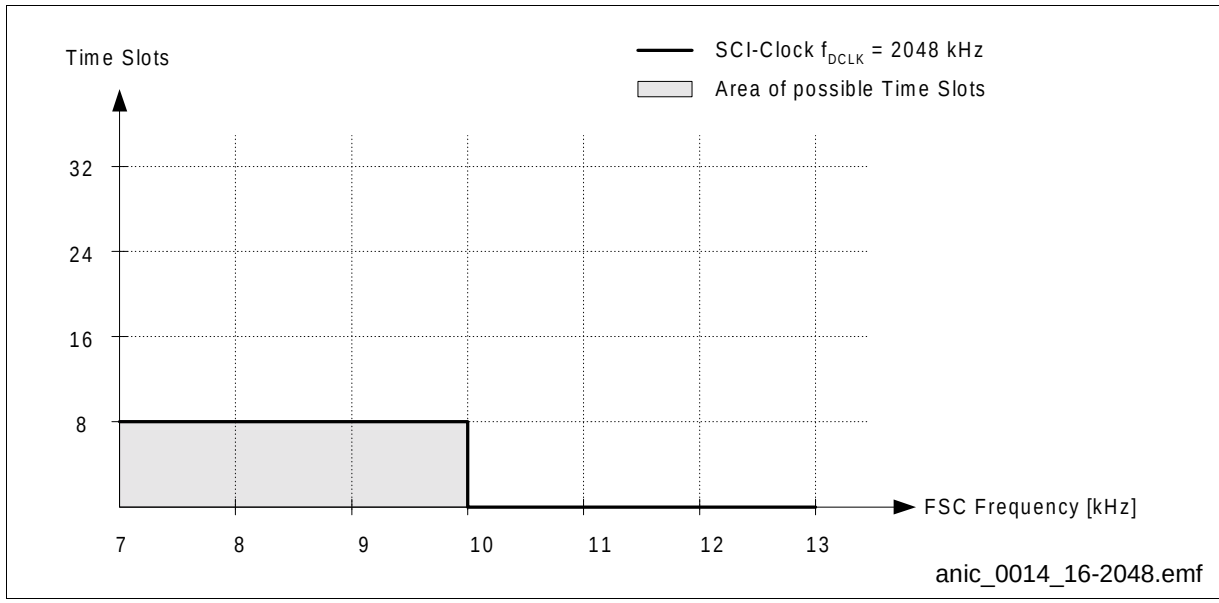


Figure 19 Time Slots for 16 k Sampling Mode and SCI-Clock 2048 kHz

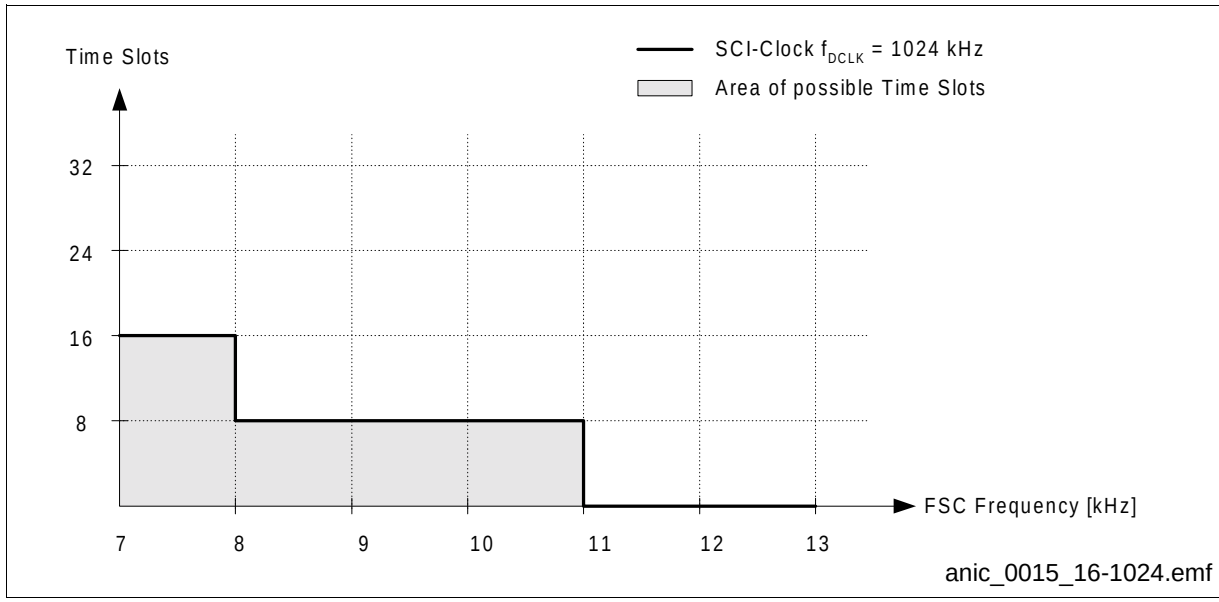


Figure 20 Time Slots for 16 k Sampling Mode and SCI-Clock 1024 kHz

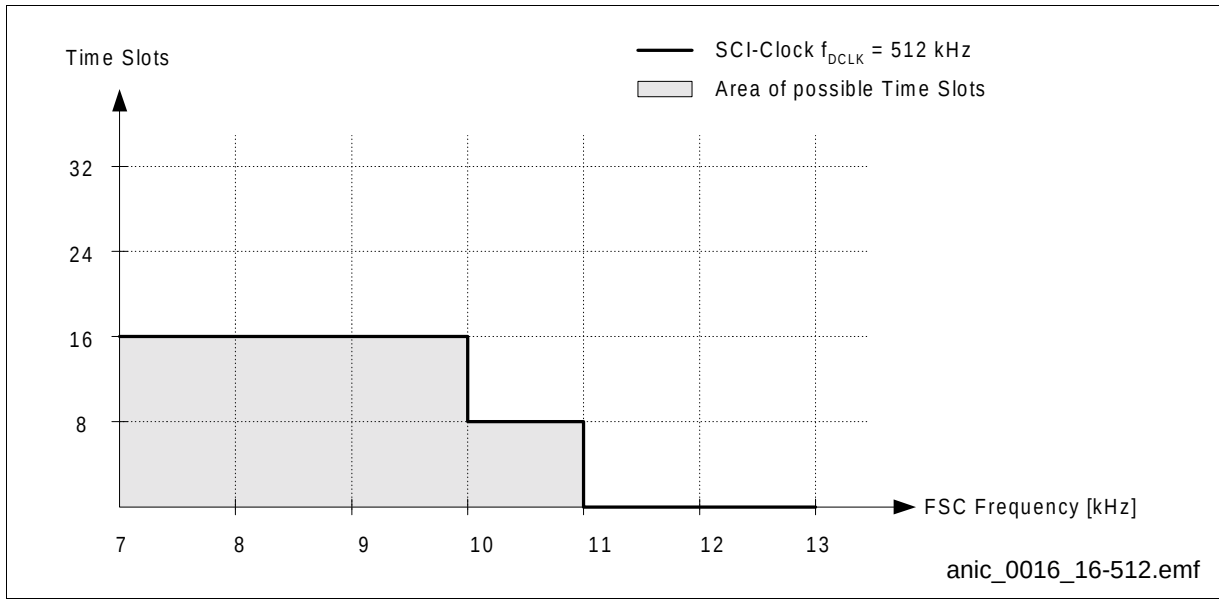


Figure 21 Time Slots for 16 k Sampling Mode and SCI-Clock 512 kHz

5.2.1 PCM Interface Timing Examples

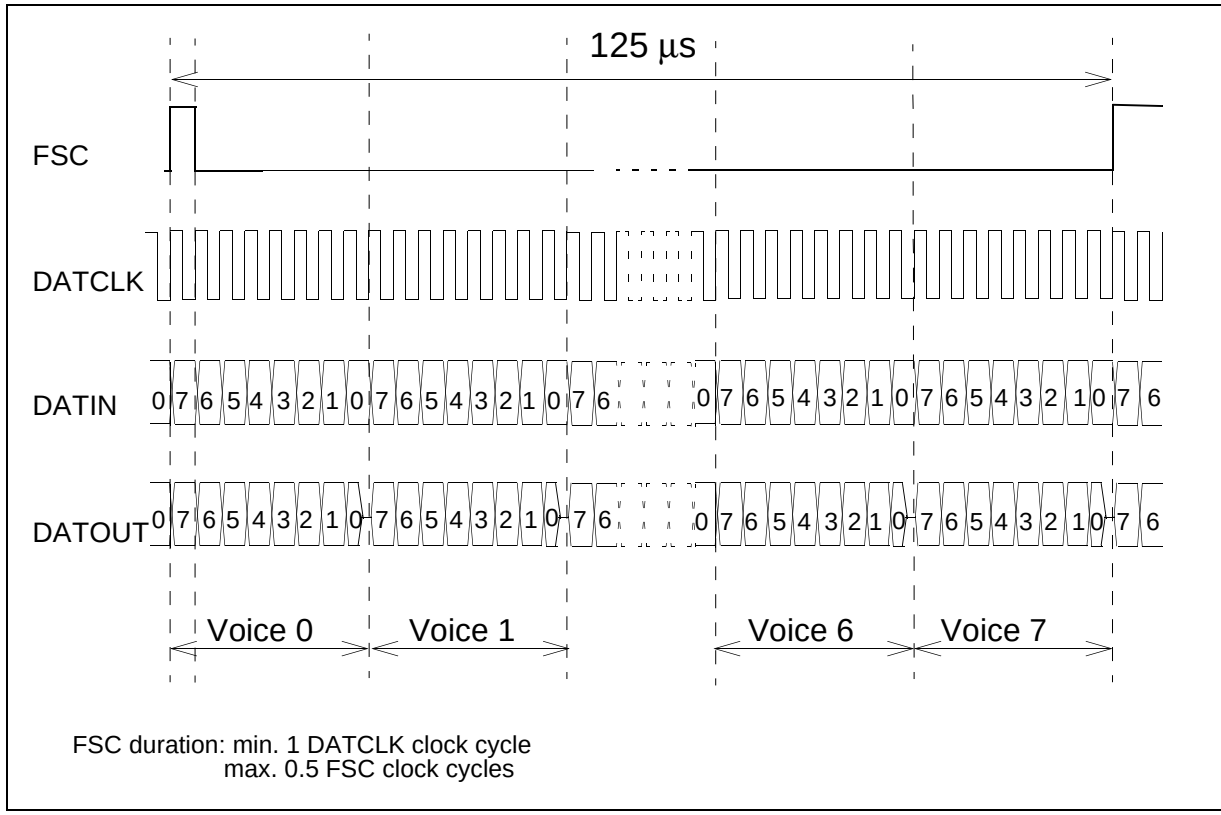


Figure 22 Example for Single Clock Rate, 512 kb/s

For special purposes the DATIN and DATOUT pins may be strapped together, and form a bi-directional datapin.

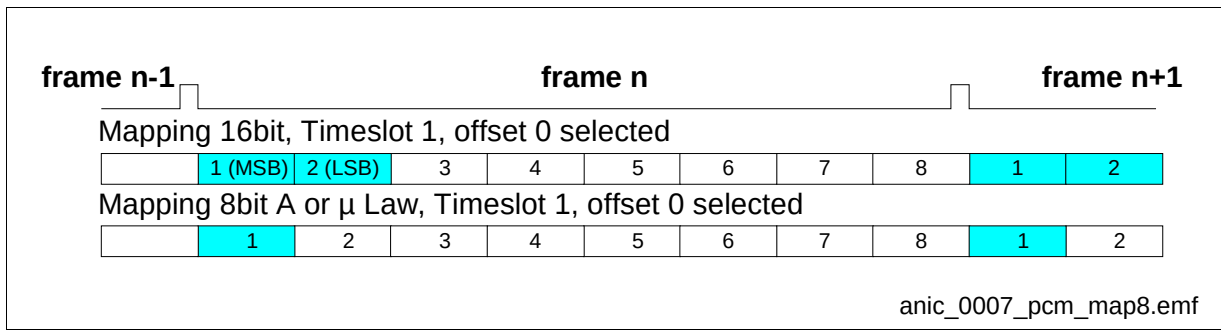


Figure 23 Mapping of Linear and Companded Data into PCM Slots for 8 kHz

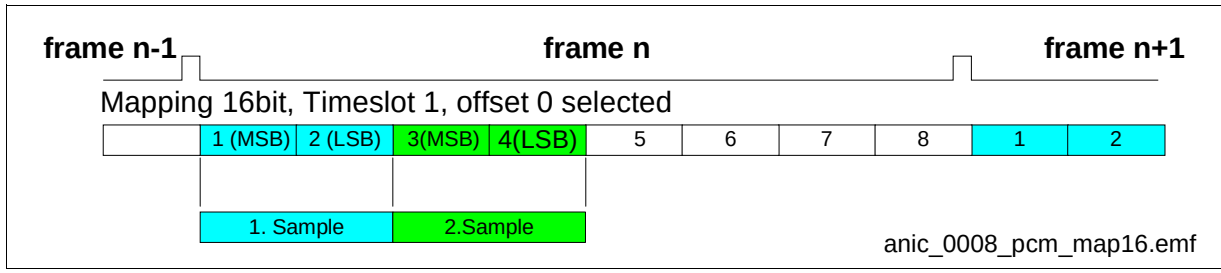


Figure 24 Mapping of Linear Data into PCM Slots for 16 kHz

Note: Using the 16 kHz sampling mode only the linear mode is availble.

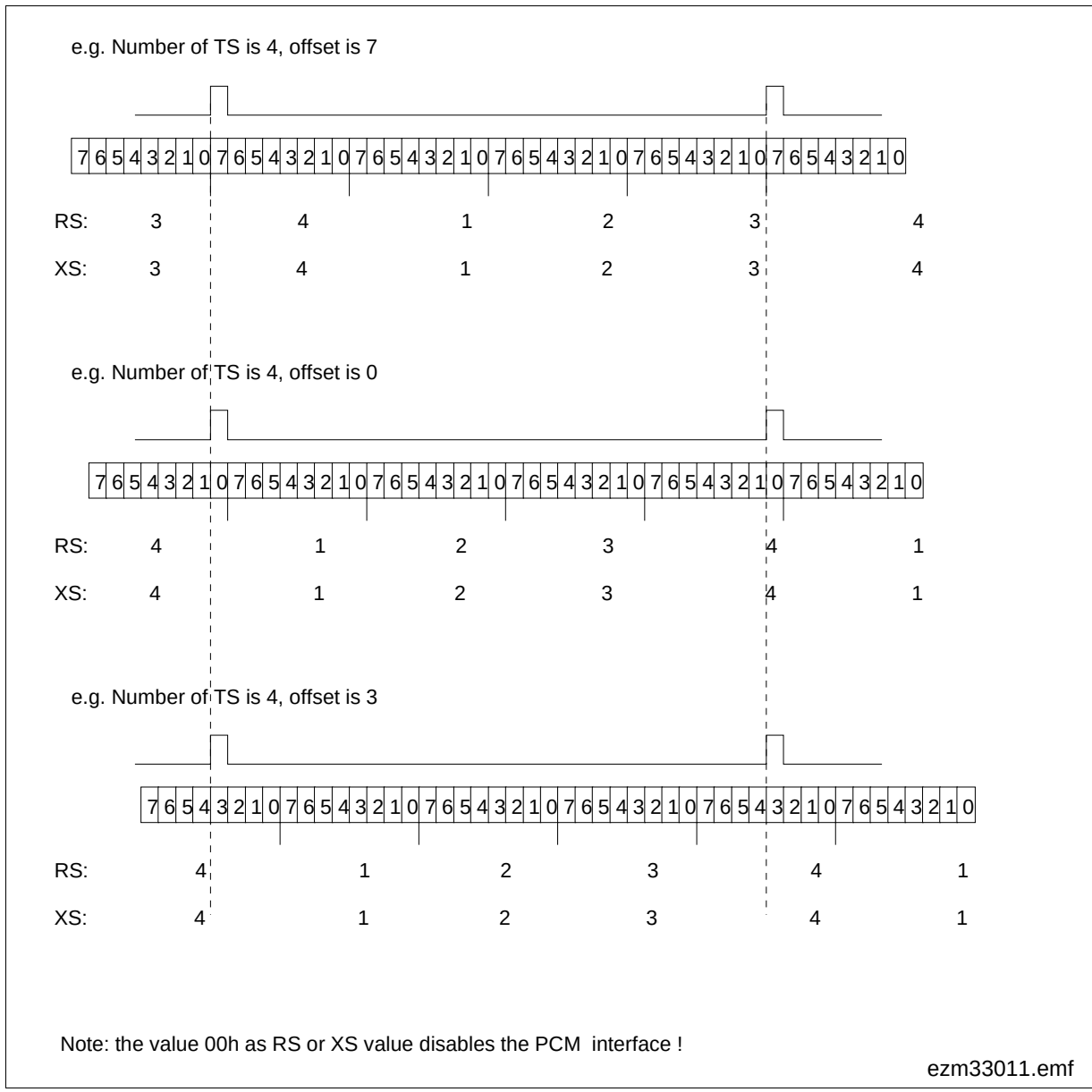


Figure 25 PCM Interface Frames

5.3 Serial Control Interface

The Serial Control Interface is used to communicate with an external host, e.g., a microcontroller.

The internal configuration registers, the auxiliary ports, and the Coefficient RAM (CRAM) of the ANIC are programmable via the Serial Control Interface. This Interface consists of 4 pins:

Table 7 Serial Control Interface Pins

CS	Chip select input, for enabling interface (active low)
DCLK	SCI-Clock input, f_{DCLK} = 1 kHz to 2048 kHz
DIN	Data input
DOUT	Data output

The host asserts $\overline{CS}$ low to initialize a communication with ANIC. Following a falling edge of $\overline{CS}$ the first 8 bits received at DIN determine the command type. The CLK clocks can be continously running or gated. However, there must be 16 low CLK pulses within the $\overline{CS}$ low interval to complete a READ or WRITE transaction.

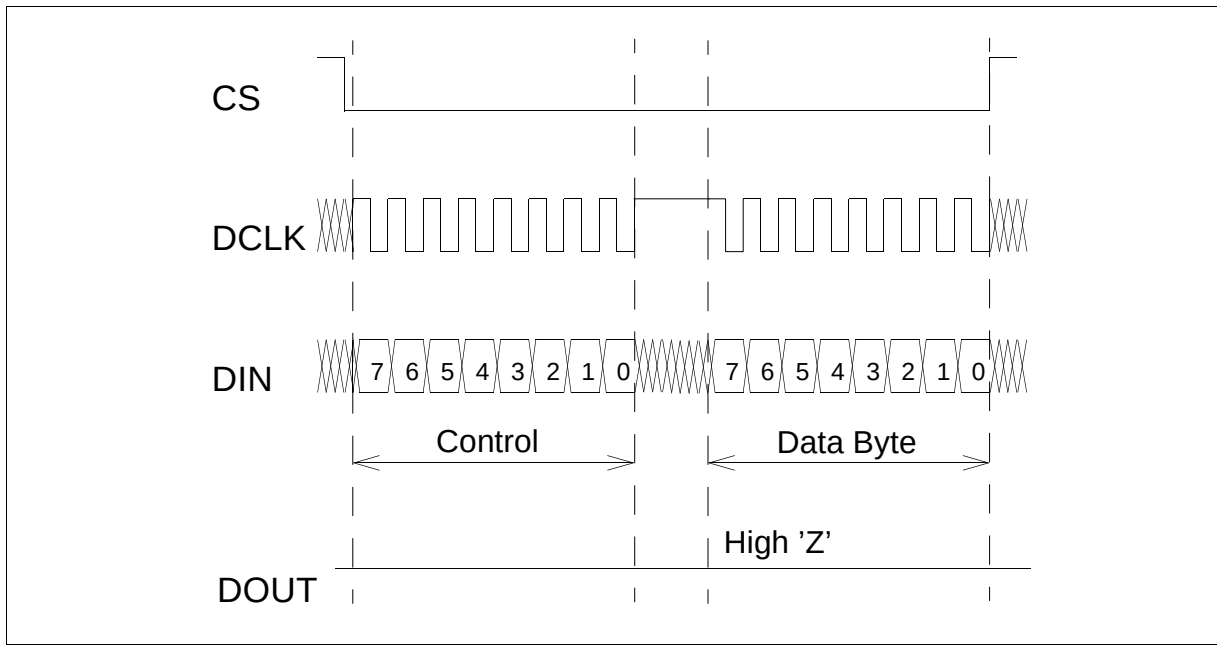


Figure 26 Example for a Write Access

If the first eight bits received via DIN specify a read-command, the ANIC will start to response via DOUT with its specific register byte

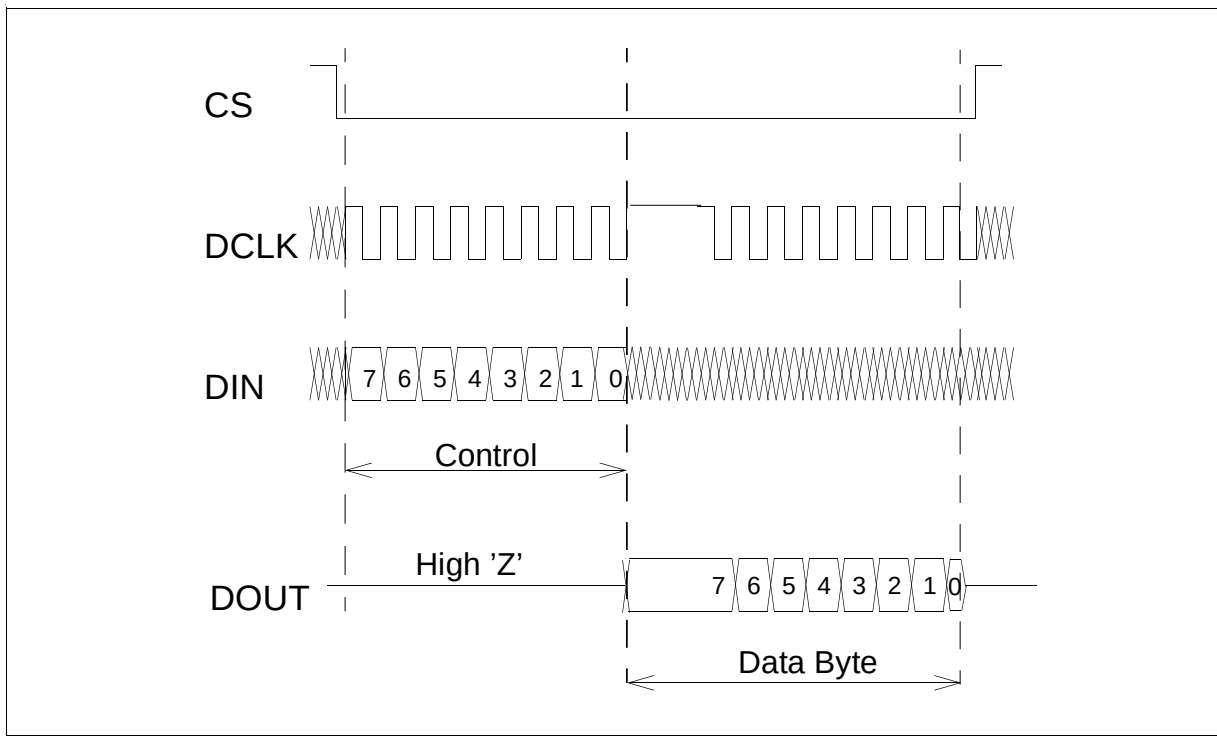


Figure 27 Example for a Read Access

Note: In order to avoid bus contention, bit 0 (LSB) at DOUT is only asserted during the positive half-cycle of DCLK, and is high-impedance during the negative half-cycle of DCLK.

The data transfer is synchronized by DCLK. DIN is latched at the falling edge of DCLK, while DOUT changes with the rising edge of DCLK. During execution of a command which is followed by output data (read command), the device will not accept any new command via DIN. The data transfer sequence can be interrupted by setting CS to high.

To reduce the number of connections to the µ Controller DIN and DOUT may be strapped together to a bidirectional datapin.

5.3.1 Programming of ANIC via the Serial Control Interface

			CMD command word		

Bit	7	6	5	4	3	2	1	0
	R/nW[1)]	**I**	**A3**	**A2**	**A1**	**A0**	**1**	**x**

1) R/nW is the MSB and will be transferred first.

x		Don´t care
A[3:0]		Offset address for basic and indexed addressing mode.
	A[3:0] = 0000	Offset 0
	....	
	A[3:0] = 1111	Offset 15
I		Use of index register
	I = 0	Use offset address A[3:0] (Basic addressing mode)
	I = 1	Use Index register + offset address A[3:0] (Indexed addressing mode)
R/nW		Read or write data
	R/nW = 0	Write Data to ANIC
	R/nW = 1	Read data from ANIC

- RAM address of Indexregister: 0

256 Byte RAM: 0h to FFh

128 Byte CRAM: 100h to 17Fh

- Calculating the Index (I) and Offset (O) out of the C/RAM-address (Adr):

I = INT (Adr / 16) * 8 (I must be a multiple of 8)

O = Adr – 2 * I (O must be between 0 and 15)

5.3.1.1 Example for Write Operation

Write data value FBh to RAM-address AFh = 10101111

First Step:

Write Indexregister.

- Write Command on DIN:

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**0**	**0**	**1**	**X**

- Index on DIN:
  I = INT (Adr / 16) * 8 = INT (AFh / 16) * 8 = 01010000 = 50h.

Bit	7	6	5	4	3	2	1	0
	0	**1**	**0**	**1**	**0**	**0**	**0**	**0**

Second Step:

Write data value FBh = 11111011 in indexed addressing mode.

- Write Command on DIN:
  Offset A[3:0] = Adr – 2*I = AFh – 2 * 50h = 1111

Bit	7	6	5	4	3	2	1	0
	0	**1**	**1**	**1**	**1**	**1**	**1**	**X**

- Data on DIN:

Bit	7	6	5	4	3	2	1	0
	1	**1**	**1**	**1**	**1**	**0**	**1**	**1**

5.3.1.2 Example for Read Operation

Read data from CRAM-address 17Dh = 101111101

First Step:

Write Indexregister:

- Write Command on DIN:

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**0**	**0**	**1**	**X**

- Index on DIN:
  I = INT (Adr / 16) * 8 = INT (17Dh / 16) * 8 = 10111000 = B8h.

Bit	7	6	5	4	3	2	1	0
	1	**0**	**1**	**1**	**1**	**0**	**0**	**0**

Second Step:

Read data in indexed addressing mode.

- Read Command on DIN:
  Offset A[3:0] = Adr – 2*I = 17Dh – 2 * B8h = 1101

Bit	7	6	5	4	3	2	1	0
	1	**1**	**1**	**1**	**0**	**1**	**1**	**X**

- Data following Read Command on DOUT:

Bit	7	6	5	4	3	2	1	0
	d7	**d6**	**d5**	**d4**	**d3**	**d2**	**d1**	**d0**

5.4 Digital Isolation Interface

The isolation between ANIC-A and ANIC-D and therefore from the TIP/RING side to the host/datapump side can be realized in two ways:

Capacitive Interface

Isolation is realized by six capacitances. The two “A”, “B” and “C” capacitors must match to within 5 % of the selected value between 5 to 30 pF.

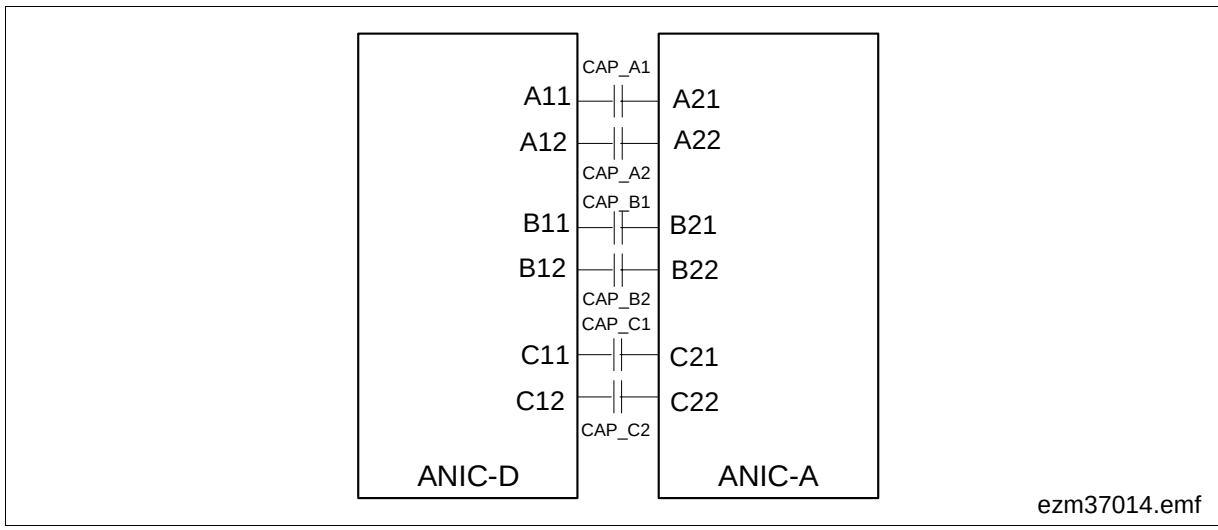


Figure 28 Isolation by Capacitive Interface

Inductive Interface

Isolation is realized by extra small transformers provided by third party.

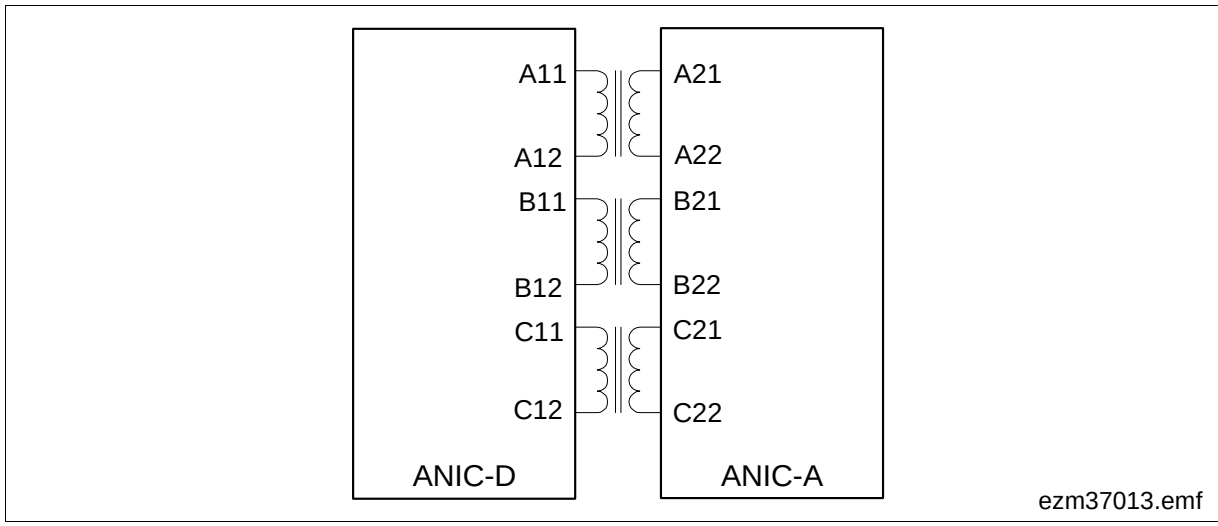


Figure 29 Isolation by Inductive Interface

6 Programming

ANIC uses a simple type of 8 bit command structure. To access the configuration registers or configuration RAM index addressing (paging) is used. The index register is located in the 0 page. This page can be programmed directly by setting the bit INDEX to ’0’. Register located in other pages can be addressed using the index register and setting the bit INDEX to ’1’.

6.1 Register Map

6.1.1 Overview

All dark grey area is reserved for internal use and must not be addressed by commands. The contents of the light grey area is supplied by Infineon Technologies as coefficients for country specific adaptations.

I: Index, O: Offset, T: Type, D: Default

Table 8 Register Overview

I	O	T	D	MSB Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB Bit0
0	0	RW	00h	Index(7)	Index(6)	Index(5)	Index(4)	Index(3)	Index(2)	Index(1)	Index(0)
0	1	R	00h	MET	RING	THR	TONE	SIA1	SIA0	SIOD1	SIOD0
0	2	RW	00h	E_MET	E_RING	E_THR	E_TONE	E_SIA1	E_SIA0	E_SIOD1	E_SIOD0
0	3	RW	00h	0	0	0	0	State(3)	State(2)	State(1)	State(0)
0	4	R	00h	RG(1)	RG(0)	TG(1)	TG(0)	TR(3)	TR(2)	TR(1)	TR(0)
0	5	R	00h	MET	RING	TONE(1)	TONE(0)	SIA1	SIA0	SIOD1_I	SIOD0_I
0	6	RW	00h	SOA3	SOA2	SOA1	SOA0	x	SOD0	SIOD1_O	SIOD0_O
0	7	R	00h	MTR7	MTR6	MTR5	MTR4	MTR3	MTR2	MTR1	MTR0
0	8	R	00h	MRG7	MRG6	MRG5	MRG4	MRG3	MRG2	MRG1	MRG0
0	9	R	00h	MTG7	MTG6	MTG5	MTG4	MTG3	MTG2	MTG1	MTG0
0	10	RW	00h	PULSE	CMD_ MODE	PCM_ LOOP	RING_ VAL	DCDC	ANIC-A_ LOOP	SIOD1_ C	SIOD0_ C
0	11	RW	00h	0	0	TS5	TS4	TS3	TS2	TS1	TS0
0	12	RW	00h	0	0	RS5	RS4	RS3	RS2	RS1	RS0
0	13	RW	00h	0	0	XS5	XS4	XS3	XS2	XS1	XS0
0	14	RW	00h	16K	OS2	OS1	OS0	COMP	A/MU	0	EDGE
0	15	RW	00h	TR0(7)	TR0(6)	TR0(5)	TR0(4)	TR0(3)	TR0(2)	TR0(1)	TR0(0)
8	0	RW	00h	TR1(7)	TR1(6)	TR1(5)	TR1(4)	TR1(3)	TR1(2)	TR1(1)	TR1(0)
8	1	RW	00h	TR2(7)	TR2(6)	TR2(5)	TR2(4)	TR2(3)	TR2(2)	TR2(1)	TR2(0)
8	2	RW	00h	TR3(7)	TR3(6)	TR3(5)	TR3(4)	TR3(3)	TR3(2)	TR3(1)	TR3(0)
8	3	RW	00h	TG0(7)	TG0(6)	TG0(5)	TG0(4)	TG0(3)	TG0(2)	TG0(1)	TG0(0)

Table 8 Register Overview (Continued)

I	O	T	D	MSB Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB Bit0
8	4	RW	00h	TG1(7)	TG1(6)	TG1(5)	TG1(4)	TG1(3)	TG1(2)	TG1(1)	TG1(0)
8	5	RW	00h	RG0(7)	RG0(6)	RG0(5)	RG0(4)	RG0(3)	RG0(2)	RG0(1)	RG0(0)
8	6	RW	00h	RG1(7)	RG1(6)	RG1(5)	RG1(4)	RG1(3)	RG1(2)	RG1(1)	RG1(0)
8	7	RW	00h	E_RG(1)	E_RG(0)	E_TG(1)	E_TG(0)	E_TR(3)	E_TR(2)	E_TR(1)	E_TR(0)
8	8	RW	00h	SHOW_ RING	SHOW_ MET	E_TONE (1)	E_TONE (0)	x	x	x	TEST_ TONE
8	9	RW	00h	0	0	RG1	RG0	TG1	TG0	TR1	TR0
8	10	RW	01h	RG_ PER(7)	RG_ PER(6)	RG_ PER(5)	RG_ PER(4)	RG_ PER(3)	RG_ PER(2)	RG_ PER(1)	RG_ PER(0)
8	11	RW	01h	RG_ DEG(7)	RG_ DEG(6)	RG_ DEG(5)	RG_ DEG(4)	RG_ DEG(3)	RG_ DEG(2)	RG_ DEG(1)	RG_ DEG(0)
8	12	RW	01h	MET_ PER(7)	MET_ PER(6)	MET_ PER(5)	MET_ PER(4)	MET_ PER(3)	MET_ PER(2)	MET_ PER(1)	MET_ PER(0)
8	13	RW	01h	MMPER (7)	MMPER (6)	MMPER (5)	MMPER (4)	MMPER (3)	MMPER (2)	MMPER (1)	MMPER (0)
8	14	R	12h	HW_ VER(3)	HW_ VER(2)	HW_ VER(1)	HW_ VER(0)	SW_ VER(3)	SW_ VER(2)	SW_ VER(1)	SW_ VER(0)
8	15		00h	x	x	x	x	x	RING_ EXT	HOOK_ CMD	PCM_ MM
16	0	RW	00h	x	0	DC_K3	DC_K2	DC_K1	DC_K0	DC_U1	DC_U0
16	1	RW	00h	x	0	0	0	XAGX_ K1	XAGX_ K0	RAGR_ K1	RAGR_ K0
16	2	RW									
16	3	RW									
16	4	RW									
16	5	RW									
16	6	RW									
16	7	RW									
16	8	RW									
16	9	RW									
16	10	RW									
16	11	RW									
48	7	RW	0Ah	RING_ TO(7)	RING_ TO(6)	RING_ TO(5	RING_ TO(4)	RING_ TO(3)	RING_ TO(2	RING_ TO(1)	RING_ TO(0)
48	8	RW	03h	TONE_ TO(7)	TONE_ TO(6)	TONE_ TO(5	TONE_ TO(4)	TONE_ TO(3)	TONE_ TO(2	TONE_ TO(1)	TONE_ TO(0)
96	12	RW	50h	0	COT2	DHPR2	MM	FSC16	COT1	COR2	COR1
96	13	RW	3Ch	ALF	IM	FRR	FRX	AR	AX	RIP	0

Table 8 Register Overview (Continued)

I	O	T	D	MSB Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	LSB Bit0
96	14	RW	D8h	LPX	LPR	TG	LM2	LM1	LB64	LBZ	TH
96	15	RW	10h	EN_TB	0	RGS	MET_ MMG	DHPTH	0	DHPR1	DHPX
128	0	RW	00h	CRAM	CRAM	CRAM	CRAM	CRAM	CRAM	CRAM	CRAM
	....	RW	00h	CRAM	CRAM	CRAM	CRAM	CRAM	CRAM	CRAM	CRAM
	....	RW	00h	CRAM	CRAM	CRAM	CRAM	CRAM	CRAM	CRAM	CRAM
184	0	RW	00h	CRAM	CRAM	CRAM	CRAM	CRAM	CRAM	CRAM	CRAM
	....	RW	00h	CRAM	CRAM	CRAM	CRAM	CRAM	CRAM	CRAM	CRAM
	....	RW	00h	CRAM	CRAM	CRAM	CRAM	CRAM	CRAM	CRAM	CRAM

Note: Registers 16/2 to 16/11 are for internal use only.
Registers 128/0 to 184/15 represent the coefficient RAM address area.

CRAM and on-hook CRAM coefficients are shown in **Table 9** and **Table 12**. Coefficients of the same colour can be modified independendly of other coefficients.

Table 9 CRAM Definitions for Coefficients

	Byte 7/15		Byte 6/14		Byte 5/13		Byte 4/12		Byte 3/11		Byte 2/10		Byte 1/9		Byte 0/8[1)]		Index	Index hex.
TH1	BA25	BA24	BA23	BA22	BA21	BA20	BA19	BA18	BA17	BA16	BA15	BA14	BA13	BA12	BA11 1)	BA10 1)	128	80h
TH2	HT	B23	B22	B21	B13	B12	B11	FB4	FB3	FB2	FB1	FB0	BA29	BA28	BA27 1)	BA26 1)		
TH3	HP2	HP1	B72	B71	B63	B62	B61	B53	B52	B51	B43	B42	B41	B33	B32	B31	136	88h
RIP1	--	R43	R42	R41	R33	R32	R31	R23	R22	R21	R13	R12	R11	RM3	RM2	RM1		
IM1	--	Z53	Z52	Z51	Z43	Z42	Z41	Z33	Z32	Z31	Z23	Z22	Z21	Z13	Z12	Z11	144	90h
IM2	ZH1	ZH2	ZH3	ZH4	Z63	Z62	Z61	ZB9	ZB8	ZB7	ZB6	ZB5	ZB4	ZB3	ZB2	ZB1		
RIP2	RH3	RH2	RH1	C_TR 3	C_TR 2	C_TR 1	--	RB9	RB8	RB7	RB6	RB5	RB4	RC3	RC2	RC1	152	98h
FRR	--	FR43	FR42	FR41	FR33	FR32	FR31	FR23	FR22	FR21	FR13	FR12	FR11	FR03	FR02	FR01		
FRX	--	X43	X42	X41	X33	X32	X31	X23	X22	X21	X13	X12	X11	X03	X02	X01	160	A0h
AR	AR22	AR21	AR20	AR14	AR13	AR12	AR11	AR10										
AX									AX22	AX21	AX20	AX14	AX13	AX12	AX11	AX10		
LM1	LT4	LT3	LT2	LT1	QT	TN3	TN2	TN1									168	A8h
LM2									LA4	LA3	LA2	LA1	QA	AC3	AC2	AC1		
TG	T18	T17	T16	T15	T14	T13	T12	T11										
RGS									X63	X62	X61	CM5	CM4	CM3	CM2	CM1		
METD	G4	G3	G2	G1	MET D4	MET D3	MET D2	MET D1	Q	SF	BT4	BT3	BT2	BT1	MU2	MU1	176	B0h
MMG	MM2	MM1	MM0	K	Z83	Z82	Z81	Z73	Z72	Z71	FR53	FR52	FR51	X53	X52	X51		
LPR	LR53	LR52	LR51	LR43	LR42	LR41	LR33	LR32	LR31	LR23	LR22	LR21	LR13	LR12	LR11	--	184	B8h
LPX	LX53	LX52	LX51	LX43	LX42	LX41	LX33	LX32	LX31	LX23	LX22	LX21	LX13	LX12	LX11	--		

1) For example "Byte 0/8" means: 0 = Offset for byte BA10/BA11 , 8 = Offset for byte BA26/BA27

Table 10 CRAM Definitions for Coefficients (see Table 9)

Flagname	Coefficient Group	Definition
TH	TH1, TH2, TH3	Transhybrid optimization
RIP	RIP1, RIP2	Ring impedance, level metering
IM	IM1, IM2	Line impedance matching
FRR	FRR	Frequency response receive
FRX	FRX	Frequency response transmit
AR	AR	Gain in receive direction
AX	AX	Gain in transmit direction
LM	LM1, LM2	Level metering
TG	TG	Tone generator
RGS	RGS	Level metering frequency response transmit
MET_MMG	METD	Metering signal detection
	MMG	Multi purpose measurement gain
LPR	LPR	Low pass filter receive
LPX	LPX	Low pass filter transmit

The coefficients for transhybrid optimization TH1, TH2 and TH3 (see **Table 10**) are different in ON-HOOK CONVERSATION and CONVERSATION state. When switching to these states, the host must also download the corresponding coefficients TH1, TH2 and TH3 to the ANIC-D. This has to be done as there is no automatic swapping implemented for this coefficients in the ANIC-D firmware.

Table 11 RAM Definitions for Coefficients (see Table 12)

Coefficients Group	Usage of Coefficients
FRR	Frequency response in ON-HOOK RECEIVE state.
AR	Gain in ON-HOOK RECEIVE state

Table 12 RAM Definitions for Coefficients

	Byte 7 / 15		Byte 6 / 14		Byte 5 / 13		Byte 4 / 12		Byte 3 / 11		Byte 2 / 10		Byte 1 / 9		Byte 0 / 8[1)]		Index/Offset	
																	dec.	hex.
FRR													FR53	FR52	FR51	X53	80/12	50/C
FRR	--	FR43	FR42	FR41	FR33	FR32	FR31	FR23	FR22	FR21	FR13	FR12	FR11	FR03	FR02	FR01	80/14	50/E
AR									AR22	AR21	AR20	AR14	AR13	AR12	AR11	AR10	88/06	58/6

1) For example "Byte 0 / 8" means: 0 = Offset for byte BA10 / BA11 , 8 = Offset for byte BA26 / BA27

6.1.2 Detailed Register Descriptions

Register Description Example:

Index	Offset	Short Name	Long Name	Type	Default Value

7	6	5	4	3	2	1	0

If the Type-box shows "rw", unused bits ("x") are not allowed to be changed: Read-Modify-Write commands are necessary.

0	0		Register 0	rw	00_H

Bit	7	6	5	4	3	2	1	0
	Index (7)	**Index (6)**	**Index (5)**	**Index (4)**	**Index (3)**	**Index (2)**	**Index (1)**	**Index (0)**

Index [7:0] Used to set the index of the page to which should be read/written. The formula to get the index value is:

Index = Integer(Address/16)*8
Offset = Address – (2*index)

Example: Writing to address 130.
Index = INT(130/16)*8 = 64
Offset = 130 – (2*64) = 2

0	1		Register 1	r	00_H

Bit	7	6	5	4	3	2	1	0
	MET	**RING**	**THR**	**TONE**	**SIA1**	**SIA0**	**SIOD1**	**SIOD0**

This register is used for signalling which interrupt has caused a HI -> LOW transition on the $\overline{\text{INT}}$ line. All interrupts will have the granularity of 125 µs. Faster events can not be detected safely. A read operation will clear this register and sets the $\overline{\text{INT}}$ pin back to inactive (high)

SIOD0		Signals interrupt on change of pin RINGIND/SIOD0 (ANIC-D) when configured as input.
	SIOD0 = 0	No interrupt detected.
	SIOD0 = 1	Interrupt detected.
SIOD1		Signals interrupt on change of pin SIOD1 (ANIC-D) when configured as input.
	SIOD1 = 0	No interrupt detected.
	SIOD1 = 1	Interrupt detected.
SIA0		Signals interrupt on change of pin SI0 (ANIC-A).
	SIA0 = 0	No interrupt detected.
	SIA0 = 1	Interrupt detected.
SIA1		Signals interrupt on change of pin SI1 (ANIC-A).
	SIA1 = 0	No interrupt detected.
	SIA1 = 1	Interrupt detected.
TONE		Signals interrupt on tone detection (see register 5 for indication which tone was detected).
	Tone = 0	No interrupt detected.
	Tone = 1	Interrupt detected.
THR		Signals interrupt on line reversal, disconnect or 50 Hz metering signals (see register 4 for indication which line voltage passed threshold)
	THR = 0	No interrupt detected.
	THR = 1	Interrupt detected.

RING Signals interrupt on valid ring or ring threshold depending on bit RING_VAL in register 10.

Ring = 0	No interrupt detected.
Ring = 1	Interrupt detected.

MET Signals interrupt on the rising edge of the metering event.

MET = 0	No interrupt detected.
MET = 1	Interrupt detected.

0	2		Register 2	rw	00_H

Bit	7	6	5	4	3	2	1	0
	E_MET	**E_RING**	**E_THR**	**E_ TONE**	**E_SIA1**	**E_SIA0**	**E_ SIOD1**	**E_ SIOD0**

Maskregister for interrupts

E_x

E_x = 0	Ignore (mask) according interrupt
E_x = 1	Enable according interrupt

Note: For SIA0, SIA1, RINGIND/SIOD0 and SIOD1 the correct pin values will be shown in register 5 even if the interrupt is disabled. This makes it possible to find out the level at the input pins by polling.

0	3		Register 3	rw	00_H

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**State(3)**	**State(2)**	**State(1)**	**State(0)**

This register is used to program ANIC operating states:
Please note that the external hook switch is handled automatically by default when changing between the operating states (bit HOOK_CMD register 31 = 0). For details on the external circuitry please refer to the Application Note "Understanding the External Components of the ANIC Chip Set".

State [3:0]

State [3:0] = 0000	IDLE
State [3:0] = 0001	PULSE COMMAND
State [3:0] = 0011	CONVERSATION
State [3:0] = 0100	ON-HOOK RECEIVE
State [3:0] = 0101	ON-HOOK CONVERSATION
State [3:0] = 0110	RING
all others	internal use only

0	4		Register 4	r	00_H

Bit	7	6	5	4	3	2	1	0
	RG(1)	**RG(0)**	**TG(1)**	**TG(0)**	**TR(3)**	**TR(2)**	**TR(1)**	**TR(0)**

This register is used for the indication of threshold values. The value is updated if a measured voltage passes the actual programmed threshold value. This threshold indication can be masked in register 23. Masked indications are held ’0’ all the time. Reading this register by the host clears the register to 0x00.
The voltage range is 0 to 5 V in 2´s complement.

TR(x)

TR(x) = 0 Programmed threshold value for TIP-RING voltage wasn´t passed.

TR(x) = 1 Programmed threshold value for TIP-RING voltage was passed.

TG(x)]

TG(x) = 0 Programmed threshold value for TIP-GROUND voltage wasn´t passed.

TG(x) = 1 Programmed threshold value for TIP-GROUND voltage was passed.

RG(x)

RG(x) = 0 Programmed threshold value for RING-GROUND voltage wasn´t passed.

RG(x) = 1 Programmed threshold value for RING-GROUND voltage was passed.

0	5		Register 5	r	00_H

Bit	7	6	5	4	3	2	1	0
	MET	**RING**	**TONE (1)**	**TONE (0)**	**SIA1**	**SIA0**	**SIOD1_I**	**SIOD0_I**

This register is used for indication of ring, tone and input values. The values are updated if the according event occurs.
For the tones this indication can be masked in register 24. Masked indications are held ’0’ all the time. Reading this register by the host clears the tone indication bits no.4 and no.5 to ’0’.

SIOD0_I Digital input value on general purpose input/output pin RINGIND/SIOD0 (ANIC-D)

SIOD0_I = 0 Input value at pin RINGIND/SIOD0 below TTL threshold.

SIOD0_I = 1 Input value at pin RINGIND/SIOD0 above TTL threshold.

SIOD1_I Digital input value on general purpose input/output pin SIOD1 (ANIC-D)

SIOD1_I = 0 Input value at pin SIOD1 below TTL threshold.

SIOD1_I = 1 Input value at pin SIOD1 above TTL threshold.

SIA0 Digital input value on pin SI0 (ANIC-A, galvanic isolated)

SIA0 = 0 Input value on pin SI0 below TTL.

SIA0 = 1 Input value on pin SI0 above TTL threshold.

SIA1 Digital input value on pin SI1 (ANIC-A, galvanic isolated)

SIA1 = 0 Input value on pin SI1 below TTL threshold.

SIA1 = 1 Input value on pin SI1 above TTL threshold.

TONE(x) Programmed tone (x) was detected.

TONE(x) = 0 No tone detected.

TONE(x) = 1 Tone was detected.

RING		Signals either ring threshold or valid ring, depending on RING_VAL in register 10.
	RING = 0	Ring off
	RING = 1	Ring on

MET		Signals if metering signal is present.
	MET = 0	Metering signal off
	MET = 1	Metering signal on

0	6		Register 6	r	00_H

Bit	7	6	5	4	3	2	1	0
	SOA3	**SOA2**	**SOA1**	**SOA0**	**x**	**SOD0**	**SIOD1_O**	**SIOD0_O**

Output values

SIOD0_O The value of this bit is put out on the general purpose input/ output pin RINGIND/SIOD0 (ANIC-D), if programmed as output.

SIOD0_O = 0 Voltage at pin RINGIND/SIOD0 greater than V_{DD} – 0.5 V

SIOD0_O = 1 Voltage at pin RINGIND/SIOD0 below 0.5 V

SIOD1_O The value of this bit is put out on the general purpose input/ output pin SIOD1 (ANIC-D), if programmed as output.

SIOD1_O = 0 Voltage at pin SIOD1greater than V_{DD} – 0.5 V

SIOD1_O = 1 Voltage at pin SIOD1below 0.5 V

SOD0 The value of this bit is put out on the general purpose output pin METIND/SOD0 (ANIC-D).

SOD0 = 0 Voltage at pin METIND/SOD0 greater than V_{DD} – 0.5 V

SOD0 = 1 Voltage at pin METIND/SOD0 below 0.5 V

SOA0 The value of this bit is put out on the general purpose output pin SO0 (ANIC-A, galvanic isolated output).

SOA0 = 0 Voltage at pin SO0 greater than V_{DD} – 0.5 V

SOA0 = 1 Voltage at pin SO0 below 0.5 V

SOA1 The value of this bit is put out on the general purpose output pin SO1Q on (ANIC-A, galvanic isolated output). Note that SO1Q is a inverted output which shows high if programmed to ’0’.

SOA1 = 0 Voltage at pin SO1Q below 0.5 V

SOA1 = 1 Voltage at pin SO1Q greater than V_{DD} – 0.5 V

SOA2 The value of this bit is put out on the general purpose output pin SO2 (ANIC-A, galvanic isolated output).

SOA2 = 0 Voltage at pin SO2 greater than V_{DD} – 0.5 V

SOA2 = 1 Voltage at pin SO2 below 0.5 V

SOA3 The value of this bit is put out on the general purpose output pin SO3Q on (ANIC-A, galvanic isolated output). Note that SO3Q is a inverted output which shows high if programmed to ’0’.

SOA3 = 0 Voltage at pin SO3Q below 0.5 V

SOA3 = 1 Voltage at pin SO3Q greater than V_{DD} – 0.5 V

0	**7**		Register 7	**r**	**00_H**

Bit	7	6	5	4	3	2	1	0
	MTR7	**MTR6**	**MTR5**	**MTR4**	**MTR3**	**MTR2**	**MTR1**	**MTR0**

Measurement result TIP-RING, can be polled all the time

0	8		Register 8	r	00_H

Bit	7	6	5	4	3	2	1	0
	MRG7	**MRG6**	**MRG5**	**MRG4**	**MRG3**	**MRG2**	**MRG1**	**MRG0**

Measurement result RING-GROUND, can be polled all the time

Example:

If

- CRAM coefficient B0h/0Fh = 52h and B0h/0Eh = 10h (see **Table 9**)
- default measurement resolution = 5 V (see register 25)

then

- at + 5 V M2-M3 voltage the measurement result is 0111 1111
- at – 5 V M2-M3 voltage the measurement result is 1000 0000

Table 13 shows 8 bit measurement results obtained at different resolutions set in register 25 for exemplary M2-M3 voltages of + 0.5 V, 0 V and – 0.5 V.

Table 13 Measurement Result Examples

Resolution [1]	**M2-M3 Voltage** [2]	**Result**	**Resolution**	**M2-M3 Voltage**	**Result**
5 V	+ 0.5 V	0000 1101	2.5 V	+ 0.5 V	0001 1010
	0 V	0000 0000		0 V	0000 0000
	– 0.5 V[3]	1111 0011		– 0.5 V	1110 0100
1.25 V	+ 0.5 V	0011 0100	0.625 V	+ 0.5 V	0110 1000
	0 V	0000 0000		0 V	0000 0000
	– 0.5 V	1100 1010		– 0.5 V	1001 0110

1) see register 25

2) Voltage between pins M2 and M3 of PSB 4450 (peak value).

3) Voltage at – 0.5 V is 2´s complement of voltage on + 0.5 V

0	9		Register 9	r	00_H

Bit	7	6	5	4	3	2	1	0
	MTG7	**MTG6**	**MTG5**	**MTG4**	**MTG3**	**MTG2**	**MTG1**	**MTG0**

Measurement result TIP-GROUND, can be polled all the time

0	10		Register 10	rw	00_H

Bit	7	6	5	4	3	2	1	0
	PULSE	**CMD_ MODE**	**PCM_ LOOP**	**RING_ VAL**	**DCDC**	**ANIC-A_ LOOP**	**SIOD1_ C**	**SIOD0_ C**

Configuration of GPIO, sampling rate and testloops.

SIODx_C Configuration of pin SIODx as input or output.

SIODx_C = 0 Pin SIODx works as input

SIODx_C = 1 Pin SIODx works as output

ANIC-A_LOOP Loop back PCM data via ANIC-A.

ANIC-A_LOOP = 0 Loop back disabled

ANIC-A_LOOP = 1 Loop back enabled

DCDC Switch DCDC clock (2 MHz) to DCDC_CLK pin

DCDC = 0 Logic 0 on DCDC_CLK pin

DCDC = 1 DCDC clock is switched to DCDC_CLK pin

RING_VAL Enables software check if signal is a valid ring

RING_VAL = 0 Ring signal detection in ANIC-A only, a signal above the threshold of 7 V will cause a RING interrupt.

RING_VAL = 1 Checking in ANIC-D if signal is a valid ring according to amplitude and frequency defined by CRAM coefficients.

PCM_LOOP Loop back PCM data via PCM Interface

PCM_LOOP = 0 Loop back disabled

PCM_LOOP = 1 Loop back enabled

CMD_MODE Stay in current power mode

CMD_MODE = 0 Automatic change between power modes enabled.

CMD_MODE = 1 Mode change only by command.

PULSE Low impedance dialing pulse: operational only in pulse command mode (PULSE_CMD, register 5).

PULSE = 0 No pulse (“Break”)

PULSE = 1 Pulse (“Make”)

0	**11**		Register 11	**rw**	**00_H**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**TS5**	**TS4**	**TS3**	**TS2**	**TS1**	**TS0**

Number of timeslots per PCM frame, value 0x00 disables PCM Interface

0	**12**		Register 12	**rw**	**00_H**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**RS5**	**RS4**	**RS3**	**RS2**	**RS1**	**RS0**

Receive timeslot in PCM frame, value 0x00 disables PCM Interface

0	**13**		Register 13	**rw**	**00_H**

Bit	7	6	5	4	3	2	1	0
	0	**0**	**XS5**	**XS4**	**XS3**	**XS2**	**XS1**	**XS0**

Transmit timeslot in PCM frame, value 0x00 disables PCM Interface

0	14		Register 14	rw	00_H

Bit	7	6	5	4	3	2	1	0
	16K	**OS2**	**OS1**	**OS0**	**COMP**	**A/MU**	**x**	**EDGE**

PCM configuration register

EDGE Selects falling or rising edge for data transmit or receive.

EDGE = 0 Receive slope with falling edge, transmit slope with rising edge.

EDGE = 1 Receive slope with rising edge, transmit slope with falling edge.

A/MU Selects compression law

A/MU = 0 µ-Law selected

A/MU = 1 A-Law selected

COMP Enables compander

0 16-Bit PCM, no Compander used

1 8-Bit PCM, Compander used

OS2, OS1, OS0 PCM-Offset in number of data-clock periods

000 one data clock period added

...

111 eight data clock periods added

16k Selects the sampling mode

0 8 k sampling mode selected (sampling rate = 6 to 12 kHz)

1 16 k sampling mode selected (sampling rate = 12 to 24 kHz)

0	15		Register 15	rw	00_H

Bit	7	6	5	4	3	2	1	0
	TR0(7)	**TR0(6)**	**TR0(5)**	**TR0(4)**	**TR0(3)**	**TR0(2)**	**TR0(1)**	**TR0(0)**

Threshold value for THR interrupt for TIP-RING voltage Nr. 0

Note: For all threshold values the same range as for the measurement results defined in register 25 is considered. To give an interrupt for the according threshold, the bits in register 23 serve as enable bits besides the general enable bit in register 4.

8	0		Register 16	rw	00_H

Bit	7	6	5	4	3	2	1	0
	TR1(7)	**TR1(6)**	**TR1(5)**	**TR1(4)**	**TR1(3)**	**TR1(2)**	**TR1(1)**	**TR1(0)**

Threshold value for THR interrupt for TIP-RING voltage Nr. 1

8	1		Register 17	rw	00_H

Bit	7	6	5	4	3	2	1	0
	TR2(7)	**TR2(6)**	**TR2(5)**	**TR2(4)**	**TR2(3)**	**TR2(2)**	**TR2(1)**	**TR2(0)**

Threshold value for THR interrupt for TIP-RING voltage Nr. 2

8	2		Register 18	rw	00_H

Bit	7	6	5	4	3	2	1	0
	TR3(7)	**TR3(6)**	**TR3(5)**	**TR3(4)**	**TR3(3)**	**TR3(2)**	**TR3(1)**	**TR3(0)**

Threshold value for THR interrupt for TIP-RING voltage Nr. 3

8	3		Register 19	rw	00_H

Bit	7	6	5	4	3	2	1	0
	TG0(7)	**TG0(6)**	**TG0(5)**	**TG0(4)**	**TG0(0)**	**TG0(0)**	**TG0(0)**	**TG0(0)**

Threshold value for THR interrupt for TIP-GROUND voltage Nr. 0

8	4		Register 20	rw	00_H

Bit	7	6	5	4	3	2	1	0
	TG1(7)	**TG1(6)**	**TG1(5)**	**TG1(4)**	**TG1(3)**	**TG1(2)**	**TG1(1)**	**TG1(0)**

Threshold value for THR interrupt for TIP-GROUND voltage Nr. 1

8	5		Register 21	rw	00_H

Bit	7	6	5	4	3	2	1	0
	RG0(7)	**RG0(6)**	**RG0(5)**	**RG0(4)**	**RG0(3)**	**RG0(2)**	**RG0(1)**	**RG0(0)**

Threshold value for THR interrupt for RING-GROUND voltage Nr. 0

8	6		Register 22	rw	00_H

Bit	7	6	5	4	3	2	1	0
	RG1(7)	**RG1(6)**	**RG1(5)**	**RG1(4)**	**RG1(3)**	**RG1(2)**	**RG1(1)**	**RG1(0)**

Threshold value for THR interrupt for RING-GROUND voltage Nr. 1

8	7		Register 23	rw	00_H

Bit	7	6	5	4	3	2	1	0
	E_RG(1)	**E_RG(0)**	**E_TG(1)**	**E_TG(0)**	**E_TR(3)**	**E_TR(2)**	**E_TR(1)**	**E_TR(0)**

Configuration of threshold interrupts

E_TR(x) Enable the according threshold indication in register 4 (TIP-RING voltage threshold)

E_TR(x) = 0 Threshold indication disabled

E_TR(x) = 1 Threshold indication enabled

E_TG(x) Enable the according threshold indication in register 4 (TIP-GROUND voltage threshold)

E_TG(x) = 0 Threshold indication disabled

E_TG(x) = 1 Threshold indication enabled

E_RG(x) Enable the according threshold indication in register 4 (RING-GROUND voltage threshold)

E_RG(x) = 0 Threshold indication disabled

E_RG(x) = 1 Threshold indication enabled

8	8		Register 24	rw	00_H

Bit	7	6	5	4	3	2	1	0
	SHOW_ RING	**SHOW_ MET**	**E_ TONE(1)**	**E_ TONE(0)**	**x**	**x**	**x**	**TEST_ TONE**

General Configurations

TEST_TONE Enables the test tone generation. Level and frequency are determined by coefficients.

TEST_TONE = 0 Test tone generation off

TEST_TONE = 1 Test tone generation on

E_TONE(0) Enables the tone detection of tone 0

E_TONE(0) = 0 Disable the tone detection. The according indication in register 5 will remain ’0’.

E_TONE(0) = 1 Enable the tone detection. Detected tones are indicated in register 5.

E_TONE(1) Enables the tone detection of tone 1

E_TONE(1) = 0 Disable the tone detection. The according indication in register 5 will remain ’0’.

E_TONE(1) = 1 Enable the tone detection. Detected tones are indicated in register 5.

SHOW_MET Enables metering indication

SHOW_MET = 0 No metering indication

SHOW_MET = 1 The metering signals are signalled via indication on pin METIND/SOD0.

SHOW_RING	Enables ring indication
SHOW_RING = 0	No ring indication
SHOW_RING = 1	The ring is signalled via indication on pin RINGIND/ SIOD0, if configured as output (SIOD0_C = 1 in register 10). Signals either ring threshold or valid ring, depending on RING_VAL in register 10.

8	9		Register 25	rw	00_H

Bit	7	6	5	4	3	2	1	0
	0	**0**	**RG1**	**RG0**	**TG1**	**TG0**	**TR1**	**TR0**

Configuration for measurement resolution at TIP-RING, RING-GROUND and TIP-GROUND. Since the measurement results stored in register 7 to register 9 are only 8 bit values the actually measured internal result of 16 bit is shifted according this bits. This configuration affects the values in register 7 to register 9 and register 15 to register 22.

TR[1:0] Measurement resolution at TIP-RING

- TR[1:0] = 00 5 V (bit 15 to 8 of the 16 bit measurement value)
- TR[1:0] = 01 2.5 V (bit 14 to 7 of the 16 bit measurement value)
- TR[1:0] = 10 1.25 V (bit 13 to 6 of the 16 bit measurement value)
- TR[1:0] = 11 0.625 V (bit 12 to 5 of the 16 bit measurement value)

TG[1:0] Measurement resolution at TIP-GROUND

- TG[1:0] = 00 5 V (bit 15 to 8 of the 16 bit measurement value)
- TG[1:0] = 01 2.5 V (bit 14 to 7 of the 16 bit measurement value)
- TG[1:0] = 10 1.25 V (bit 13 to 6 of the 16 bit measurement value)
- TG[1:0] = 11 0.625 V (bit 12 to 5 of the 16 bit measurement value)

RG[1:0] Measurement resolution at RING-GROUND

- RG[1:0] = 00 5 V (bit 15 to 8 of the 16 bit measurement value)
- RG[1:0] = 01 2.5 V (bit 14 to 7 of the 16 bit measurement value)
- RG[1:0] = 10 1.25 V (bit 13 to 6 of the 16 bit measurement value)
- RG[1:0] = 11 0.625 V (bit 12 to 5 of the 16 bit measurement value)

8	10		Register 26	rw	01_H

Bit	7	6	5	4	3	2	1	0
	RG_ PER(7)	**RG_ PER(6)**	**RG_ PER(5)**	**RG_ PER(4)**	**RG_ PER(3)**	**RG_ PER(2)**	**RG_ PER(1)**	**RG_ PER(0)**

Ring persistance time in steps of 1 ms: Time from detecting a ring depending on register 10 to the signalling of a ring interrupt. If the ring disappears during this time, no interrupt is signalled. This functionality helps to suppress short rings.

Note: Minimum ring persistance time is 1 ms.

8	11		Register 27	rw	01_H

Bit	7	6	5	4	3	2	1	0
	RG_ DEG(7)	**RG_ DEG(6)**	**RG_ DEG(5)**	**RG_ DEG(4)**	**RG_ DEG(3)**	**RG_ DEG(2)**	**RG_ DEG(1)**	**RG_ DEG(0)**

Ring deglitch time in step of 1 ms to prevent detecting noise on line as ring.

Note: Minimum ring deglitch time is 1 ms.

8	12		Register 28	rw	01_H

Bit	7	6	5	4	3	2	1	0
	MET_ PER(7)	**MET_ PER(6)**	**MET_ PER(5)**	**MET_ PER(4)**	**MET_ PER(3)**	**MET_ PER(2)**	**MET_ PER(1)**	**MET_ PER(0)**

Metering signal and tone persistance in steps of 1 ms. If a detected tone or metering signal disappears during this time, no interrupt is signalled. This functionality helps to supress tone or metering signal interrupts during transients of the system.

8	13		Register 29	r	01_H

Bit	7	6	5	4	3	2	1	0
	MMPER (7)	**MMPER (6)**	**MMPER (5)**	**MMPER (4)**	**MMPER (3)**	**MMPER (2)**	**MMPER (1)**	**MMPER (0)**

Measurement persistance time for indication of threshold passing in steps of 1 ms. If a voltage on the line passes a threshold level then this time is waited before an interrupt is signalled to avoid spike indications.

8	14		Register 30	r	12_H

Bit	7	6	5	4	3	2	1	0
	Hw_ver (3)	**Hw_ver (2)**	**Hw_ver (1)**	**Hw_ver (0)**	**Sw_ver (3)**	**Sw_ver (2)**	**Sw_ver (1)**	**Sw_ver (0)**

Software and hardware version of ANIC-D.

Sw_ver[0:3] Output of ANIC-D software version

Hw_ver[0:3] Output of ANIC-D hardware version

8	15		Register 31	r	00_H

Bit	7	6	5	4	3	2	1	0
	x	**x**	**x**	**x**	**x**	**RING_ EXT**	**HOOK_ CMD**	**PCM_MM**

PCM_MM Allows voice or measurement data to be switched to the PCM Interface.

PCM_MM = 0 Voice-data are switched to PCM Interface (default).

PCM_MM = 1 Measurement-data are switched to PCM-Interface.

HOOK_CMD Enables automatic or host controlled handling of the hook switch.

HOOK_CMD = 0 Automatic handling of hook switch during state-switch (default).

HOOK_CMD = 1 Host must handle the hook switch.

RING_EXT Enables internal or external ring impedance.

RING_EXT = 0 Ring impedance is synthezied by ANIC in RING state (default).

RING_EXT = 1 Exernal ring impedance must be used in RING state.

16	0		Register 32	rw	00_H

Bit	7	6	5	4	3	2	1	0
	x	**0**	**DC_K3**	**DC_K2**	**DC_K1**	**DC_K0**	**DC_U1**	**DC_U0**

DC-characteristic, provided with CRAM Coefficients.

DC_U[1:0] U_0 (DCU) value, see also **Table 16**.

DC_U[1:0] = 00	0 V
DC_U[1:0] = 01	2.5 V
DC_U[1:0] = 10	1 V
DC_U[1:0] = 11	3.1 V

DC_K[2:0] R value, see also **Table 17**.

DC_K[2:0] = 000	100 Ω
DC_K[2:0] = 001	200 Ω
DC_K[2:0] = 010	280 Ω
DC_K[2:0] = 011	560 Ω
DC_K[2:0] = 100	1000 Ω

DC_K3 I_{LIM} value, see also **Table 15**.

	min	typ	max	condition
DC_K3 = 0	100 mA	110 mA	120 mA	T_A = 0 °C to 70 °C
DC_K3 = 1	50 mA	55 mA	60 mA	T_A = 0 °C to 70 °C

16	1		Register 33	rw	00_H

Bit	7	6	5	4	3	2	1	0
	x	**0**	**0**	**0**	**XAGX_ K1**	**XAGX_ K0**	**RAGR_ K1**	**RAGR_ K0**

Transmit and receive gain, provided by CRAM Coefficients

RAGR_K0,1 Receive gain in PSB 4450 block

RAGR_K0,1 = 00 0 dB

RAGR_K0,1 = 01 – 3.5 dB

RAGR_K0,1 = 10 6 dB

RAGR_K0,1 = 11 2.5 dB

XAGX_K0,1 Transmit gain in PSB 4450 block

XAGX_K0,1 = 00 – 12 dB

XAGX_K0,1 = 01 – 18 dB

XAGX_K0,1 = 10 – 8.5 dB

XAGX_K0,1 = 11 – 14.5 dB

48	7		Register 103	rw	$0A_H$

Bit	7	6	5	4	3	2	1	0
	RING_ TO(7)	**RING_ TO(6)**	**RING_ TO(5**	**RING_ TO(4)**	**RING_ TO(3)**	**RING_ TO(2**	**RING_ TO(1)**	**RING_ TO(0)**

Ring timeout in steps of 10 ms to ensure constant detection of the ring signal in case of a short interruptions without generating a new interrupt. Default value is 100 ms.

48	8		Register 104	rw	03_H

Bit	7	6	5	4	3	2	1	0
	MET_ TO(7)	**MET_ TO(6)**	**MET_ TO(5**	**MET_ TO(4)**	**MET_ TO(3)**	**MET_ TO(2**	**MET_ TO(1)**	**MET_ TO(0)**

AC, metering and tone timeout in steps of 1 ms to ensure constant detection of the respective signal in case of a short interruptions without generating a new interrupt. Default value is 3 ms.

96	12		Register 204	rw	50_H

Bit	7	6	5	4	3	2	1	0
	0	**COT2**	**DHPR2**	**MM**	**FSC16**	**COT1**	**COR2**	**COR1**

DSP flags, provided by CRAM coefficients. This flags are modified automatically according to the power states.

COR1 Cut off receive path 1

COR1 = 0 Off

COR1 = 1 On

COR2 Cut off receive path 2

COR2 = 0 Off

COR2 = 1 On

COT1 Cut off transmit path 1

COT1 = 0 Off

COT1 = 1 On

FSC16 Enables 16 kHz decimation

FSC16 = 0 Off

FSC16 = 1 On

MM Enables measurement decimation

MM = 0 Off (transparent mode)

MM = 1 On

DHPR2 Disable high pass receive

DHPR2 = 0 Off

DHPR2 = 1 On

COT2 Cut off transmit path 2

COT2 = 0 Off

COT2 = 1 On

96	13		Register 205	rw	$3C_H$

Bit	7	6	5	4	3	2	1	0
	ALF	**IM**	**FRR**	**FRX**	**AR**	**AX**	**RIP**	**0**

DSP flags, provided by CRAM coefficients. This flags are modified automatically according to the power states.

RIP Enables level metering and ring impedance

RIP = 0 Off

RIP = 1 On

AX Gain transmit

AX = 0 Off

AX = 1 On

AR Gain receive

AR = 0 Off

AR = 1 On

FRX Frequency response transmit

FRX = 0 Off

FRX = 1 On

FRR Frequency response receive

FRR = 0 Off

FRR = 1 On

IM Impedance matching

IM = 0 Off

IM = 1 On

ALF Close 8 kHz analog loop

ALF = 0 Off

ALF = 1 On

96	14		Register 206	rw	$D8_H$

Bit	7	6	5	4	3	2	1	0
	LPX	**LPR**	**TG**	**LM2**	**LM1**	**LB64**	**LBZ**	**TH**

DSP flags, provided by CRAM coefficients. This flags are modified automatically according to the power states.

TH Trans hybrid filter

TH = 0 Off

TH = 1 On

LBZ Loop back via impedance path

LBZ = 0 Off

LBZ = 1 On

LB64 Loop back at 64 kHz sampling rate

LB64 = 0 Off

LB64 = 1 On

LM1 Level metering tone 1 (for modem tone detection and on-hook signalling from CO)

LM1 = 0 Off

LM1 = 1 On

LM2 Level metering tone 2 (for modem tone detection and on-hook signalling from CO)

LM2 = 0 Off

LM2 = 1 On

TG Tone generator

TG = 0 Off

TG = 1 On

LPR Enable programmable low pass receive characteristic

LPR = 0	Off
LPR = 1	On

LPX Enable programmable low pass transmit characteristic

LPX = 0	Off
LPX = 1	On

96	15		Register 207	rw	10_H

Bit	7	6	5	4	3	2	1	0
	EN_TB	**0**	**RGS**	**MET_ MMG**	**DHPTH**	**0**	**DHPR1**	**DHPX**

DSP flags, provided by CRAM coefficients. This flags are modified automatically according to the power states.

DHPX Disable high pass transmit

DHPX = 0 Off

DHPX = 1 On

DHPR1 Disable high pass receive 1

DHPR1 = 0 Off

DHPR1 = 1 On

DHPTH Disable high pass trans hybrid

DHPTH = 0 Off

DHPTH = 1 On

MET_MMG Enable metering signal detection and measurement gain

MET_MMG = 0 Off

MET_MMG = 1 On

EN_TB Enable low pass in ring path

EN_TB = 0 Off

EN_TB = 1 On

RGS Level metering frequency response transmit

RGS = 0 Off

RGS = 1 On

128-184	**0-15**		Register 256 - Register 383	**rw**	**00_H**

Bit	7	6	5	4	3	2	1	0
	CRAM	**CRAM**	**CRAM**	**CRAM**	**CRAM**	**CRAM**	**CRAM**	**CRAM**

CRAM Coefficients

7 Operating Modes

7.1 Operating Modes of ANIC System

Table 14 Operating Modes

Mode	Impedance to the Line	System
On-hook Modes		
IDLE	AC and DC high ohmic	Power safe, ready for setup (transition state, not a valid powermode)
RING	Ring impedance via AC loop	RING level metering
ON-HOOK CONVERSATION	AC impedance, high DC resistance	Receiving and transmitting of data without DC impedance. After ring detection, automatic switch to ring mode.
ON-HOOK RECEIVE	AC and DC high ohmic	Receiving of data without DC impedance. After ring detection, automatic switch to ring mode.
Off-hook Modes		
CONVERSATION	AC impedance & DC resistance	Receiving and transmitting of data with DC impedance.
PULSE COMMAND	“Make” or “Break” according to the PULSE bit (register10) without current limitation.	

In this chapter the basic operation modes will be explained. Each operating mode can be entered by a command.

7.2 On-hook

7.2.1 RESET (Basic Setting Mode)

Condition: $\overline{\text{RESET}}$ pin ='0', external master clock can be inactive.

The PSB 4451 has no internal power on reset. For valid operation the power must be asserted and after that an active low $\overline{\text{RESET}}$ (minimum length $t_{RESET,min}$ = 300 ns) must be given to the chip. Since all control is done via a controller in the chip a "boot" time of ~ 2000 cycles is necessary to get into an stable operation mode. The first mode after reset is IDLE. In this mode only the setup of the chip is possible (read and write registers). Registers will be reseted to the default values.

Note: As all information is stored within PSB 4451 and permanently transferred to PSB 4450, a power on reset of PSB 4450 will NOT force PSB 4450 into the basic setting mode, as it is reprogrammed immediately to its former power state by PSB 4451.

7.2.2 IDLE Mode

Condition: $\overline{\text{RESET}}$ pin = '1', external master clock active.

Will be entered after reset. The coefficients must be downloaded to ensure proper functionallity in all other modes. Only the digital interface of the ANIC is active in this mode. ANIC will send a maskable interrupt on any change of a GPI pin.

Note: IDLE is not a valid powermode for the PSB 4450 (entered only after reset).

7.2.3 RING Mode

Condition: $\overline{\text{RESET}}$ pin = '1', external master clock active

In this mode, a valid ring can be signalled by an interrupt depending on the RING_VAL bit.

The programmed Ring impedance will be synthesized. ANIC will also measure the voltage between TIP-RING, TIP-GND and RING-GND.

Tone detection, measurement-threshold interrupts and changes of the GPI pin will be indicated by maskable interrupts.

7.2.3.1 RING - Automatic State Transitions

Automatic Mode 1: Valid ring is signalled

Automatic Mode 2: Ring threshold is signalled

If the line voltage is higher than the ring threshold and ANIC is in on-hook mode, it is immediately switched to RING state and sets a deglitched ring signal bit. Depending on the programmed mode there are two possibilities:

a.) signal ring only if valid: the DSP checks the frequency and level of the believed ring signal and signals only valid rings to the host.

b.) signal any ring: any voltage higher than the threshold is immediately signalled as a ring indication to the host.

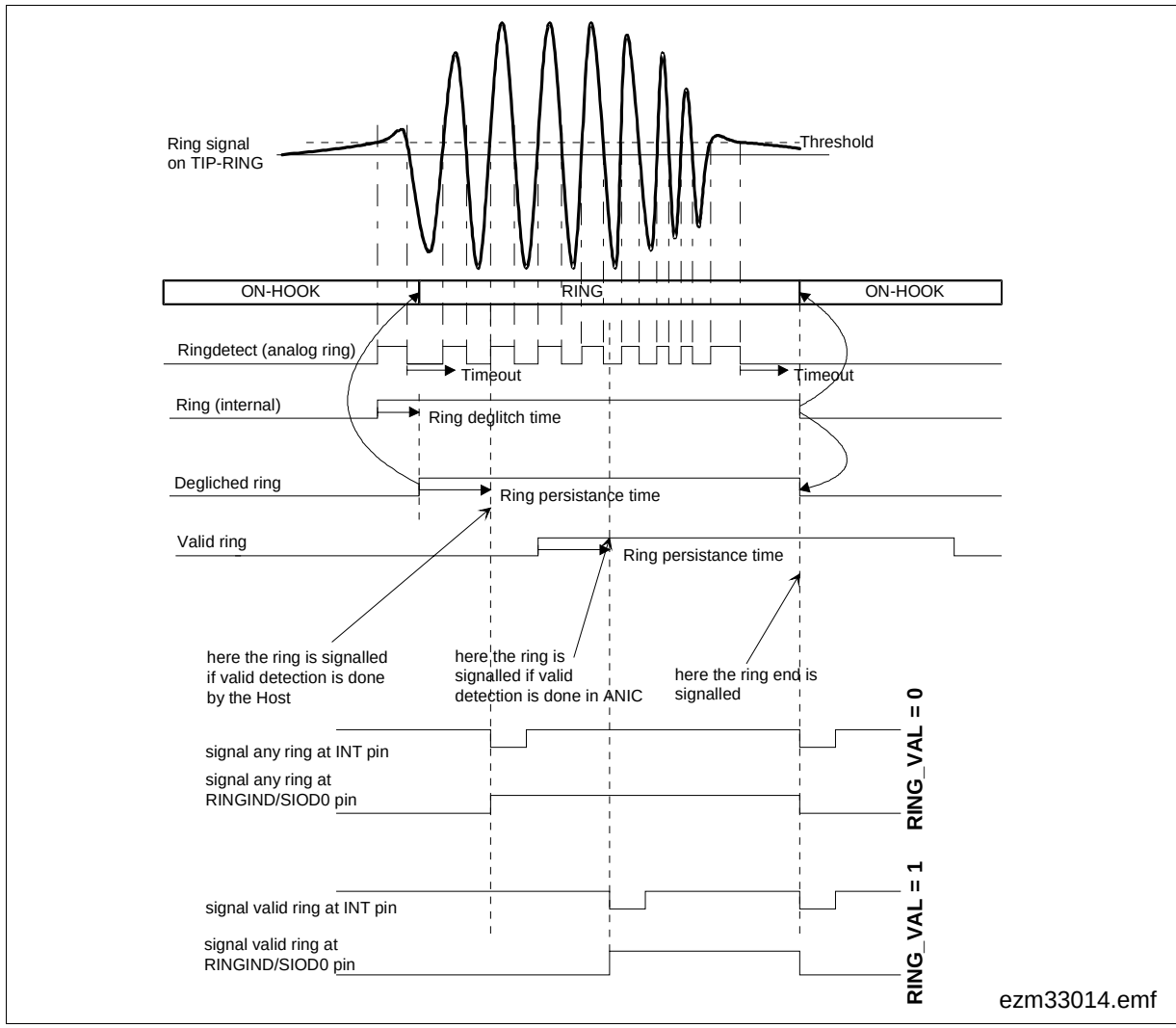


Figure 30 Ring Detect

Note: If ANIC is not in any on-hook mode and a ring interrupt is received, the first task of the interrupt service routine should be to switch the system into the RING mode to prevent damage of the ANIC-A.

7.2.4 ON-HOOK CONVERSATION Mode

Condition: $\overline{\text{RESET}}$ pin = ’1’, external master clock active

The programmed AC impedance for on-hook transmission will be synthesized. ANIC is able to receive and transmit voice or data. So an incoming CLIP (Calling Line Identification Presentation) will see the programmed AC impedance and will be transmitted to the selected PCM timeslot. ANIC will also measure the voltage between TIP-RING, TIP-GROUND and RING-GROUND. If a ring occurs ANIC will enter the Ring Mode.

Tone detection, metering, measurement-threshold interrupts and changes of the GPI pin will be indicated by maskable interrupts.

7.2.5 ON-HOOK RECEIVE Mode

Condition: $\overline{\text{RESET}}$ pin = ’1’, external master clock active

ANIC is able to receive voice and data. So an incoming CLIP (Calling Line Identification Presentation) will see a high AC impedance and will be transmitted to the selected PCM timeslot. ANIC will also measure the voltage between TIP-RING, TIP-GROUND and RING-GROUND. If a ring occurs ANIC will enter the Ring Mode.

Tone detection, metering, measurement-threshold interrupts and changes of the GPI pin will be indicated by maskable interrupts.

7.3 Off-hook

7.3.1 CONVERSATION Mode

Condition: $\overline{\text{RESET}}$ pin = ’1’, external master clock active

The programmed DC characteristic will be synthesized. An AC impedance can be programmed. ANIC is able to receive and transmit voice. ANIC will also measure the voltage between TIP-RING, TIP-GROUND and RING-GROUND. The metering signal detection is signalled via interrupt.

Tone detection, metering, measurement-threshold interrupts and changes of the GPI pin will be indicated by maskable interrupts.

For going on-hook, on of the three valid operating modes ON-HOOK RECEIVE, ON-HOOK CONVERSATION or RING has to be selected.

7.4 PULSE COMMAND Mode

It is possible to implement the pulse dialing by alternating between a short and a high ohmic impedance on TIP and RING. The pulse duration for “Make” and “Break” (see register 10) must be controlled by the external host (µC).

8 Electrical Characteristics

8.1 Programmable Filters

A set of programmable filters is used to adapt the whole system to:

- country standards
- board designs (EMI capacitors etc.)
- telephone lines

8.2 DC Characteristics

Within the following chapter the DC performance of the ANIC will be described.

8.2.1 DC Termination

The DC termination is enabled in off-hook mode and disabled during on-hook mode. The DC Termination can be programmed according the formula:

for $I_{TIP\text{-}RING} < I_{LIM}$: $I_{TIP\text{-}RING}(U_{TIP\text{-}RING}) = (U_{TIP\text{-}RING} - U)/R$

for $I_{TIP\text{-}RING} = I_{LIM}$: $I_{TIP\text{-}RING}(U_{TIP\text{-}RING}) = I_{LIM}$

*Note: U is the sum of the U_0 value (see **Table 16**) and the flow voltage of the diodes in the external bridge (typ. 2 x 0.7 V) plus all other external components inserted in series into the loop.*

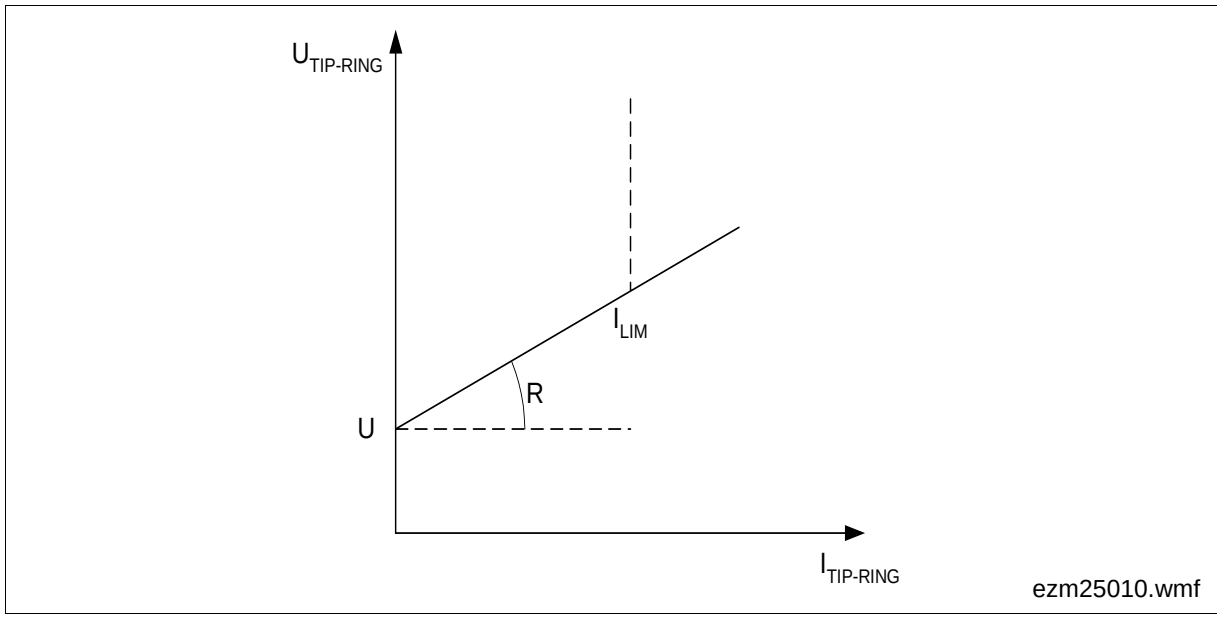


Figure 31 DC Termination Characteristics

8.2.2 Programming Ranges for DC Termination

Table 15 Selectable Values for I_{LIM}

I_{LIM} [1)]
55 mA
110 mA

1) for temperature depency see **Page 80**.

Table 16 Selectable Values for U_0

U_0 (DCU)
0 V
1 V
2.5 V
3.1 V

Table 17 Selectable Values for R

R (DCR)
95 Ω
190 Ω
270 Ω
530 Ω
960 Ω

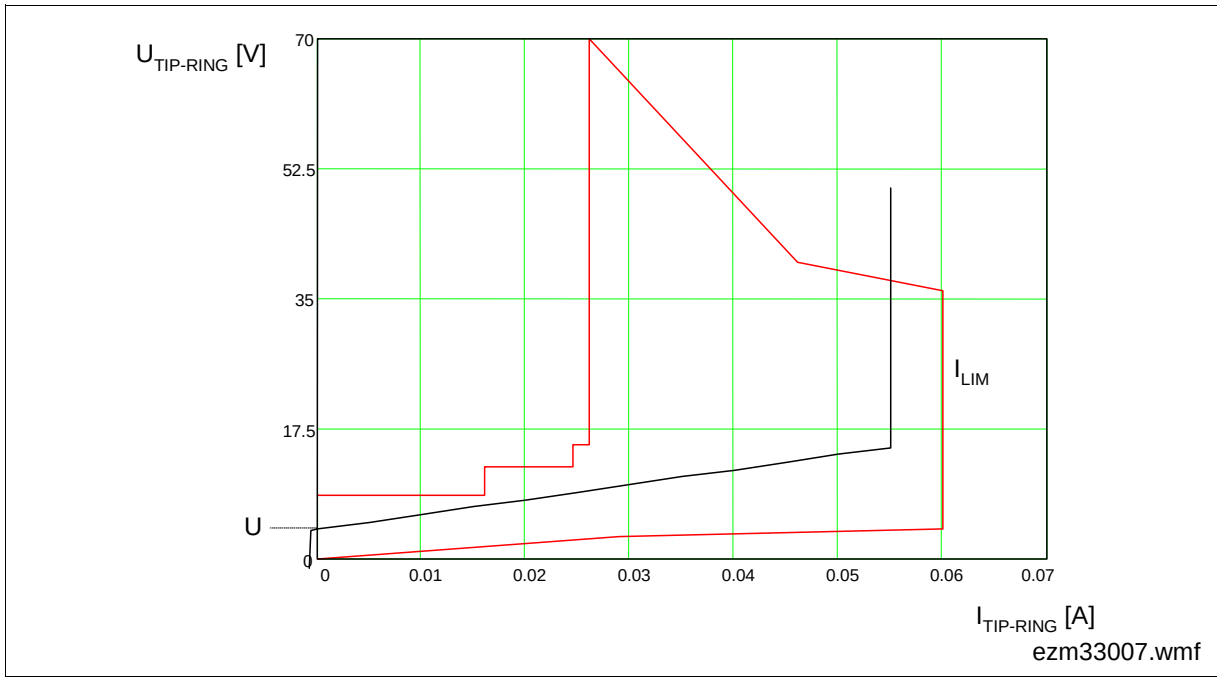


Figure 32 DC Characteristics for France

The diagram above shows the programmed DC feeding characteristics $I_{TIP\text{-}RING}$ (with U_0 = 2,5 V , R = 200 Ω , I_{LIM} = 55 mA) of the ANIC chip set to fulfill the I_{LIM} requirements according to france telecommunication standards.

8.2.3 Line Current in PULSE COMMAND Mode

Uab = 30 V DC

Parameter	Symbol	Limit Values			Unit
		min	typ	max	
Input current at break	I_{in}	–	–	< 500	µA

8.3 AC Termination

8.3.1 Ringer Impedance

Uab = 70 Vrms

Parameter	Symbol	Limit Values			Unit
		min	typ	max	
Ringer impedance (10 Hz < f < 80 Hz)[1)]	R_{IN}	2	–	8	kΩ
Typical capacitors	C_{IN}[2)]	1.5	–	3	µF

1) Ringer impedance is generated only in ring mode.

2) Values achievable with two external capacitors of each 3.3 µF.

8.4 DC Measurement

Parameter	Symbol	Limit Values			Unit
		min	typ	max	
Resolution		–	–	8	Bit
Absolut error	ΔV_{IN}	–	–	3 %	
Relative error	ΔV_{IN}	–	–	1 %	

8.4.1 Ring Detect Levels and Frequencies

Parameter	Symbol	Limit Values			Unit	Tolerance
		min	typ	max		
Programmable range for ring-level detection	V_{ring}	10	–	150	V	± 10%
Ring-level detection step size	ΔV_{ring}	–	–	5	V	± 10%
Programmable range for frequency detection	F_{ring}	10	–	80	Hz	± 10%

8.4.2 On-hook and Off-hook Settling Time

Parameter	Symbol	Limit Values			Unit	Tolerance
		min	typ	max		
Time off-hook to on-hook[1)]	t_{ON}	–	–	0.5	ms	
Time on-hook to off-hook[1)]	t_{OFF}	–	–	0.5	ms	

1) Time from CS to until loop current is above or below 15 mA, for 8 or 16 kHz sampling frequency only.

9 Electrical Performance Characteristics

Functionality and performance is guaranteed for T_A = 0 °C to 70 °C by production testing. Extented temperature range operation at – 40 °C < T_A < 85 °C is guaranteed by design, characterization and periodically sampling and testing production devices at the temperature extremes.

9.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings		Unit
		min	max	
Supply voltage PSB 4451	V_{DD}	– 0.3	4.6	V
Input voltages PSB 4451	VD_{IN}	– 0.3	5.5	V
Supply voltage PSB 4450	V_{DDA}	– 0.3	7.0	V
Input voltages PSB 4450	V_{IN}	– 0.3	10.3	V
DC input and output current (free from latch-up)	I_{in} , I_{out}	–	100	mA
Storage temperature	T_{ST}	– 55	150	°C
Ambient temperature under bias	T_A	– 40	85	°C
Max. power dissipation	$PDmax$	–	1	W

Note: Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at maximum levels may degrade performance and affect reliability.

9.2 Recommended Operating Conditions

Parameter	Symbol	Conditions			Unit
		min	typ	max	
Digital supply voltage PSB 4451	V_{DD}	3.0	3.3	3.6	V
Analog supply voltage PSB 4450	V_{DDA}	4.75	5.0	5.25	V
Ambient temperature under bias	T_A	– 40	25	110	°C
Junction Temperature	T_J	– 40	25	125	°C
Operating frequency	f_{MCLK}	16.384	24.576	33	MHz
Clock duty cycle	–	45	50	55	%
Signal rise and fall time	t_r, t_f	–	–	10	ns

Note: Extended operation outside the recommended limits may degrade performance and affect reliability.

9.3 DC Characteristics

9.3.1 PSB 4450

V_{DDA} = 5 V ± 5 %; T_A = – 40 °C to 85 °C, unless otherwise stated.

Table 18 DC Characteristics PSB 4450

Parameter	Symbol	Conditions	Spec. Limits			Unit
			min	typ	max	
Power-up time	t_{PU}	–	–	–	100	ms
Supply Current						
IDLE mode	I_{DDA1}	V_{ring} = 60 Vdc + 90 Vrms, f_{ring} = 25 – 50 Hz $V_{TIP-RING}$ = 30 Vdc	–	2.5	3	mA
ON-HOOK CONVERSATION and ON-HOOK RECEIVE modes	I_{DDA2}		–	17	20	mA
RING mode	I_{DDA4}	–	–	–	10	mA
CONVERSATION mode	I_{DDA5}	–	–	–	10	mA
Digital Interface						
Low-level input voltage	V_{IL}	–	–	–	0.8	V
High-level input voltage	V_{IH}	–	2.0	–	–	V
Low-level output voltage	V_{OL}	I_{OL} = 5 mA	–	–	0.5	V
High-level output voltage	V_{OH}	I_{OH} = – 5 mA	3.25	–	–	V
Input current low	I_{IL}	$V_{IL} = V_{GNDA}$	–	–	± 1	µA
Input current high	I_{IH}	$V_{IH} = V_{DDA}$	–	–	± 1	µA
Input Resistance DC						
On-hook: IDLE mode RING mode	R_{IN}	200 V	–	–	1[1)]	MΩ
Off-hook:						
Pulse dialing	R_{IN}	Inter-pulsing period (make)	–	–	200	W
CONVERSATION mode	R_{IN}	–	–	–	–	W
Power supply rejection	PSRR	Ripple: 0 - 150 kHz; 70 mVrms				

Table 18 DC Characteristics PSB 4450 (Continued)

either supply/direction		300 Hz - 3.4 kHz	40	–	–	dB
either supply/direction		3.4 kHz - 150 kHz	25	–	–	dB

1) Higher impedances can be achived by the use of an external hook switch (see Application Note "Understanding the External Components of the ANIC Chip Set")

9.3.2 PSB 4451

V_{DD} = 3.3 V ± 5 %; T_A = – 40 °C to 85 °C, unless otherwise stated.
All digital inputs are 5 V tolerant.

Table 19 DC Characteristics PSB 4451

Parameter	Symbol	Conditions	Spec. Limits			Unit
			min	typ	max	
Supply Current						
IDLE mode	I_{DD0}	V_{DD} = 3.3 V f_{MCLK} = 25 MHz no load	–	11	15	mA
ON-HOOK CONVERSATION and ON-HOOK RECEIVE modes	I_{DD1}		–	22	30	mA
RING mode	I_{DD3}		–	22	30	mA
CONVERSATION mode	I_{DD4}		–	22	30	mA
Low-level Input Voltage						
– at CMOS Inputs: RINGIND/SIOD0, SIOD1, $\overline{CS}$, DCLK , DIN, DATCLK, DATIN, FSC, $\overline{RESET}$	V_{IL1}	–	0	–	0.8	V
– at clock Input: MCLK1	V_{IL2}	–	– 0.2 V	–	0.8	V
High-level Input Voltage						
– at CMOS Inputs: RINGIND/SIOD0, SIOD1, $\overline{CS}$, DCLK , DIN, DATCLK, DATIN, FSC, $\overline{RESET}$	V_{IH1}	–	2.0	–	5.5	V
– at clock Input: MCLK1	V_{IH2}	–	2.5	–	V_{DD} + 0.2	V
Low-level Output Voltage						
- at pins: DOUT, $\overline{INT}$, DATOUT, FSC, DATCLK, DCDCCLK	V_{OL1}	I_{OL1} = 5 mA	–	–	0.5	V
- at pins: SIOD1, METIND/SOD0	V_{OL2}	I_{OL2} = 2.5 mA	–	–	0.5	V

Table 19 DC Characteristics PSB 4451 (Continued)

High-level Output Voltage						
- at pins: DOUT, DATOUT, FSC, DATCLK, DCDCCLK	V_{OH1}	I_{OH1} = – 5 mA	V_{DD} – 0.5	–	–	V
- at pins: SIOD1, METIND/SOD0	V_{OH2}	I_{OH2} = – 2.5 mA	V_{DD} – 0.5	–	–	V
Input Current Low						
- at CMOS inputs: RINGIND/SIOD0, SIOD1, $\overline{CS}$, DCLK , DIN, DATCLK, DATIN,FSC, $\overline{RESET}$	I_{IL}	$V_{IL} = V_{GND}$	–	–	± 1	µA
Input Current High						
- at CMOS Inputs: RINGIND/SIOD0, SIOD1, $\overline{CS}$, DCLK , DIN, DATCLK, DATIN, FSC, $\overline{RESET}$	I_{IH}	$V_{IH} = V_{DD}$	–	–	± 1	µA
Tristate Current Low						
Tristates, Bidirectionals: DOUT[1)], DATCLK, DATOUT[1)], SIOD1, FSC, $\overline{INT}$[2)]	I_{OZL}	$V_{IL} = V_{GND}$	–	–	± 1	µA
Tristate Current High						
Tristates, Bidirectionals: DOUT[1)], DATCLK, DATOUT[1)], SIOD1, FSC, $\overline{INT}$[2)]	I_{OZH}	$V_{IH} = V_{DD}$	–	–	± 1	µA

1) 660 kΩ internal pull-up resistor (range 330 kΩ to 2 MΩ) not taken into consideration.

2) 33 kΩ internal pull-up resistor (range 16.5 kΩ to 100 kΩ) not taken into consideration.

9.4 AC Transmission Characteristics

Unless otherwise stated, the transmission characteristics are guaranteed within the following test conditions:

T_A = – 40 °C to 85 °C

V_{DD} = 3.3 V ± 5 %

V_{DDA} = 5 V ± 5 %

Line impedance Z_L = 600 ± 0.1 % Ω

Termination impedance Z_M = 600 Ω

digital: 0 dBm0 = – 3.14 dB FS

analog: 0 dBm is equal to the voltage of 0.775 Vrms when loaded with 600 Ω

f = 1014 Hz.

AGR = 0 dB, AGX = – 8.5 dB

Note: Informations on degradiation due to extended temperature range is available on request.

9.4.1 Absolute Gain Error Off-hook

Parameter	Symbol	Limit Values			Unit	Test Condition
		min	typ	max		
Absolute gain error receive	AE_R					– 10 dBm
T_A = 25 °C; V_{DDA} = 5 V		– 0.3	± 0.2	0.3	dB	
T_A = 0 - 70 °C; V_{DDA} = 5 V		– 0.3	± 0.3	0.3	dB	
Absolute gain error transmit	AE_X					– 10 dBm0
T_A = 25 °C; V_{DDA} = 5 V		– 0.3	± 0.2	0.3	dB	
T_A = 0 - 70 °C; V_{DDA} = 5 V		– 0.3	± 0.3	0.3	dB	

9.4.2 Absolute Gain Error On-hook

Parameter	Symbol	Limit Values			Unit	Test Condition
		min	typ	max		
Absolute gain error receive	AE_R					– 10 dBm
T_A = 25 °C; V_{DDA} = 5 V		– 0.5	± 0.2	0.5	dB	
T_A = 0 - 70 °C; V_{DDA} = 5 V		– 0.5	± 0.3	0.5	dB	
Absolute gain error transmit	AE_X					– 10 dBm0
T_A = 25 °C; V_{DDA} = 5 V		– 0.5	± 0.2	0.5	dB	
T_A = 0 - 70 °C; V_{DDA} = 5 V		– 0.5	± 0.3	0.5	dB	

9.4.3 Gain Tracking Off / On-hook

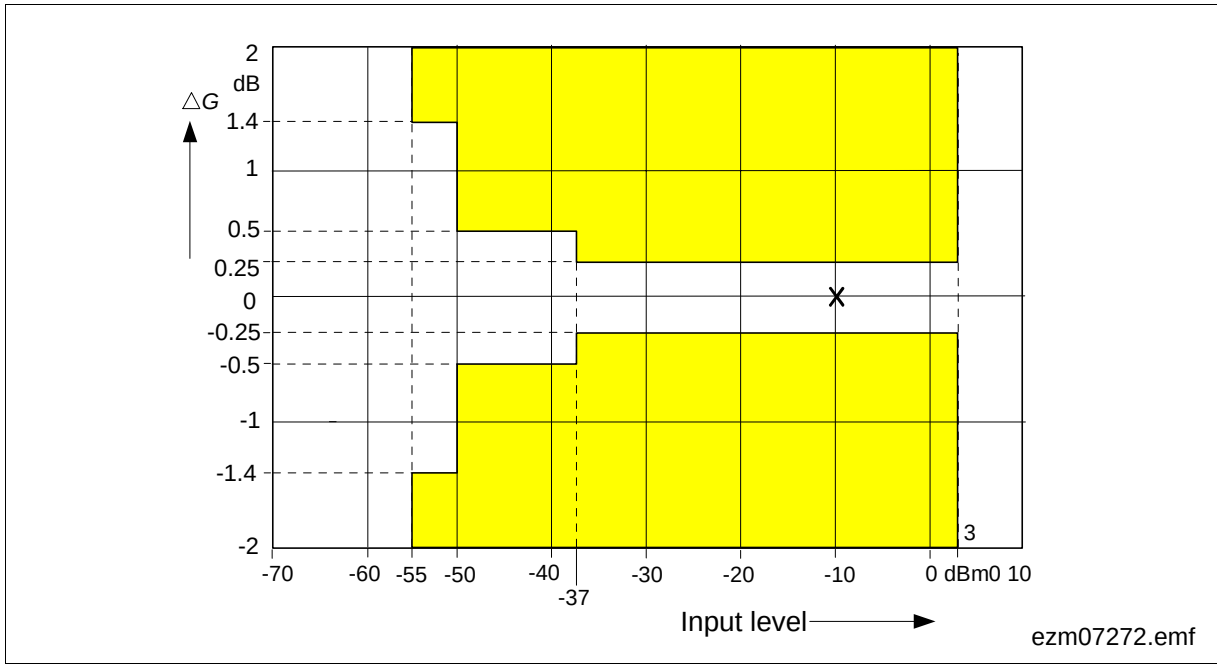


Figure 33 Gain Tracking Off / On-hook (Receive or Transmit)

Note: measured with sine wave f = 1014 Hz, reference level is – 10 dBm(0)

9.4.4 Idle Channel Noise

Parameter	Symbol	Limit Values			Unit	Test Condition
		min	typ	max		
Idle channel noise:						
transmit, A-law	N_{TP}	–	–	– 67.4	dBm0p	psophometric V_{IN} = 0 V
transmit, µ-law	N_{TC}	–	–	17.5	dBmc	C-message V_{IN} = 0 V
receive, A-law	N_{RP}	–	– 85	– 78.0	dBm0p	psophometric idle code + 0
receive, µ-law	N_{RC}	–	5	12.0	dBmc	C-message idle code + 0

9.4.5 Out of Band Idle Channel Noise at TIP/RING

With an idle code applied to the digital input, the level of any resulting out-of-band power spectral density (measured with 3 kHz bandwidth) at the analog output, will be not greater than the limit curve shown in the figure below.

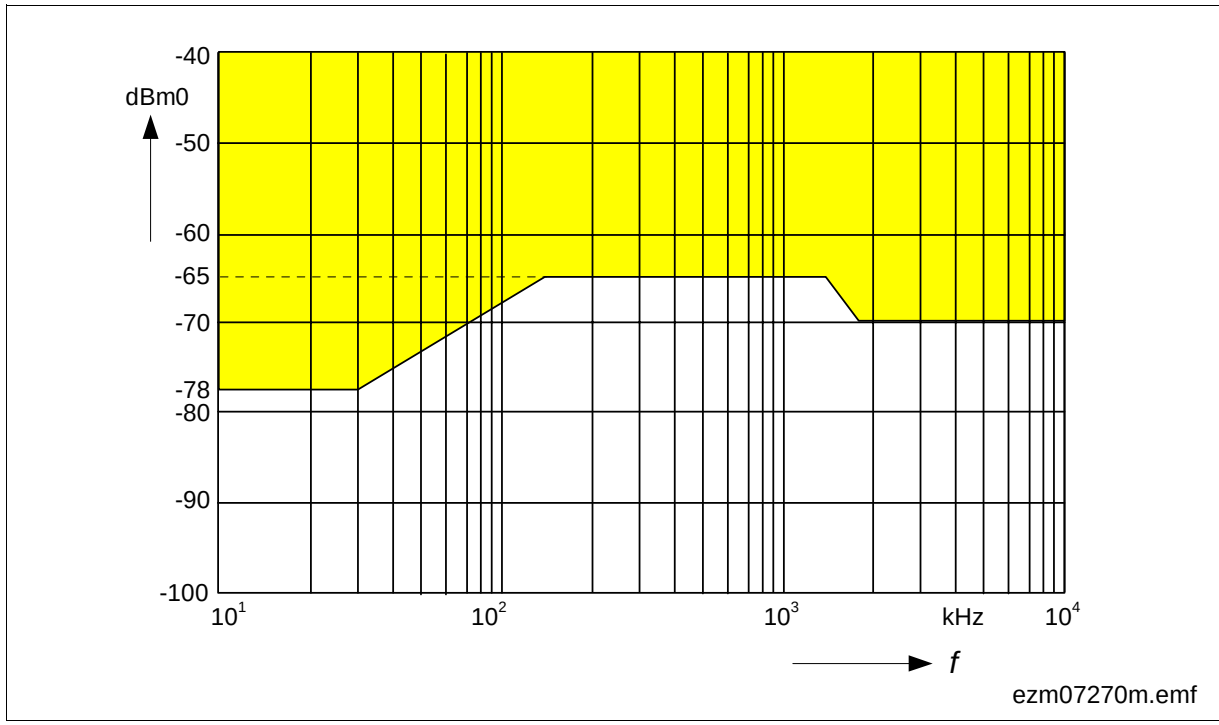


Figure 34 Out of Band Idle Channel Noise

9.4.6 Harmonic Distortion plus Noise Off-hook

– 10 dBm(0); Z_L = 600 Ω; f = 1014 Hz

Parameter	Symbol	Limit Values			Unit	Test condition
		min	typ	max		
HDN receive	THDN_R_c	74	–	–	dBFS	C-weighted
HDN transmit	THDN_T_c	73	–	–	dBm	
HDN receive	THDN_R_l	72	–	–	dBFS	linear-weighted[1)]
HDN transmit	THDN_T_l	71	–	–	dBm	

1) Linear weighted values are guaranteed by design. Characterization and periodically samples will be applied to production devices at this test conditions.

9.4.7 Harmonic Distortion plus Noise On-hook

– 10 dBm(0); Z_L = 600 Ω; f = 1014 Hz

Parameter	Symbol	Limit Values			Unit	Test condition
		min	typ	max		
HDN receive	THDN_R_c	64	67	–	dBFS	C-weighted
HDN transmit	THDN_T_c	64	67	–	dBm	
HDN receive	THDN_R_l	62	65	–	dBFS	linear-weighted[1)]
HDN transmit	THDN_T_l	62	65	–	dBm	

1) Linear weighted values are guaranteed by design. Characterization and periodically samples will be applied to production devices at this test conditions.

9.4.8 Harmonic Distortion Off-hook

– 10 dBm0; Z_L = 600 Ω; f = 100 to 2000 Hz, 2nd and 3rd harmonic

Parameter	Symbol	Limit Values			Unit	Test Condition
		min	typ	max		
HD receive	HDN_R	80	–	–	dBm0	–
HD transmit	HDN_T	80	–	–	dBm	–
HD of echo signals via TIP-RING	HDN_E_l	80	–	–	dBm0	–

The gain deviations stay within the limits in the figures below.

9.4.9 Harmonic Distortion On-hook

– 10 dBm0; Z_L = 600 Ω; f = 100 to 2000 Hz, 2nd and 3rd harmonic

Parameter	Symbol	Limit Values			Unit	Test Condition
		min	typ	max		
HD receive	HDN_R	70	–	–	dBm0	–
HD transmit	HDN_T	70	–	–	dBm	–
HD of echo signals via TIP-RING	HDN_E_l	70	–	–	dBm0	–

9.4.10 Total Distortion

The signal to distortion ratio exceeds the limits in the following figure.

9.4.10.1 Total Distortion Measured with Sine Wave

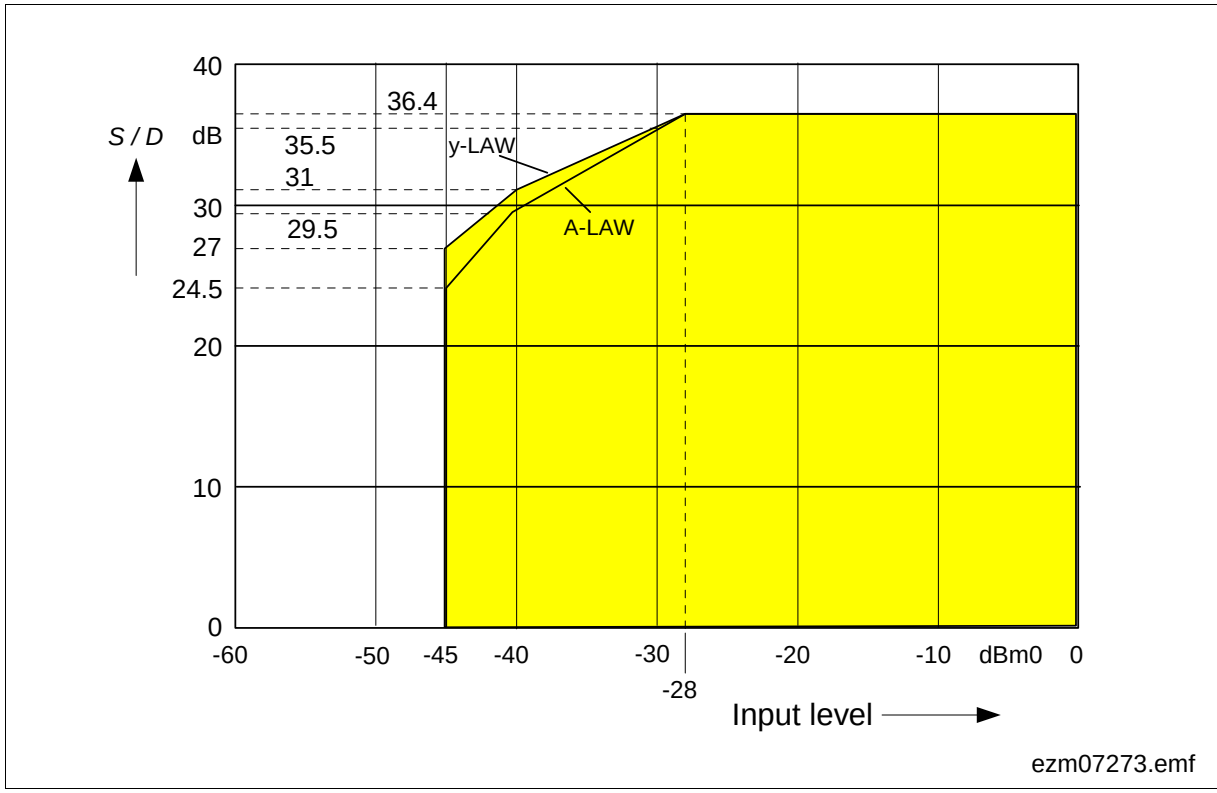


Figure 35 Total Distortion Receive or Transmit

Note: measured with sine wave ƒ = 1014 Hz (C-message weighted for µ-law, psophometrically weighted for A-law).

9.4.10.2 Total Distortion Measured with Noise According to CCITT

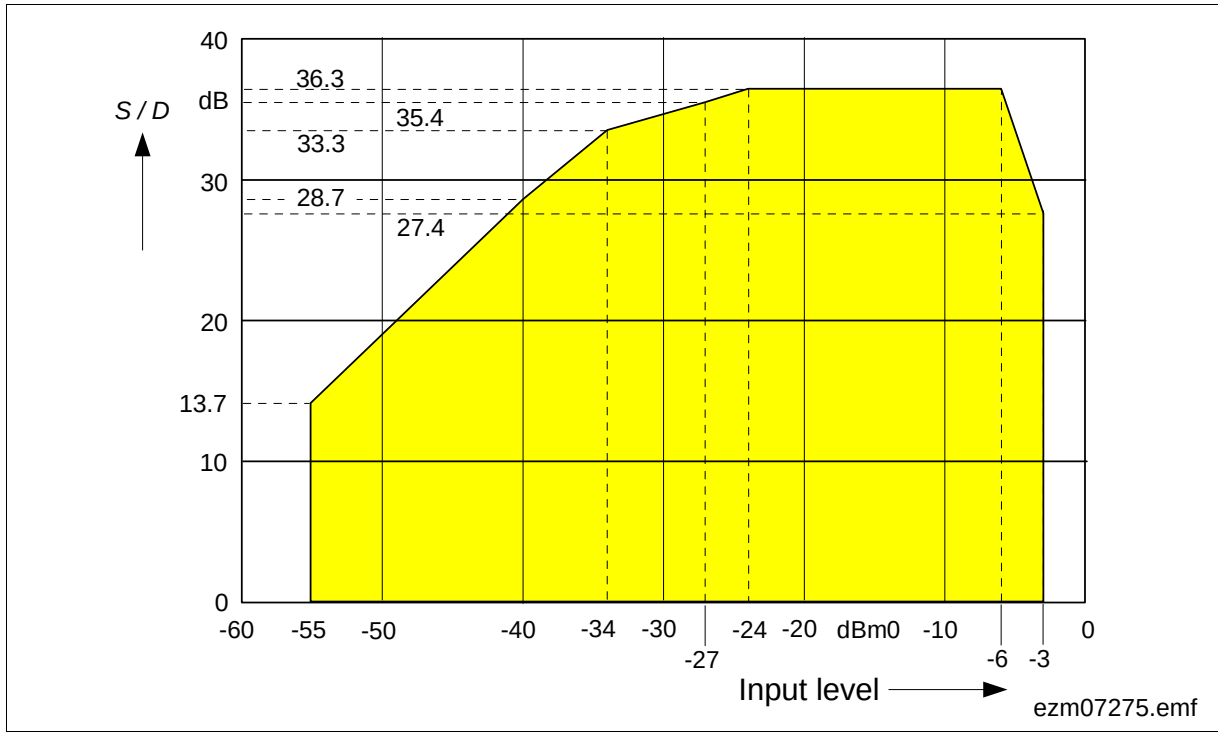


Figure 36 Total Distortion Receive

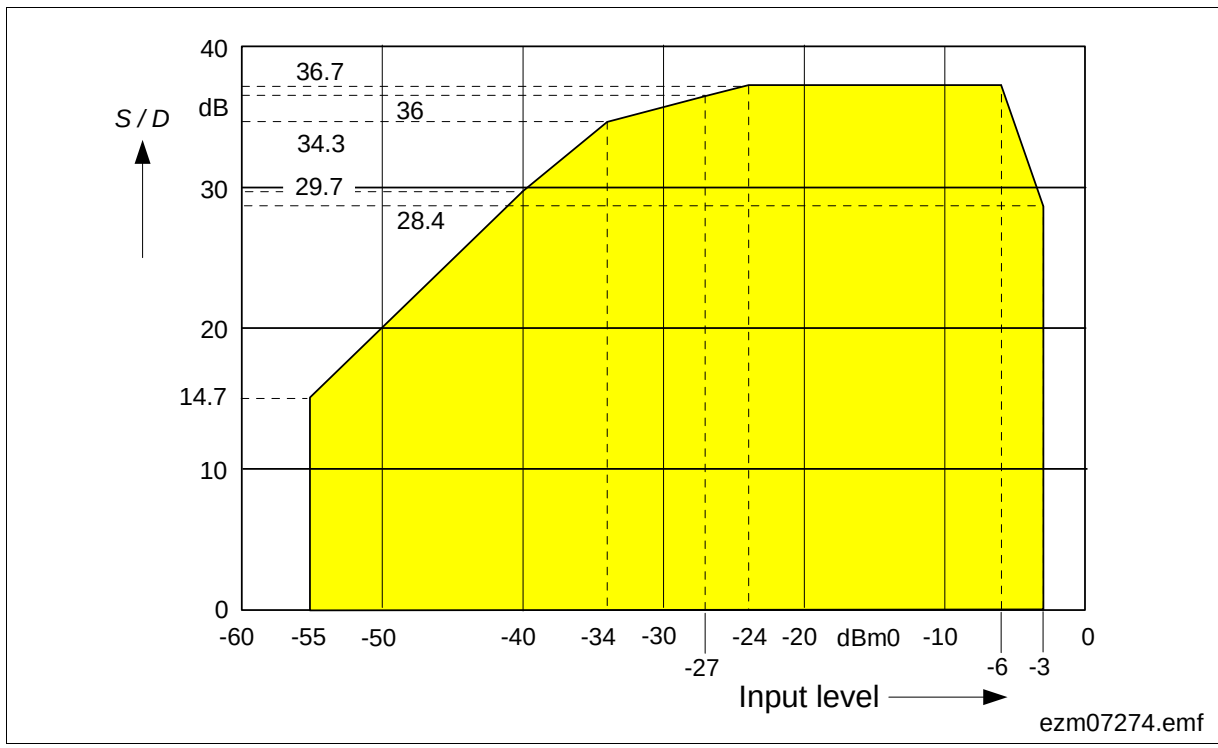


Figure 37 Total Distortion Transmit

9.4.11 Return Loss

The return loss at a level of 0 dBm0 is better than 16 dB in a 300 - 3600 Hz bandwidth within the following range of AC impedances: Z_{AC} = 500 - 1500 Ω (0 to - 30°).

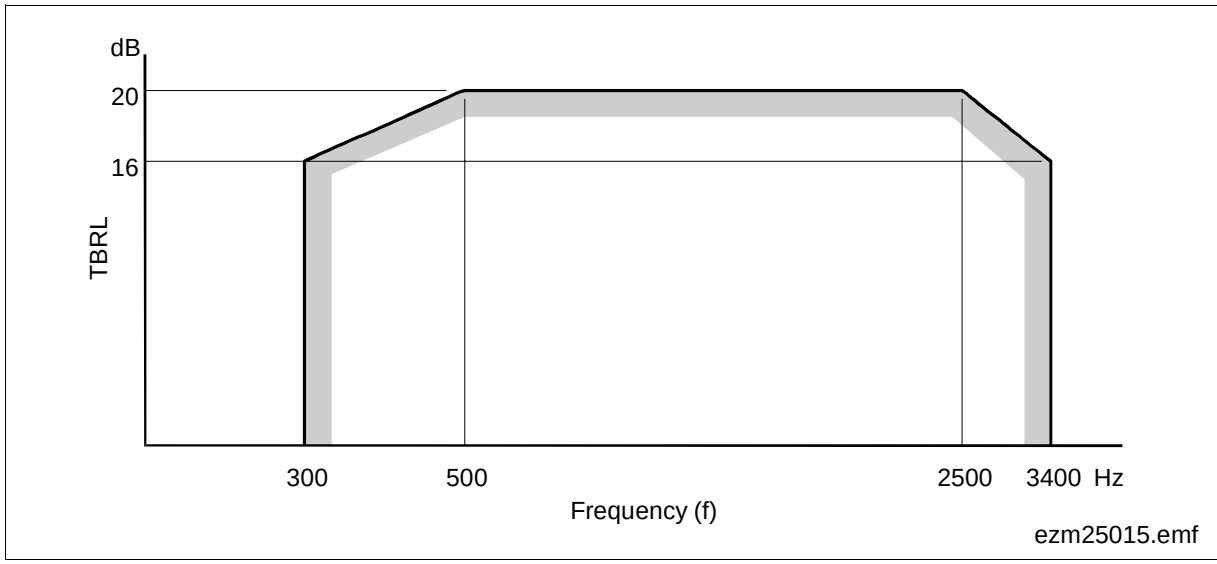


Figure 38 Return Loss

9.4.12 Frequency Response

The following tables and diagrams are for on-hook transmission as well as for off-hook transmission.

9.4.12.1 Receive

Reference frequency 1014 Hz, input signal level – 10 dBm

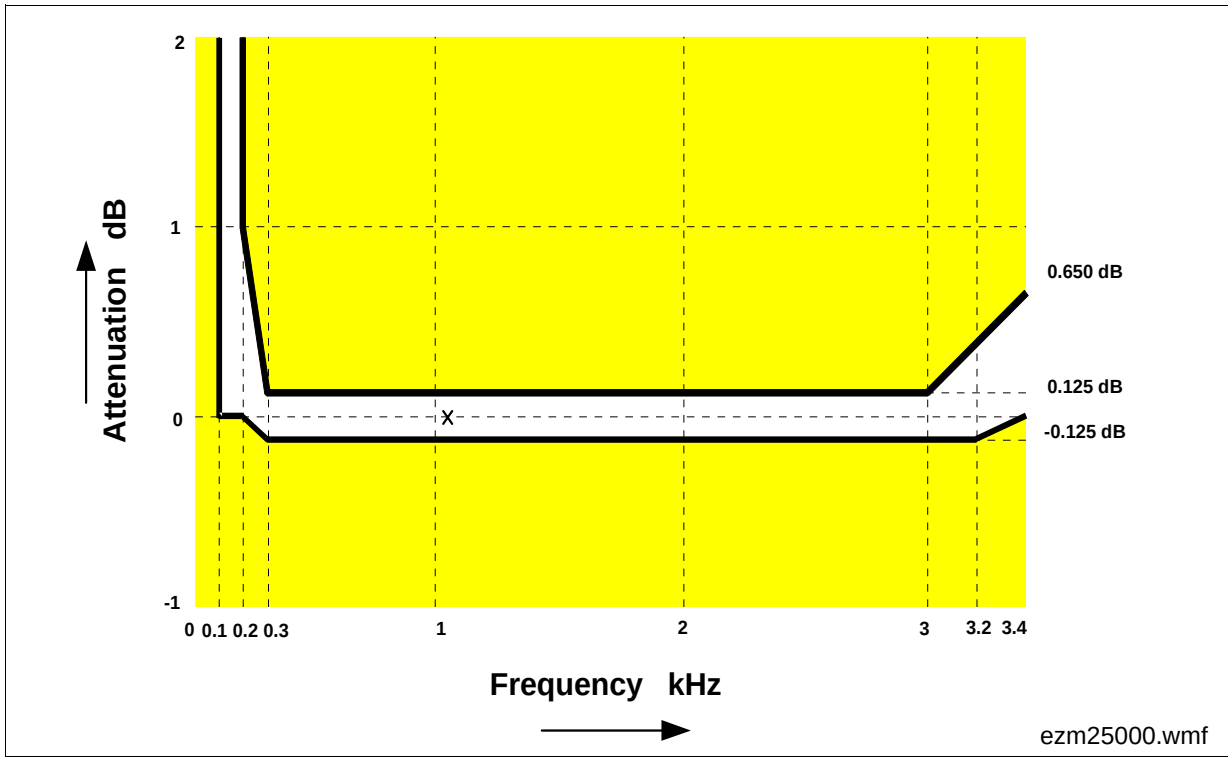


Figure 39 Frequency Response Receive

9.4.12.2 Transmit

Reference frequency 1014 Hz, input signal level – 10 dBm

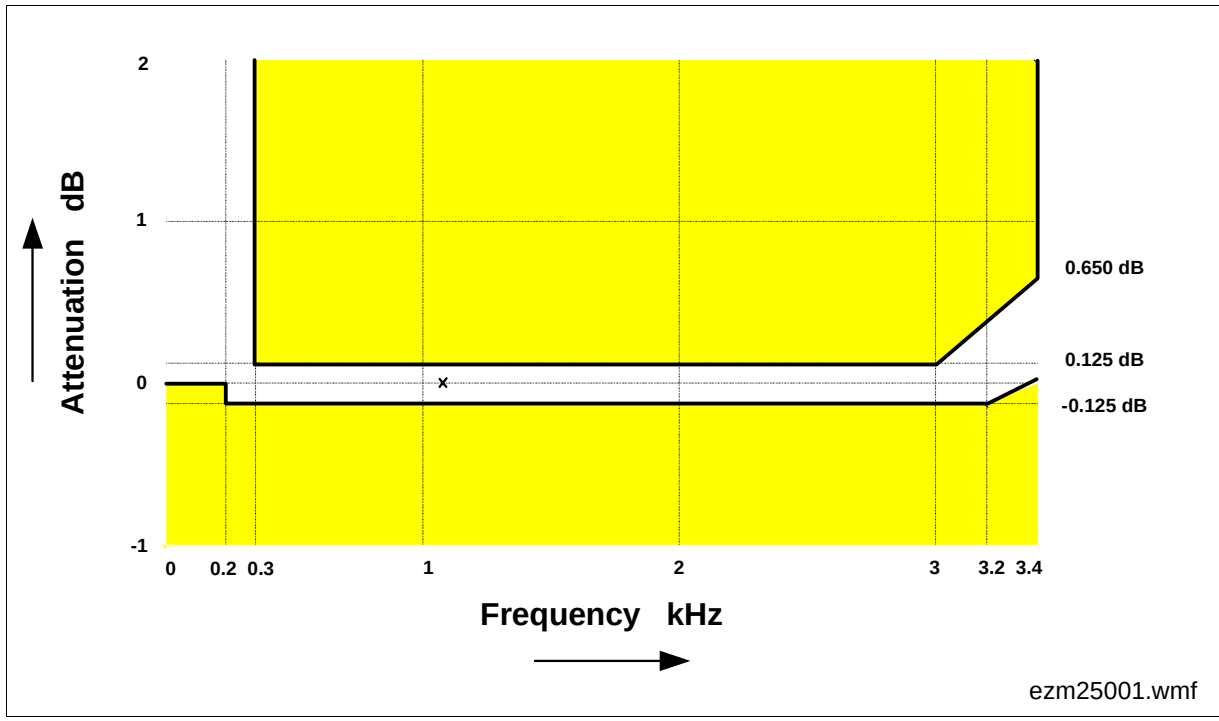


Figure 40 Frequency Response Transmit (HPX is off)

9.4.13 Group Delay

Group delay is per definition[1)] the time of propagation between two points of a certain point (e.g. the crest) of the envelope of a wave.

For a given frequency it is equal to the first derivative of the phase shift measured in radians, between these points, with reference to the angular frequency measured in radians per second.

Group Delay remains within the limits in the figures below.

9.4.13.1 Group Delay Absolute Values

Parameter	Symbol	Limit Values			Unit	Reference
		min	typ	max		
Receive delay	DRA	–	–	340	µs	Input signal level 0 dBm0
Transmit delay	DXA	–	–	400	µs	

The absolute group delay refers to the minimum group delay measured in the frequency band 500 Hz - 2800 Hz.

9.4.13.2 Group Delay Distortion

Taking as the reference the minimum group delay, in the frequency range between 500 Hz and 2800 Hz, of the receive or transmit connection, the group delay distortion of that connection should lie within the limits shown in **Figure 41** and **Figure 42**.

Group delay distortion is measured in accordance with ITU-T Recommendation O.81.

1) from CCIT Blue Book, Volume 1, Fascicle 1.3 "Terms and Definitions. Abbreviations and Acronyms".

Group Delay Distortion Receive

Input signal level – 10 dBm

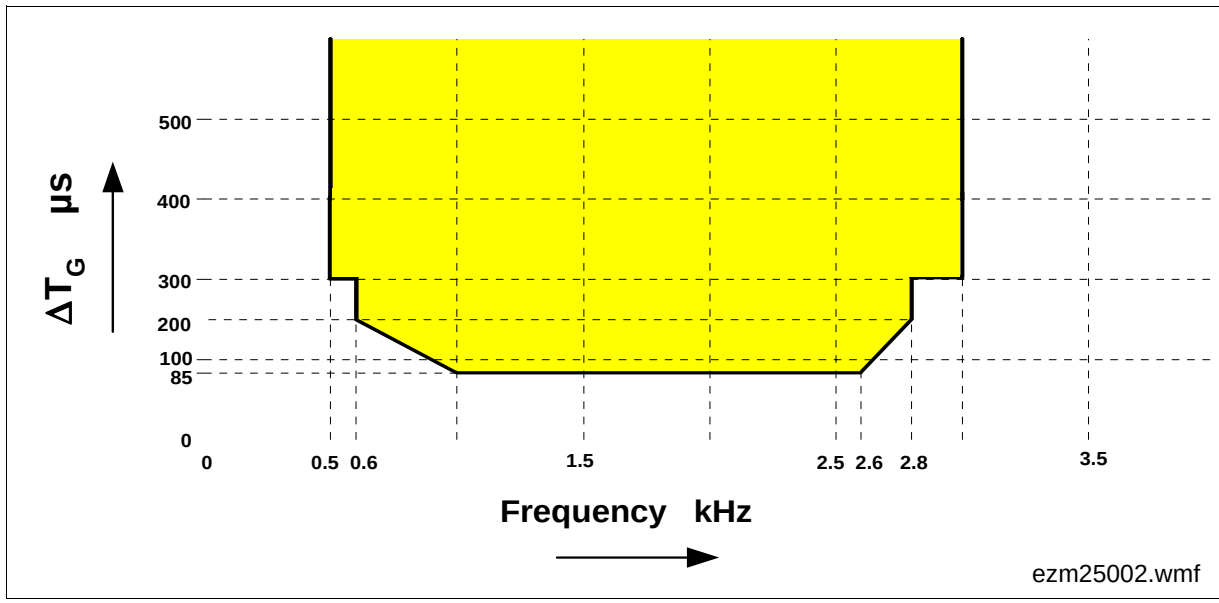


Figure 41 Group Delay Distortion Receive

Group Delay Distortion Transmit

Input signal level – 10 dBm0

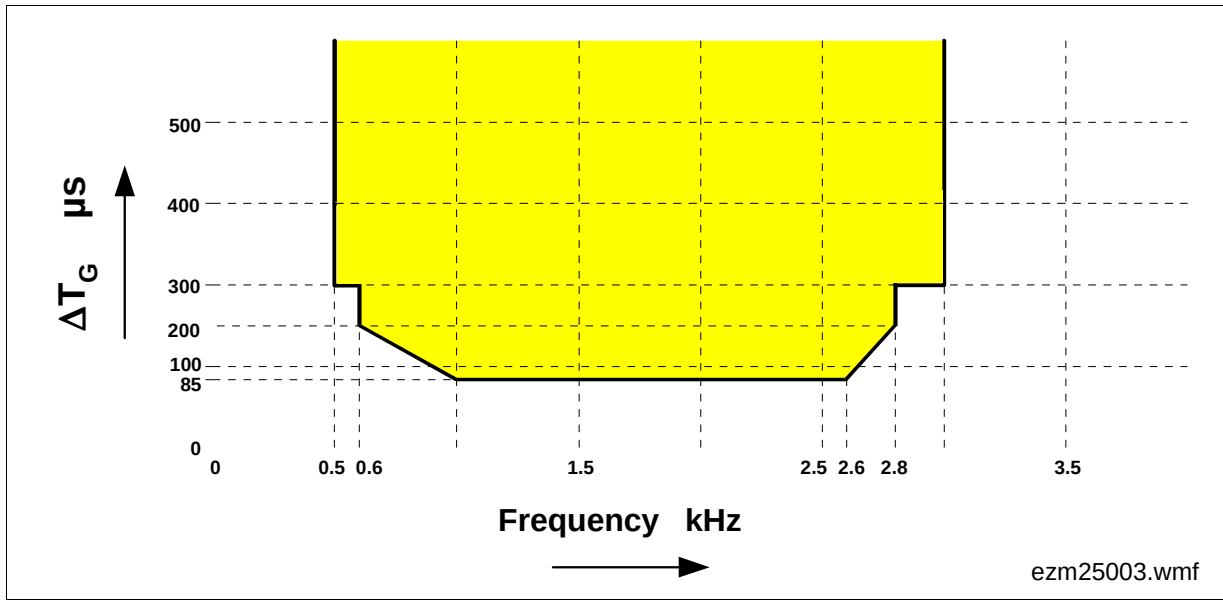


Figure 42 Group Delay Distortion Transmit

9.4.14 Out-of-Band Signals at TIP-RING Receive

When an 0 dBm0 out-of-band sine-wave signal with a frequency of << 100 Hz or 3.4 kHz to 100 kHz) is applied to the analog input, the level of any resulting frequency component at the digital output will stay at least X dB below a 0 dBm0 (1014 Hz sine wave reference signal at the analog input.[1])

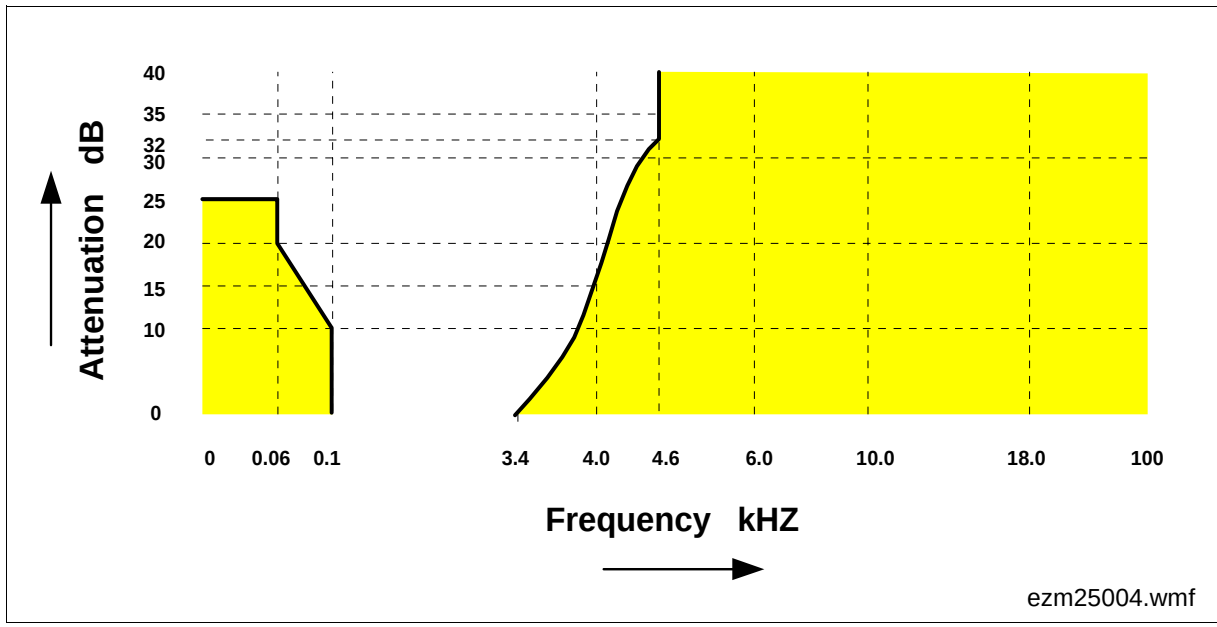


Figure 43 Out of Band Receive Discrimination

[1] Poles at 12 kHz ± 150 Hz and 16 kHz ± 150 Hz will be provided

9.4.15 Out-of-Band Signals at TIP-RING Transmit

When a 0 dBm0 sine wave with a frequency of (300 Hz to 3.99 kHz) is applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0 1014 Hz sine-wave reference signal at the analog output.

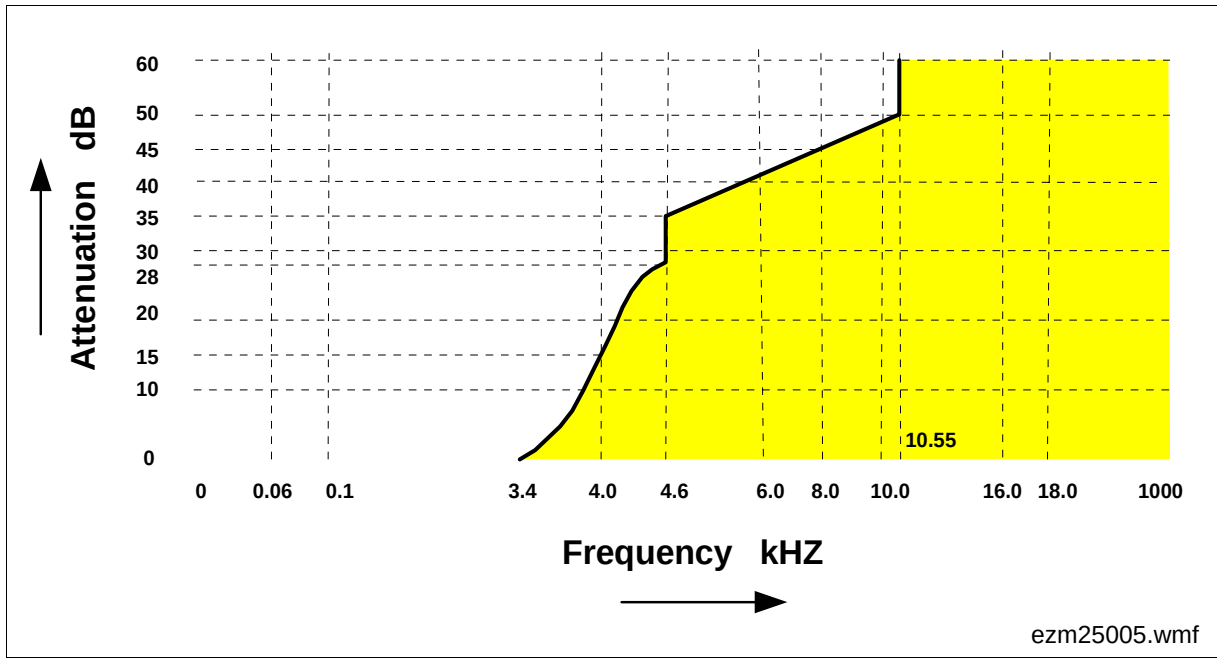


Figure 44 Out of Band Transmit Discrimination

9.4.16 Trans-Hybrid Loss

Parameter	Symbol	Limit Values		Unit	Test Condition
Trans-hybrid loss at		min	typ		
300 Hz	THL 300	27	–	dB	T_A = 25° C; V_{DDA} = 5 V;
500 Hz	THL 500	33	–	dB	
2500 Hz	THL2500	29	–	dB	
3000 Hz	THL3000	27	–	dB	
3400 Hz	THL3400	27	–	dB	

The listed values for THL correspond to a typical variation of the signal amplitude and delay in the analog blocks.

Amplitude = typ. ± 0.8 dB

Delay = typ. ± 0.5 µs

9.4.17 Metering Detection Sensibility

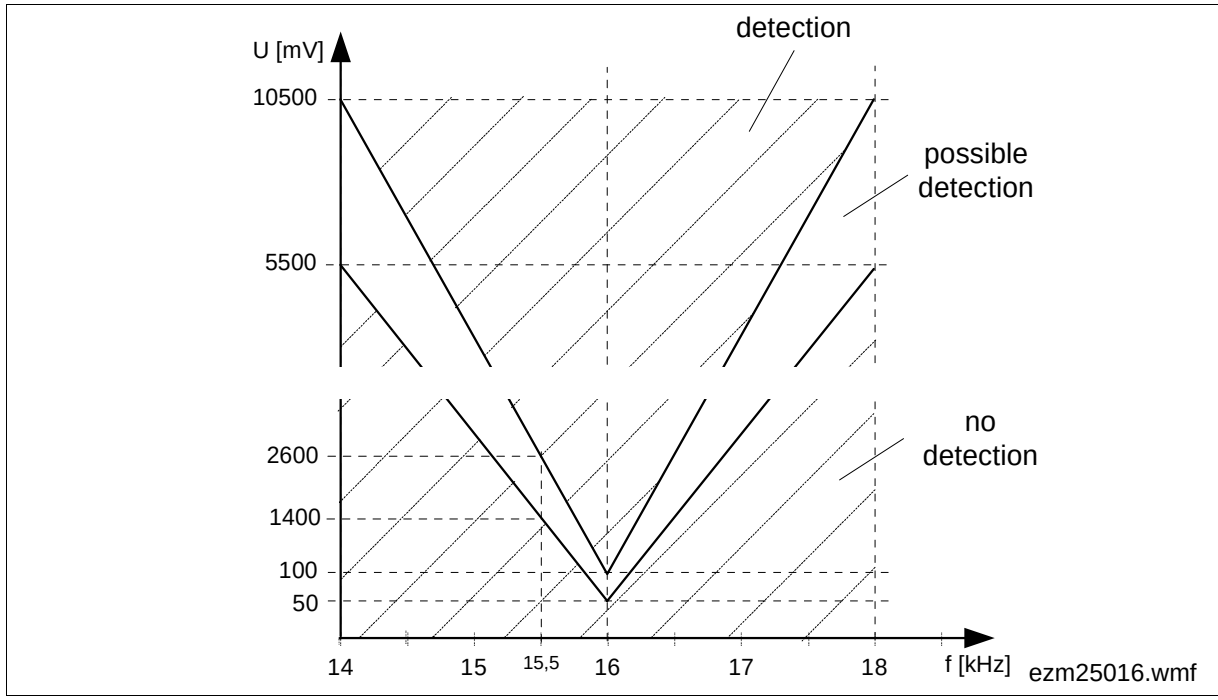


Figure 45 Metering Detection Sensibility 16 kHz (Typical)

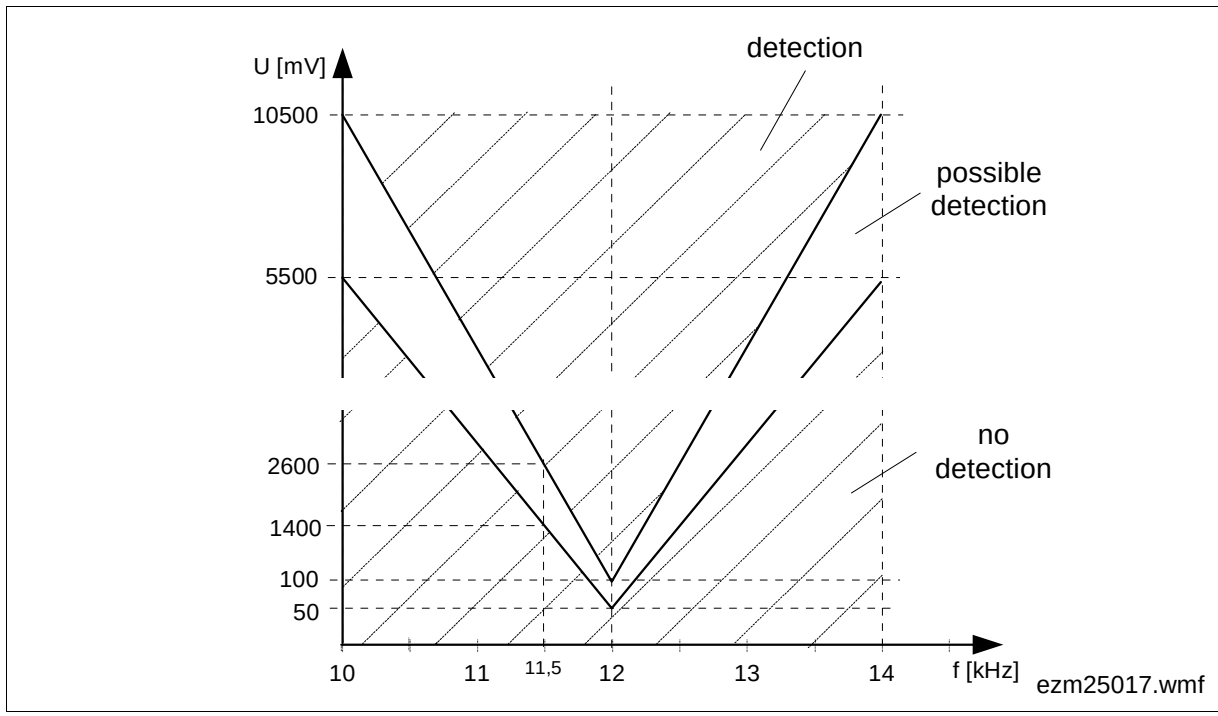


Figure 46 Metering Detection Sensibility 12 kHz (Typical)

9.5 AC Timing Characteristics

9.5.1 Input/ Output Waveform for AC Tests

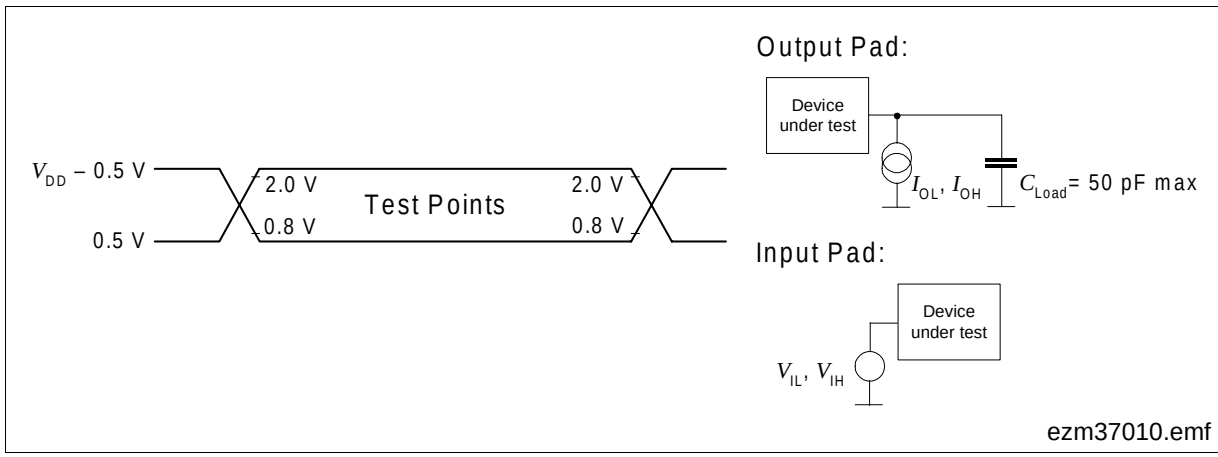


Figure 47 Waveform for AC Tests

During AC-Testing, the CMOS inputs are driven at a low level of 0.8 V and a high level of 2.0 V. The CMOS outputs are measured at 0.5 V and V_{DD} – 0.5 V respectively.

9.5.2 Reset Timing

To reset the ANIC, pulses applied to the $\overline{\text{RESET}}$ pin must be less than 0.8 V and longer than $t_{RESET,min}$ (300 ns). Pulses shorter than $t_{RESET,ignore}$ (60 ns) are ignored.

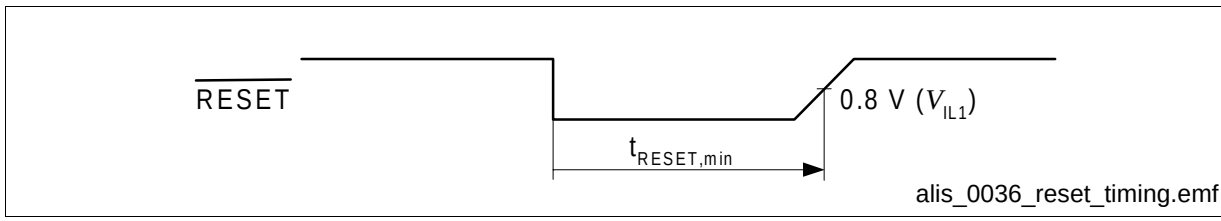


Figure 48 Reset Timing

9.5.3 Serial Control Interface Timing

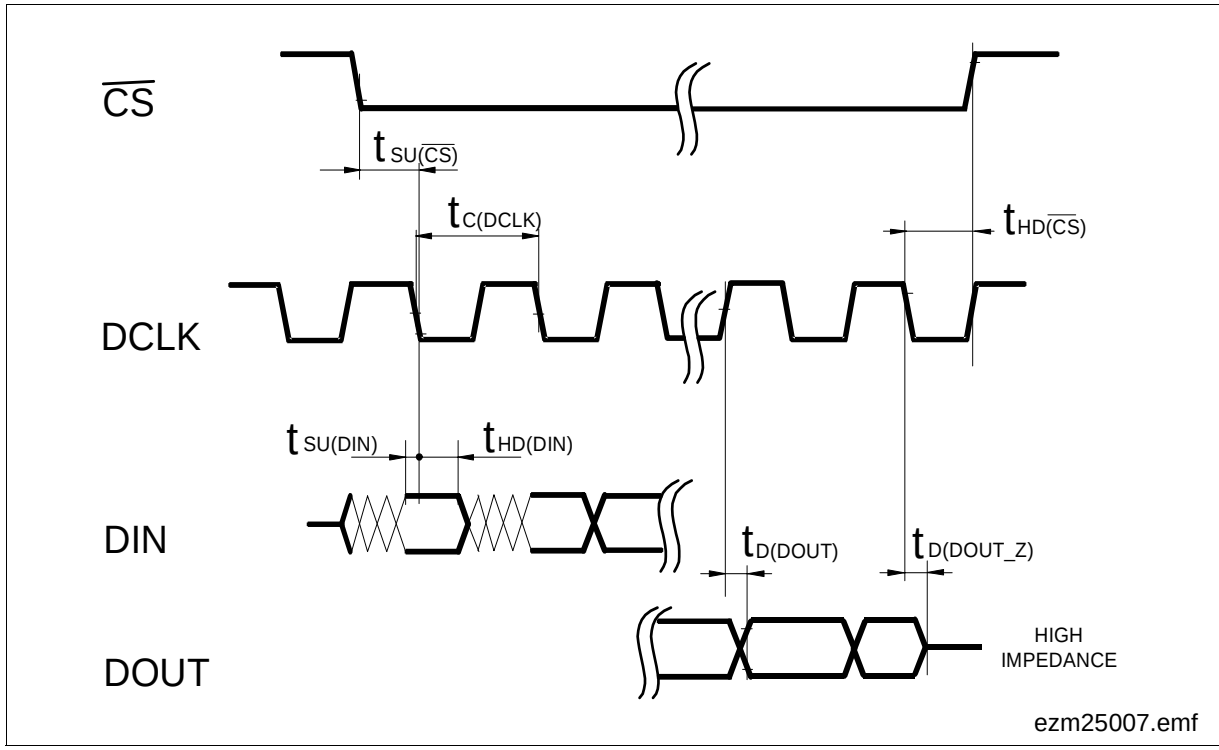


Figure 49 Serial Control Interface Timing

Table 20 Serial Control Interface Switching Characteristics

V_{DD} = 3.3 V ± 5 %; T_A = – 40 °C to 85 °C, unless otherwise stated.
DCLK doesn´t need to have a constant frequency

Parameter	Symbol	Limit Values			Unit
		min	typ	max	
DCLK cycle time	$t_{C(DCLK)}$	488	–	10^6	ns
DCLK duty cycle	–	45	50	55	%
DCLK frequency (SCI-Clock f_{DCLK})	–	1	–	2048	kHz
Setup time: $\overline{CS}$↓ until next DCLK↓	$t_{SU(\overline{CS})}$	2*T_{MCLK}	–	–	ns
Hold time: last DCLK↓ until $\overline{CS}$↑	$t_{HD(\overline{CS})}$	2*T_{MCLK}	–	–	ns
Setup time: DIN valid before DCLK↓	$t_{SU(DIN)}$	20	–	–	ns
Hold time: last DCLK↓ until DIN invalid	$t_{HD(DIN)}$	20	–	–	ns
Delay time: DCLK↑ until DOUT valid	$t_{D(DOUT)}$	–	–	20	ns
Delay time: last DCLK↓ until DOUT_Z (when DOUT goes to tristate) at I_{OL1} = 5 mA	$t_{D(DOUT\_Z)}$	5	10	40	ns

Note: Internal pull-up resistor at DOUT: 660 kΩ (range 330 kΩ to 2 MΩ).

9.5.4 PCM Interface Timing

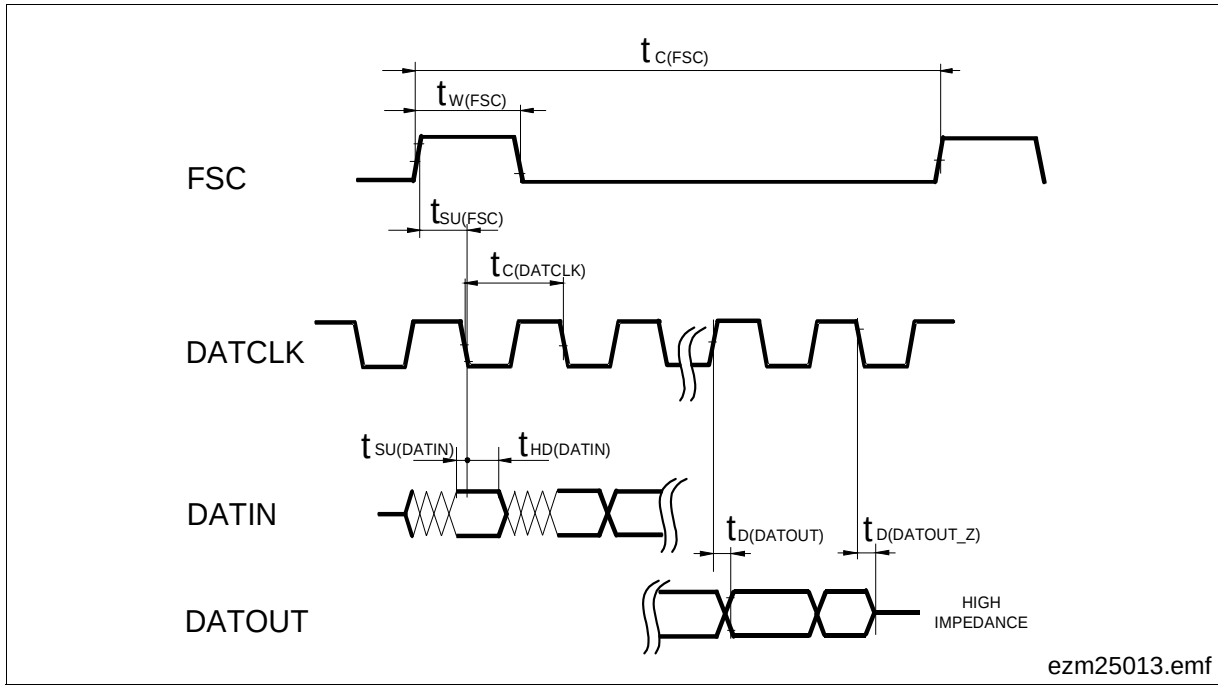


Figure 50 PCM Interface Timing

Note: DATOUT goes to tristate on the last bit of 8 or 16 bits transferred in a FSC frame before DATOUT switches to high impedance.

Table 21 PCM Interface Switching Characteristics

V_{DD} = 3.3 V ± 5 %; T_A = – 40 °C to 85 °C, unless otherwise stated.

The last data bit of a certain timeslot on DATOUT changes to tristate after approximately $t_{C(DATCLK)}$ / 2.

Parameter	Symbol	Limit Values			Unit
		min	typ	max	
DATCLK (PCM-Clock) cycle time	$t_{C(DATCLK)}$	488	–	1953	ns
DATCLK (PCM-Clock) duty cycle	–	45	50	55	%
DATCLK (PCM-Clock) frequency	–	512	–	2048	kHz
Frame Synchronization Clock (FSC) cycle time	$t_{C(FSC)}$	83	125	166	µs
FSC frequency	–	6	8	12	kHz
FSC pulse width (as input)	$t_{W(FSC)}$	$t_{C(DATCLK)}$	–	–	ns
Setup time: DATIN valid before DATCLK↓	$t_{SU(DATIN)}$	20	–	–	ns
Hold time: last DATCLK↓ until DATIN invalid	$t_{HD(DATIN)}$	20	–	–	ns
Delay time: DATCLK↑ until DATOUT valid	$t_{D(DATOUT)}$	–	–	20	ns
Setup time: FSC↑ until next DATCLK↓	$t_{SU(FSC)}$	$4*T_{MCLK}$	–	–	ns
Delay time: last DATCLK↓ until DATOUT_Z (when DATOUT goes to tristate, LSB only) at I_{OL1} = 5 mA	$t_{D(DATOUT\_Z)}$	5	10	40	ns

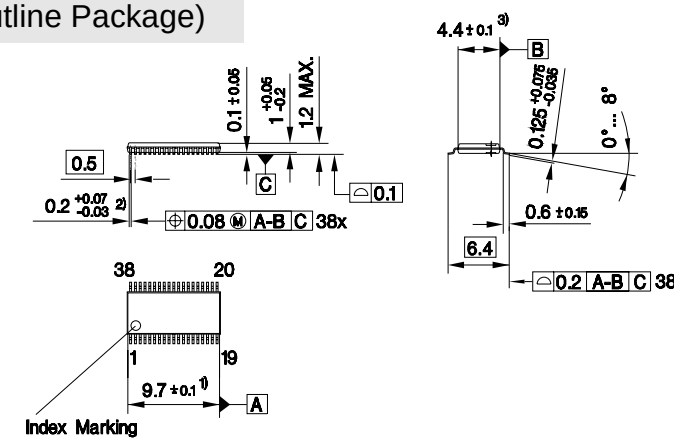
Note: Internal pull-up resistor at DATOUT: 660 kΩ (range 330 kΩ to 2 MΩ)

10 Application Circuit

For an application circuit see our Application Note "Understanding the External Components of the ANIC Chip Set".

11 Package Outlines

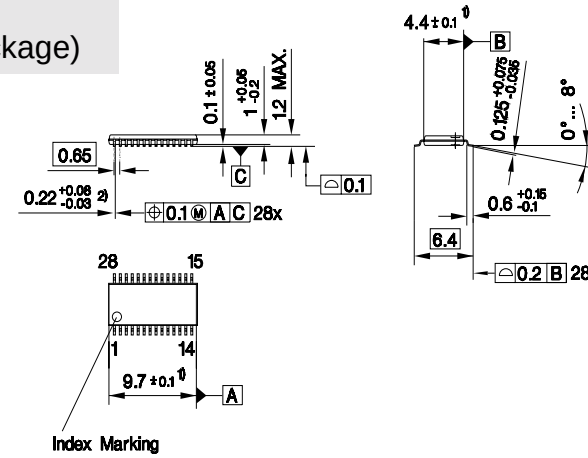
P-TSSOP38 PSB 4450
(Plastic Thin Shrink Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.08 max. per side
3) Does not include plastic or metal protrusion of 0.25 max. per side

Gps09158.eps

P-TSSOP28 PSB 4451
(Plastic Thin Shrink Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

Gps05867.eps

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our data book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

12 Glossary

ADC	Analog-to-Digital Converter
ANIC	Analog Network Interface Circuit
CLIP	Calling Line Identification Presentation
CO	Central Office
CODEC	Coder/Decoder
CRAM	Coefficient RAM
DAA	Data Access Arrangement
DAC	Digital-to-Analog Converter
DLC	Digital Loop Carrier
DSL	Digital Subscriber Line
DSP	Digital Signal Processing
EMC	Electro Magnetic Compatibility
FCC	Federal Communications Commission
GPI	General Purpose Input
GPO	General Purpose Output
Mbits/s	Mega Bits Per Second
MDSL	Mid-rate Digital Subscriber Line
MLT	Mechanical Loop Testing
MUX	Multiplexer
PCM	Pulse Code Modulation
PBX	Private Branch Exchange
VDD	Voltage Drain Drain
µCI, SCI	Serial Control Interface

13 Index

R

S

T

V

Infineon goes for Business Excellence

“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

http://www.infineon.com

Published by Infineon Technologies AG