19-3151; Rev 1; 7/04

MAXIM

14-Bit, 4-Channel, Software-Programmable, Multiranging, Simultaneous-Sampling ADC

General Description

The MAX1338 14-bit, analog-to-digital converter (ADC) offers four simultaneously sampled, fully differential input channels, with independent track-and-hold (T/H) circuitry for each channel. The input channels are individually software programmable for input ranges of ±10V, ±5V, ±2.5V, and ±1.25V. The input channels feature fault tolerance to ±17V. The internal T/H circuits have a 16ns aperture delay and 100ps aperture-delay matching.

A 14-bit parallel bus provides the conversion result with a maximum per-channel output rate of 150ksps (600ksps for all four channels). The MAX1338 has an on-board oscillator and 2.5V internal reference. An external clock and/or reference can also be used.

The MAX1338 operates from a +5V supply for analog inputs and digital core. The device operates from a +2.7V to +5.25V supply for the digital I/O lines. The MAX1338 features two power-saving modes: standby mode and shutdown mode. Standby mode allows rapid wake-up and reduces quiescent current to 4mA (typ), and shutdown mode reduces sleep current to less than 10µA (typ).

The MAX1338 is available in an 8mm x 8mm x 0.8mm, 56-pin, thin QFN package. The device operates over the extended -40°C to +85°C temperature range.

Applications

Multiple-Channel Data Recorders

Vibration Analysis

Motor Control: 3-Phase Voltage, Current, and Power Measurement

Optical Communication Equipment

Features

- **150ksps Sample Rate per Channel**
- **All Four Input Channels Simultaneously Sampled**
  - **16ns Aperture Delay**
  - **100ps Aperture-Delay Matching**
- **Channel-Independent Software-Selectable Input Range: ±10V, ±5V, ±2.5V, ±1.25V**
- **±17V Fault-Tolerant Inputs**
- **Dynamic Performance at 10kHz Input**
  - **SNR: 77dB**
  - **SINAD: 76dB**
  - **SFDR: 98dBc**
  - **THD: -83dBc**
- **DC Performance**
  - **INL: ±2 LSB**
  - **DNL: ±1 LSB**
  - **Offset Error: ±4 LSB**
  - **Gain Error: ±0.1% FSR**
- **14-Bit Parallel Interface**
- **Internal Clock and Reference Voltage**
- **+5V Analog and Digital Supplies**
- **+2.7V to +5.25V Digital I/O Supply**
- **56-Pin Thin QFN Package (8mm x 8mm x 0.8mm)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1338ETN	-40°C to +85°C	56 Thin QFN-EP*

**EP = Exposed pad.*

Pin Configuration appears at end of data sheet.

14-Bit, 4-Channel, Software-Programmable, Multiranging, Simultaneous-Sampling ADC

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND .....-0.3V to +6V
DV_{DD} to DGND.....-0.3V to +6V
DRV_{DD} to DRGND.....-0.3V to +6V
AV_{DD} to DV_{DD} .....-0.3V to +0.3V
DGND to DRGND .....-0.3V to +0.3V
AGND to DGND.....-0.3V to +0.3V
AGND to DRGND .....-0.3V to +0.3V
AIN0+, AIN0-, AIN1+, AIN1-, AIN2+, AIN2-, AIN3+, AIN3- to AGND .....-17V to +17V
D0–D13 to DRGND.....-0.3V to (DRV_{DD} + 0.3V)
REFADC, REFP1, REFP2, REFN1, REFN2, COM1, COM2 to AGND.....-0.3V to (AV_{DD} + 0.3V)
INTCLK/$\overline{EXTCLK}$ to AGND.....-0.3V to (AV_{DD} + 0.3V)
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, CONVST, to DRGND.....-0.3V to (DRV_{DD} + 0.3V)
SHDN, STANDBY, CLK, $\overline{EOC}$, $\overline{EOLC}$ to DRGND.....-0.3V to (DRV_{DD} + 0.3V)
Maximum Current into Any Pin .....±50mA
Continuous Power Dissipation (T_A = +70°C)
56-Pin Thin QFN (derate 31.3mW /°C above +70°C)....2500mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range.....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Junction to Ambient Thermal Resistance θ_{JA}.....32°C/W
Junction to Case Thermal Resistance θ_{JC}.....2°C/W

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD} = +5.0V, DRV_{DD} = +3.0V, AGND = DGND = DRGND = 0, INTCLK/$\overline{EXTCLK}$ = AGND, f_{CLK} = 5MHz, input range = ±10V, REFP2 = REFP1, REFN2 = REFN1, COM1 = COM2, 1.0nF from REFADC to AGND, 1.0µF and 0.1µF from COM1 to AGND, 0.1µF from REFP1 to AGND, 0.1µF from REFN1 to AGND, 1.0µF from REFP1 to REFN1. Typical values are at T_A = +25°C. T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		14			Bits
Integral Nonlinearity	INL	(Note 1)		±1	±3	LSB
Differential Nonlinearity	DNL	No missing codes (Note 1)		±0.25	±1	LSB
Offset Error		(Note 1)		±4	±16	LSB
Offset-Error Temperature Coefficient				5		ppm/°C
Offset-Error Matching				±10		LSB
Gain Error		Offset nulled (Notes 1, 2)		±0.1	±0.35	%FSR
Channel Gain-Error Matching		Offset nulled		±20		LSB
Gain-Error Temperature Coefficient		Offset nulled		10		ppm/°C
DYNAMIC PERFORMANCE (at f_{IN} = 10kHz, A_{IN} = -0.2dBFS)						
Sampling Rate Per Channel		Simultaneous on all channels			150	ksps
Signal-to-Noise Ratio	SNR	(Note 1)	75	77		dB
Signal-to-Noise Plus Distortion	SINAD	(Note 1)	74	76		dB
Total Harmonic Distortion	THD	(Note 1)		-83	-80	dBc
Spurious-Free Dynamic Range	SFDR	Range 0 (Note 1)	85			dBc
Channel-to-Channel Isolation		(Note 1)	80			dB
ANALOG INPUTS (AIN_)						
Input Differential Voltage Range		Range set bits = (0,0)	-10		+10	V
		Range set bits = (0,1)	-5		+5	
		Range set bits = (1,0)	-2.5		+2.5	
		Range set bits = (1,1)	-1.25		+1.25	

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +5.0V, DRV_{DD} = +3.0V, AGND = DGND = DRGND = 0, INTCLK/$\overline{EXTCLK}$ = AGND, f_{CLK} = 5MHz, input range = ±10V, REFP2 = REFP1, REFN2 = REFN1, COM1 = COM2, 1.0nF from REFADC to AGND, 1.0µF and 0.1µF from COM1 to AGND, 0.1µF from REFP1 to AGND, 0.1µF from REFN1 to AGND, 1.0µF from REFP1 to REFN1. Typical values are at T_A = +25°C. T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Common-Mode Range		Range set bits = (0,0)	-5		+5	V
		Range set bits = (0,1)	-2.5		+2.5	
		Range set bits = (1,0)	-1.25		+1.25	
		Range set bits = (1,1)	-0.625		+0.625	
Input Resistance		All settings		6.25		kΩ
Input Capacitance				15		pF
Small-Signal Bandwidth	SSBW	(Note 1)		1		MHz
Full-Power Bandwidth	FPBW	(Note 1)		75		kHz
INTERNAL REFERENCE (REFADC)						
Output Voltage			2.475	2.5	2.525	V
Differential Reference Voltage	REFP–REFN			2.5		V
Output-Voltage Temperature Coefficient				50		ppm/°C
Load Regulation				5		V/mA
EXTERNAL REFERENCE						
REFADC Voltage Input Range			2.0	2.5	3.0	V
REFADC Input Current		(Note 3)	-250		+250	µA
REFADC Input Resistance	R_{REF}			5		kΩ
REFADC Input Capacitance				15		pF
TRACK/HOLD (T/H)						
Aperture Delay	t_{AD}	(Note 1)		16		ns
Aperture-Delay Matching				100		ps
Aperture Jitter	t_{AJ}	(Note 1)		50		ps_{RMS}
CLOCK-SELECT INPUT (INTCLK/$\overline{EXTCLK}$)						
Input-Voltage High	V_{IH}		0.7 x AV_{DD}			V
Input-Voltage Low	V_{IL}				0.3 x AV_{DD}	V
DIGITAL INTERFACE AND CONTROL INPUTS ($\overline{CS}$, $\overline{RD}$, $\overline{WR}$, CONVST, SHDN, CLK, STANDBY)						
Input-Voltage High	V_{IH}		0.7 x DRV_{DD}			V
Input-Voltage Low	V_{IL}				0.3 x DRV_{DD}	V
Input Hysteresis				50		mV
Input Capacitance	C_{IN}			15		pF

14-Bit, 4-Channel, Software-Programmable, Multiranging, Simultaneous-Sampling ADC

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +5.0V, DRV_{DD} = +3.0V, AGND = DGND = DRGND = 0, INTCLK/$\overline{EXTCLK}$ = AGND, f_{CLK} = 5MHz, input range = ±10V, REFP2 = REFP1, REFN2 = REFN1, COM1 = COM2, 1.0nF from REFADC to AGND, 1.0µF and 0.1µF from COM1 to AGND, 0.1µF from REFP1 to AGND, 0.1µF from REFN1 to AGND, 1.0µF from REFP1 to REFN1. Typical values are at T_A = +25°C. T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current	I_{IN}	V_{IN} = 0 or DRV_{DD}			±1	µA
DIGITAL INTERFACE AND CONTROL OUTPUTS ($\overline{EOC}$, $\overline{EOLC}$)						
Output-Voltage High	V_{OH}	Sourcing 0.8mA	DRV_{DD} - 0.6			V
Output-Voltage Low	V_{OL}	Sinking 1.6mA			0.4	V
PARALLEL DIGITAL I/O (D0–D7)						
Output-Voltage High	V_{OH}	Sourcing 0.8mA	DRV_{DD} - 0.6			V
Output-Voltage Low	V_{OL}	Sinking 1.6mA			0.4	V
Leakage Current					1	µA
Tristate Output Capacitance		$\overline{RD}$ = 1 or $\overline{CS}$ = 1		15		pF
Input-Voltage High	V_{IH}		0.7 x DRV_{DD}			V
Input-Voltage Low	V_{IL}				0.3 x DRV_{DD}	V
Input Hysteresis				50		mV
Input Capacitance	C_{IN}			15		pF
Input Current	I_{IN}	V_{IN} = 0 or DRV_{DD}			±1	µA
PARALLEL DIGITAL OUTPUTS (D8–D13)						
Output-Voltage High	V_{OH}	Sourcing 0.8mA	DRV_{DD} - 0.6			V
Output-Voltage Low	V_{OL}	Sinking 1.6mA			0.4	V
Leakage Current					1	µA
Tristate Output Capacitance				15		pF
POWER SUPPLIES						
Analog Supply Voltage	AV_{DD}		4.75	5	5.25	V
Digital Supply Voltage	DV_{DD}		4.75	5	5.25	V
Parallel Digital I/O Supply Voltage	DRV_{DD}		2.70		5.25	V
Analog Supply Current	AI_{DD}			41	60	mA
		SHDN = 1		0.005	0.1	
		STANDBY = 1, SHDN = 0		4.2	5	
Digital Supply Current	DI_{DD}				3	mA
		SHDN = 1		0.001	0.05	
		STANDBY = 1, SHDN = 0		0.001	0.05	
Digital Driver Supply Current	DRI_{DD}				3	mA
		SHDN = 1		0	0.05	
		STANDBY = 1, SHDN = 0		0	0.05	
Analog Power-Supply Rejection		4.75V to 5.25V (Note 1)		75		dB

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +5.0V, DRV_{DD} = +3.0V, AGND = DGND = DRGND = 0, INTCLK/$\overline{EXTCLK}$ = AGND, f_{CLK} = 5MHz, input range = ±10V, REFP2 = REFP1, REFN2 = REFN1, COM1 = COM2, 1.0nF from REFADC to AGND, 1.0µF and 0.1µF from COM1 to AGND, 0.1µF from REFP1 to AGND, 0.1µF from REFN1 to AGND, 1.0µF from REFP1 to REFN1. Typical values are at T_A = +25°C. T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figures 4, 5, and 6)						
Time to First Conversion Result	t_{EOC1}	Internal clock	2.9	3.2	3.5	µs
		External clock		16		CLK Cycles
Time to Subsequent Conversions	t_{NEXT}	Internal clock		600		ns
		External clock		3		CLK Cycles
CONVST Pulse-Width Low	t_{CONVST}	Internal clock	0.2			µs
		External clock	0.1			
$\overline{CS}$ Pulse Width	t_{CS}		30			ns
$\overline{RD}$ Pulse-Width Low	t_{RDL}		30			ns
$\overline{RD}$ Pulse-Width High	t_{RDH}		30			ns
$\overline{WR}$ Pulse-Width Low	t_{WRL}		30			ns
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_{CTW}		0			ns
$\overline{WR}$ to $\overline{CS}$ Hold Time	t_{WTC}		0			ns
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{CTR}		0			ns
$\overline{RD}$ to $\overline{CS}$ Hold Time	t_{RTC}		0			ns
Data Access Time ($\overline{RD}$ Low to Valid Data)	t_{ACC}	Figure 1			30	ns
Bus Relinquish Time ($\overline{RD}$ High to D_ High-Z)	t_{REQ}	Figure 1	5		30	ns
CLK Rise to End-of-Conversion ($\overline{EOC}$) Rise/Fall Delay	t_{EOCD}			20		ns
CLK Rise to End-of-Last-Conversion ($\overline{EOLC}$) Fall Delay	t_{EOLCD}			20		ns
CONVST Rise to $\overline{EOLC}$ Fall Delay	$t_{CVEOLCD}$			20		ns
$\overline{EOC}$ Pulse-Width Low	t_{EOC}	Internal clock	180	200		ns
		External clock		1		CLK Cycle
Wake-Up Time From Standby				7		µs
Wake-Up Time From Shutdown		All bypass capacitors discharged		5		ns

14-Bit, 4-Channel, Software-Programmable, Multiranging, Simultaneous-Sampling ADC

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +5.0V, DRV_{DD} = +3.0V, AGND = DGND = DRGND = 0, INTCLK/$\overline{EXTCLK}$ = AGND, f_{CLK} = 5MHz, input range = ±10V, REFP2 = REFP1, REFN2 = REFN1, COM1 = COM2, 1.0nF from REFADC to AGND, 1.0µF and 0.1µF from COM1 to AGND, 0.1µF from REFP1 to AGND, 0.1µF from REFN1 to AGND, 1.0µF from REFP1 to REFN1. Typical values are at T_A = +25°C. T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{EOC}$ Fall to $\overline{RD}$ Fall Setup Time	t_{EOCRD}		0			ns
$\overline{EOLC}$ Fall to $\overline{RD}$ Fall Setup Time	t_{EOLCRD}		0			ns
Input Data Setup Time	t_{DTW}		10			ns
Input Data Hold Time	t_{WTD}		10			ns
External CLK Period	t_{CLK}		166	200		ns
External CLK High Period	t_{CLKH}	Logic sensitive to rising edges	60			ns
External CLK Low Period	t_{CLKL}	Logic sensitive to rising edges	60			ns
External Clock Frequency	f_{CLK}	(Note 4)	1		6	MHz
Internal Clock Frequency	f_{INT}		5.0	5.25	5.5	MHz
CONVST High to CLK Edge	t_{CNTC}		30			ns
Quiet Time	t_{QUIET}		600			ns

Note 1: See definition for this parameter in the *Definitions* section.
Note 2: Differential reference voltage (REFP–REFN) error nulled.
Note 3: This is the load the MAX1338 presents to an external reference at REFADC.
Note 4: Minimum CLK frequency is limited only by the internal T/H droop rate. Limit the time between the rising edge of CONVST to the falling edge of $\overline{EOLC}$ to a maximum of 0.25ms.

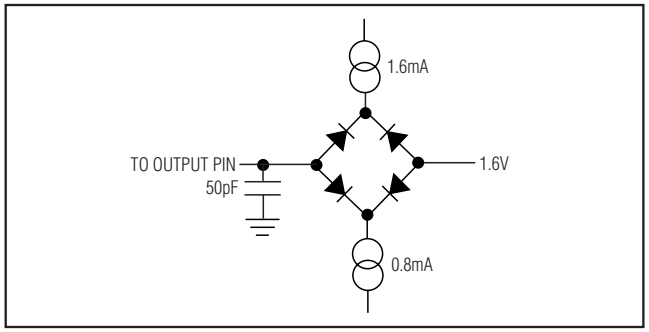


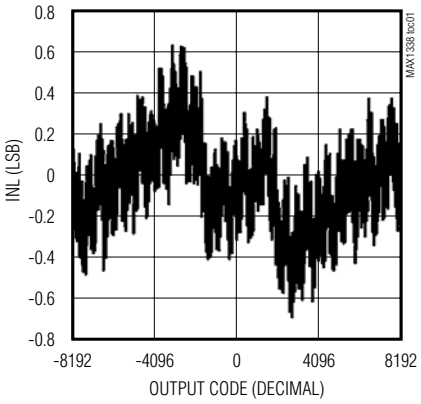
Figure 1. Load Circuit for Data Access Time and Bus-Relinquish Time

14-Bit, 4-Channel, Software-Programmable, Multiranging, Simultaneous-Sampling ADC

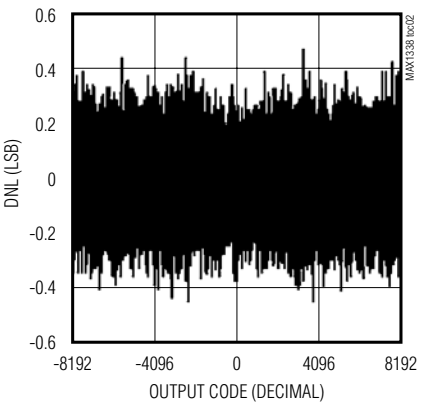
Typical Operating Characteristics

(AV_{DD} = DV_{DD} = +5.0V, DRV_{DD} = +3.0V, AGND = DGND = DRGND = 0, INTCLK/$\overline{EXTCLK}$ = AGND, f_{CLK} = 5MHz, input range = ±10V, REFP2 = REFP1, REFN2 = REFN1, COM1 = COM2, 1.0nF from REFADC to AGND, 1.0µF and 0.1µF from COM1 to AGND, 0.1µF from REFP1 to AGND, 0.1µF from REFN1 to AGND, 1.0µF from REFP1 to REFN1.)

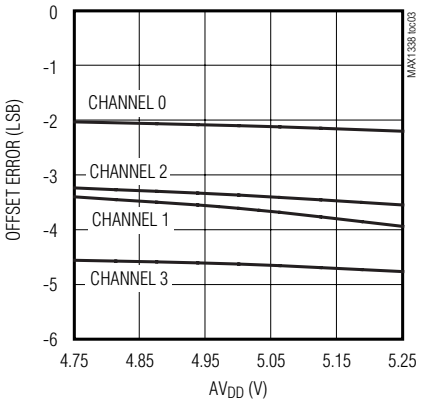
INTEGRAL NONLINEARITY vs. OUTPUT CODE



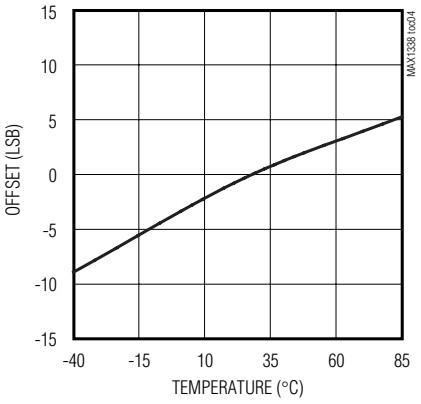
DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE



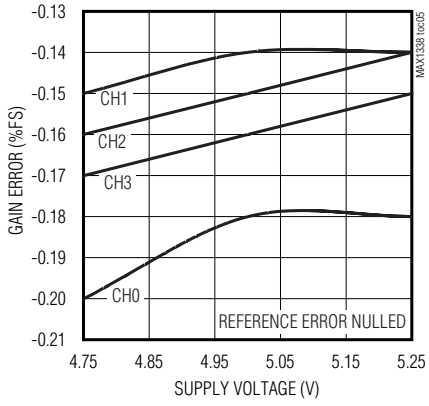
OFFSET ERROR vs. SUPPLY VOLTAGE



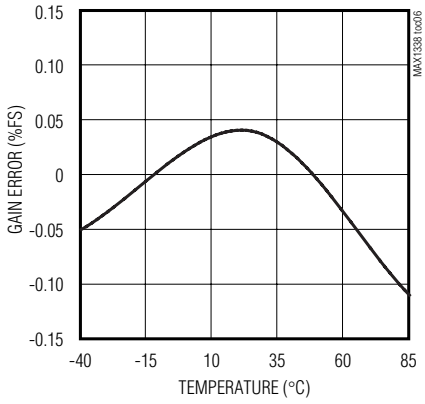
OFFSET ERROR vs. TEMPERATURE



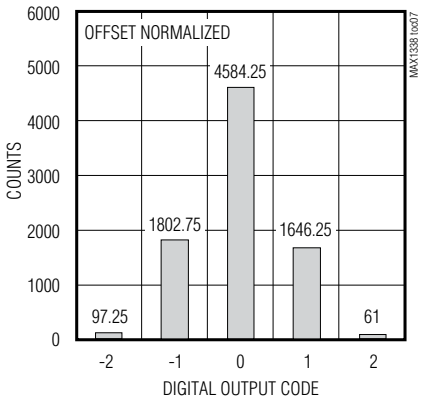
GAIN ERROR vs. SUPPLY VOLTAGE



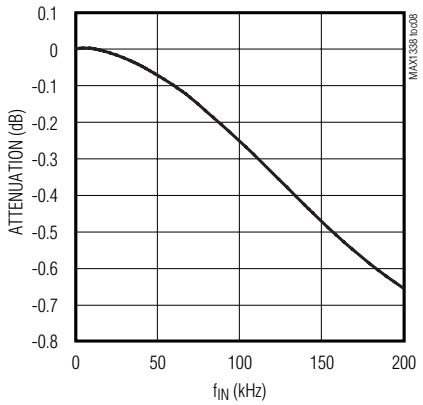
GAIN ERROR vs. TEMPERATURE



OUTPUT HISTOGRAM (DC INPUT)



ANALOG INPUT BANDWIDTH

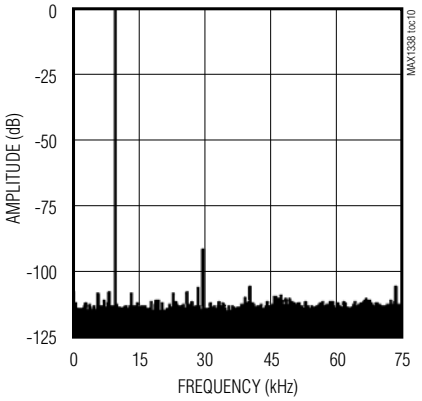


14-Bit, 4-Channel, Software-Programmable, Multiranging, Simultaneous-Sampling ADC

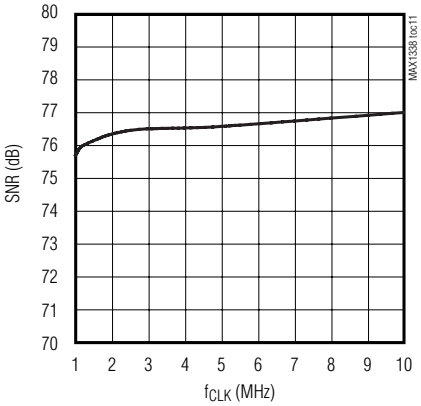
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = +5.0V, DRV_{DD} = +3.0V, AGND = DGND = DRGND = 0, INTCLK/$\overline{EXTCLK}$ = AGND, f_{CLK} = 5MHz, input range = ±10V, REFP2 = REFP1, REFN2 = REFN1, COM1 = COM2, 1.0nF from REFADC to AGND, 1.0µF and 0.1µF from COM1 to AGND, 0.1µF from REFP1 to AGND, 0.1µF from REFN1 to AGND, 1.0µF from REFP1 to REFN1.)

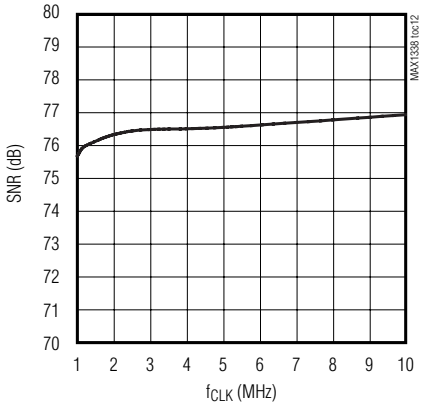
FFT AT f_{SAMPLE} = 150ksps, f_{IN} = 10kHz



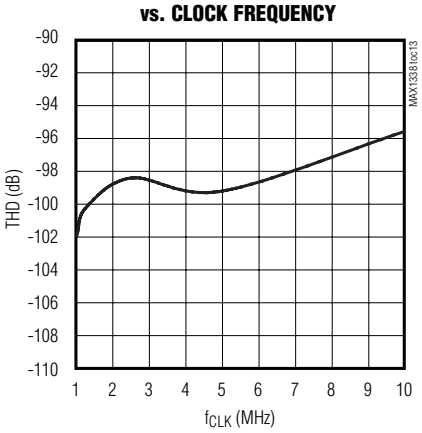
SIGNAL-TO-NOISE RATIO vs. CLOCK FREQUENCY



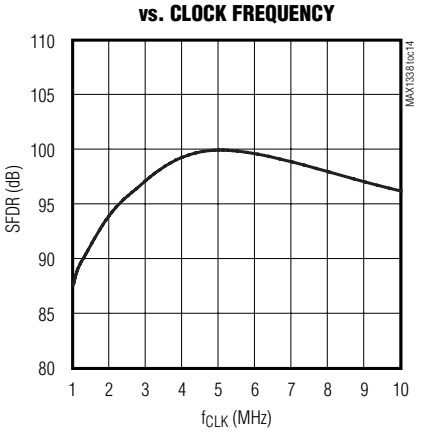
SIGNAL-TO-NOISE PLUS DISTORTION vs. CLOCK FREQUENCY



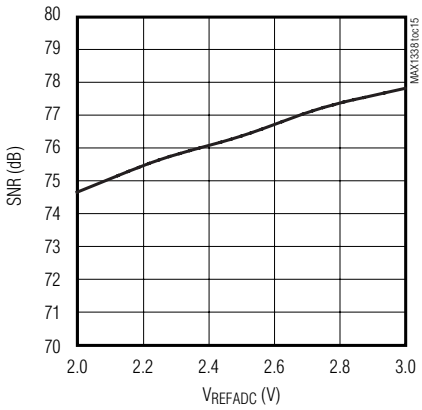
TOTAL HARMONIC DISTORTION vs. CLOCK FREQUENCY



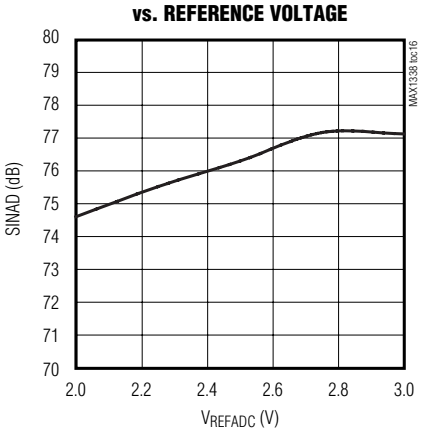
SPURIOUS-FREE DYNAMIC RANGE vs. CLOCK FREQUENCY



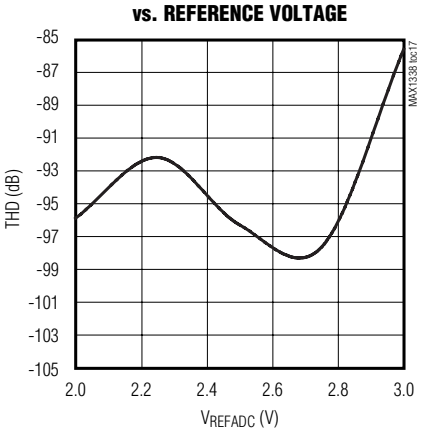
SIGNAL-TO-NOISE RATIO vs. REFERENCE VOLTAGE



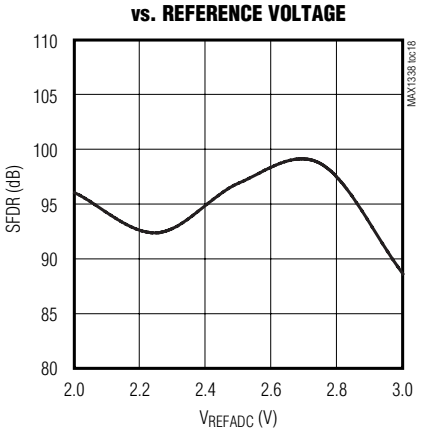
SIGNAL-TO-NOISE PLUS DISTORTION vs. REFERENCE VOLTAGE



TOTAL HARMONIC DISTORTION vs. REFERENCE VOLTAGE



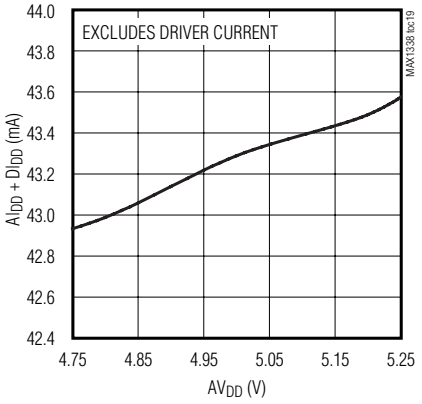
SPURIOUS-FREE DYNAMIC RANGE vs. REFERENCE VOLTAGE



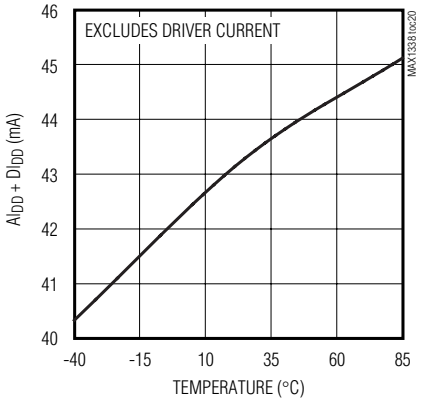
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = +5.0V, DRV_{DD} = +3.0V, AGND = DGND = DRGND = 0, INTCLK/$\overline{EXTCLK}$ = AGND, f_{CLK} = 5MHz, input range = ±10V, REFP2 = REFP1, REFN2 = REFN1, COM1 = COM2, 1.0nF from REFADC to AGND, 1.0µF and 0.1µF from COM1 to AGND, 0.1µF from REFP1 to AGND, 0.1µF from REFN1 to AGND, 1.0µF from REFP1 to REFN1.)

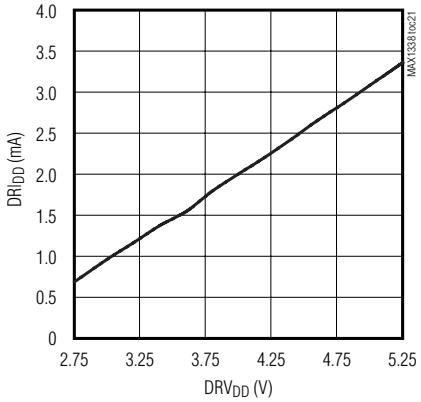
SUPPLY CURRENT vs. SUPPLY VOLTAGE



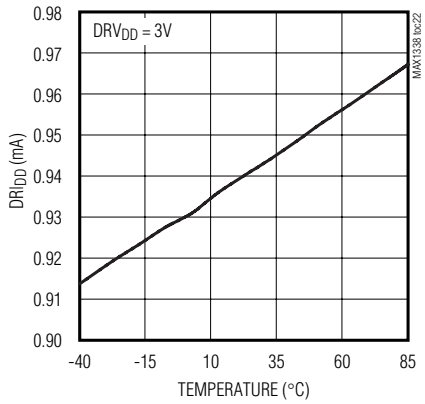
SUPPLY CURRENT vs. TEMPERATURE



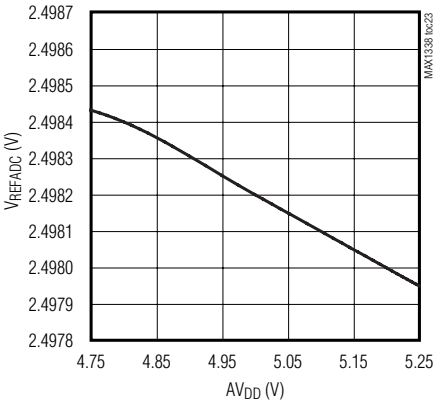
DRIVER SUPPLY CURRENT vs. SUPPLY VOLTAGE



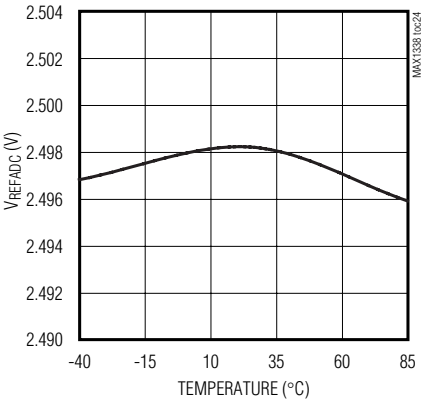
DRIVER SUPPLY CURRENT vs. TEMPERATURE



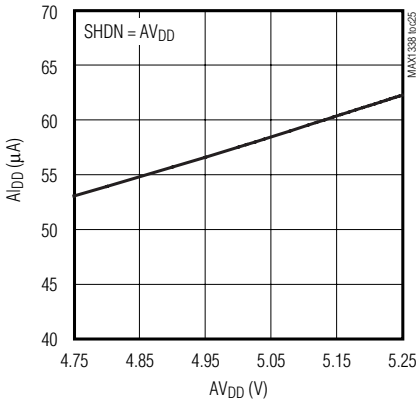
REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



REFERENCE VOLTAGE vs. TEMPERATURE



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE

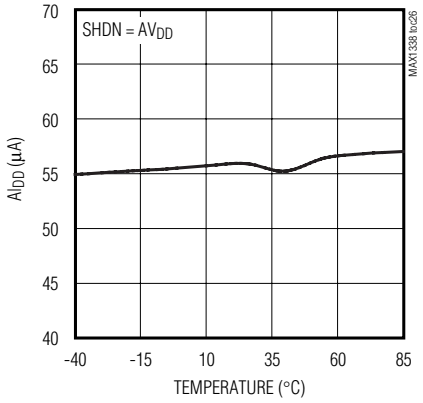


14-Bit, 4-Channel, Software-Programmable, Multiranging, Simultaneous-Sampling ADC

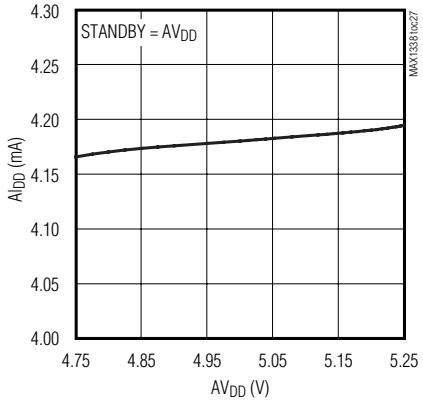
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = +5.0V, DRV_{DD} = +3.0V, AGND = DGND = DRGND = 0, INTCLK/$\overline{EXTCLK}$ = AGND, f_{CLK} = 5MHz, input range = ±10V, REFP2 = REFP1, REFN2 = REFN1, COM1 = COM2, 1.0nF from REFADC to AGND, 1.0µF and 0.1µF from COM1 to AGND, 0.1µF from REFP1 to AGND, 0.1µF from REFN1 to AGND, 1.0µF from REFP1 to REFN1.)

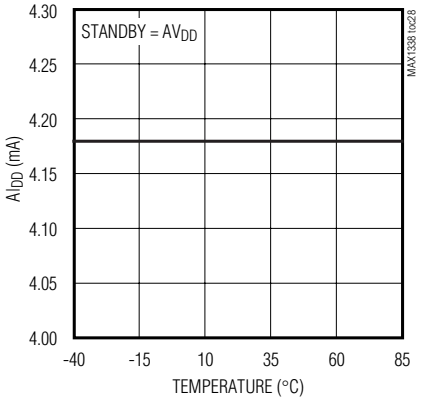
SHUTDOWN CURRENT vs. TEMPERATURE



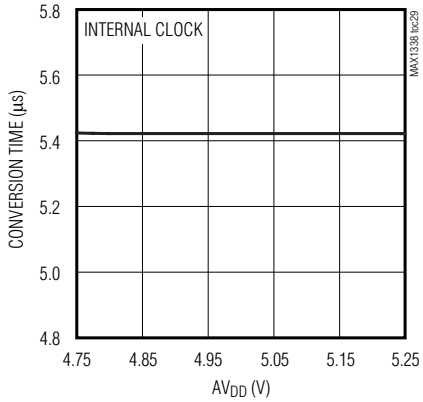
STANDBY CURRENT vs. SUPPLY VOLTAGE



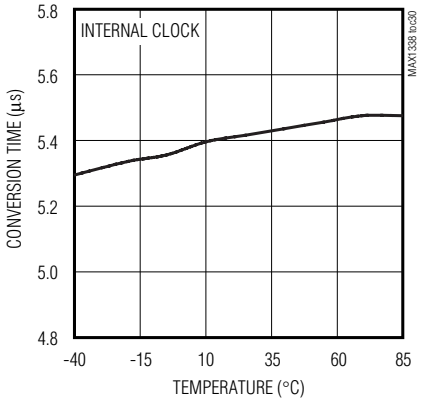
STANDBY CURRENT vs. TEMPERATURE



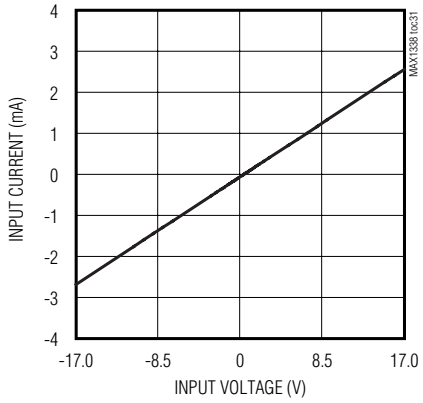
CONVERSION TIME vs. SUPPLY VOLTAGE



CONVERSION TIME vs. TEMPERATURE



ANALOG INPUT CURRENT vs. ANALOG INPUT VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1, 7, 9, 17, 19	AV_{DD}	Analog Power Input. AV_{DD} is the power input for the analog section of the converter. Connect a +4.75V to +5.25V power supply to AV_{DD}. Bypass each AV_{DD} to AGND with a 0.1µF capacitor very close to the device. Bypass AV_{DD} to AGND with a bulk capacitor of at least 4.7µF where power enters the board. Connect all AV_{DD} pins to the same potential.
2	AIN0+	Channel 0 Differential Analog Input
3	AIN0-	Channel 0 Differential Analog Input
4	AIN1+	Channel 1 Differential Analog Input
5	AIN1-	Channel 1 Differential Analog Input
6, 8, 14, 16, 18, 20, 28	AGND	Analog Ground. AGND is the power return for AV_{DD}. Connect all AGNDs to the same potential.
10	AIN2+	Channel 2 Differential Analog Input
11	AIN2-	Channel 2 Differential Analog Input
12	AIN3+	Channel 3 Differential Analog Input
13	AIN3-	Channel 3 Differential Analog Input
15	INTCLK/$\overline{EXTCLK}$	Clock-Select Input. Force INTCLK/$\overline{EXTCLK}$ high for internal clock mode. Force INTCLK/$\overline{EXTCLK}$ low for external clock mode.
21	REFADC	ADC Reference Bypass or Input. REFADC is the bypass point for an internally generated reference voltage. Bypass REFADC with a 1.0nF capacitor to AGND. REFADC can be driven externally by a precision external voltage reference. See the *Reference* section and the *Typical Operating Circuit*.
22	REFP1	Positive Differential Reference Bypass Point 1. Connect REFP1 to REFP2.
23	REFP2	Positive Differential Reference Bypass Point 2. Connect REFP2 to REFP1. Bypass REFP2 with a 0.1µF capacitor to AGND. Also bypass REFP2 to REFN2 with a 0.1µF capacitor.
24	COM1	Common-Mode Voltage Bypass Point 1. Connect COM1 to COM2.
25	COM2	Common-Mode Voltage Bypass Point 2. Connect COM2 to COM1. Connect a 1.0µF capacitor from COM2 to AGND.
26	REFN1	Negative Differential Reference Bypass Point 1. Connect REFN1 to REFN2.
27	REFN2	Negative Differential Reference Bypass Point 2. Connect REFN2 to REFN1. Bypass REFN2 with a 0.1µF capacitor to AGND. Also bypass REFN2 to REFP2 with a 0.1µF capacitor.
29	D0	Data Input/Output Bit 0 (LSB)
30	D1	Data Input/Output Bit 1
31	D2	Data Input/Output Bit 2
32	D3	Data Input/Output Bit 3
33	D4	Data Input/Output Bit 4
34	D5	Data Input/Output Bit 5
35	D6	Data Input/Output Bit 6
36	D7	Data Input/Output Bit 7
37	D8	Data Output Bit 8
38	D9	Data Output Bit 9
39	D10	Data Output Bit 10
40	D11	Data Output Bit 11

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Pin Description (continued)

PIN	NAME	FUNCTION
41	D12	Data Output Bit 12
42	D13	Data Output Bit 13 (MSB)
43	DRV_{DD}	Digital I/O Power-Supply Input. DRV_{DD} is the power input for the digital I/O buffers and drivers. Connect a +2.7V to +5.25V power supply to DRV_{DD}. Bypass DRV_{DD} to DRGND with a 0.1µF capacitor very close to the device.
44	DRGND	Driver Ground. DRGND is the power-supply return for DRV_{DD}.
45	$\overline{EOC}$	End-of-Conversion Output. $\overline{EOC}$ goes low to indicate the end of a conversion. $\overline{EOC}$ returns high after one clock period.
46	$\overline{EOLC}$	End-of-Last-Conversion Output. $\overline{EOLC}$ goes low to indicate the end of the last conversion. $\overline{EOLC}$ returns high when CONVST goes low for the next conversion sequence.
47	$\overline{RD}$	Read Input. Forcing $\overline{RD}$ low initiates a read command of the parallel data bus, D0–D13. D0–D13 are high impedance while either $\overline{RD}$ or $\overline{CS}$ is high.
48	$\overline{WR}$	Write Input. Forcing $\overline{WR}$ low initiates a write command for configuring the device through D0–D7.
49	$\overline{CS}$	Chip-Select Input. Forcing $\overline{CS}$ low activates the digital interface. D0–D13 are high impedance while either $\overline{CS}$ or $\overline{RD}$ is high.
50	CONVST	Convert Start Input. CONVST initiates the conversion process. The analog inputs are sampled on the rising edge of CONVST.
51	CLK	External-Clock Input. CLK accepts a 1MHz to 6MHz external clock signal. For externally clocked conversions, apply the clock signal to CLK and force INTCLK/$\overline{EXTCLK}$ low. For internally clocked conversions, connect CLK to DGND and force INTCLK/$\overline{EXTCLK}$ high.
52	STANDBY	Standby-Control Input. Forcing STANDBY high partially powers down the device but leaves all the reference-related circuitry alive. Use STANDBY instead of SHDN when quick wake-up is required.
53	SHDN	Shutdown-Control Input. Force SHDN high to place the device into full shutdown. When in full shutdown, all circuitry within the device is powered down and all reference capacitors are allowed to discharge. Allow 1ms for wake-up from full shutdown before starting a conversion.
54	DV_{DD}	Digital Power-Supply Input. DV_{DD} is the power input for the digital circuitry. Connect a +4.75V to +5.25V power supply to DV_{DD}. Bypass DV_{DD} to DGND with a 0.1µF capacitor very close to the device.
55, 56	DGND	Digital Ground. Power return for DV_{DD}.
—	EP	Exposed Pad. Connect to AGND.

Detailed Description

The MAX1338 simultaneously samples four differential analog inputs with internal T/H circuits, and sequentially converts them to a digital code with a 14-bit ADC. Output data is provided by a 14-bit parallel interface. At power-up, all channels default to a ±10V input range. Program different input ranges (±10V, ±5V, ±2.5V, or ±1.25V) using the configuration register. Different input ranges between ±12V and ±1.0V are realized using an external reference. All channels offer input protection to ±17V, independent of the selected input range.

The internal clock operates the ADC at 5MHz, or uses an external conversion clock from 1MHz to 6MHz. $\overline{EOC}$ goes low when the result of each conversion is available, and $\overline{EOLC}$ goes low when the last conversion result is available. Standby and shutdown modes, selectable through logic-control inputs, save power between conversions. Figure 2 shows a block diagram of the MAX1338.

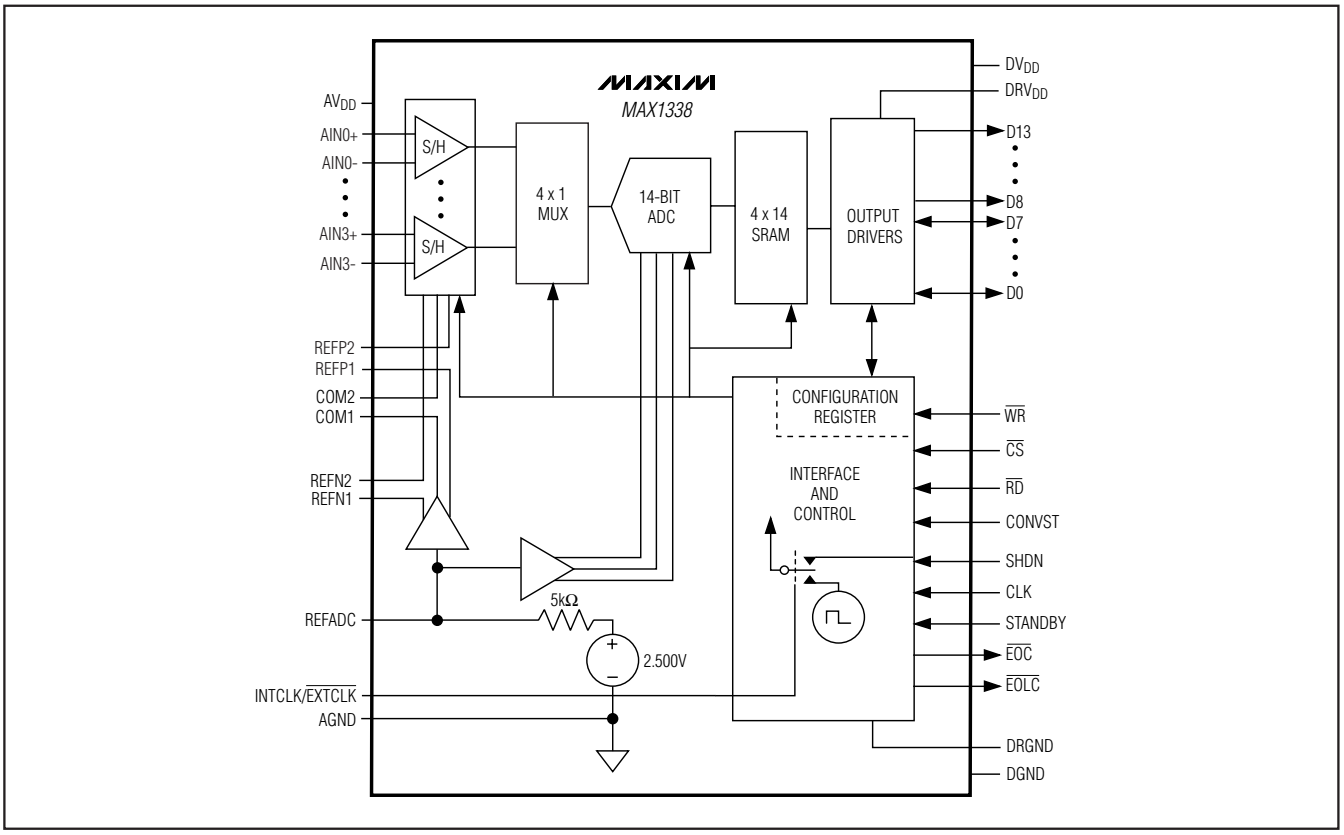

Figure 2. Functional Diagram

Power-Supply Inputs

Three separate power supplies power the MAX1338. A +5V analog supply, AV_{DD}, powers the analog input and converter sections. A +5V digital supply, DV_{DD}, powers the internal logic circuitry, and a +2.7V to +5V digital supply (DRV_{DD}), powers the parallel I/O and the control I/O (see the *Typical Operating Circuit*). Bypass the power supplies as indicated in the *Layout, Grounding, and Bypassing* section. Power-supply sequencing is not required for the MAX1338.

Analog Inputs

Software-Selectable Input Range

The MAX1338 provides four independent, software-selectable, analog input voltage ranges for each channel. The selectable input ranges are $\pm V_{REF}$ x 4 (the power-up default condition), $\pm V_{REF}$ x 2, $\pm V_{REF}$, and $\pm V_{REF}$ x 0.5. Using the 2.5V internal reference, the selectable input ranges are ±10V (power-up default), ±5V, ±2.5V, and ±1.25V. Program the analog input ranges with the configuration register through the parallel I/O. See the *Configuration Register* section for programming details.

Input Protection

Protection at the analog inputs provides ±17V fault immunity for the MAX1338. This protection circuit limits the current at the analog inputs to less than ±2mA. Input fault protection is active in standby, in shutdown, during normal operation, and over all input ranges.

Track and Hold (T/H)

To preserve relative phase information between input channels, each input channel has a dedicated T/H amplifier. The rising edge of CONVST represents the sampling instant for all channels. All samples are taken within an aperture delay (t_{AD}) of 16ns. The aperture delay of all channels is matched to within 100ps.

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Figure 3 shows the equivalent analog input T/H circuit for one analog input.

As conversion begins, the T/H circuits hold the analog signals. After the 12th clock cycle (or 2.4µs in internal clock mode) into the conversion process, the last analog input sample begins shifting through the converter, and the T/H circuits begin to track the analog inputs again in preparation for the next CONVST rising edge.

Due to the resistive load presented by the analog inputs, any significant analog input source resistance, R_{SOURCE}, increases gain error. Limit R_{SOURCE} to a maximum of 20Ω to limit the effect to less than 0.1%. Drive the input with a wideband buffer (>1MHz) that can drive the ADC's input impedance.

Selecting an Input Buffer

Most applications require an input buffer to achieve 14-bit accuracy. Although slew rate and bandwidth are important, the most critical specification is output impedance. Use a low-noise, low-distortion amplifier with low output impedance, for best gain-accuracy performance.

Input Bandwidth

The input-tracking circuitry has a 1MHz small-signal bandwidth. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Data Throughput

The data throughput (f_{TH}) of the MAX1338 is a function of the clock speed (f_{CLK}). The MAX1338 operates from a 5MHz internal clock or an external clock between 1MHz and 6MHz. For fastest throughput, read the conversion result during conversion (Figure 5), and calculate data throughput using:

$$f_{TH} = \frac{1}{t_{QUIET} + \frac{26}{f_{CLK}}}$$

where t_{QUIET} is the period of bus inactivity before the rising edge of CONVST.

Clock Modes

The MAX1338 provides an internal clock of 5MHz. Alternatively, use an external clock of 1MHz to 6MHz.

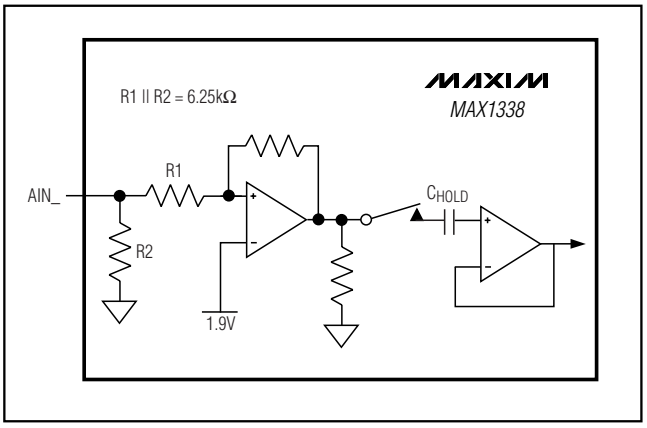

Figure 3. Simplified Typical Input Circuit

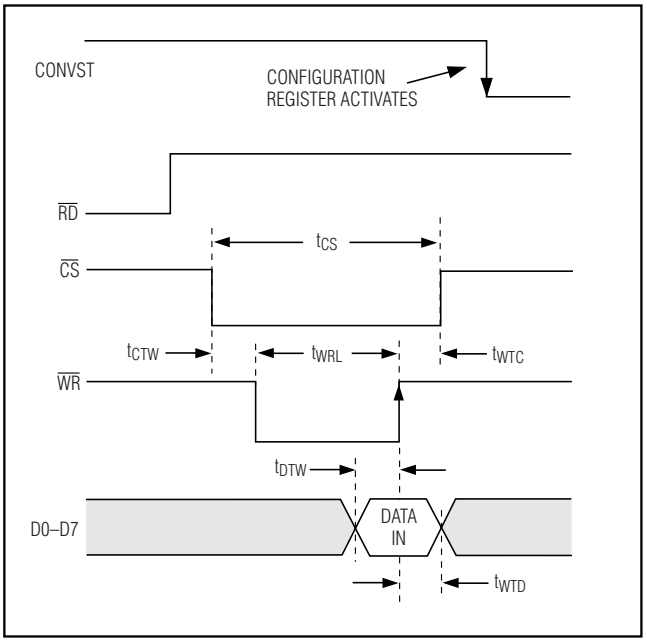

Figure 4. Write Timing

Internal Clock

Internal clock mode frees the microprocessor from the burden of running the ADC conversion clock. For internal-clock operation, connect INTCLK/$\overline{EXTCLK}$ to AV_{DD} and CLK to DRGND. Note that INTCLK/$\overline{EXTCLK}$ is referenced to the analog power supply, AV_{DD}. Total conversion time for all four channels using the internal clock is 6µs (typ).

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External Clock

For external clock operation, force INTCLK/$\overline{EXTCLK}$ low and connect an external clock source to CLK. Use an external clock frequency from 1MHz to 6MHz with a duty cycle between 40% and 60%. Choose a minimum clock frequency of 1MHz to prevent linearity errors caused by excessive droop in the T/H circuits.

Applications Sections

Power-On Reset

At power-up, all channels default to a ±10V input range. After applying power, allow a 1ms wake-up time to elapse and perform one dummy conversion before initiating first conversion.

Power Saving

Full Shutdown

During shutdown, the analog and digital circuits in the MAX1338 power down and the device draws less than 0.06mA from AV_{DD}, and less than 10µA from DV_{DD}. Select shutdown mode using the SHDN input. Force SHDN high to enter shutdown mode. When coming out of shutdown, allow the 1ms wake-up and then perform one dummy conversion before making the first conversion.

Standby

Standby is similar to shutdown but the reference circuits remain powered up, allowing faster wake-up. Enter standby by forcing STANDBY high. After coming out of standby, perform a dummy conversion before making the first conversion.

Digital Interface

The digital interface consists of two sections: a control I/O section and a parallel I/O section. The control I/O section includes the following control signals: chip select ($\overline{CS}$), read ($\overline{RD}$), write ($\overline{WR}$), end of conversion ($\overline{EOC}$), end of last conversion ($\overline{EOLC}$), convert start (CONVST), power-down (SHDN), standby (STANDBY), and external-clock input (CLK).

The bidirectional parallel I/O section sets the 8-bit input range configuration register using D0–D7 (see the *Configuration Register* section) and outputs the 14-bit conversion result using D0–D13. The I/O operations are controlled by the control I/O signals $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$. All parallel I/O bits are high impedance when either $\overline{RD}$ = 1 or $\overline{CS}$ = 1. Figures 4, 5, and 6 and the *Timing Characteristics* section detail the operation of the digital interface.

Table 1. Configuration Register

I/O LINE	REGISTER NAME	FUNCTION
D0	CH0R0	Channel 0 input range setting bit 0
D1	CH0R1	Channel 0 input range setting bit 1
D2	CH1R0	Channel 1 input range setting bit 0
D3	CH1R1	Channel 1 input range setting bit 1
D4	CH2R0	Channel 2 input range setting bit 0
D5	CH2R1	Channel 2 input range setting bit 1
D6	CH3R0	Channel 3 input range setting bit 0
D7	CH3R1	Channel 3 input range setting bit 1

Table 2. Input-Range Register Settings

REGISTER SETTING		SELECTED INPUT RANGE	ALLOWABLE COMMON-MODE RANGE
CH_R0	CH_R1		
0	0	-10V to +10V	±5V
0	1	-5V to +5V	±2.5V
1	0	-2.5V to +2.5V	±1.25V
1	1	-1.25V to +1.25V	±0.625V

Configuration Register

The MAX1338 uses an 8-bit configuration word to set the input range for each channel. Table 1 and Table 2 describe the configuration word and the input-range settings.

Write to the configuration register by forcing $\overline{CS}$ and $\overline{WR}$ low, loading bits D0–D7 onto the parallel bus, and then forcing $\overline{WR}$ high. The configuration bits are latched on the rising edge of $\overline{WR}$ (Figure 4). It is possible to write to the configuration register at any point during the conversion sequence. However, it will not be active until the next convert-start signal. At power-up, the configuration register contains all zeros, making all channels default to the maximum input range, -10V to +10V. Shutdown and standby do not change the configuration register, but the configuration register can be programmed while the MAX1338 is in shutdown or standby modes.

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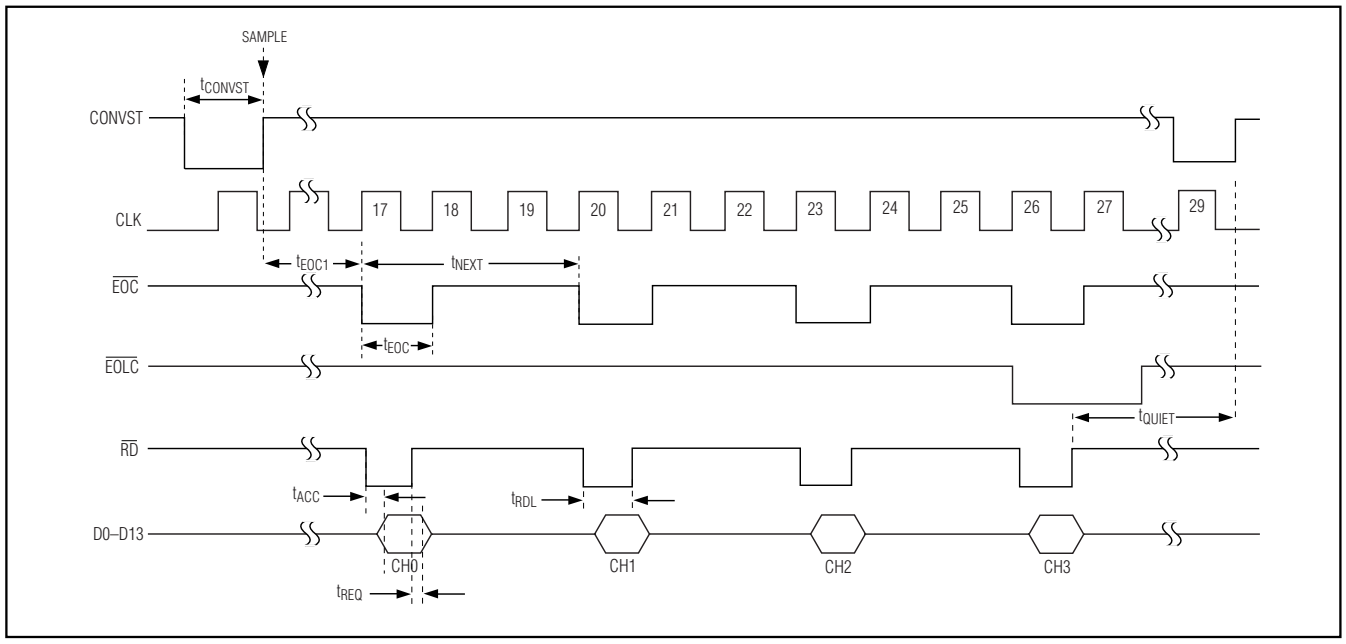

Figure 5. Reading During a Conversion—Internal or External Clock

Starting a Conversion

Internal Clock

For internal clock operation, force INTCLK/EXTCLK high. To start a conversion using internal clock mode, pull CONVST low for at least t_{CONVST}. The T/H acquires the signal while CONVST is low. An EOC signal pulses low when the first result becomes available, and for each subsequent result until the end of the conversion cycle. The EOLC signal goes low when the last conversion result becomes available (Figure 6).

External Clock

For external clock operation, force INTCLK/EXTCLK low. To start a conversion using external clock mode, pull CONVST low for at least t_{CONVST}. The T/H circuits track the input signal while CONVST is low. Conversion begins on the rising edge of CONVST. Apply an external clock to CLK. To avoid T/H droop degrading the sampled analog input signals, the first CLK pulse must occur within 10µs after the rising edge of CONVST and have a minimum 1MHz clock frequency. The first conversion result is available for read on the rising edge of the 17th clock cycle, and subsequent conversions on every 3rd clock cycle thereafter, as indicated by EOC and EOLC.

Reading a Conversion Result

Reading During a Conversion

Figure 5 shows the interface signals to initiate a read operation during a conversion cycle. CS can be held low permanently, low during the RD cycles, or it can be the same as RD. After initiating a conversion by bringing CONVST high, wait for EOC to go low (about 3.4µs in internal clock mode) or 17 clock cycles (external clock mode) before reading the first conversion result. Read the conversion result by bringing RD low, which latches the data to the parallel digital output bus. Bring RD high to release the digital bus. Wait for the next falling edge of EOC (about 600ns in internal clock mode or three clock cycles in external clock mode) before reading the next result. When the last result is available, EOLC goes low, along with EOC. Wait three clock cycles, t_{QUIET}, before starting the next conversion cycle.

Reading After a Conversion

Figure 6 shows the interface signals for a read operation after a conversion using an external clock. At the falling of EOLC, on the 26th clock pulse after the initiation of a conversion, driving CS and RD low places the first conversion result onto the parallel I/O bus. Read the conversion result on the rising edge of RD. Successive low pulses of RD place the successive conversion results

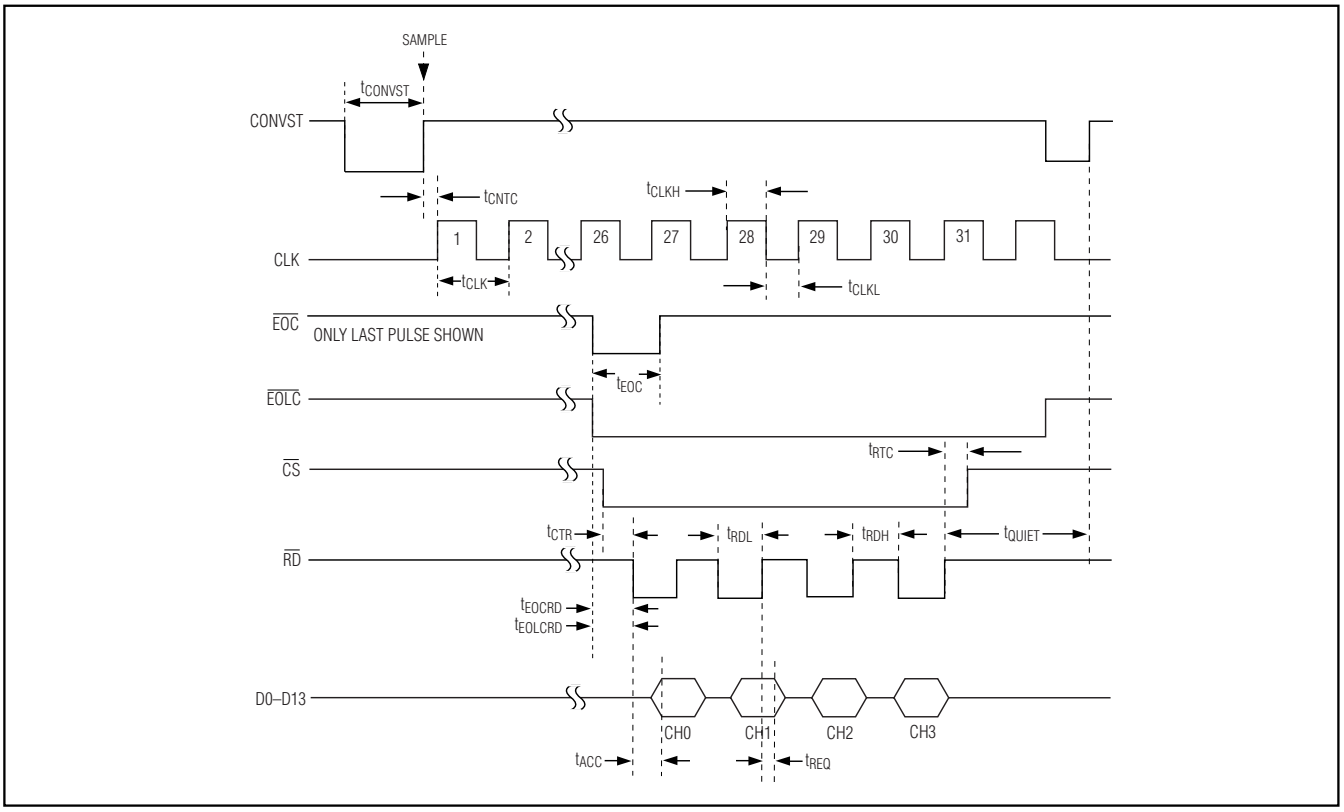

Figure 6. Reading After a Conversion—External Clock

onto the bus. After reading all four channels, bring $\overline{CS}$ high to release the parallel I/O. After waiting t_{QUIET}, pulse CONVST low to initiate the next conversion.

Reference

Bypass the reference inputs as indicated in Table 3.

Internal Reference

The internal reference supports all input ranges for the MAX1338.

External Reference

Implement external-reference operation by overdriving the internal reference voltage. Override the internal reference voltage by connecting a 2.0V to 3.0V external reference at REF. The REF input impedance is typically 5kΩ. For more information about using an external reference, see the *Transfer Functions* section.

Table 3. Reference Bypass Capacitors

LOCATION	BYPASS CAPACITORS
REFADC bypass capacitor to AGND	1nF
REFP1 bypass capacitor to AGND	0.1µF
REFN1 bypass capacitor to AGND	0.1µF
REFP1 to REFN1 capacitor	1.0µF
COM1 bypass capacitor to AGND	1.0µF ll 0.1µF

Transfer Functions

Digital Correction

Factory trim procedures digitally shift the transfer function to reduce bipolar zero-code offset to less than ±4 LSBs (typ). Depending on initial conditions, the transfer function is shifted up or down, as required. The maximum shift that any transfer function experiences is 64 codes, which can have a small effect at the extremes of the transfer function, as shown in Figure 7.

14-Bit, 4-Channel, Software-Programmable, Multiranging, Simultaneous-Sampling ADC

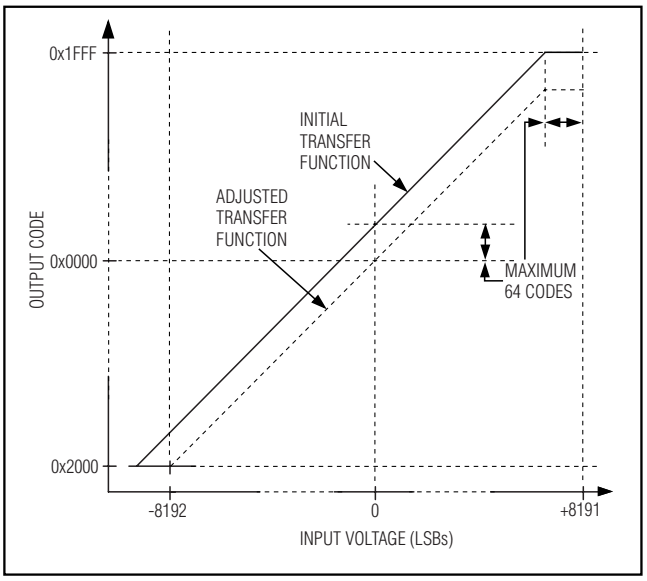

Figure 7. Example of Digitally Adjusted Transfer Function—Shifted Down to Minimize Zero-Code Offset

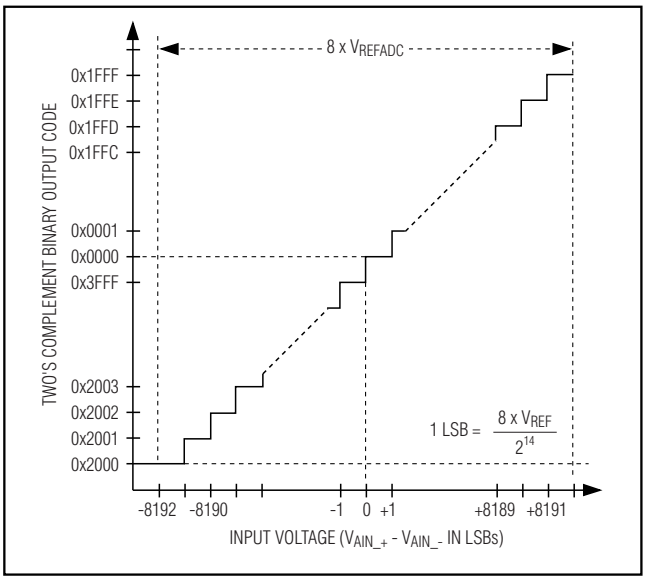

Figure 8. ±10V Transfer Function

Input Range Settings

Table 4 shows the two's complement output for a selection of inputs.

The full-scale input range (FSR) depends on the selected range, and the voltage at REF, as shown in Table 5. Also shown in Table 5 are the allowable common-mode ranges for the differential inputs.

Calculate the LSB size using:

$$1\,LSB = \frac{A \times V_{REFADC}}{2^{14}}$$

where A = gain multiplier for the selected input range, from Table 6.

Determine the input voltage as a function of V_{REF}, and the output code using:

$$V_{AIN\_+} - V_{AIN\_-} = V_{REFADC} \times A \times \frac{CODE}{2^{14}}$$

where A = gain multiplier for the selected input range, from Table 6.

Figures 8, 9, 10, and 11 show the transfer functions for the four selectable input ranges.

Applications Information

Layout, Grounding, and Bypassing

For best performance, the board layout must follow some simple guidelines. Separate the control I/O and parallel I/O signals from the analog signals, and run the clock signals separate from everything. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package. Run the parallel I/O signals together as a bundle.

The MAX1338 has an exposed underside pad for a low-inductance ground connection and low thermal resistance. Connect the exposed pad to the circuit board ground plane. Figure 12 shows the recommended system ground connections. Establish an analog ground point at AGND and a digital ground point at DGND. Connect all analog grounds to the analog ground point. Connect all digital grounds to the digital ground point. For lowest noise operation, make the power-supply ground returns as low impedance and as short as possible. Connect the analog ground point to the digital ground point at one location.

High-frequency noise in the power supplies degrades the ADC's performance. Bypass AV_{DD} to AGND with a parallel combination of 0.1µF and 2.2µF capacitors, bypass DV_{DD} to DGND with a parallel combination of 0.1µF and 2.2µF capacitors, and bypass DRV_{DD} to DRGND with a parallel combination of 0.1µF and 2.2µF capacitors. If the supply is very noisy use a ferrite bead as a lowpass filter, as shown in Figure 12.

Table 4. Code Table with V_{REF} = 2.500V

INPUT VOLTAGE (V)				DECIMAL EQUIVALENT OUTPUT ($CODE_{10}$)	TWO'S COMPLEMENT BINARY OUTPUT CODE
±10V INPUT RANGE SELECTED	±5V INPUT RANGE SELECTED	±2.5V INPUT RANGE SELECTED	±1.25V INPUT RANGE SELECTED		
9.9988	4.9994	2.4998	1.2499	8191	01 1111 1111 1111 → 0x1FFF
9.9976	4.9988	2.4997	1.2498	8190	01 1111 1111 1110 → 0x1FFE
0.0012	0.0006	0.0002	0.0001	1	00 0000 0000 0001 → 0x0001
0	0	0	0	0	00 0000 0000 0000 → 0x0000
-0.0012	-0.0006	-0.0002	-0.0001	-1	11 1111 1111 1111 → 0x3FFF
-9.9988	-4.9994	-2.4998	-1.2499	-8191	10 0000 0000 0001 → 0x2001
-10.0000	-5.0000	-2.5000	-1.2500	-8192	10 0000 0000 0000 → 0x2000

Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. For these devices, this straight line is a line drawn between the endpoints of the transfer function, once offset and gain errors have been nulled.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1 LSB. For these devices, the DNL of each digital output code is measured and the worst-case value is reported in the *Electrical Characteristics* table. A DNL error specification of less than ±1 LSB guarantees no missing codes and a monotonic transfer function.

Offset Error

Offset error indicates how well the actual transfer function matches the ideal transfer function at a single point. Typically, the point at which the offset error is specified is at or near the zero scale of the transfer function or at or near the midscale of the transfer function.

For the MAX1338, the ideal zero-scale digital output transition from 0x3FFF to 0x0000 occurs with an analog input voltage of zero. Offset error is the amount of analog input-voltage deviation between the measured input voltage and the calculated input voltage at the zero-scale transition.

Table 5. Input Ranges

SELECTED INPUT RANGE (V)	V_{REFADC} (V)	FULL-SCALE INPUT RANGE (V)	ALLOWABLE COMMON-MODE RANGE (V)
±10	2.0	±8	±5
	2.5	±10	±5
	3.0	±12	±5
±5	2.0	±4	±2.5
	2.5	±5	±2.5
	3.0	±6	±2.5
±2.5	2.0	±2	±1.25
	2.5	±2.5	±1.25
	3.0	±3	±1.25
±1.25	2.0	±1	±0.625
	2.5	±1.25	±0.625
	3.0	±1.5	±0.625

Table 6. LSB Size with V_{REF} = 2.500V

SELECTED INPUT RANGE (V)	GAIN MULTIPLIER (A)	LSB SIZE (mV)
±10	8	1.2207
±5	4	0.6104
±2.5	2	0.1526
±1.25	1	0.0736

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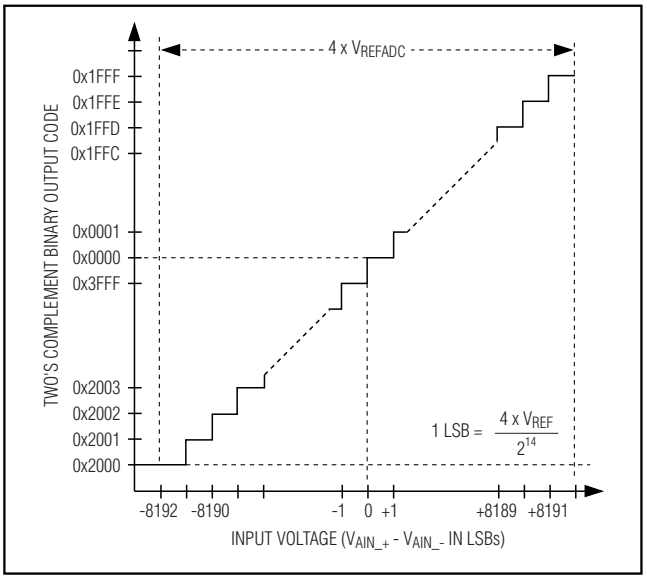


Figure 9. ±5V Transfer Function

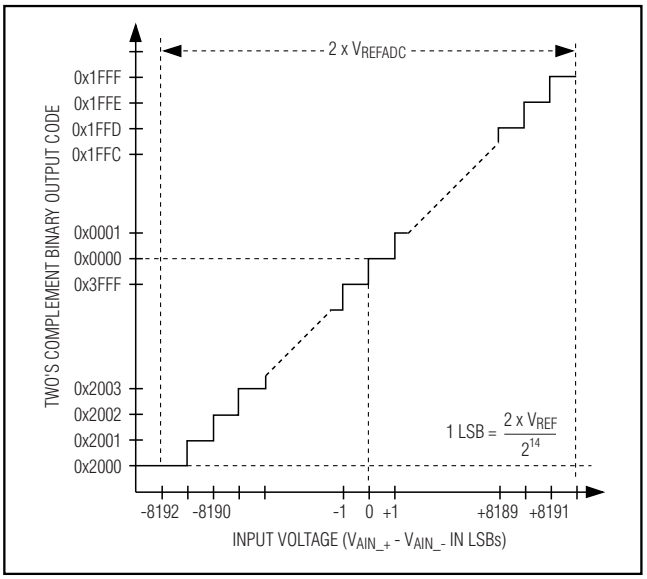


Figure 10. ±2.5V Transfer Function

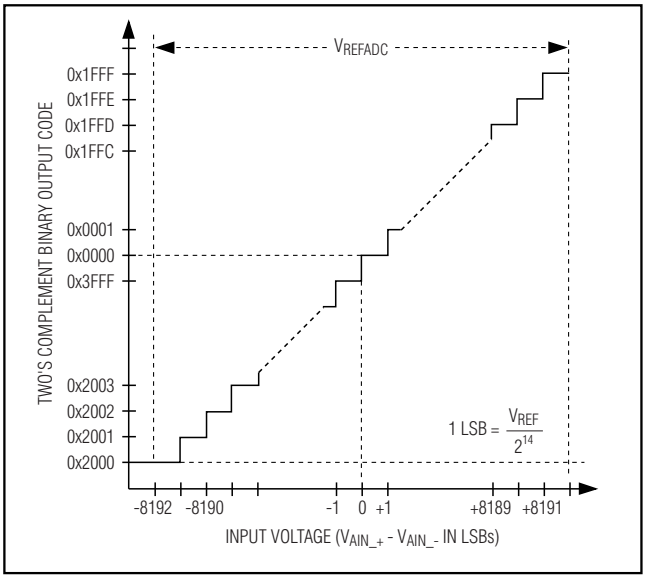


Figure 11. ±1.25V Transfer Function

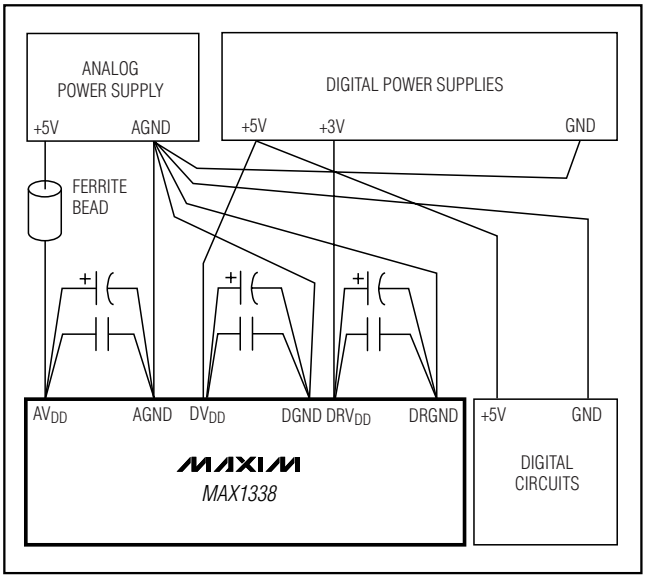


Figure 12. Power-Supply Grounding and Bypassing

Gain Error

Gain error indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. For the MAX1338, the gain error is the difference between the measured positive full-scale and negative full-scale transition points minus the difference between the ideal positive full-scale and negative full-scale bipolar transition points.

Signal-to-Noise Ratio (SNR)

SNR is a measure of the converter's noise characteristics. For a waveform perfectly reconstructed from digital samples, SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization noise error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

where N = 14 bits. In reality, there are other noise sources such as thermal noise, reference noise, and clock jitter. SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD indicates the converter's noise and distortion performance.

SINAD is computed by taking the ratio of the RMS signal to the RMS noise plus distortion. RMS noise plus distortion includes all spectral components to the Nyquist frequency excluding the fundamental and the DC offset.

$$SINAD(dB) = 20 \times \log\left[\frac{SIGNAL_{RMS}}{(NOISE + DISTORTION)_{RMS}}\right]$$

Effective Number of Bits (ENOB)

ENOB specifies the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB for a full-scale sinusoidal input waveform is computed from:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion (THD)

THD is a dynamic indication of how much harmonic distortion the converter adds to the signal.

THD is the ratio of the RMS sum of the first five harmonics of the fundamental signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}\right)$$

where V_1 is the fundamental amplitude and V_2–V_6 are the amplitudes of the 2nd- through 6th-order harmonics.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset. SFDR is specified in decibels relative to the carrier (dBc).

Aperture Delay

Aperture delay (t_{AD}) is the time delay from the sampling clock edge to the instant when an actual sample is taken.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in aperture delay.

Channel-to-Channel Isolation

Channel-to-channel isolation indicates how well each analog input is isolated from the others. The channel-to-channel isolation for the MAX1338 is measured by applying a DC -0.5dBFS sine wave to the ON channel while a high frequency 10kHz -0.5dBFS sine wave is applied to all OFF channels. An FFT is taken for the ON channel. From the FFT data, channel-to-channel crosstalk is expressed in dB as the power ratio of the DC signal applied to the ON channel and the high-frequency crosstalk signal from the OFF channels.

Power-Supply Rejection (PSRR)

PSRR is defined as the shift in gain error when the analog power supply is changed from 4.75V to 5.25V.

Small-Signal Bandwidth

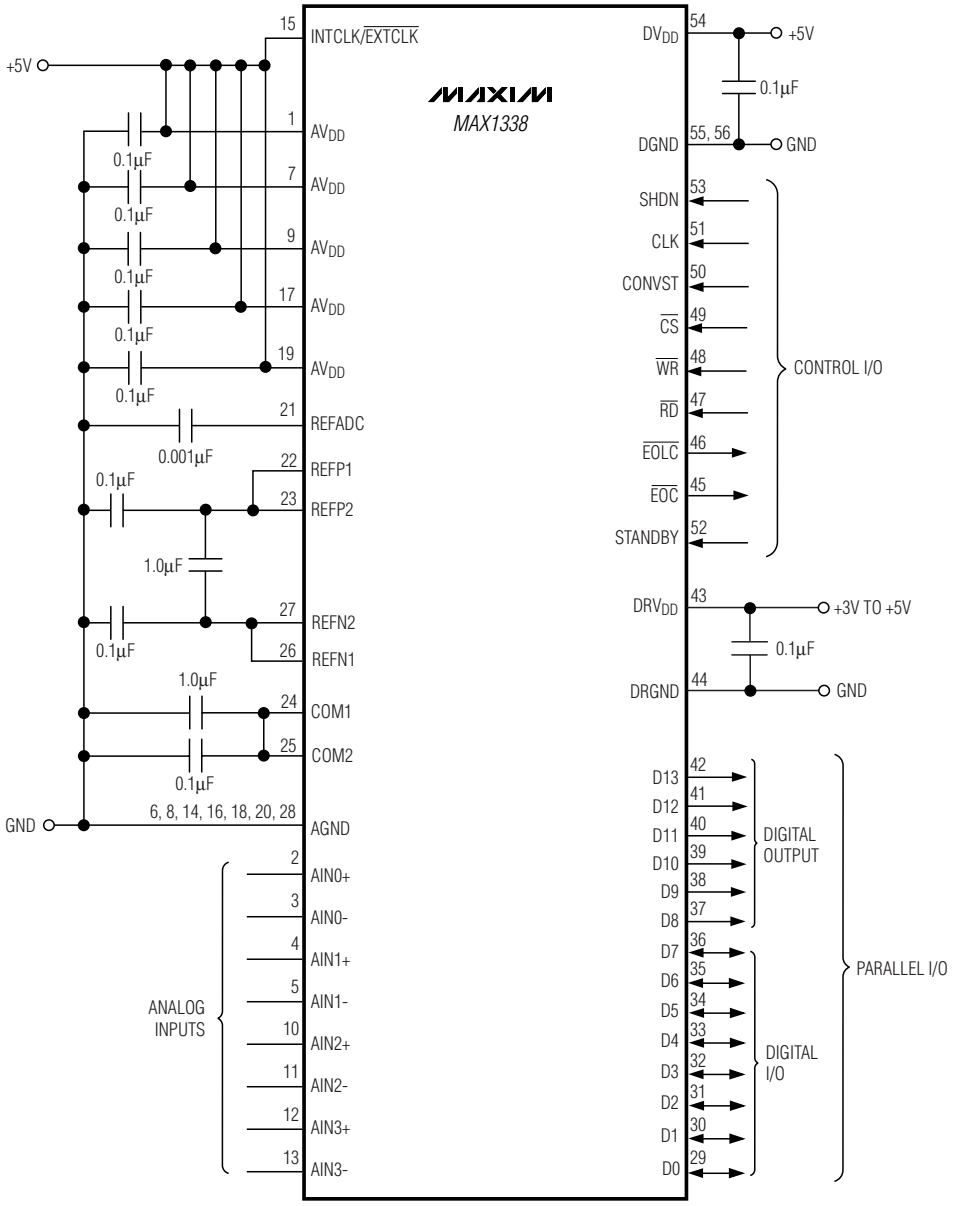
A -20dBFS sine wave is applied to the MAX1338 input. The frequency is increased until the amplitude of the digitized conversion result decreases 3dB.

Full-Power Bandwidth

A -0.5dBFS sine wave is applied to the MAX1338 input. The frequency is increased until the amplitude of the digitized conversion result decreases 3dB.

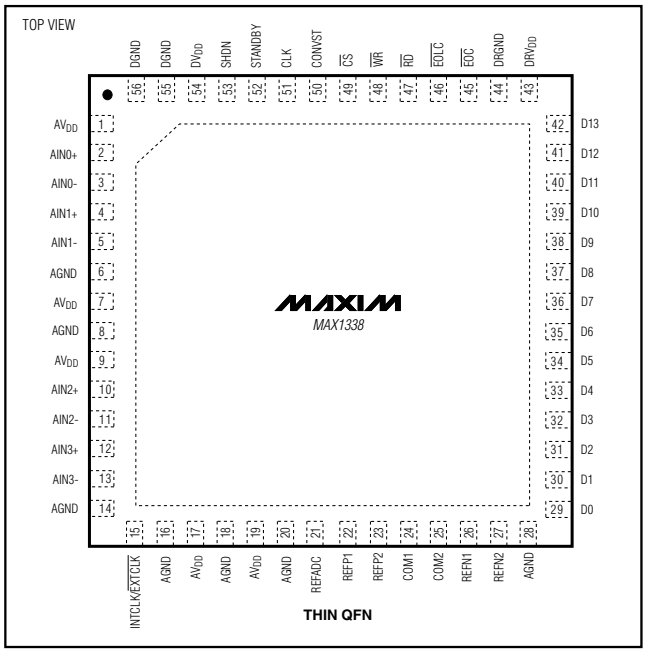
14-Bit, 4-Channel, Software-Programmable, Multiranging, Simultaneous-Sampling ADC

Typical Operating Circuit



14-Bit, 4-Channel, Software-Programmable, Multiranging, Simultaneous-Sampling ADC

Pin Configuration



Chip Information

TRANSISTOR COUNT: 27,000

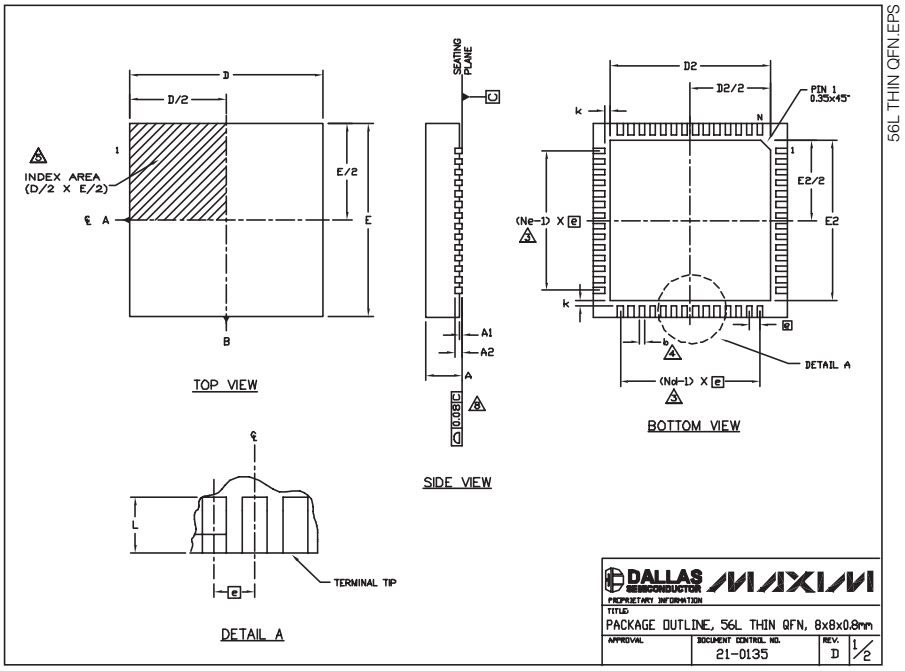
PROCESS: BiCMOS

EXPOSED PAD: Connect to AGND

14-Bit, 4-Channel, Software-Programmable, Multiranging, Simultaneous-Sampling ADC

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.225mm MAXIMUM (0.009 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE WITHIN HATCHED AREA AS SHOWN.
   EITHER AN INDENTATION MARK OR INK/LASER MARK IS ACCEPTABLE.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. PACKAGE WARPAGE MAX 0.01mm.
8. APPLIES TO EXPOSED PAD AND TERMINALS.
   EXCLUDES INTERNAL DIMENSION OF EXPOSED PAD.
9. MEETS JEDEC MO220.

SYMBOL	56L 8x8			NOTE
	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	
b	0.20	0.25	0.30	4
D	7.90	8.00	8.10	
E	7.90	8.00	8.10	
e	0.50 BSC			
N	56			3
Nd	14			3
Ne	14			3
L	0.30	0.40	0.50	
A1	0.00	0.02	0.05	
A2	0.20 REF			
k	0.25	--	--	

PKG. CODE	EXPOSED PAD VARIATION						JEDEC	DOWN BONDS ALLOWED
	D2			E2				
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T5688-1	6.50	6.65	6.70	6.50	6.65	6.70	WLLD-5	NO
T5688-2	6.50	6.65	6.70	6.50	6.65	6.70	WLLD-5	YES
T5688-3	6.50	6.65	6.70	6.50	6.65	6.70	WLLD-5	NO

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 56L THIN QFN, 8x8x0.8mm
APPROVAL | DOCUMENT CONTROL NO. 21-0135 | REV. D | 2/2

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