Agilent Technologies
Innovating the HP Way

PLL Frequency Synthesizer

Technical Data

HPLL-8001

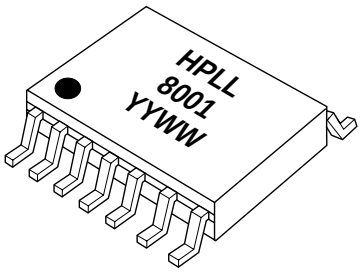
Features

- **Low Operating Current Consumption (4 mA, typ.)**
- **High Input Sensitivity, High Input Frequencies (50 MHz)**
- **Synchronous Programming of the Counters (n-, n/a-, r-counters)**
- **Switchable Modulus Trigger Edge**
- **Large Dividing Ratios for Small Channel Spacing, A counter 0 to 127, N counter 3 to 16,380, R counter 3 to 65,535**
- **Serial Control 3-wire Bus: Data, Clock (<10 MHz), Enable**
- **Switchable Polarity and Programmable Phase Detector Current**
- **2 Programmable Outputs**
- **Digital Phase Detector Output Signals (e.g. for External Charge Pump)**
- **DRFI, DVFI Outputs (e.g. for Prescaler Standby)**
- **Lock Detect Output with Gated Anti-backlash Pulse (quasi digital lock detect)**

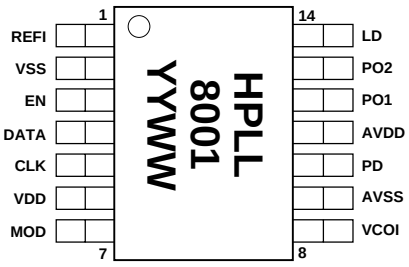
Applications

- **GSM Handsets and Base Stations**
- **PCS/PCN**
- **DECT**
- **Wireless LAN**

Plastic SOP-14



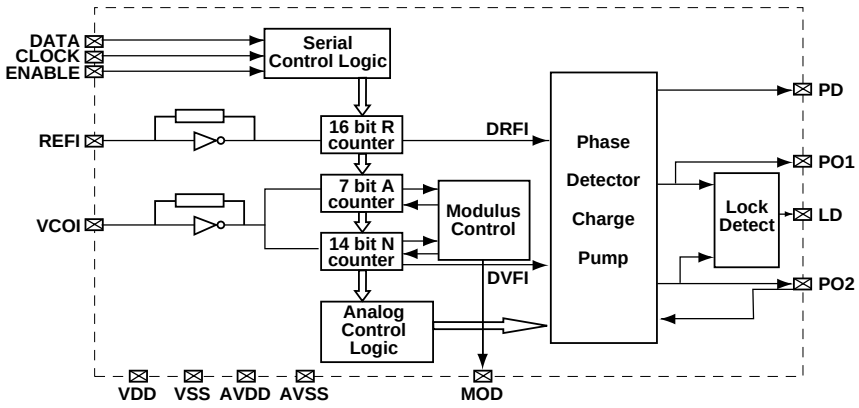
Pin Configuration



Description

The HPLL-8001 is a phase-locked loop (PLL) frequency synthesizer intended for use in a frequency generation loop with an external dual modulus prescaler and VCO. The VCO frequency is divided by the dual modulus prescaler, which is then fed to the internal A and N counters. The reference frequency is fed to an internal R counter to define the channel spacing. Both frequencies are compared in the phase detector which drives the charge pump. A lock detect is provided to monitor the lock state of the loop. All blocks are programmed by a serial 3-wire bus interface.

Functional Block Diagram



HPLL-8001 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum
V_{CC}	Supply Voltage	V	7
P_T	Power Dissipation [2, 3]	mW	400
P_{in}	RF Input Power	dBm	+15
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Recommended operating range of V_{cc} = 2.7 to 5.5V, T_a = -40 to +85°C.

Thermal Resistance[2]:
θ_{jc} = 150°C/W

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{case} = 25°C.
3. Derate at 7 mW/°C for T_{case} > 90°C.

HPLL-8001 Summary Characterization Information

Standard test conditions apply unless otherwise noted.

Current Consumption			
Symbol	**Parameters and Test Conditions**	**Units**	**Typ.**
I_S	Current Consumption[1] @ V_{DD} = 4.5 – 5.5 V	mA	6.8
	@ V_{DD} = 2.7 – 3.0 V	mA	3.1
	Standby	µA	0.06

Note:
1. F_{VF} = 50 MHz, V_{VF} = 150 mVrms, F_{RF} = 50 MHz, V_{RF} = 150 mVrms, I_{PD} = 0.250 mA, I_{REF} = 100 µA

VCO Input Frequency (pin 8), Reference Input Frequency (pin 1)

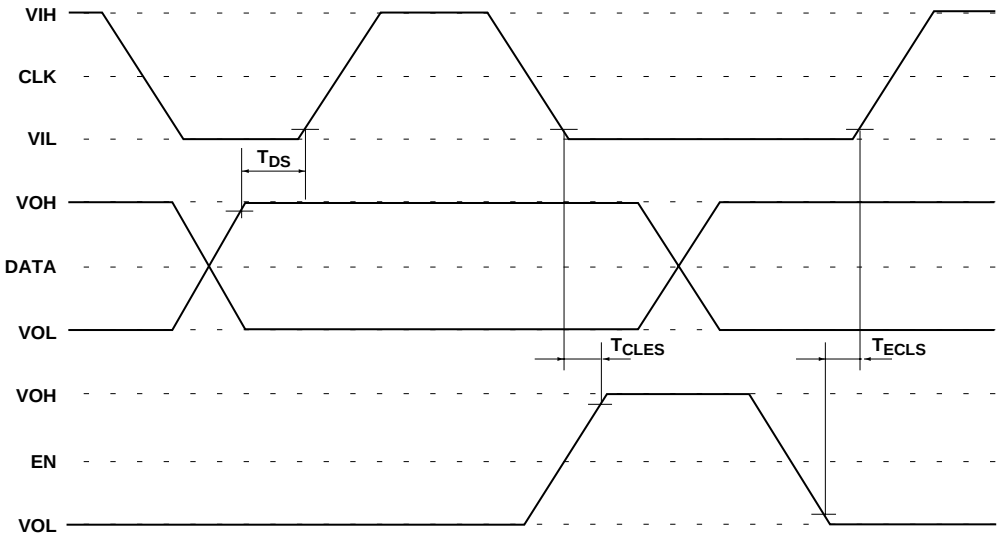
Symbol	Parameters and Test Conditions			Units	Typ.
F_{REFI}	Reference Frequency Range	V_{REFI} = 100 mVrms	V_{DD} = 4.5 V	MHz	4 - 60
		V_{REFI} = 100 mVrms	V_{DD} = 2.7 V	MHz	4 - 30
F_{VCOI}	Oscillator Frequency Range[2]				
	Dual Mode	V_{VCOI} = 200 mVrms	V_{DD} = 4.5 V	MHz	4 - 65
		V_{VCOI} = 200 mVrms	V_{DD} = 2.7 V	MHz	4 - 30
	Single HF Mode	V_{VCOI} = 200 mVrms	V_{DD} = 4.5 V	MHz	4 - 160
		V_{VCOI} = 200 mVrms	V_{DD} = 2.7 V	MHz	4 - 100
	Single LF Mode	V_{VCOI} = 100 mVrms	V_{DD} = 4.5 V	MHz	4 - 90
		V_{VCOI} = 100 mVrms	V_{DD} = 2.7 V	MHz	4 - 35

Note:
2. Minimum Slew Rate = 4 V/ms, Input Capacitance = 4 pF
Input Current low = 150 µA, Input Current high = 150 µA

Inputs EN (pin 3), Data (pin 4), CLK (pin 5)

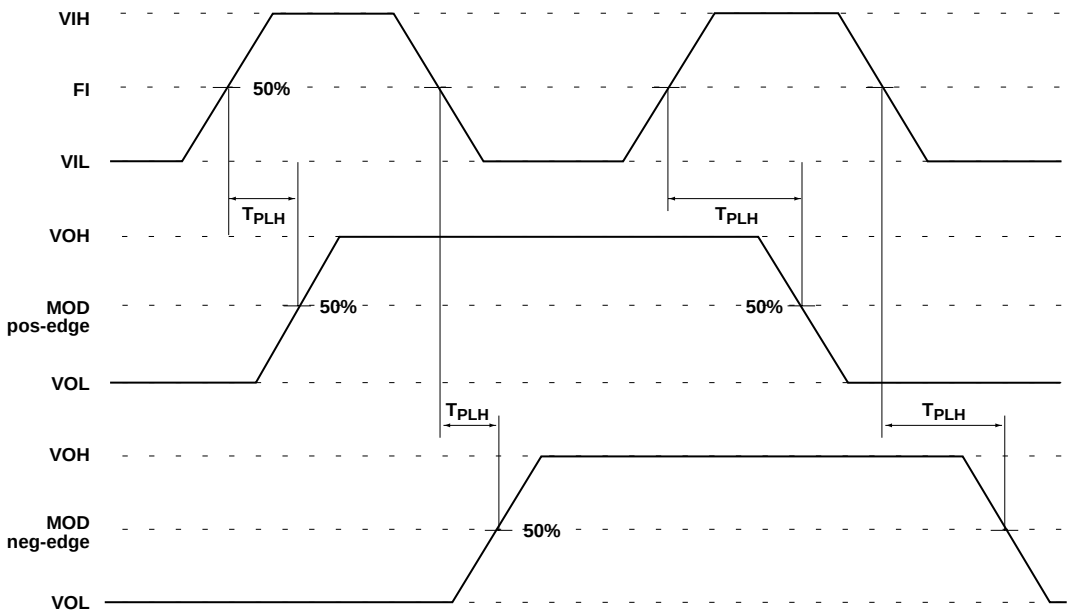
Symbol	Parameters and Test Conditions	Units	Min	Typ	Max
V_{IL}	Voltage Input Low at I_{IL} = 10 µA	V			$0.3V_{DD}$
V_{IH}	Voltage Input High at I_{IH} = 100 µA	V	$0.7V_{DD}$		
F_{CLK}	Clock Frequency	MHz			10
T_R , T_F	Rise and Fall Time of CLK	µs			1
T_{CLW}	CLK Pulse Width (high)	ns			60
T_{DS}	Data Setup Time	ns			20
T_{CLES}	CLK-Enable Setup Time	ns			20
T_{ECLS}	Enable-CLK Setup Time	ns			20
T_{ENW}	EN Pulse Width (high)	ns			60
	Propagation Delay Time (Enable - Port 1)	µs			1

Note:
These values are valid under the following conditions: V_{DD} = 2.7 to 5.5 V.



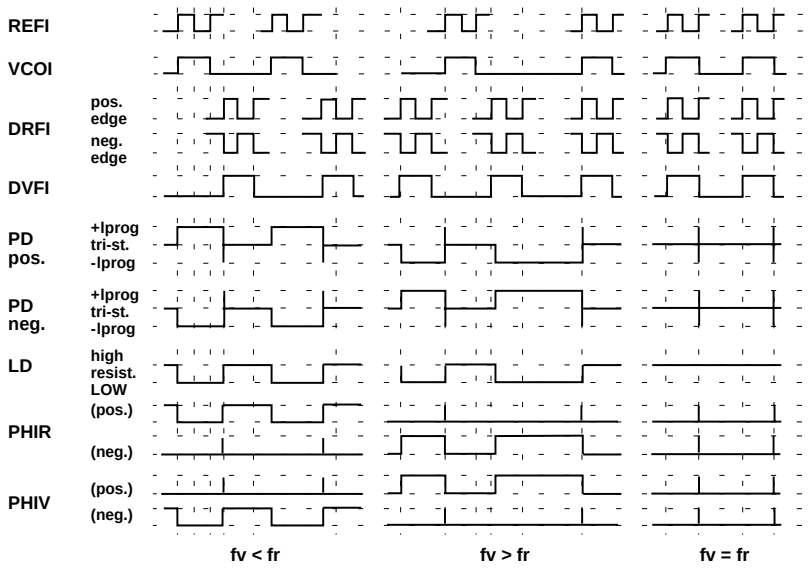
Output MOD Modulus Control (pin 7)

Symbol	Parameters and Test Conditions	Units	Min	Typ	Max
V_{OH}	Voltage Output High I_{OH} = 2 mA, V_{DD} = 4.5–5.5 V	V	V_{DD}–0.4		
	I_{OH} = 1.2 mA, V_{DD} = 2.7–3.3 V	V	V_{DD}–0.4		
V_{OL}	Voltage Output Low I_{OL} = 0.5 mA, V_{DD} = 4.5–5.5 V	V			0.8
	I_{OL} = 0.3 mA, V_{DD} = 2.7–3.3 V	V			0.8
T_R, T_F	Rise and Fall Time V_{DD} = 4.5–5.5 V, C_L = 5 pF	ns		1	3
	V_{DD} = 2.7–3.3 V, C_L = 5 pF	ns		3	6
T_{PHL}, T_{PLH} (VCOI to MOD)	Propagation Delay from high to low and low to high V_{DD} = 4.5–5.5 V, C_L = 5 pF	ns		6	9
	V_{DD} = 2.7–3.3 V, C_L = 5 pF	ns		15	17



Output PD Phase Detector (pin 10)

Symbol	Parameters and Test Conditions				
	B14	B13	B12	**Units**	**Typ.**
Icp (V_{DD} = 4.5 – 5.5 V)	0	0	0	mA	0.15
	0	0	1	mA	0.21
	0	1	0	mA	0.31
	0	1	1	mA	0.44
	1	0	0	mA	0.63
	1	0	1	mA	0.89
	1	1	0	mA	1.26
	1	1	1	mA	1.69
	Standby			nA	0.1
Icp (V_{DD} = 2.7 – 3.3 V)	0	0	0	mA	0.14
	0	0	1	mA	0.20
	0	1	0	mA	0.29
	0	1	1	mA	0.40
	1	0	0	mA	0.58
	1	0	1	mA	0.79
	1	1	0	mA	1.06
	1	1	1	mA	1.26
	Standby			nA	0.1

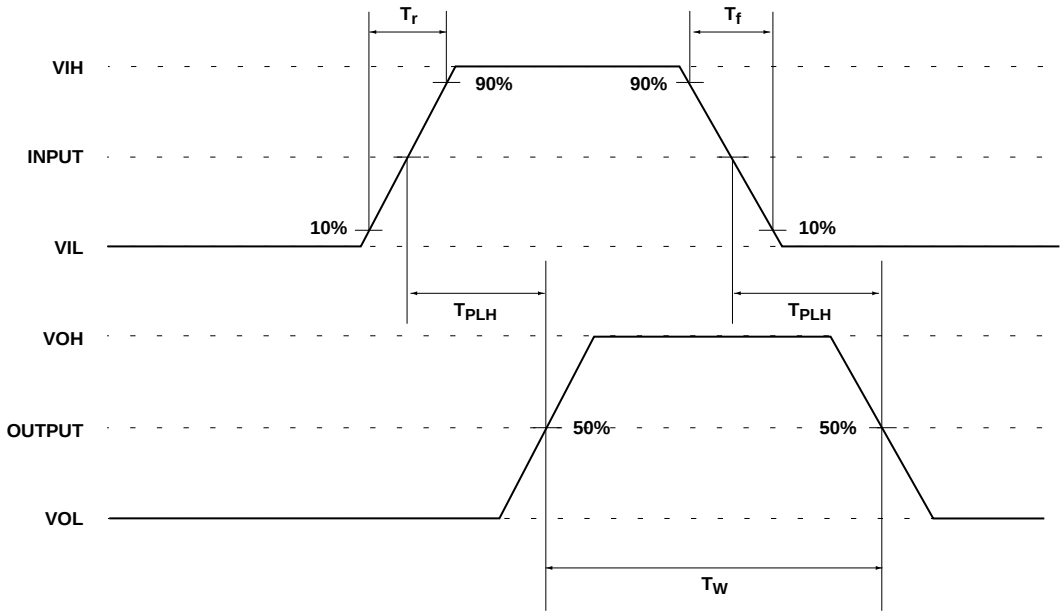


Input-Output PO2 Programmable Input-Output (pin 13)

Symbol	Parameters and Test Conditions	Units	Min	Typ	Max
V_{OH}	Voltage Output High I_{OH} = 2 mA, V_{DD} = 4.5–5.5 V	V	VDD–0.8		
	I_{OH} = 1.2 mA, V_{DD} = 2.7– 3.3 V	V	VDD–0.8		
V_{OL}	Voltage Output Low I_{OL} = 2 mA, V_{DD} = 4.5–5.5 V	V			0.8
	I_{OL} = 1.2 mA, V_{DD} = 2.7– 3.3 V	V			0.8
T_F	Fall Time V_{DD} = 4.5–5.5 V, MF01, MF02, C_L = 10 pF	ns		3	4
	V_{DD} = 2.7– 3.3 V, MF01, MF02, C_L = 10 pF	ns		5	6
T_R	Rise Time V_{DD} = 4.5–5.5 V, MF01, MF02, C_L = 10 pF	ns		6	7
	V_{DD} = 2.7– 3.3 V, MF01, MF02, C_L = 10 pF	ns		12	14
V_{REF}	Reference Voltage, Iref = 100 µA	V	0.8	1.1	1.3

Output LD Lock Detect (pin 14)

Symbol	Parameters and Test Conditions	Units	Min	Typ	Max
V_{OL}	Voltage Output Low I_{OL} = 0.5 mA, V_{DD} = 5 V	V			0.8
	I_{OL} = 0.5 mA, V_{DD} = 2.7 V	V			0.8
T_F	Fall Time V_{DD} = 4.5–5.5 V	ns		5	6
	V_{DD} = 2.7– 3.3 V	ns		8	10



HPLL-8001 Pin Description Table

No.	Mnemonic	Description	Typical Signal
1	REFI	Reference Frequency	High sensitivity preamplifier input for the r-counter. The input can be AC-coupled for small input signals or DC-coupled for large input signals.
2	VSS	Ground for digital logic	0 V
3	EN	3-wire interface: Enable	Enable line of the serial interface with internal pull-up resistor. When EN=H, the input signal CLK and DATA are internally disabled. When EN=L, the received data is transferred to the latches on the positive edge of the EN signal.
4	DATA	3-wire interface: Data	Serial DATA input with internal pull-up resistor. The last two bits before the EN-signal define the destination address.
5	CLK	3-wire interface: Clock	Clock line with internal pull-up resistor. The serial DATA is read into the internal shift register on the positive edge (see pulse diagram for serial data control).
6	VDD	Positive supply voltage for digital logic	
7	MOD	Modulus Control	For an external dual modulus prescaler. The modulus output is low at the beginning of the cycle. When the a-counter has reached its set value, MOD switches to high. When the n-counter has reached its set value, MOD switches to low and the cycle starts again. When the prescaler has the counter factor P or P+1 (P for MOD=H, P+1 for MOD=L), the overall scaling factor is NP+A. The value of the a-counter must be smaller than that of the n-counter. The trigger edge of the modulus signal to the input signal can be selected (see programming tables and MOD A, B) according to the needs of the prescaler. In single modulus operation and for standby operation, the output is low.
8	VCOI	VCO frequency	High sensitivity preamplifier input for the n-counter. The input can be AC-coupled for small input signals or DC-coupled for large input signals.
9	AVSS	Ground for analog logic	Pins VDD and AVDD and also pins VSS and AVSS must have the same power supply voltage.
10	PD	Phase detector	Tristate charge pump output. The level of the charge pump output current can be programmed using the digital interface. frequency $F_V<F_R$ or F_V lagging: p source active frequency $F_V>F_R$ or F_V leading: n source active frequency $F_V=F_R$ & PLL locked: PD tristate standby mode: PD tristate The polarity of the output signals of the phase detector can be programmed.
11	AVDD	Positive supply voltage for analog logic	

HPLL-8001 Pin Description Table, continued

No.	Mnemonic	Description	Typical Signal
12	PO1	Programmable output	Multifunction Output for the signals F_{RN} , ϕ_V , ϕ_{VN} and PROBIT (F_{RN}, ϕ_V are the inverted signals of F_R, ϕ_{VN}).
13	PO2	Programmable I/O	For the output signals F_{VN}, ϕ_{RN} and the input signal I_{REF} - The signals ϕ_R and ϕ_V are the digital output signals of the phase and frequency detector for use with external active current sources. - The signals F_{RN} and F_{VN} are the scaled down signals of the reference frequency and VCO-frequencies. - The programmed bit PROBIT is assigned to PO1 output in the internal charge pump mode. The standby mode does not affect this function. - In the internal charge pump mode the input signal I_{REF} determines the value of the PD-output current.
14	LD	Lock detect	Unipolar output of the phase detector in the form of a pulse-width modulated signal. The LD-pulse width corresponds to the phase difference. In the locked state the LD-signal is at H-level. In standby mode the output is resistive.

Programmable Reference Divider (R Counter Register)

1	1	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16

Note: R16 is the MSB of the R counter value. R16 is the first bit which is transferred to the HPLL-8001.

Programmable Dividers (N and A Counter Registers)

Dual Mode

0	1	N1	N2	N3	.....	N12	N13	N14	A1	A2	A3	A4	A5	A6	A7

Single Mode

0	1	N1	N2	N3	N4	N5	N6	N7	N8	N10	N11	N12	N13	N14			

Note: N14 is the MSB of the N counter value. A7 is the MSB of the A counter value. A7 is the first bit which is transferred to the HPLL-8001.

Status Registers

1	0	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

B1 is the first bit which is transferred to the HPLL-8001.

B1:

B1	**Counter loading**
0	asynchronous counter load
1	synchronous counter load

B2 and B3:

B2	**B3**	**PO1**	**PO2**	**Modes**
0	0	F_{RN}	F_{VN}	Test Modes
0	1	ϕ_V	ϕ_{RN}	External Charge Pump, Mode 1
1	0	ϕ_{VN}	ϕ_{RN}	External Charge Pump, Mode 2
1	1	PROBIT	I_{REF}	Internal Charge Pump mode

B4:

B2	**PD Polarity**
0	negative
1	positive
positive means increasing VCO frequency with increasing voltage	

B5 and B6:

B5	**B6**	**Modes**
Standby 2	**Standby 1**	
0	0	Standby mode 1: All functions
0	1	powered down
1	0	Standby mode 2: Counters, charge pump, and outputs are off. Only preamplifiers stay active
1	1	Normal operation: All functions are active

B7 and B8:

Anti Backlash Pulse Width			
B8	**B7**	Typical	Unit
0	0	10	ns
0	1	6	ns
1	0	4	ns
1	1	2	ns

B9 and B10:

B9	B10	Modes
Single/Dual Mode	Preamplifier Select	
0	0	VCOI input: single HF mode
0	1	VCOI input: single LF mode
1	0	VCOI input: dual mode, VCOI trigger LH edge
1	1	VCOI input: dual mode, VCOI trigger HL edge

B11:

B11	Output bit PROBIT on PO1
0	0
1	1

B12, B13, and B14:

	B14	B13	B12	Charge pump current	
				Typ.	Units
VDD = 4.5 – 5.5 V	0	0	0	0.15	mA
	0	0	1	0.21	mA
	0	1	0	0.31	mA
	0	1	1	0.44	mA
	1	0	0	0.63	mA
	1	0	1	0.89	mA
	1	1	0	1.26	mA
	1	1	1	1.69	mA
	Standby			0.1	nA
VDD = 2.7 – 3.3 V	0	0	0	0.14	mA
	0	0	1	0.20	mA
	0	1	0	0.29	mA
	0	1	1	0.40	mA
	1	0	0	0.58	mA
	1	0	1	0.79	mA
	1	1	0	1.06	mA
	1	1	1	1.26	mA
	Standby			0.1	nA

Reduced Status Register

0	0	B14	B13	B12	B11

B11 is the first bit which is transferred to the HPLL-8001.

Functional Description

Frequency Divider

The division ratio can be calculated as follows:

FVCO = (N x P + A) / R x FREF where,

FVCO: Output frequency of the external VCO
FREF: Reference oscillator frequency
N: divide ratio of the N counter $3 \leq N \leq 16380$
A: divide ratio of the A counter $0 \leq A \leq 127$
R: divide ratio of the R counter $3 \leq R \leq 65535$
P: divide ratio of the external dual modulus prescaler

Phase Detector and Charge Pump

The phase detector is a digital, edge-sensitive comparator with UP and DOWN outputs. Both outputs can be monitored at the outputs PO1 and PO2. The phase detector drives a charge pump, which is a switch with a tristate state. The output current can be programmed in 8 steps between 0.15 mA and 1.69 mA (VDD = 4.5 to 5.5 V) with a reference current of 100 µA.

If VCOI < REFI, the charge pump delivers a positive current to the external loop filter. If VCOI > REFI, the charge pump sinks a negative current from the external loop filter. The charge pump output can be inverted by software.

Anti-backlash pulses are generated to extend the very short phase difference between VCOI and REFI.

Programming

The HPLL-8001 can be programmed through a 3-wire interface. Four different words can be sent over this interface to program the internal registers. All four words consists of a 2-bit address and a variable data portion. When EN=L, the data is transferred. It is loaded into the internal registers at the rising edge of EN. The last two bits which are transferred, form the address bits. When EN=H, the input signals, CLK and DATA, are internally disabled.

The Status registers contains all status information.

The reduced Status register is a reduced version of the status register.

The N and A counter register and the R counter register contain the applicable counter values.

The programming of the device must start with the loading of the status register.

The N, A and R counters can be loaded synchronously or asynchronously. If synchronous loading is selected, all counters are loaded when they reach the value zero. As a result, the phase difference between the divided VCOI and REFI signal remains the same.

For synchronous loading the following order of programming must be followed:

1) programming of synchronous loading using the status register
2) programming of the R counter
3) programming of the N, A counters

The rising edge of EN enables the synchronous loading of all counters at their zero value.

Standby

The HPLL-8001 has two standby modes.

In standby mode 1, the whole device is powered down with the exception of the serial interface.

In standby mode 2, the serial interface and the input amplifiers are active. All other parts are powered down.

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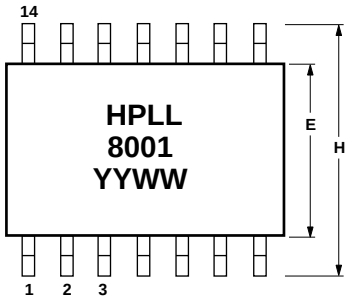
Part Number Ordering Information

Part Number	No. of Devices	Container
HPLL-8001-BLK	56	Tube
HPLL-8001-TR1	1000	7" Reel

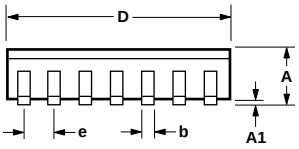
Package Dimensions

JEDEC Standard SOP-14

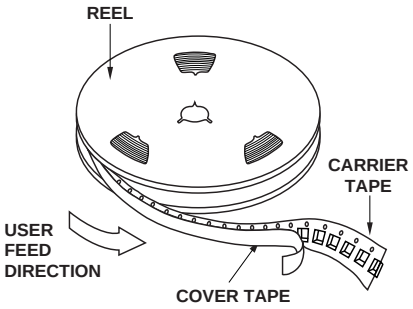


SYMBOL	DIMENSIONS	
	MIN.	MAX.
A	1.35 (0.053)	2.01 (0.079)
A1	0.080 (0.003)	0.300 (0.012)
b	0.330 (0.013)	0.510 (0.020)
D	8.56 (0.337)	8.89 (0.350)
E	3.81 (0.150)	4.09 (0.161)
e	1.27 BSC (0.500)	
H	5.79 (0.151)	6.40 (0.252)
L	0.300 (0.012)	1.27 (0.050)
θ	0	10

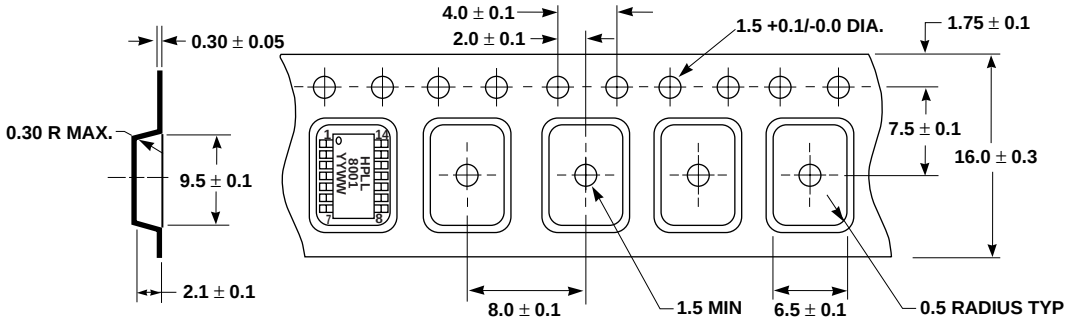
Meets JEDEC outline dimensions.
Dimensions are in millimeters (inches).
Tolerances: .XX = ±.01, .XXX = ±.002



Device Orientation



Tape Dimensions and Product Orientation



DIMENSIONS ARE SHOWN IN MILLIMETERS

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Data subject to change.

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