3SxLC

REV2

Memec Design

BOARD NAME :	**SPARTAN 3 EVALUATION BOARD**
BOARD PART NUMBER :	**DS-BD-3SxLC-PQ208**
BOARD REVISION :	**2**

Memec Board	MemecBoard Calgary, Alberta Canada	BOARD TITLE: SPARTAN 3Sx EVALUATION BOARD	PAGE TITLE: TITLE PAGE	LAST MODIFIED: Monday, April 12, 2004	SIZE	C	DESIGNER	JBE	REVISION	2	SHEET	1 of 8

VOLTAGE	INPUT JACK	REGULATION	LED
VIN (5V)	JP1 Barrel Jack SMT; TP6; VINJACK; 5V	VINJACK; VINUSB; SW1 SPDT Slide 6A; JP32 1X2; INSTALL SHUNT TO POWER THE BOARD FROM USB; C56 330u; 5V	
3.3V	TP8; 3.3V	5V; R98 10k 1%; 3V3ENABLE; U2 TPS78633KTT (ENABLE, IN, GND, OUT, BYPASS/FB, GND); C162 330u; C3 2.2u; C163 2.2u; C175 .01u 6 0402; JP22 1X2; 3.3V DISABLE; Q5 Si2333; C182 .1u 6 0603; C183 47n 6 0402; R129 100; R130 210k 1%; SOFTSTART CIRCUIT; 3.3V	3.3V; R115 100; DS6 GREEN; LABEL = 3.3V
2.5V	TP7; 2.5V	5V; 2V5ENABLE; U1 TPS79525DCQ (EN, IN, GND, OUT, BYPASS/FB); C159 330u; C1 2.2u; C160 2.2u; C161 .1u 6 0603; Q6 Si2333; C184 .1u 6 0603; C185 47n 6 0402; R131 100; R132 121k 1%; SOFTSTART CIRCUIT; 2.5V	2.5V; R1 100; DS1 GREEN; LABEL = 2.5V
1.2V	TP7; 1.2V; 2.5V	5V; U3 TPS54110PWP (PGND, VIN, VBIAS, SS/ENA, SYNC, RT, PH, BOOT, PWRGD, COMP, VSENSE, AGND); L1 6.2uH; C191 1u 6 0603; C192 10u 6.3 1206; C193 10u 6.3 1206; C100 10u 6.3 1206; C104 .1u 6 0603; C105 47n 6 0402; C103 10u 6.3 1206; C195 330u; 1.2V; 3V3ENABLE; R3 73.2k 1%; R24 30.1k 1%; C187 27p 6 0603; C186 2.7n 6 0603; C194 22u 6 1206; 2.5V; R13 10k 1%; 1V2ENABLE; JP34 1X2; 1.2V DISABLE; C189 1u 6 0603; R135 28.7k 1%; R134 1.91k 1%; R127 10k 1%	5V; R2 330 1%; DS2 GREEN; LABEL = 1.2V; 1.2V; Q3 BCR108

GROUND TEST LOOPS

TP5

FEET

NE1 Little Rubber Feet -Thick MOUNT TO BOTTOM AS PER SSB
NE2 Little Rubber Feet -Thick MOUNT TO BOTTOM AS PER SSB
NE3 Little Rubber Feet -Thick MOUNT TO BOTTOM AS PER SSB
NE4 Little Rubber Feet -Thick MOUNT TO BOTTOM AS PER SSB

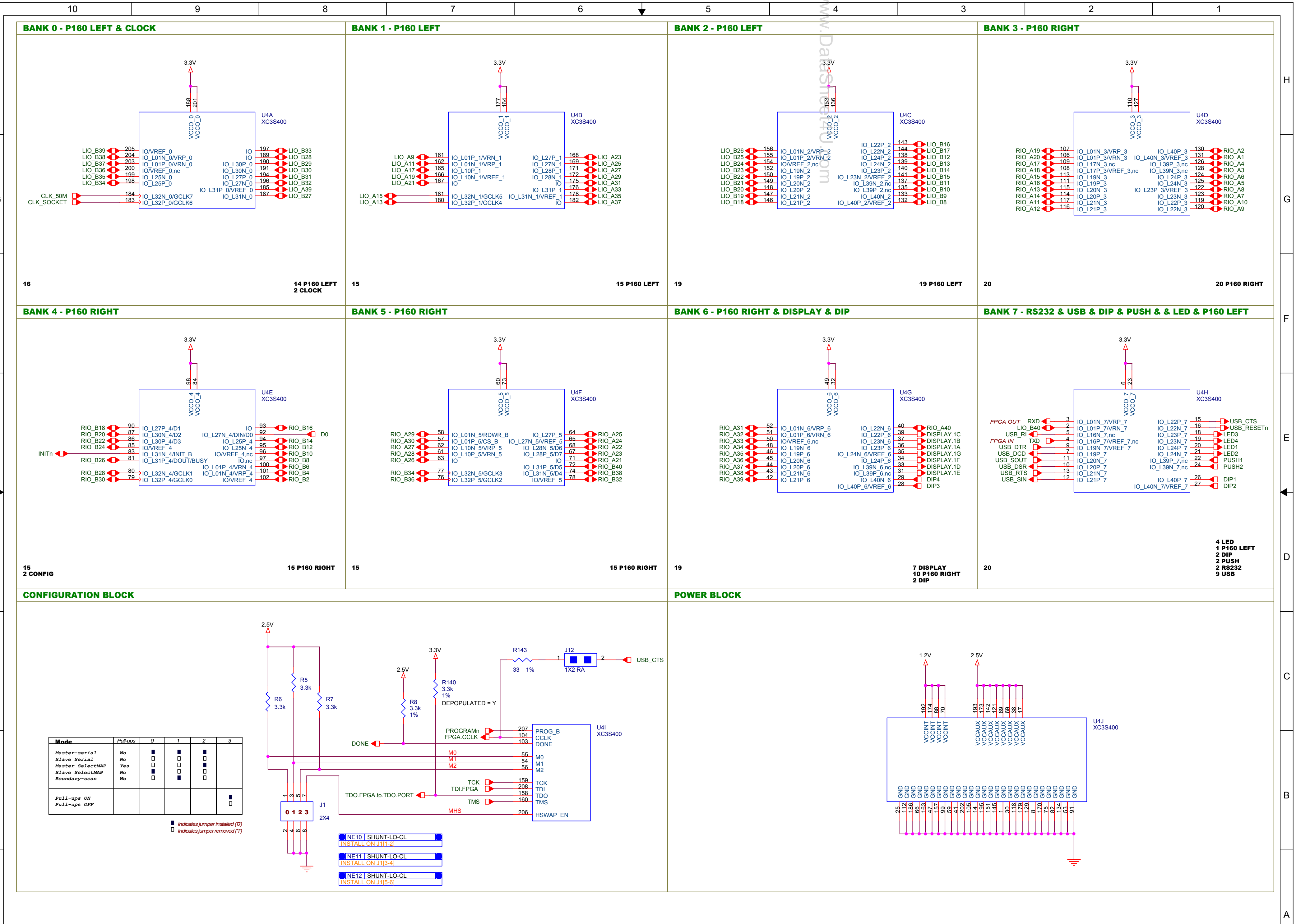
MOUNTING HOLES

NE6 Mounting Hole (.125)
NE7 Mounting Hole (.125)
NE8 Mounting Hole (.125)
NE9 Mounting Hole (.125)

SUPERVISOR

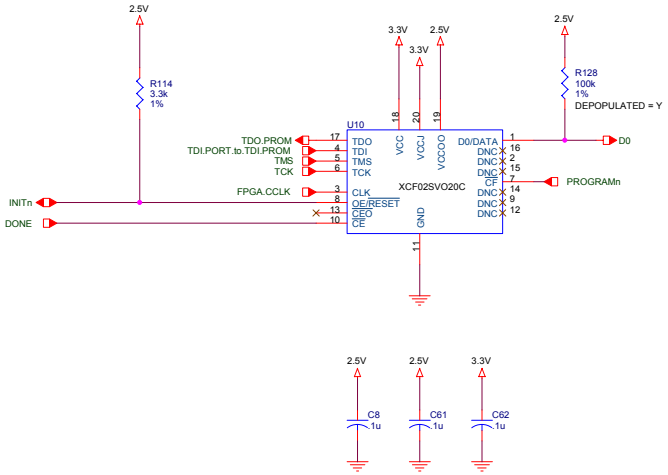
5V; U5 TLC7733IPW (VDD, SENSE, RESET, RESET, CONTROL, RESIN, CT, GND); 2V5ENABLE; C188 4.7u 6 0603; R133 3.3k 1%; R12 3.3k 1%; JP33 1X2; 2.5V DISABLE

MemecBoard Calgary, Alberta Canada	BOARD TITLE: SPARTAN 3Sx EVALUATION BOARD	PAGE TITLE: POWER	LAST MODIFIED: Monday, April 12, 2004	SIZE	C	DESIGNER	JBE	REVISION	2	SHEET	2	of	8

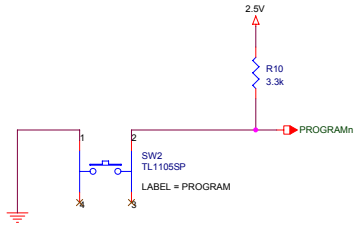


MemecBoard Calgary, Alberta Canada	BOARD TITLE **SPARTAN 3Sx EVALUATION BOARD**	PAGE TITLE FPGA	LAST MODIFIED Monday, April 12, 2004	SIZE	C	DESIGNER	JBE	REVISION	2	SHEET	3 of 8

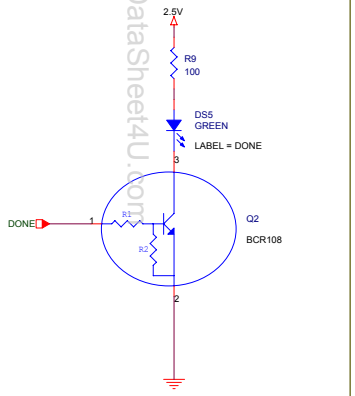
PROM (PLATFORM FLASH)



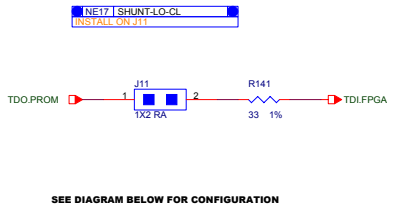
PROGRAM PUSHBUTTON



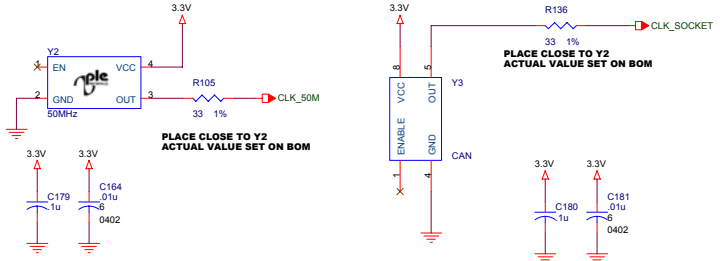
DONE LED



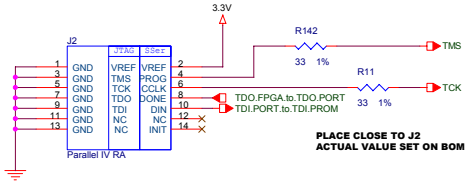
PROM JTAG BYPASS



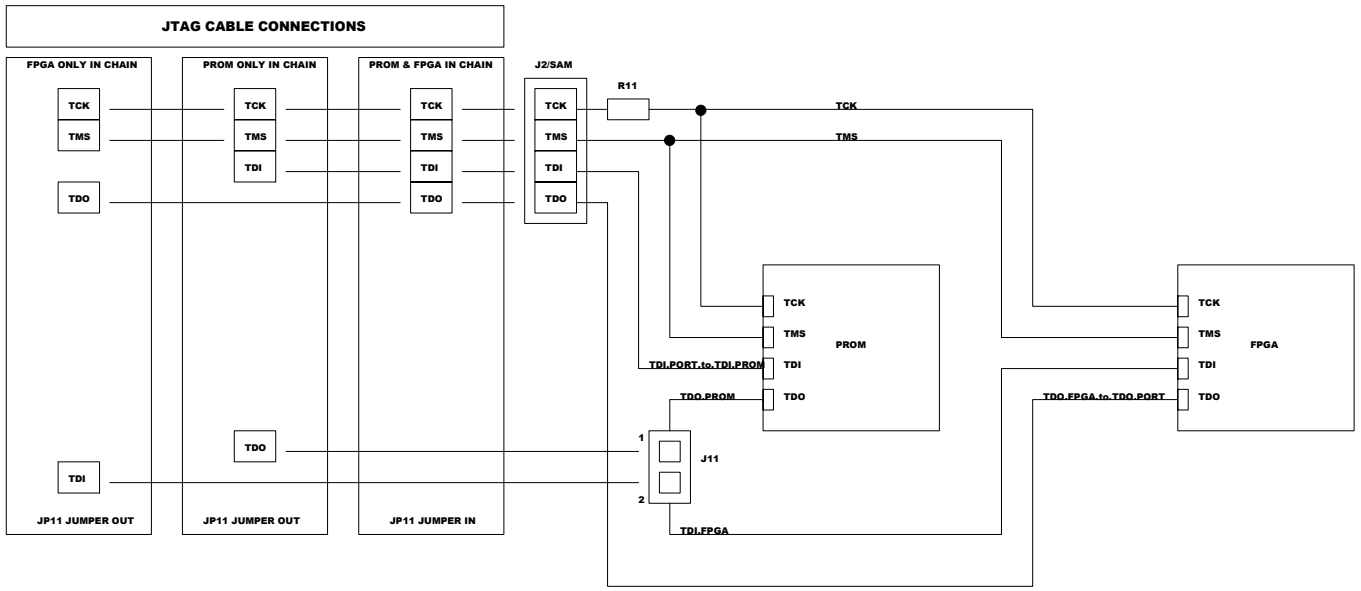
CLOCKs



JTAG PORT

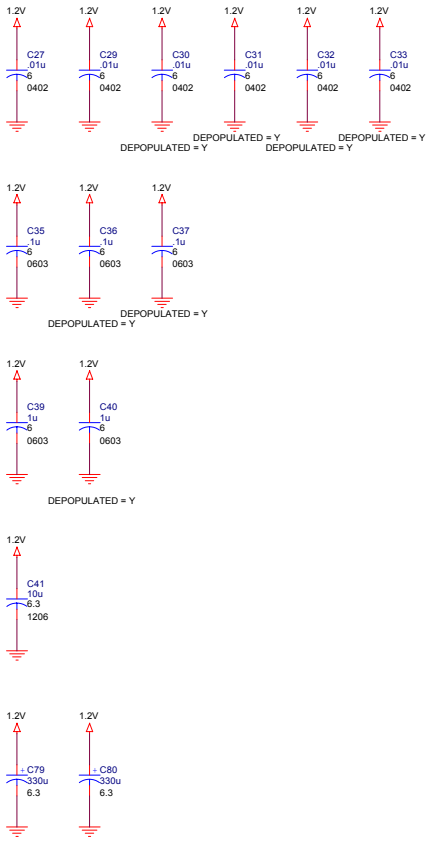


JTAG CONNECTION DIAGRAM

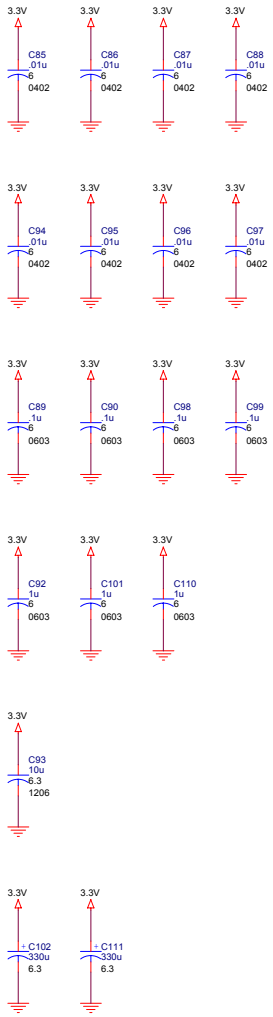


MemecBoard Calgary, Alberta Canada	BOARD TITLE: SPARTAN 3Sx EVALUATION BOARD	PAGE TITLE: FPGA PERIPHERALS	LAST MODIFIED: Monday, April 12, 2004	SIZE	C	DESIGNER	JBE	REVISION	2	SHEET	4	of	8

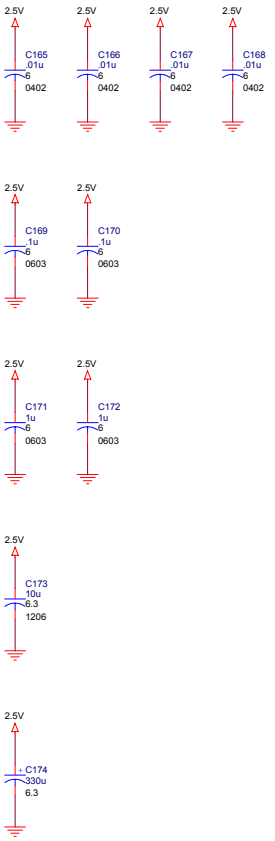
FPGA CORE DECOUPLING (4 pins)



FPGA BANK DECOUPLING (16 pins)



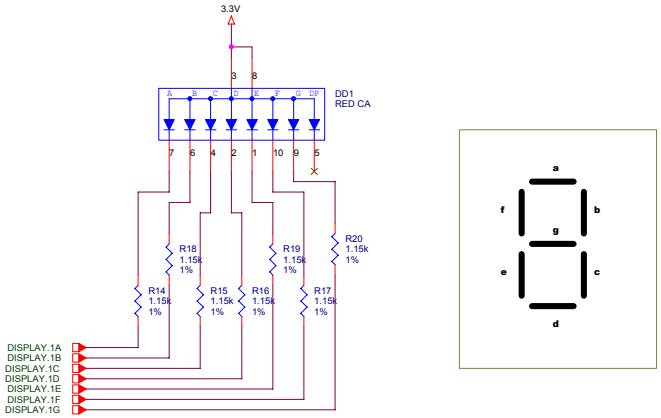
FPGA AUX DECOUPLING (8 pins)



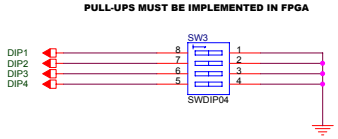
AS PER XILINX APP NOTE UPDATE

MemecBoard Calgary, Alberta Canada	BOARD TITLE SPARTAN 3Sx EVALUATION BOARD	PAGE TITLE DECOUPLING	LAST MODIFIED Monday, April 12, 2004	SIZE	C	DESIGNER	JBE	REVISION	2	SHEET	5 of 8

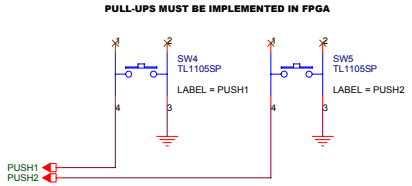
SEVEN SEGMENT DISPLAYs



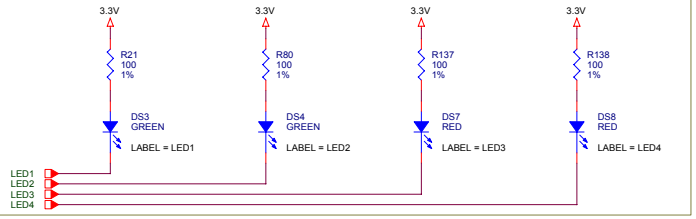
DIP SWITCH



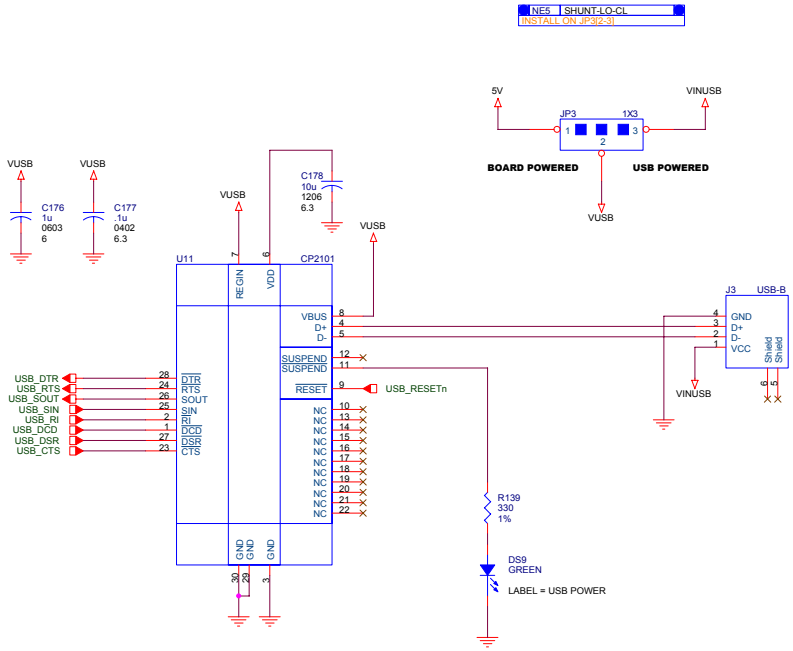
PUSHBUTTONS



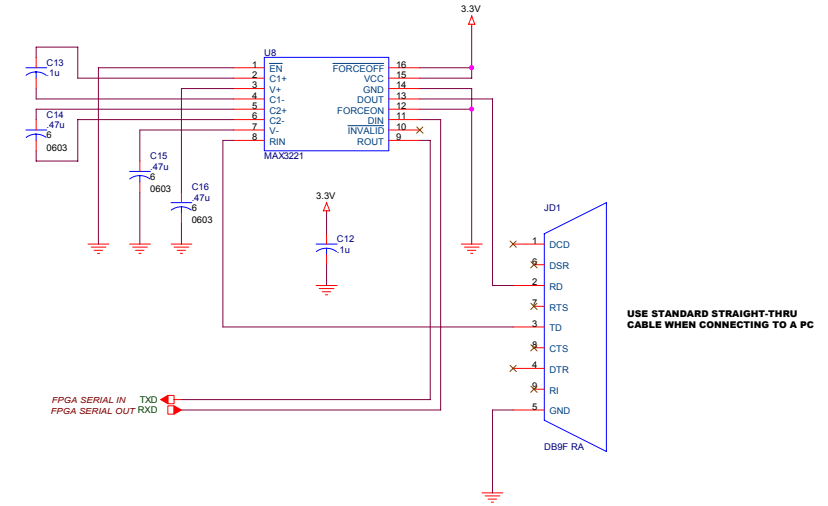
LEDs



USB



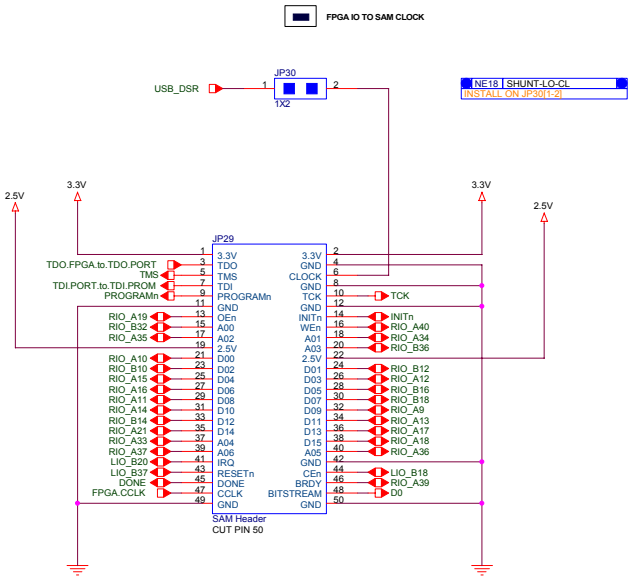
SERIAL PORT



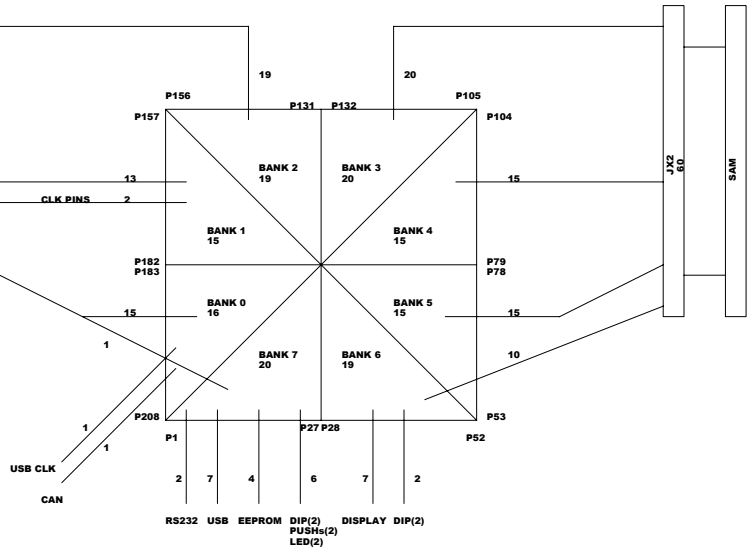
MemecBoard Calgary, Alberta Canada	BOARD TITLE SPARTAN 3Sx EVALUATION BOARD	PAGE TITLE USER IO	LAST MODIFIED Monday, April 12, 2004	SIZE	C	DESIGNER	JBE	REVISION	2	SHEET	6 of 8

P160

SYSTEM ACE MODULE



PLACEMENT



USED		AVAILABLE	
DISPLAY	7		
EEPROM	4		
RS232	2	BANK 0	16
DIP	4	BANK 1	15
PUSH	2	BANK 2	19
LEDs	2	BANK 3	20
JX1	49	BANK 4	15
JX2	60	BANK 5	15
CLOCK	2	BANK 6	19
USB	7	BANK 7	20
TOTAL :	139	TOTAL :	139

MemecBoard Calgary, Alberta Canada	BOARD TITLE SPARTAN 3Sx EVALUATION BOARD	PAGE TITLE P160 & SAM	LAST MODIFIED Monday, April 12, 2004	SIZE C	DESIGNER JBE	REVISION 2	SHEET 7 of 8

REV A	REV 1	REV 2
CHANGED USB FROM TI TO CYGNAL	ADDED CCLK JUMPER	
ADDED ASSEMBLY NOTES	CHANGED SAM CLOCK JUMPER CONNECTIONS	
ADDED CLOCK SOCKET	CHANGED SSD TO 0750	
REMOVED EEPROM	CHANGED SSD RESISTOR VALUES TO 1.15k	
CHANGED U5 SUPERVISOR	MODIFIED JTAG CHAIN FOR 3.3V OPERATION	
CHANGED 1.2V CONVERTER TO SWIFT	ADDED OPTIONAL PULL-UP ON FPGA's TDO	
REDESIGNED POWER SEQUENCING	ADDED ALTERNATE PART NUMBER FOR INDUCTOR (L1)	
ADDED SOFTSTART CIRCUITS TO 2.5V AND 3.3V	REMOVED REDUNDANT PULL-UP FROM DONE LINE	
CHANGED DONE LED DRIVE TRANSISTOR TO BCR108		
ADDED TWO USER LEDs		
REDUCED CURRENT THROUGH 1.2V LED (100 TO 330 OHM)		
ADDED JUMPER BLOCK TO USB UART SIGNALS		