DATA SHEET

Part No.	AN12969A
Package Code No.	UBGA031-W-3030AEA

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Contents

AN12969A

I²C bus control compatible AGC built-in stereo BTL amplifier IC (For driving a piezoelectric speaker)

■ Overview

AN12969A has a built-in AGC function in a stereo BTL amplifier for driving a piezoelectric speaker to prevent noise at output clip, and has a built-in a charge-pump power supply for driving speaker output amplifiers.

And I²C bus control method is applied in switching of each mode like some Standby function is turned ON/OFF.

■ Features

- The piezoelectric speaker can be driven by applying the circuit of high withstand voltage power amplifier.
- On level in AGC can be selected by controlling I²C bus.
- Attack and recovery times in AGC can be selected by controlling I²C bus.
- Resistance and capacitor, which were used for conventional analog AGC aren't needed anymore.
- I²C is controlled almost in the same way as those of AN12959A.
- Shut-down function is mounted.
- Amplifier gain switching
- The input circuit constructs a bus boost circuit easily and improves the sound quality of the piezoelectric speaker.
- The supply for speaker output amplifier isn't needed anymore.

■ Applications

- Audio amplifier for mobile, such as a cellular phone

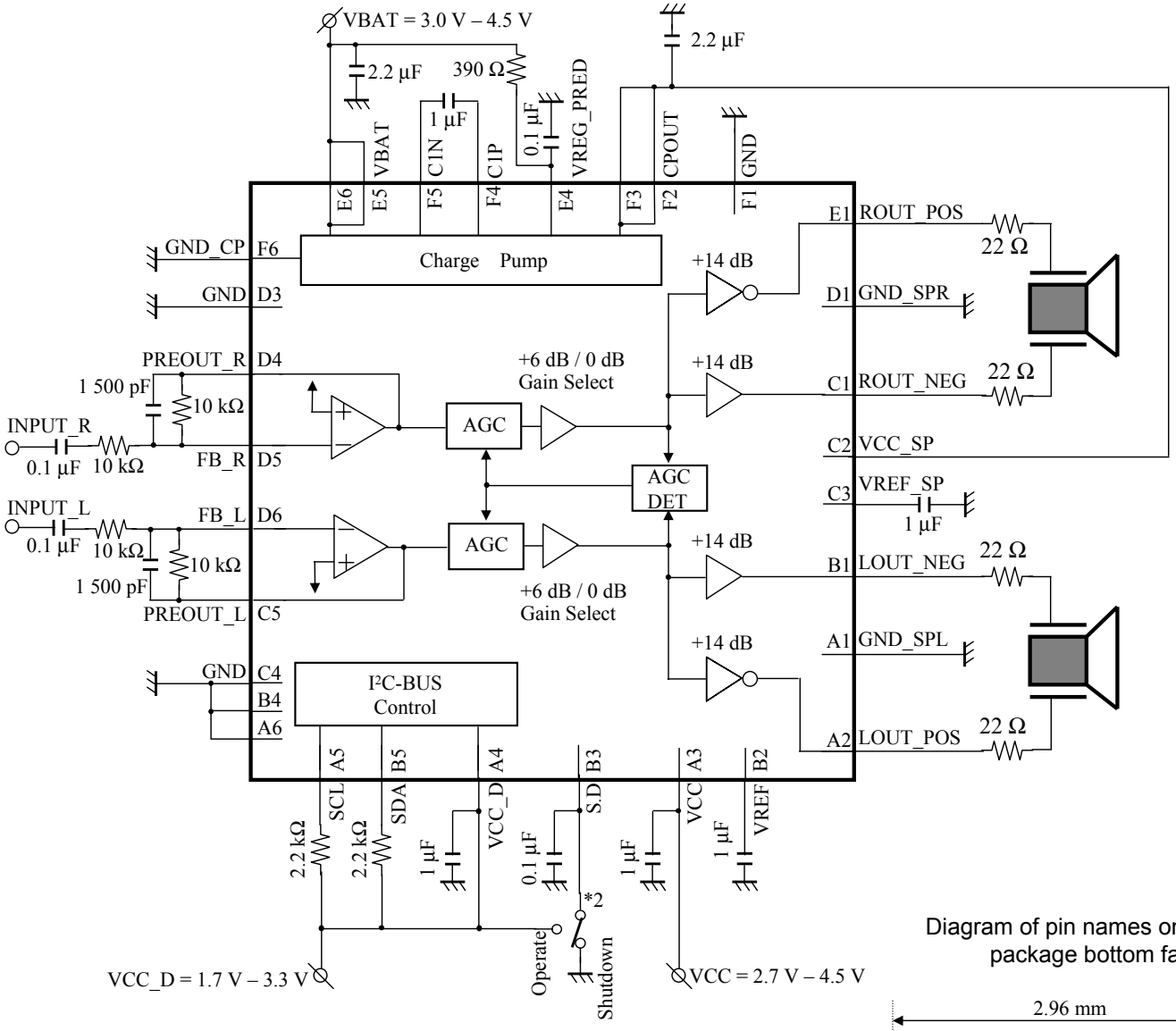
■ Package

- 31 pin Plastic Quad 6 Column BGA Package(0.5 mm Pitch)

■ Type

- Silicon Monolithic Bi-CMOS IC

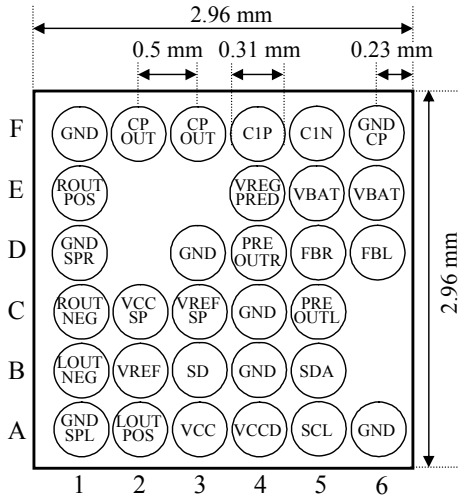
■ Application Circuit Example



B3 pin Operate voltage

VCC_D = 1.8 V	VCC_D = 2.6 V
Operate > 1.62 V	Operate > 2.34 V
Shut-down < 0.18 V	Shut-down < 0.26 V

Diagram of pin names on package bottom face



Note) N.C. pin is without a solder ball.

Note) This circuit and these circuit constants show an example and do not guarantee the design as a mass-production set.
*2 : The threshold voltage at Pin B3 has the VCC_D dependency.
*3 : This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.

■ Pin Descriptions

Pin No.	Pin name	Type	Description
A1	GND_SPL	Ground	Grounding (For speaker L-channel)
A2	LOUT_POS	Output	Speaker output L-channel (+)
A3	VCC	Power Supply	Power supply V_{CC}
A4	VCC_D	Power Supply	V_{CC_D} for logic circuit
A5	SCL	Input	SCL
A6	GND	Ground	Grounding
B1	LOUT_NEG	Output	Speaker output L-channel (–)
B2	VREF	Input	Reference voltage pin
B3	S.D	Input	Shut-down pin
B4	GND	Ground	Grounding
B5	SDA	Input / Output	SDA
B6	N.C.	—	N.C.
C1	ROUT_NEG	Output	Speaker output R-channel (–)
C2	VCC_SP	Power Supply	V_{CC_SP} for the circuit of speaker output
C3	VREF_SP	Input	Reference voltage pin for the circuit of speaker output
C4	GND	Ground	Grounding
C5	PREOUT_L	Output	First amplifier output L-channel
C6	N.C.	—	N.C.
D1	GND_SPR	Ground	Grounding (For speaker R-channel)
D2	N.C.	—	N.C.
D3	GND	Ground	Grounding
D4	PREOUT_R	Output	First amplifier output R-channel
D5	FB_R	Input	First amplifier negative feedback input R-channel
D6	FB_L	Input	First amplifier negative feedback input L-channel

■ Pin Descriptions (continued)

Pin No.	Pin name	Type	Description
E1	ROUT_POS	Output	Speaker output R-channel (+)
E2	N.C.	—	N.C.
E3	N.C.	—	N.C.
E4	VREG_PRED	Output	VREG capacitor pin for charge pump gate-driver
E5	VBAT	Power Supply	V_{BAT} for Charge-pump
E6	VBAT	Power Supply	V_{BAT} for Charge-pump
F1	GND	Ground	Grounding
F2	CPOUT	Output	Charge-pump output
F3	CPOUT	Output	Charge-pump output
F4	C1P	Output	Charge pump flying capacitor pin (+)
F5	C1N	Output	Charge pump flying capacitor pin (−)
F6	GND_CP	Ground	Grounding (For charge-pump)

■ Absolute Maximum Ratings

A No.	Parameter	Symbol	Range	Unit	Note
1	Supply voltage	V_{CC},V_{BAT}	5.0	V	*1
		V_{CC_D}	3.6		
2	Supply current	I_{CC}	—	A	—
3	Power dissipation	P_D	136	mW	*2
4	Operating ambient temperature	T_{opr}	–20 to +70	°C	*3
5	Storage temperature	T_{stg}	–55 to +150	°C	

Note) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : The power dissipation shown is the value at T_a = 70°C for the independent (unmounted) IC package with a heat sink. When using this IC, refer to the • P_D-T_a diagram in the ■ Technical Data and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.

*3 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

■ Operating supply voltage range

Parameter	Symbol	Range	Unit	Note
Supply voltage range	V_{CC}	2.7 to 4.5	V	*1
	V_{CC_D}	1.7 to 3.3		*1, *2
	V_{BAT}	3.0to 4.5		*1

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: The I²C bus of this product is designed to correspond to Standard mode(100 Kbps) and Fast mode(400 Kbps) in Philips Corporation I²C specification version 2.1 at V_{CC_D} = 1.7 V to 3.3 V. However, not correspond to High Speed mode (< 3.4 Mbps).

■ Electrical Characteristics

Note) Unless otherwise specified, T_a = 25°C±2°C, V_{CC} = 3.0 V,V_{CC_D} = 1.8 V, V_{BAT} =3.8 V

B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
Circuit Current								
1	Circuit current 1A at non-signal	IVCC1A	Non-signal, STB = OFF, SP_SAVE = OFF, AGC = ON	—	0.5	1.0	mA	—
2	Circuit current 2A at non-signal	IVCC2A	Non-signal, STB = OFF, SP_SAVE = OFF, AGC = ON	—	28	46	mA	—
3	Circuit current 3A at non-signal	IVCC3A	Non-signal, STB = OFF, SP_SAVE = OFF, AGC = ON	—	0.1	10	µA	—
4	Circuit current 1B at non-signal	IVCC1B	Non-signal, STB = ON, SP_SAVE = ON, AGC = ON	—	0.1	1.0	µA	—
5	Circuit current 2B at non-signal	IVCC2B	Non-signal, STB = ON, SP_SAVE = ON, AGC = ON	—	0.1	1.0	µA	—
6	Circuit current 3B at non-signal	IVCC3B	Non-signal, STB = ON, SP_SAVE = ON, AGC = ON	—	0.1	1.0	µA	—
7	Circuit current 1C at non-signal	IVCC1C	Non-signal, STB = OFF, SP_SAVE = ON, AGC = ON	—	0.5	1.0	mA	—
8	Circuit current 2C at non-signal	IVCC2C	Non-signal, STB = OFF, SP_SAVE = ON, AGC = ON	—	19	23	mA	—
9	Circuit current 3C at non-signal	IVCC3C	Non-signal, STB = OFF, SP_SAVE = ON, AGC = ON	—	0.1	10	µA	—
I/O Characteristics								
10	SP reference output level	VSPOL VSPOR	V_{IN} = –26.0 dBV, f = 1 kHz, RL = 100 Ω	–1.0	0.0	1.0	dBV	—
11	SP reference output distortion	THSPOL THSPOR	V_{IN} = –26.0 dBV, f = 1 kHz, RL = 100 Ω, to THD5th	—	0.07	0.5	%	—
12	SP reference output noise voltage	VNSPOL VNSPOR	Non-Signal using A curve filter	—	–75	–68	dBV	—
13	Output level at SP Save	VSSPOL VSSPOR	V_{IN} = –26.0 dBV, f = 1 kHz, RL = 100 Ω using A curve filter	—	–114	–90	dBV	—
14	SP AGC output level	VSPOA1L VSPOA1R	V_{IN} = –6.0 dBV, f = 1 kHz, RL = 100 Ω, V_{BAT} = 4.3 V, AGC – SELECT = [000]	11.6	12.6	13.6	dBV	—

■ Electrical Characteristics (continued)

Note) Unless otherwise specified, T_a = 25°C±2°C, V_{CC} = 3.0 V,V_{CC_D} = 1.8 V, V_{BAT} =3.8 V

B No.	Parameter	Symbol	Conditions	Limits			Unit	Note
				Min	Typ	Max		
I²C interface								
15	SCL, SDA signal input Low level	V_{IL}	—	–0.5	—	$0.3 \times V_{CC\_D}$	V	—
16	SCL, SDA signal input High level	V_{IH}	—	$0.7 \times V_{CC\_D}$	—	V_{CC_D} + 0.5	V	—
17	SDA signal output Low Level	V_{OL}	Open corrector, sync current : 3mA	0	—	$0.2 \times V_{CC\_D}$	V	—
18	SCL, SDA signal input current	I_i	Input voltage 0.1 V to 1.7 V	–10	—	10	µA	—
19	Max. frequency of SCL signal allowable to input	f_{SCL}	—	0	—	400	kHz	—
The threshold voltage at Pin B3								
20	Shut-down input Low level	Vsdlth	—	—	—	$0.1 \times V_{CC\_D}$	V	—
21	Shut-down input High level	Vsdhth	—	$0.9 \times V_{CC\_D}$	—	—	V	—

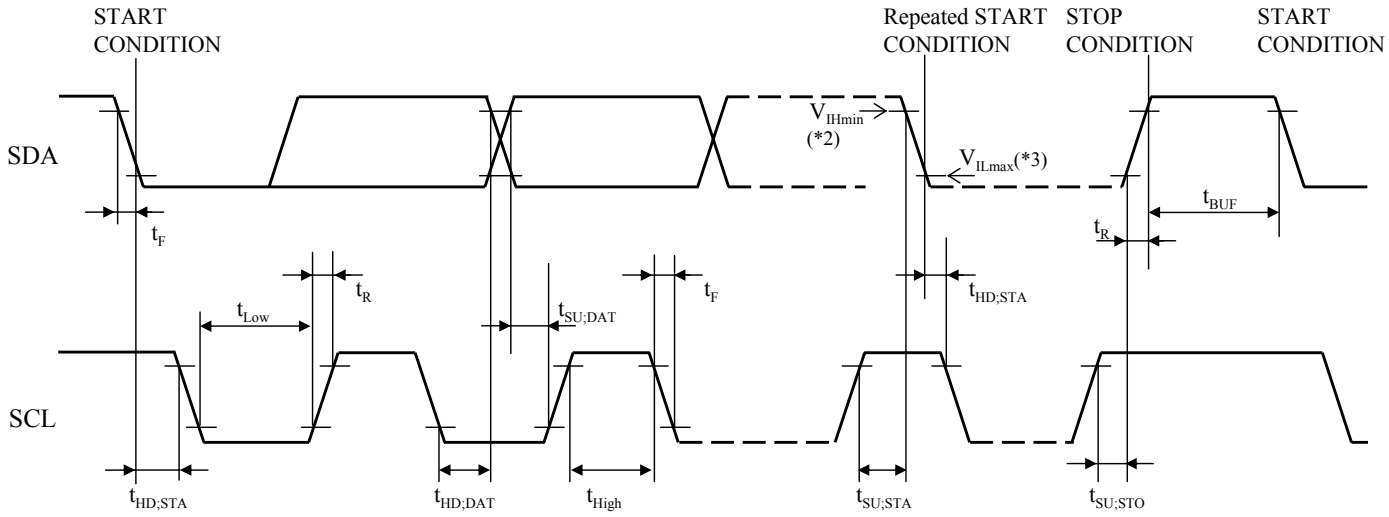
■ Electrical Characteristics (Reference values for design)

Note) Unless otherwise specified, T_a = 25°C±2°C, V_{CC} = 3.0 V,V_{CC_D} = 1.8 V, V_{BAT} =3.8 V
The characteristics listed below are reference values for design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, Panasonic will respond in good faith to user concerns.

B No.	Parameter	Symbol	Conditions	Reference values			Unit	Note
				Min	Typ	Max		
I²C interface								
22	Bus free time between stop and start conditions	t_{BUF}	—	1.3	—	—	µs	—
23	Setup time of start condition	$t_{SU;STA}$	—	0.6	—	—	µs	—
24	Hold time of start condition	$t_{HD;STA}$	—	0.6	—	—	µs	—
25	Low period of SCL clock	t_{Low}	—	1.3	—	—	µs	—
26	High period of SCL clock	t_{High}	—	0.6	—	—	µs	—
27	Rising time of SDA, SCL signal	t_R	—	—	—	0.3	µs	—
28	Falling time of SDA, SCL signal	t_F	—	—	—	0.3	µs	—
29	Data setup time	$t_{SU;DAT}$	—	0.1	—	—	µs	—
30	Data hold time	$t_{HD;DAT}$	—	0	—	0.9	µs	—
31	Setup time of stop condition	$t_{SU;STO}$	—	0.6	—	—	µs	—
Charge pump								
32	Oscillation frequency	f_{CP}	—	—	1.25	—	MHz	—

■ Electrical Characteristics (Reference values for design) (Continued)

Note) Unless otherwise specified, T_a = 25°C±2°C, V_{CC} = 3.0 V,V_{CC_D} = 1.8 V, V_{BAT} =3.8 V
The characteristics listed below are reference values for design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, Panasonic will respond in good faith to user concerns.



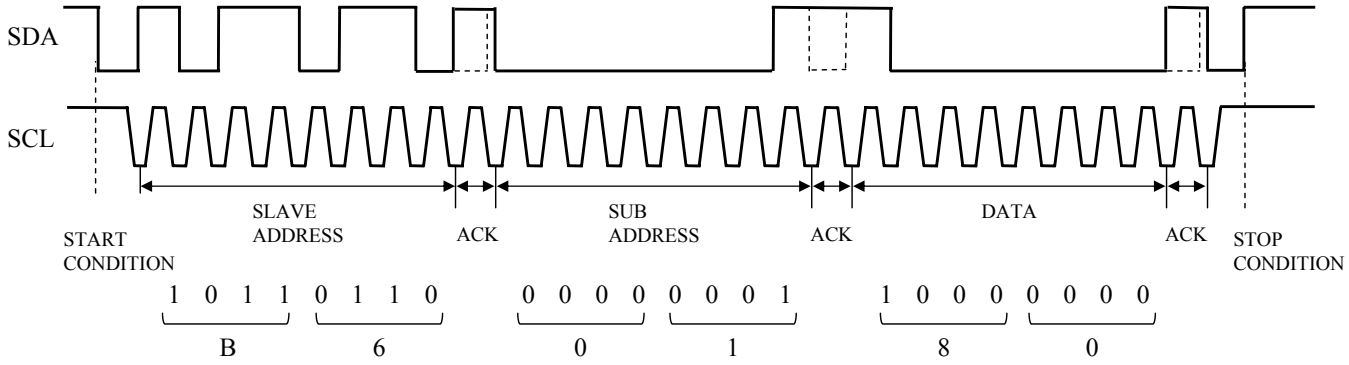
Note) 1. The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

2. *1: All values are V_{IHmin} (*2) and V_{ILmax} (*3) level standard.
*2: V_{IHmin} is the minimum limit of the signal input high level is indicated.
*3: V_{ILmax} is the maximum limit of the signal input low level is indicated.

■ Technical Data

1. I²C-bus Mode

1) Write Mode



Example of transmission messages

Two transmission messages (i.e. the SCL and SDA) are sent in synchronous serial transmission. The SCL is a clock with fixed frequency. The SDA indicates address data for the control of the reception side, and is sent in parallel in synchronization with the SCL. The data is transmitted in 8-bit, 3 octets (bytes) in principle, where every octet has an acknowledge bit. The following description provides information on the structure of the frame.

<Start Conditions>

When the level of the SDA changes to low from high while the level of the SCL is high, the data reception of the receiver will be enabled.

<Stop Conditions>

When the level of the SDA changes to high from low while the level of the SCL is high, the data reception of the receiver will be aborted.

<Slave Address>

The slave address is a specified one unique to each device. When the address of another device is sent, the reception will be aborted.

<Sub-Address>

The sub-address is a specified one unique to each function.

<Data>

Data is information under control.

<Acknowledge Bit>

The acknowledge bit is used to enable the master to acknowledge the reception of data for each octet. The master acknowledges the data reception of the receiver by transmitting a high-level signal to the receiver and receiving a low-level signal returned from the receiver as shown by the dotted lines in the above Fig. The communication will be aborted if the low signal is not returned.

The SDA will not change when the level of the SCL is high except start or stop conditions are enabled.

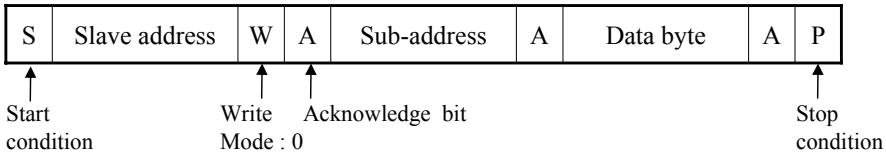
■ Technical Data (continued)

1. I²C-bus Mode (continued)

1) Write Mode (continued)

(a) I²C-bus PROTOCOL

- Slave address : 10110110 (B6Hex)
- Format (Normal)

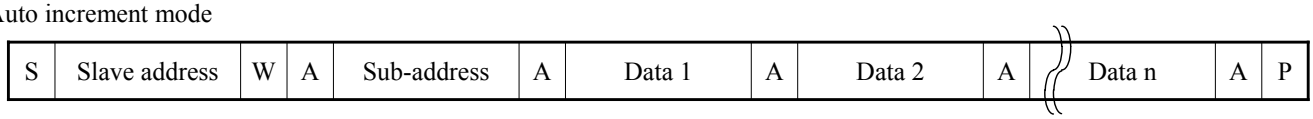


(b) Auto increment

Auto increment mode

(When the data is sent in sequence, the sub-address will change one by one and the data will be input.)

Auto increment mode



(c) Initial condition

The initial state of the device is not guaranteed. Therefore, the input of 00Hex resister-D0(Note.1) will be absolutely "0", when the power is turned ON.

(d) Sub-address Byte and Data Byte Format

Sub-address	MSB Data byte LSB							
	D7	D6	D5	D4	D3	D2	D1	D0
*0Hex	GAIN 0 → +20 dB 1 → +26 dB	0 (*1)	0 (*1)	0 (*1)	AGC 0 → OFF 1 → ON	SP Save 0 → ON 1 → OFF	All Standby 0 → ON 1 → OFF	0 (*1)
*1Hex	AGC-ON data bit3	AGC-ON data bit2	AGC-ON data bit1	AGC-REC data bit3	AGC-REC data bit2	AGC-REC data bit1	AGC-ATT data bit2	AGC-ATT data bit1
*2Hex	0 (*1,*2)	0 (*1,*2)	0 (*1,*2)	0 (*1,*2)	0 (*1,*2)	0 (*1,*2)	0 (*1,*2)	0 (*1,*2)

Note) *1: <00Hex Register>

D0, D4, D5, D6 : Always set to "0"

D1 : SP and charge-pump standby ON/OFF switch

D2 : SP Save ON/OFF switch

D3 : AGC ON/OFF switch

D7 : GAIN +20 dB / +26 dB selection

<01Hex Register>

D0, D1: AGC-attack-time selection

D2, D3, D4 : AGC-recovery-time selection

D5, D6, D7 : AGC-on-level selection

<02Hex Register>

D0 to D7 : Always set to "0". (test & adjust mode).

*2: Please use these bit only Data = "0", because they are used by our company's final test and fine-tuning AGC-on level. Note that Data = "1" is not shut-down mode.

■ Technical Data (continued)

1. I²C-bus Mode (continued)

1) Write Mode (continued)

(e) AGC-attack-time selection

Write 01Hex Register		Attack time
D1	D0	
0	0	0.5 ms
0	1	1 ms
1	0	2 ms
1	1	4 ms

(f) AGC-recovery-time selection

Write 01Hex Register			Recovery time
D4	D3	D2	
0	0	0	1.0 s
0	0	1	1.5 s
0	1	0	2.0 s
0	1	1	3.0 s
1	0	0	4.0 s
1	0	1	6.0 s

(g) AGC-on-level selection at V_{CC} = 3.0 V, V_{CC_D} = 1.8 V, V_{BAT} = 3.8 V *1

Write 01Hex Register			AGC On Level	Output (V[p-p])
D7	D6	D5		
0	0	0	12.6 dBV	12 V[p-p]
0	0	1	13.2 dBV	13 V[p-p]
0	1	0	13.9 dBV	14 V[p-p]
0	1	1	14.5 dBV	15 V[p-p]
1	0	0	15.1 dBV	16 V[p-p]
1	0	1	15.6 dBV	17 V[p-p]
1	1	0	16.1 dBV	18 V[p-p]
1	1	1	16.6 dBV	19 V[p-p]

Note) *1: At the time of V_{BAT} = 3.1 V, output is clipped, excessive clip in AGC OFF can be prevented.

(h) Amp. gain selection at V_{CC} = 3.0 V, V_{CC_D} = 1.8 V, V_{BAT} = 3.8 V

Write 00Hex Register	Gain
D7	
0	20 dB
1	26 dB

■ Technical Data (continued)

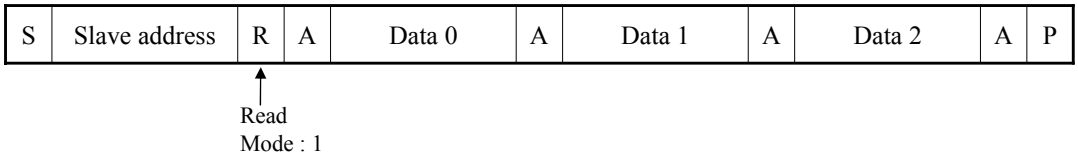
1. I²C-bus Mode (continued)

2) Read Mode

(a) I²C-bus PROTOCOL

Slave address 10110111(B7Hex)

Format



Note) At the slave address input, it is sequentially output from Data 0. There is no necessity for inputting the sub-address.

(b) Sub-address Byte and Data Byte Format

	MSB			Data byte				LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Data 0	Sub-address *0Hex Latch data D7	Sub-address *0Hex Latch data D6	Sub-address *0Hex Latch data D5	Sub-address *0Hex Latch data D4	Sub-address *0Hex Latch data D3	Sub-address *0Hex Latch data D2	Sub-address *0Hex Latch data D1	Sub-address *0Hex Latch data D0
Data 1	Sub-address *1Hex Latch data D7	Sub-address *1Hex Latch data D6	Sub-address *1Hex Latch data D5	Sub-address *1Hex Latch data D4	Sub-address *1Hex Latch data D3	Sub-address *1Hex Latch data D2	Sub-address *1Hex Latch data D1	Sub-address *1Hex Latch data D0
Data 2	Sub-address *2Hex Latch data D7	Sub-address *2Hex Latch data D6	Sub-address *2Hex Latch data D5	Sub-address *2Hex Latch data D4	Sub-address *2Hex Latch data D3	Sub-address *2Hex Latch data D2	Sub-address *2Hex Latch data D1	Sub-address *2Hex Latch data D0

■ Technical Data (continued)

2. Operating temperature guarantee of I²C-bus Control

The performance in the ambient temperature of operation is guaranteed theoretically in the design at normal temperature (25°C) by inspecting it at a speed of the clock that is about 50% earlier regarding the operating temperature guarantee of I²C-bus Control. But the following characteristics are logical values derived from the design of the IC and are not guaranteed by inspection. If a problem does occur related to these characteristics, Panasonic will respond in good faith to customer concerns.

3. Usage note of I²C-bus

1. The I²C bus of this product is designed to correspond to Standard mode(100 Kbps) and Fast mode(400 Kbps) in Philips Corporation I²C specification version 2.1. However, not correspond to High Speed mode (< 3.4Mbps).

2. This product operate as a slave device in I²C bus system.

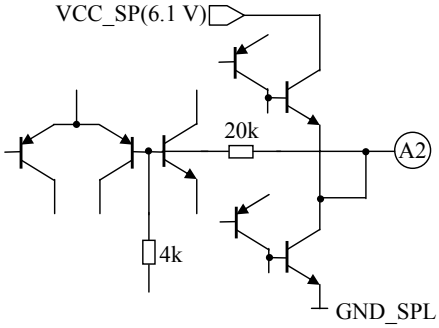
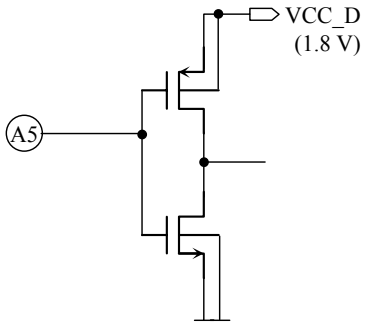
3. This product is not confirmed to operate in multi-master bus system and mixing -speed bus system. And this product is not confirmed connectivity to CBUS receiver. If using this product in these mode, please confirm availability to our company.

4. Purchase of Panasonic I²C components conveys a license to use these components in an I²C systems under the Philips I²C patent right on condition that using condition conform to I²C standard specification approved by Philips Corporation.

■ Technical Data (continued)

4. I/O block circuit diagram and pin function descriptions

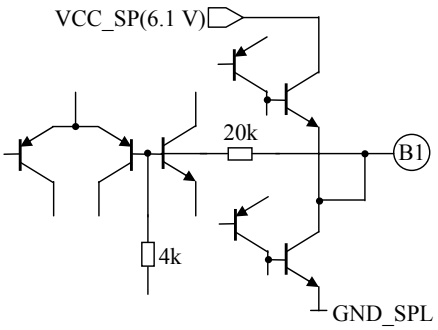
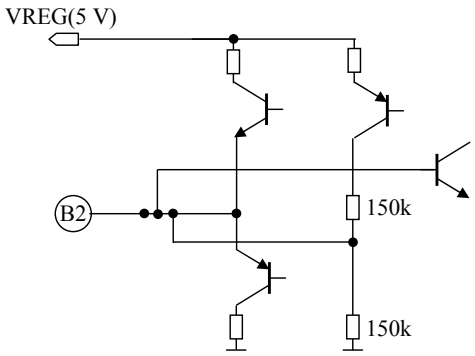
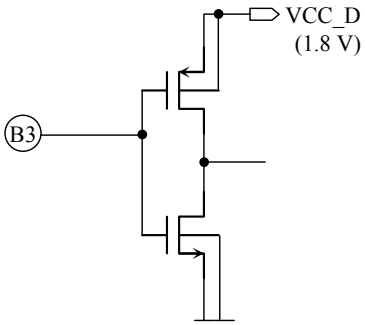
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
A1	GND_SPL DC 0 V	—	—	Ground pin for L-channel speaker output
A2	LOUT_POS  DC 2.7 V		Output impedance = Equal to or less than 1 Ω	L-channel positive speaker output pin
A3	VCC 3.0 V(typ.)	—	—	Power supply pin
A4	VCC_D 1.8 V(typ.)	—	—	Power supply pin for I^2C-BUS
A5	SCL  Hi-Z		Input impedance = Hi-Z	I^2C-BUS SCL pin
A6 B4 C4 D3 F1	GND DC 0 V	—	—	Ground pin.

■ Technical Data (continued)

4. I/O block circuit diagram and pin function descriptions (continued)

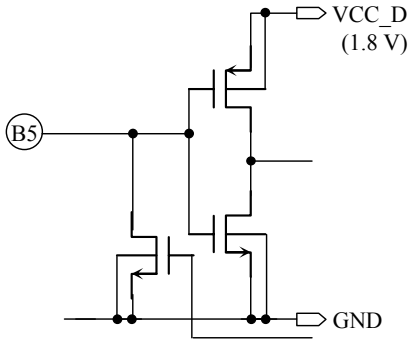
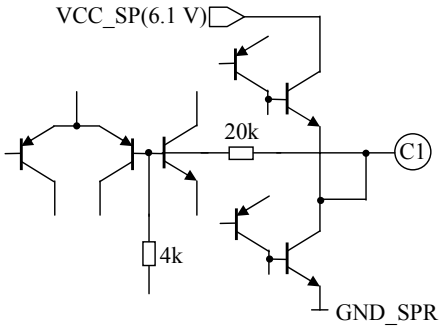
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
B1	LOUT_NEG  DC 2.7 V		Output impedance = Equal to or less than 1 Ω	L-channel negative speaker output pin
B2	VREF DC 2.5 V		Input impedance = About 75 kΩ	The reference voltage terminal for determining DC bias of the input stage of a speaker amplifier system. Please connect an external capacitor to remove a ripple.
B3	S.D Hi-Z		Input impedance = Hi-Z	Shut-down mode pin Please do not make it open, because the open S.D pin is not fixed.

■ Technical Data (continued)

4. I/O block circuit diagram and pin function descriptions (continued)

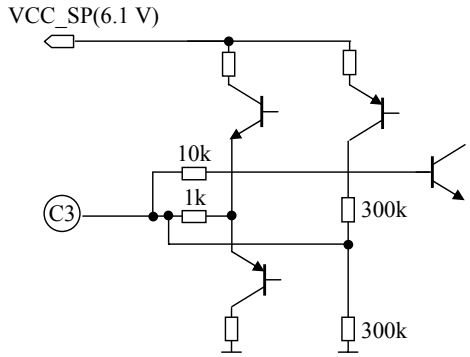
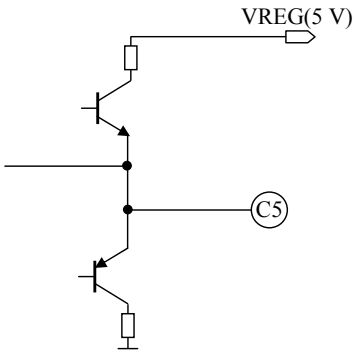
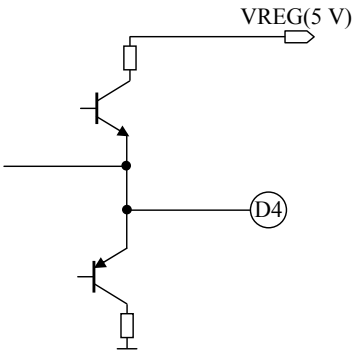
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
B5	SDA  Hi-Z		Input impedance = Hi-Z	I^2C-BUS SDA pin
B6 C6 D2 E2 E3	N.C.	—	—	N.C.
C1	ROUT_NEG  DC 2.7 V		Output impedance = Equal to or less than 1 Ω	R-channel negative speaker output pin
C2	$\frac{\text{VCC\_SP}}{2\times\text{VBAT}}$	—	—	Power supply pin for speaker output. Please connect to F2,F3 Pin (CPOUT), and connect an external capacitor to remove a rippule.

■ Technical Data (continued)

4. I/O block circuit diagram and pin function descriptions (continued)

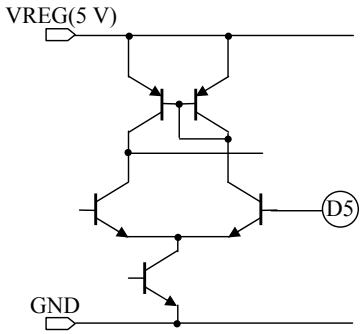
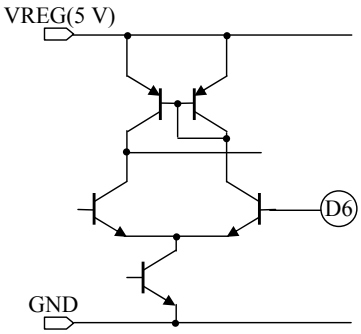
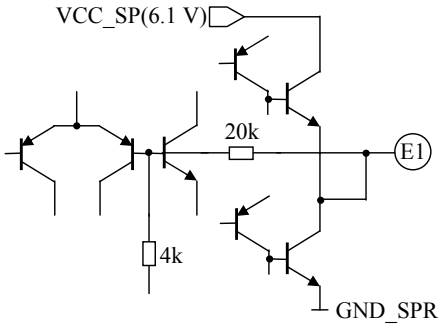
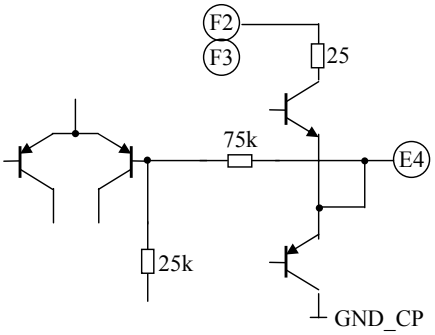
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
C3	VREF_SP DC 2.7 V		Input impedance = About 150 kΩ	The reference voltage terminal for determining DC bias of the output stage of a speaker amplifier system. Please connect an external capacitor to remove a ripple.
C5	PREOUT_L  DC 2.5 V		Output impedance = Equal to or less than 10 Ω	Output terminal of L-channel input amplifier of speaker amplifier system. Please connect external resistance for the gain setting.
D1	GND_SPR DC 0 V	—	—	GND pin for R-channel speaker output
D4	PREOUT_R  DC 2.5 V		Output impedance = Equal to or less than 10 Ω	Output terminal of R-channel input amplifier of speaker amplifier system. Please connect external resistance for the gain setting.

■ Technical Data (continued)

4. I/O block circuit diagram and pin function descriptions (continued)

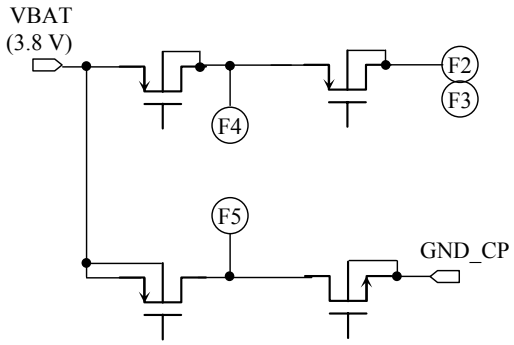
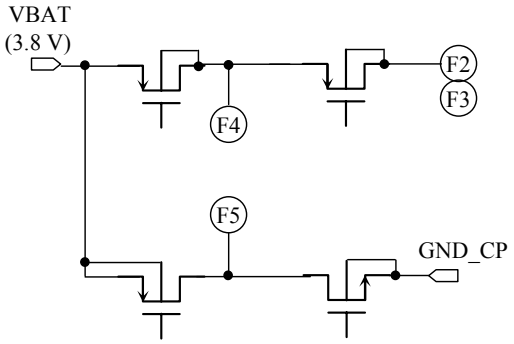
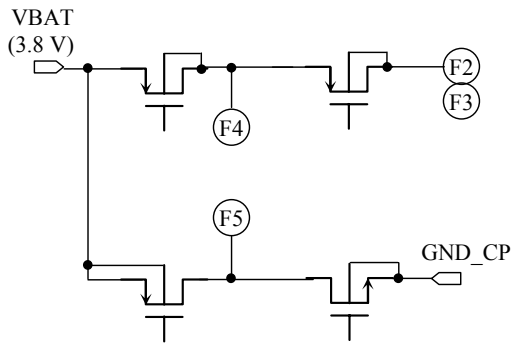
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
D5	FB_R DC 2.5 V		Input impedance = Hi-Z	Feedback terminal of R-channel input amplifier of speaker amplifier system. The gain of the R-channel input amplifier can be set by connecting an external resistance between Pin D4 and Pin D5.
D6	FB_L DC 2.5 V		Input impedance = Hi-Z	Feedback terminal of L-channel input amplifier of speaker amplifier system. The gain of the L-channel input amplifier can be set by connecting an external resistance between Pin C4 and Pin C5.
E1	ROUT_POS  DC 2.7 V		Output impedance = Equal to or less than 1 Ω	R-channel positive speaker output pin
E4	VREG_PRED DC CPOUT * 0.45		Output impedance = Equal to or less than 1	VREG capacitor pin for charge pump gate-driver

■ Technical Data (continued)

4. I/O block circuit diagram and pin function descriptions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
E5 E6	VBAT 3.8 V(typ.)	—	—	Power supply pin
F2 F3	CPOUT VBAT*2		1 Ω ≤	Charge-pump output pin Please connect an external capacitor to remove a ripple.
F4	C1P 1.25MHz VBAT to CPOUT		1 Ω ≤	Charge-pump flying capacitor connect pin.
F5	C1N 1.25MHz GND to VBAT		1 Ω ≤	Charge-pump flying capacitor connect pin.
F6	GND_CP DC 0 V	—	—	Ground pin for charge-pump.

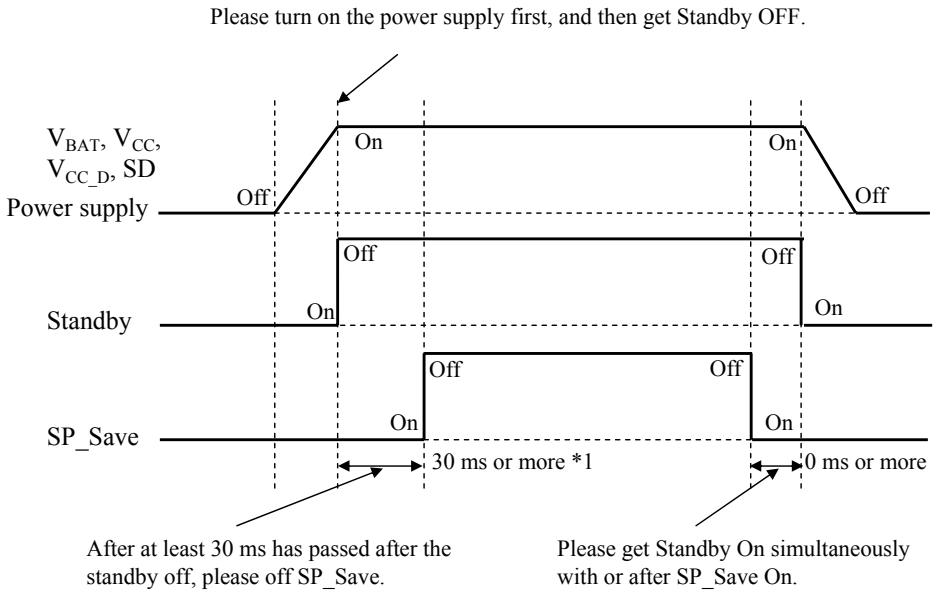
■ Technical Data (continued)

5. Power supply and logic sequence

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

The timing control of power-ON/OFF and each logic according to the procedure below should be recommended for the best pop performance caused in switching.

1) The sequence of the power supply and each logic



The basic procedure at the power-on

1. The power OFF condition.
   Both the Standby and the SP_Save are in the ON condition.
2. Power ON
3. Standby OFF
4. SP_Save OFF

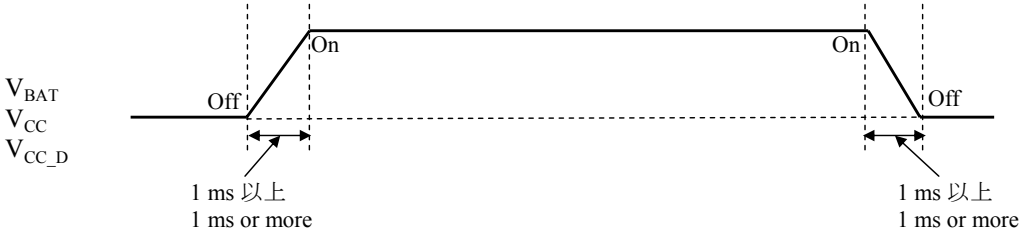
The basic procedure at the power-off

1. The power ON condition.
   Both the Standby and the SP_Save are in the OFF condition.
2. SP_Save ON (= Standby ON)
3. Standby ON
4. Power OFF

Note) *1: This IC contains the pre-charge circuit. It is time until each bias is stabilized from Standby Off. It depends for this time on the capacity value linked to a reference voltage terminal (VREF and VREFSP), and the capacity value and resistance linked to an input terminal (IN_R and IN_L). It is a recommendation value in a constant given in the example of an application circuit (block diagram).

2) The sequence of V_{BAT} and V_{CC} and V_{CC_D}

This IC does not have a rising and falling order in V_{BAT} and V_{CC} and V_{CC_D}.
Rising and falling times of them are recommended 1 ms or more.

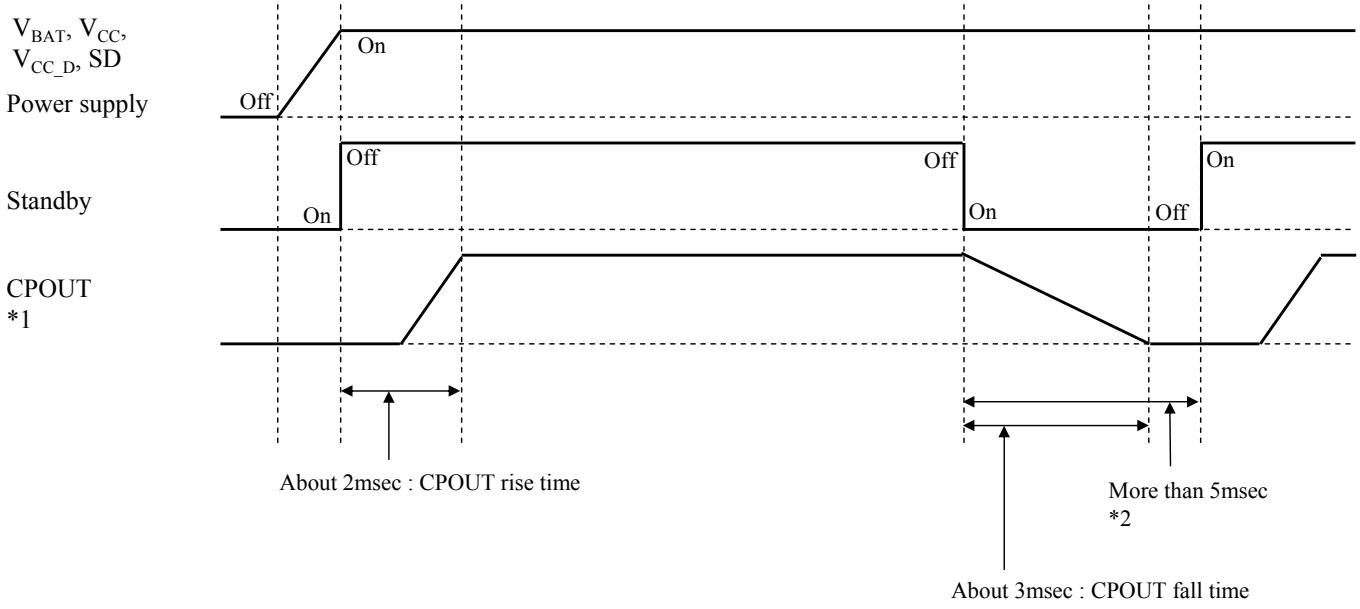


■ Technical Data (continued)

5. Power supply and logic sequence (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

3) The sequence of the charge-pump.



Note) *1: Charge-pump output CPOUT almost outputs the voltage of VBAT at the time of Standby. Also, it has a built-in discharge circuit of CPOUT pin and operates discharge to CPOUT < (V_{BAT} + 0.9 [V]) at the time of Standby.

*2: Please take more than 5msec between Standby Off and next Standby On.

■ Technical Data (continued)

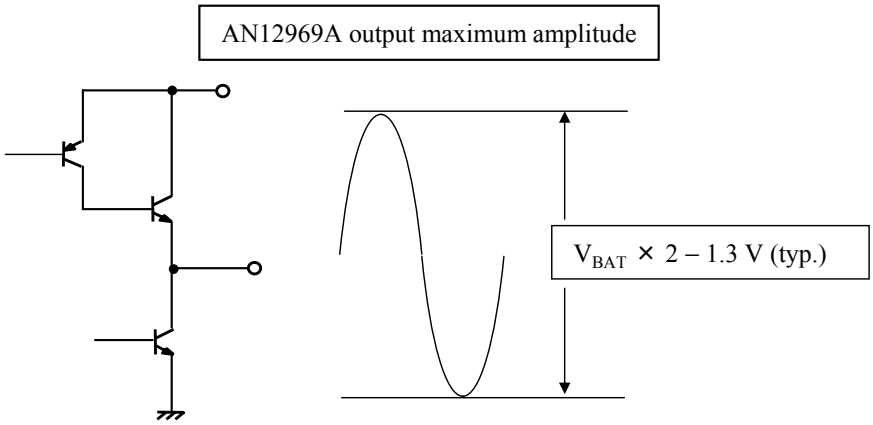
6. Explanation on mainly functions

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

6.1 Power supply

1) Power supply for output amplifier

The output amplifier operates with voltage applied to V_{CC_SP}. V_{CC_SP} is supplied from built-in charge-pump with output voltage of twice V_{BAT}.



2) Power supply for control system

The control system operates with power supply applied to V_{CC} pin. (I^2C logic, clock generation circuit, etc.)

3) Power supply for signal system

The signal system operates with the internal regulator of 5 V. 5 V, reference voltage of the internal regulator is generated from V_{CC_SP} using V_{CC} power supply. By setting signal voltage at 5 V, the dynamic range of the signal can be secured sufficiently. When the gain of the input amplifier is 0 dB, clip occurs at the amplitude of 3 V[p-p] (typ.) in input signal.

4) Power supply for I^2C interface

I^2C interface operates with power supply applied to V_{CC_D} pin. I^2C circuit operates with V_{CC}.

5) High voltage at shut-down pin

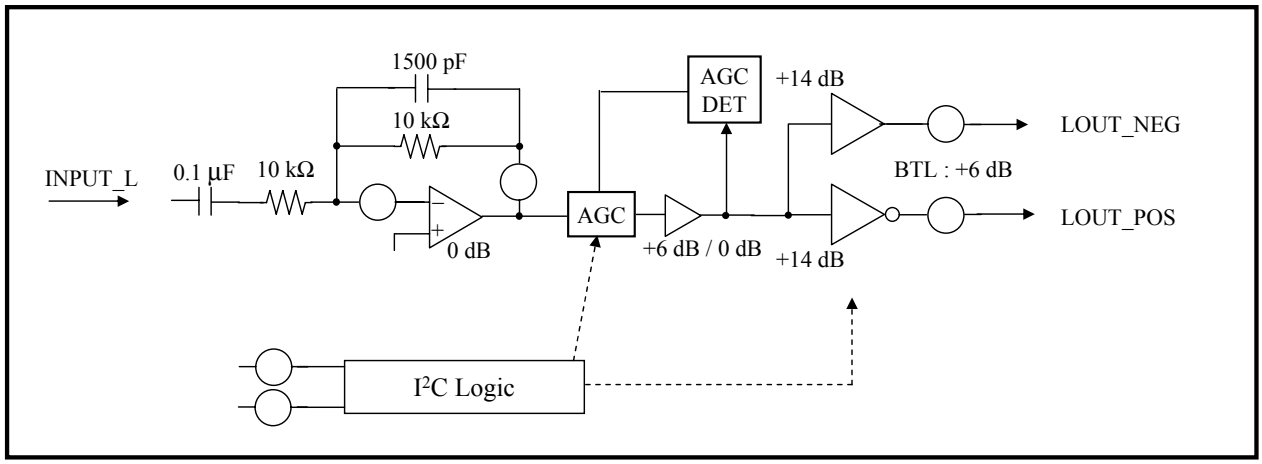
Please use the power supply applied to V_{CC_D} or apply voltage from the outside. Threshold voltage depends on the voltage to V_{CC_D}.

■ Technical Data (continued)

6. Explanation on mainly used functions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

6.2 Speaker amplifier

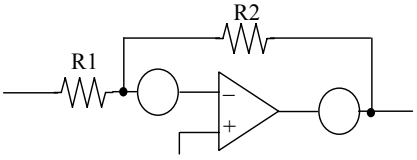


1) The gain for a speaker amplifier can be adjusted, as the gain for a input amplifier can be set with an external resistance. Input impedance is also set with the external resistance. When the gain for the input amplifier is set at ±0 dB, the total gain for the speaker amplifier is +26 dB or +20 dB (It can be selected with I^2C).

When the external resistance for the input amplifier is assumed as R1, R2,

$$\text{Gain} = 20 \log(R2 / R1)$$

$$\text{Zin} = R1$$

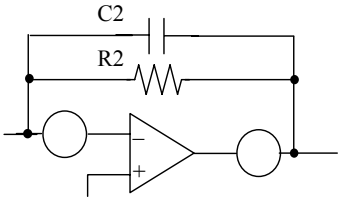


In case of R1 = 10 kΩ, R2 = 10 kΩ with the constants in the above fig, the gain for the input amplifier is ±0 dB and impedance is 10 kΩ. During operation, keep the voltage of R1 and R2 at more than 5 kΩ.

2) With an external capacity added to the input amplifier, LPF, which removes an unwanted high frequency element, can be constructed.

When external resistance is assumed as R2, capacity as C2,

$$fc = 1 / (2 \pi \times R2 \times C2)$$



In case of R2 = 10 kΩ, C2 = 1500 pF with the constants in the above fig, Cut-off frequency, fc is 10.6 kHz.

■ Technical Data (continued)

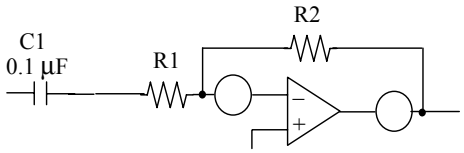
6. Explanation on mainly used functions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

6.2 Speaker amplifier (continued)

3) With the smaller capacity of the input AC coupling capacitor, HPF, which removes unwanted low frequency element, can be constructed. When input resistance is assumed as R1, and AC coupling capacitor as C1,

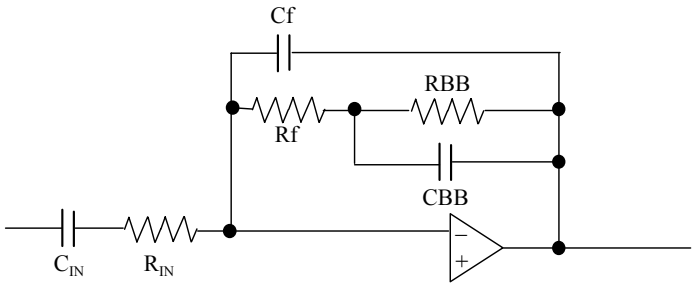
$$fc = 1 / (2 \pi \times R1 \times C1)$$



In case of R1 = 10 kΩ, C1 = 0.1 μF, cut-off frequency, fc is 160 Hz.
In case of R1 = 10 kΩ, C1 = 0.022 μF, cut-of frequency, fc is 720 Hz.

4) Bus Boost circuit can be constructed by adding capacity (RBB) and resistance (CBB) to the input amplifier.
The frequency to increase 3 dB is assumed as fo

fo =	$1 / (2 \times \pi \times Rf \times CBB)$
Bus Boost Gain	20 log ((Rf + RBB) / Rf)
Ao =	20 log ((Rf + RBB) / Rin)



6.3 Protection circuit for speaker amplifier

1) Thermal protection circuit
The thermal protection circuit operates at the T_j of approximately 150°C. The thermal protection circuit is reset automatically when the temperature drops.

2) Output pin short protection circuit
Output pin-power supply line short protection
Output-to-output pin short protection
Output pin-GND line short protection

If short-circuit is no longer detected, it will return automatically.

Note) Operation is not guaranteed although the protection circuit is built in. Moreover, hundred percent inspection is not guaranteed.

■ Technical Data (continued)

6. Explanation on mainly used functions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

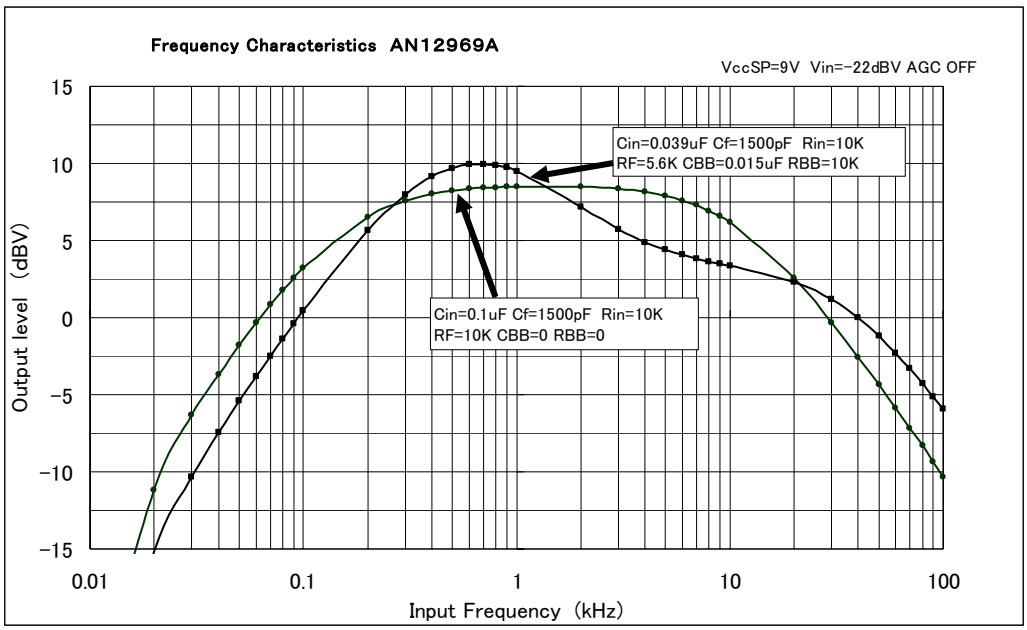
6.4 Cautions

1) Cautions about AGC

Signal output in the input amplifier is detected and converted to forward current. Compared this forward current with reference voltage, if the forward current is larger, AGC turns ON.
When the frequency band of the speaker is narrower than that of the amplifier.
If maximum input is made in low frequency band, AGC operates to decrease volume. Namely, low sound part is not heard from a speaker, but AGC reacts to low sound part to turn down the volume. Please carefully design so that the frequency bands is synchronized between the speaker and amplifier.

Note) Frequency characteristics should be set not only for the speaker, but in the built-in condition

The below Graph shows when the values of resistance and capacity are changed.

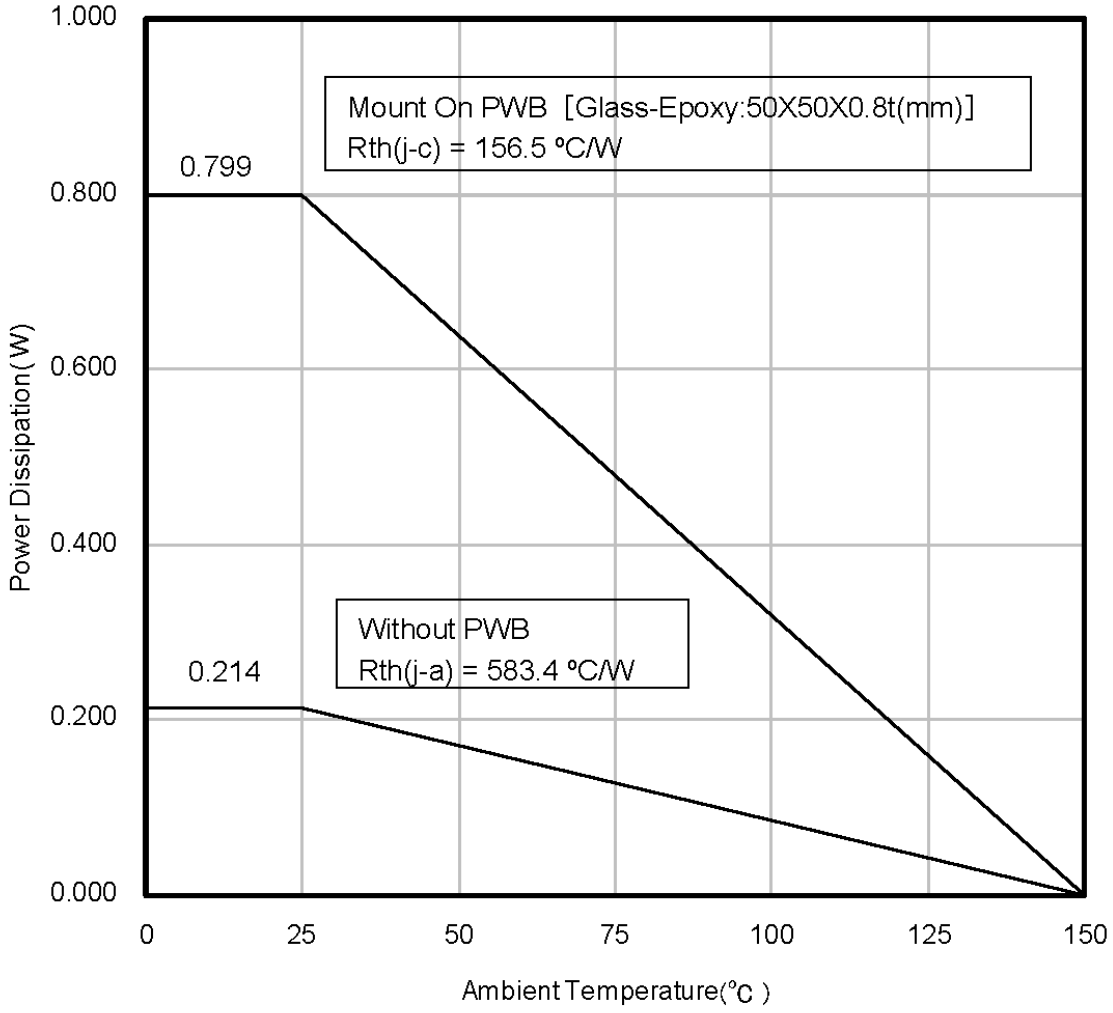


2) Cautions about shut-down with SD pin

During normal operation, when a shut-down pin is turned Low directly, shock noise comes out.
As SP_Save is set in mute, first turn ON SP_Save, and then turn ON Standby to stop operation. Finally, set shut-down pin to Low.

■ Technical Data (continued)

7. P_D — T_a diagram



■ Usage Notes

1. This IC is intended to be used for general electronic equipment [cellular phones].
   Consult our sales staff in advance for information on the following applications:
   • Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   • Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required

2. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.

3. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

4. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.

5. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-V_{CC} short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .
   And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

6. When using the LSI for new models, verify the safety including the long-term reliability for each product.

7. When the application system is designed by using this LSI, be sure to confirm notes in this book.
   Be sure to read the notes to descriptions and the usage notes in the book.

8. Please carry out the thermal design with sufficient margin such that the power dissipation will not be exceeded, based on the conditions of power supply, load and surrounding temperature. Although indicated also in the column of the maximum rating, the maximum rating becomes an instant and the marginal value which must not exceed. It sufficiently evaluates, and I use-wish-do so that it may not exceed certainly. Moreover, don't impress neither voltage nor current to PIN which is not indicated. It may destroy in both cases.

9. Please do not make it open, because the open SD pin (Pin B3) is not fixed.

Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.

(3) The products described in this book are intended to be used for standard applications or general electronic equipment (such as office equipment, communications equipment, measuring instruments and household appliances).
Consult our sales staff in advance for information on the following applications:
- Special applications (such as for airplanes, aerospace, automobiles, traffic control equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.
- Any applications other than the standard applications intended.

(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

(7) This book may be not reprinted or reproduced whether wholly or partially, without the prior written permission of our company.

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