QL24x32B
pASIC® 1 Family
Very-High-Speed CMOS FPGA

pASIC HIGHLIGHTS

...8,000 usable ASIC gates, 180 I/O pins
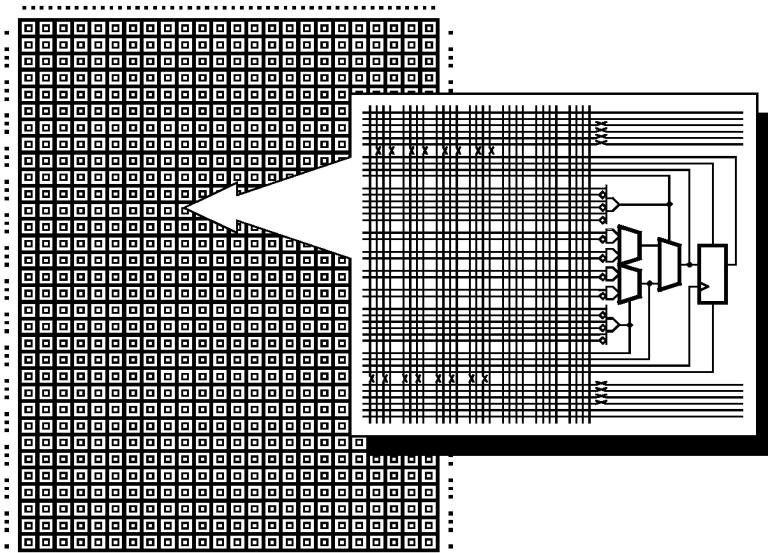
☒ **Very High Speed** – ViaLink® metal-to-metal programmable–via antifuse technology, allows counter speeds over 150 MHz and logic cell delays of under 2 ns.

☒ **High Usable Density** – An 24-by-32 array of 768 logic cells provides 8,000 usable ASIC gates (14,000 PLD gates) in 144-pin TQFP, 208-pin PQFP and 208-pin CQFP packages.

☒ **PCI-Output Drive** – Fully PCI 2.1 compliant input/output capability. (including drive current)

☒ **Low-Cost, Easy-to-Use Design Tools** – Designs entered and simulated using QuickLogic's new Quick*Works*® development environment, or with third-party CAE tools including Viewlogic, Synopsys, Mentor, Cadence and Veribest. Fast, fully automatic place and route on PC and workstation platforms using QuickLogic software.

4

pASIC 1

QL24x32B Block Diagram

768 Logic Cells

▪ = Up to 172 prog. I/O cells, 6 Input high-drive cells, 2 Input/Clk (high-drive) cells

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4-31

PRODUCT SUMMARY

The QL24x32B is a member of the pASIC 1 Family of very-high-speed CMOS user-programmable ASIC devices. The 768 logic cell field-programmable gate array (FPGA) offers 8,000 usable ASIC gates (equivalent to 14,000 PLD gates) of high-performance general-purpose logic in 144-pin TQFP and 208-pin PQFP and CQFP packages.

Low-impedance, metal-to-metal, ViaLink interconnect technology provides nonvolatile custom logic capable of operating above 150 MHz. Logic cell delays under 2 ns, combined with input delays of under 1.5 ns and output delays under 3 ns, permit high-density programmable devices to be used with today's fastest microprocessors and DSPs.

Designs can be entered using QuickLogic's Quick*Works* Toolkit or most populart third-party CAE tools. Quick*Works* combines Verilog/VHDL design entry and simulation tools with device-specific place & route and programming software. Ample on-chip routing channels allow fast, fully automatic place and route of designs using up to 100% of the logic and I/O cells, while maintaining fixed pin-outs
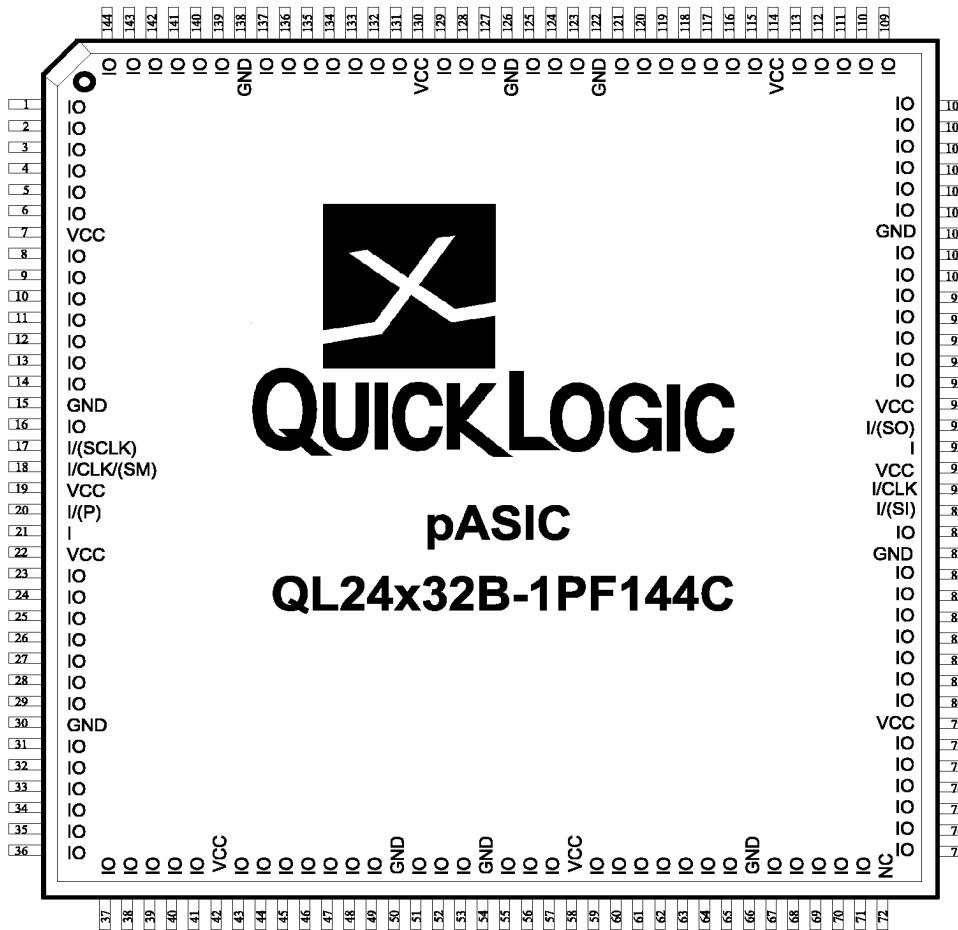
FEATURES
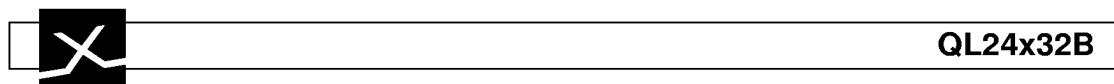
- Total of 180 I/O pins
  - 172 Bidirectional Input/Output pins
  - 6 Dedicated Input/High-Drive pins
  - 2 Clock/Dedicated input pins with fanout-independent, low-skew clock networks
  - PCI 2.1 Compliant I/Os
- Input + logic cell + output delays under 6 ns
- Chip-to-chip operating frequencies up to 110 MHz
- Internal state machine frequencies up to 150 MHz
- Clock skew < 0.5 ns
- Input hysteresis provides high noise immunity
- Built-in scan path permits 100% factory testing of logic and I/O cells and functional testing with Automatic Test Vector Generation (ATVG) software after programming
- 144-pin TQFP compatible with QL16x24B
- 0.65μ CMOS process with ViaLink programming technology
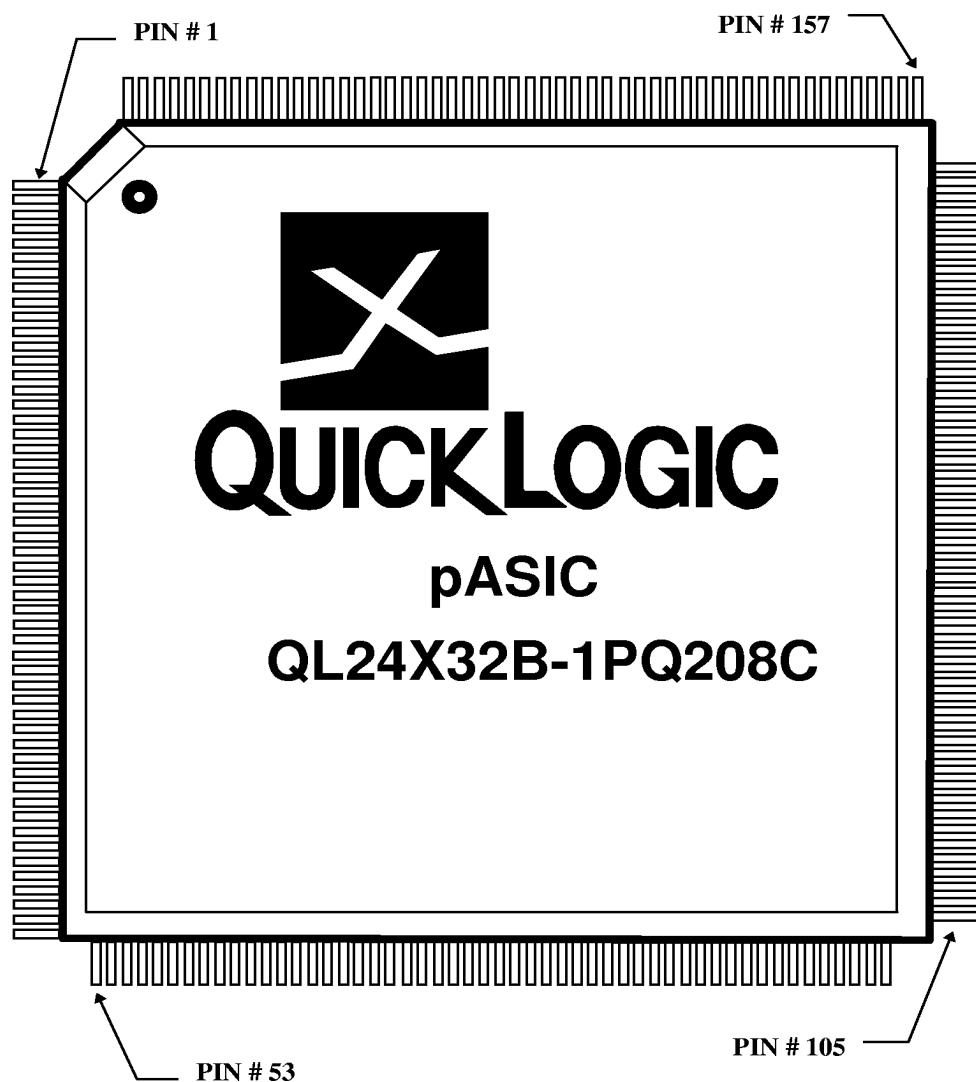
**Pinout
Diagram
144-pin TQFP**

Pinout Diagram for QL24x32B-1PF144C pASIC, 144-pin TQFP

4

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**Pinout Diagram
208-pin PQFP/CQFP**

PIN # 1

PIN # 157

PIN # 53

PIN # 105

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QL24X32B-1PQ208C

PQFP/CQFP 208 Function/Connector Table

PIN	FUN	PIN	FUN	PIN	FUN	PIN	FUN	PIN	FUN	PIN	FUN	PIN	FUN	PIN	FUN
1	I/O	27	VCC	53	I/O	79	I/O	105	I/O	131	VCC	157	I/O	183	I/O
2	I/O	28	I/P	54	I/O	80	I/O	106	I/O	132	I	158	I/O	184	I/O
3	I/O	29	I	55	I/O	81	I/O	107	I/O	133	I/SO	159	I/O	185	I/O
4	I/O	30	VCC	56	I/O	82	I/O	108	I/O	134	VCC	160	I/O	186	I/O
5	I/O	31	I/O	57	I/O	83	VCC	109	I/O	135	I/O	161	I/O	187	VCC
6	I/O	32	I/O	58	I/O	84	I/O	110	I/O	136	I/O	162	I/O	188	I/O
7	I/O	33	I/O	59	GND	85	I/O	111	I/O	137	I/O	163	GND	189	I/O
8	I/O	34	I/O	60	I/O	86	I/O	112	I/O	138	I/O	164	I/O	190	I/O
9	I/O	35	I/O	61	VCC	87	I/O	113	I/O	139	I/O	165	VCC	191	I/O
10	VCC	36	I/O	62	I/O	88	I/O	114	VCC	140	I/O	166	I/O	192	I/O
11	I/O	37	I/O	63	I/O	89	I/O	115	I/O	141	I/O	167	I/O	193	I/O
12	GND	38	I/O	64	I/O	90	I/O	116	GND	142	I/O	168	I/O	194	I/O
13	I/O	39	I/O	65	I/O	91	I/O	117	I/O	143	I/O	169	I/O	195	I/O
14	I/O	40	I/O	66	I/O	92	I/O	118	I/O	144	I/O	170	I/O	196	I/O
15	I/O	41	VCC	67	I/O	93	I/O	119	I/O	145	VCC	171	I/O	197	I/O
16	I/O	42	I/O	68	I/O	94	I/O	120	I/O	146	I/O	172	I/O	198	I/O
17	I/O	43	GND	69	I/O	95	GND	121	I/O	147	GND	173	I/O	199	GND
18	I/O	44	I/O	70	I/O	96	I/O	122	I/O	148	I/O	174	I/O	200	I/O
19	I/O	45	I/O	71	I/O	97	VCC	123	I/O	149	I/O	175	I/O	201	VCC
20	I/O	46	I/O	72	I/O	98	I/O	124	I/O	150	I/O	176	I/O	202	I/O
21	I/O	47	I/O	73	GND	99	I/O	125	I/O	151	I/O	177	GND	203	I/O
22	I/O	48	I/O	74	I/O	100	I/O	126	I/O	152	I/O	178	I/O	204	I/O
23	GND	49	I/O	75	I/O	101	I/O	127	GND	153	I/O	179	I/O	205	I/O
24	I/O	50	I/O	76	I/O	102	I/O	128	I/O	154	I/O	180	I/O	206	I/O
25	I/Sck	51	I/O	77	I/O	103	I/O	129	I/SI	155	I/O	181	I/O	207	I/O
26	I/Clk	52	I/O	78	GND	104	I/O	130	I/Clk	156	I/O	182	GND	208	I/O

4

pASIC 1

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... −0.5 to 7.0 V
Input Voltage .... −0.5 to VCC +0.5 V
ESD Pad Protection .... ±2000 V
DC Input Current .... ±20 mA
Latch-up Immunity .... ±200 mA

Storage Temperature .... −65°C to + 150°C
Lead Temperature .... 300°C

OPERATING RANGE

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min	Max	Min	Max	Min	Max	
VCC	Supply Voltage		4.5	5.5	4.5	5.5	4.75	5.25	V
TA	Ambient Temperature		-55		-40	85	0	70	°C
TC	Case Temperature			125					°C
K	Delay Factor	-X Speed Grade			0.4	2.75	0.46	2.55	
		-0 Speed Grade	0.39	1.82	0.4	1.67	0.46	1.55	
		-1 Speed Grade	0.39	1.56	0.4	1.43	0.46	1.33	
		-2 Speed Grade			0.4	1.35	0.46	1.25	

DC CHARACTERISTICS over operating range

Symbol	Parameter	Conditions	Min	Max	Unit
VIH	Input HIGH Voltage		2.0		V
VIL	Input LOW Voltage			0.8	V
VOH	Output HIGH Voltage [0]	IOH = -4 mA	3.7		V
		IOH = 16 mA	2.4		V
		IOH = -10 μA	VCC-0.1		V
VOL	Output LOW Voltage [0]	IOL = 24 mA*		0.4	V
		IOL = 10 μA		0.1	V
II	Input Leakage Current	VI = VCC or GND	-10	10	μA
IOZ	3-State Output Leakage Current	VI = VCC or GND	-10	10	μA
CI	Input Capacitance [1]			10	pF
IOS	Output Short Circuit Current [2]	VO = GND	-10	-90	mA
		VO = VCC	40	160	mA
ICC	D.C. Supply Current [3]	VI, VIO = VCC or GND		10	mA

*IOL = 24 mA for commercial range only. IOL = 12 mA for the industrial and military ranges.

Notes:

[1] Capacitance is sample tested only. CI = 20 pF max on I/(SI).
[2] Only one output at a time. Duration should not exceed 30 seconds.
[3] Commercial temperature grade only. Maximum Icc for industrial grade is 15mA and for military grade is 20 mA. For AC conditions use the formula described in the Section 9 — Power vs Operating Frequency.
[4] Stated timing for worst case Propagation Delay over process variation at VCC = 5.0V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.
[5] These limits are derived from a representative selection of the slowest paths through the pASIC logic cell *including net delays*. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

AC CHARACTERISTICS at VCC = 5V, TA = 25°C (K = 1.00)

Logic Cell

Symbol	Parameter	Propagation Delays (ns) Fanout				
		1	2	3	4	8
tPD	Combinatorial Delay [5]	1.7	2.1	2.7	3.3	5.5
tSU	Setup Time [5]	2.1	2.1	2.1	2.1	2.1
tH	Hold Time	0.0	0.0	0.0	0.0	0.0
tCLK	Clock to Q Delay	1.0	1.5	1.9	2.7	4.9
tCWHI	Clock High Time	2.0	2.0	2.0	2.0	2.0
tCWLO	Clock Low Time	2.0	2.0	2.0	2.0	2.0
tSET	Set Delay	1.7	2.2	2.7	3.3	5.5
tRESET	Reset Delay	1.5	1.9	2.3	2.8	4.6
tSW	Set Width	1.9	1.9	1.9	1.9	1.9
tRW	Reset Width	1.8	1.8	1.8	1.8	1.8

Input Cells
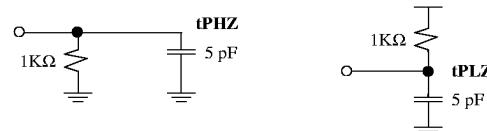
Symbol	Parameter	Propagation Delays (ns) [4]						
		1	2	3	4	8	12	16
tIN	High Drive Input Delay [6]	3.1	3.2	3.3	3.4	4.4	5.8	6.5
tINI	High Drive Input, Inverting Delay [6]	3.3	3.4	3.5	3.6	4.6	6.0	6.7
tIO	Input Delay (bidirectional pad)	1.4	1.9	2.3	3.0	4.8	6.7	8.5
tGCK	Clock Buffer Delay [7]	2.7	2.8	2.9	3.0	3.1	3.3	3.4
tGCKHI	Clock Buffer Min High [7]	2.0	2.0	2.0	2.0	2.0	2.0	2.0
tGCKLO	Clock Buffer Min Low [7]	2.0	2.0	2.0	2.0	2.0	2.0	2.0

Output Cell

Symbol	Parameter	Propagation Delays (ns) [4] Output Load Capacitance (pF)				
		30	50	75	100	150
tOUTLH	Output Delay Low to High	2.7	3.3	3.8	4.3	5.4
tOUTHL	Output Delay High to Low	2.8	3.6	4.5	5.3	6.9
tPZH	Output Delay Tri-state to High	2.1	2.6	3.1	3.7	4.8
tPZL	Output Delay Tri-state to Low	2.6	3.3	4.1	4.9	6.5
tPHZ	Output Delay High to Tri-state [8]	2.9				
tPLZ	Output Delay Low to Tri-state [8]	3.3				

Notes:

[6] See High Drive Buffer Table for more information.

[7] Clock buffer fanout refers to the maximum number of flip flops per half column. The number of half columns used does not affect clock buffer delay.

[8] The following loads are used for tPXZ:

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High Drive Buffer

Symbol	Parameter	Clock Drivers Wired Together	Propagation Delays (ns) [4]				
			Fanout				
			12	24	48	72	96
tIN	High Drive Input Delay	1	5.8	7.2			
		2		5.0	7.1		
		3			5.8	6.7	7.7
		4				5.9	6.8
tINI	High Drive Input, Inverting Delay	1	6.0	7.4			
		2		5.2	7.3		
		3			6.0	6.9	7.9
		4				6.1	7.0

AC Performance

Propagation delays depend on routing, fanout, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified in the Delay Factor table (Operating Range). The effects of voltage and temperature variation are illustrated in the graphs on page 4-47, K Factor versus Voltage and Temperature. The pASIC Development Tools incorporate data sheet AC Characteristics into the QDIF database for pre-place-and-route timing analysis. The SpDE Delay Modeler extracts specific timing parameters for precise path analysis or simulation results following place and route.

ORDERING INFORMATION

QL 24x32B - 1 PQ208 C

QuickLogic pASIC device

pASIC device part number
B = 0.65 micron CMOS

Speed Grade
X = quick
0 = fast
1 = faster
2 = fastest

Operating Range
C = Commercial
I = Industrial
M = Military
M/883C = MIL STD 883

Package Code
PF144 = 144-pin TQFP
PQ208 = 208-pin PQFP
CF208 = 208-pin CQFP