

2.5 V 200-pin DDR Small Outline SDRAM Modules

512MB Modules

PC1600, PC2100 & PC2700

Preliminary Datasheet Rev. 0.9

- 200-pin Unbuffered 8-Byte Dual-In-Line DDR-I SDRAM non-parity Small Outline Modules
- Two bank 64Mx64 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR-I SDRAM)
- Single + 2.5 V (± 0.2 V) power supply
- Built with 512 Mbit DDR-I SDRAMs organised as x 16 in 66-Lead TSOPII packages
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Serial Presence Detect with E²PROM
- Jedec standard form factor: 67.60 mm \times 31.75 mm \times 3.00 / 3.80 mm
- Jedec standard reference layout Raw Card A
- Gold plated contacts

Performance:

		-6	-7	-8	Unit
	Component Speed Grade	DDR333	DDR266A	DDR200	
	Module Speed Grade	PC2700	PC2100	PC1600	
f_{CK}	Clock Frequency (max.) @ CL = 2.5	166	143	125	MHz
f_{CK}	Clock Frequency (max.) @ CL = 2	133	133	100	MHz

The HYS64Dxx0x0GDL are industry standard 200-pin 8-byte Small Outline Dual in-line Memory Modules (DIMMs) organized as 64M x 64. The memory array is designed with Double Data Rate Synchronous DRAMs. A variety of decoupling capacitors are mounted on the PC board. The DIMMs feature serial presence detect based on a serial E²PROM device using the 2-pin I²C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

Ordering Information

Type	Compliance Code	Description	SDRAM Technology
PC2700 (CL=2.5):			
HYS64D64020GDL-6-A	PC2700-25330-A	two banks 512 MB SO-DIMM	512 MBit (x16)
PC2100 (CL=2):			
HYS64D64020GDL-7-A	PC2100-20330-A	two banks 512 MB SO-DIMM	512 MBit (x16)
PC1600 (CL=2):			
HYS64D64020GDL-8-A	PC1600-20220-A	two banks 512 MB SO-DIMM	512 MBit (x16)

Note: All part numbers end with a place code, designating the silicon-die revision. Reference information available on request. Example: HYS 64D32020GDL-8-A, indicating Rev.A die are used for DDR-SDRAM components.

The Compliance Code which is printed on the module labels describes the speed sort class ("f.e. PC2100"), the latencies (f.e. 20330 means CAS latency = 2, trcd latency = 3 and trp latency = 3) and the Raw Card used for this module

Pin Definitions and Functions

A0 - A12	Address Inputs	CS0, CS1 *)	Chip Selects
BA0, BA1	Bank Selects	V _{DD}	Power (+ 2.5 V)
DQ0 - DQ63	Data Input/Output	V _{SS}	Ground
$\overline{\text{RAS}}$	Row Address Strobe	V _{DDQ}	I/O Driver power supply
$\overline{\text{CAS}}$	Column Address Strobe	V _{DDID}	VDD Identification flag
$\overline{\text{WE}}$	Read/Write Input	V _{REF}	I/O reference supply
CKE0 - CKE1	Clock Enable	V _{DDSPD}	Serial EEPROM power supply
DQS0 - DQS8	SDRAM low data strobes	SCL	Serial bus clock
CLK0 - CLK1,	SDRAM clock (positive lines)	SDA	Serial bus data line
$\overline{\text{CLK0}}$ - $\overline{\text{CLK1}}$	SDRAM clock (negative lines)	SA0 - SA2	slave address select
DM0 - DM8	data masks	NC	no connect
DQS0 - DQS8	data strobes	DU	Dont use, reserved for future use

*) CKE1 and $\overline{\text{CS1}}$ are used on two bank modules only

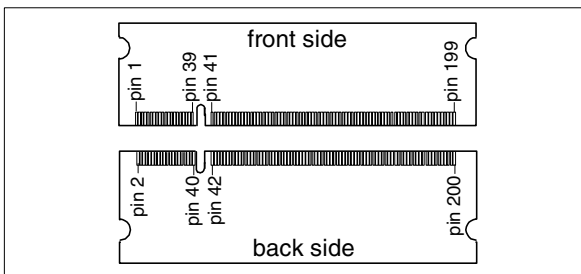
Address Format

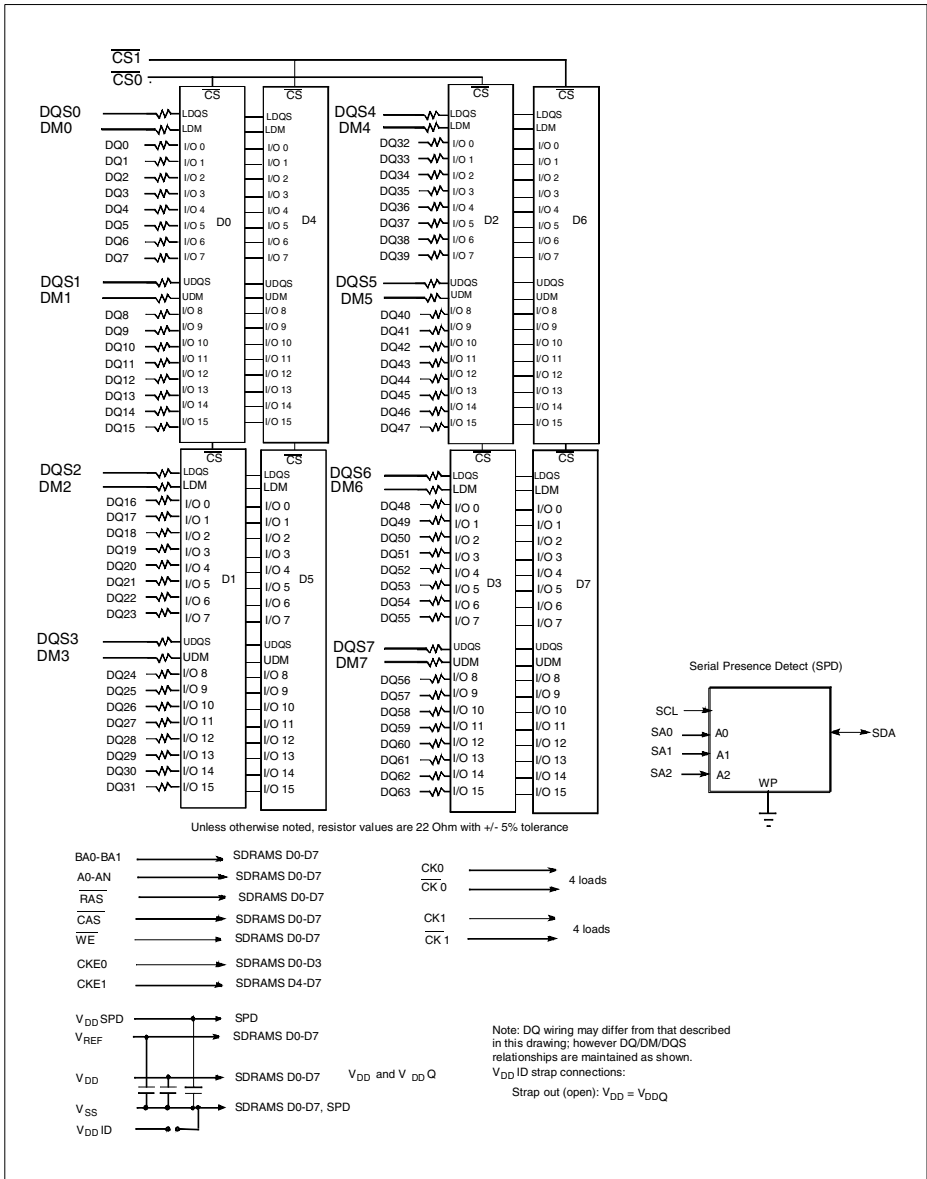
Density	Organization	Memory Banks	SDRAMs	# of SDRAMs	SDRAM density	# of row/ bank/ columns bits	Refresh	Period	Interval
512 MB	64M × 64	2	32M x 16	8	512Mbit	13/2/10	8k	64 ms	7.8 μs

Pin Configuration

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin#	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	VREF	2	VREF	51	VSS	52	VSS	101	A9	102	A8	151	DQ42	152	DQ46
3	VSS	4	VSS	53	DQ19	54	DQ23	103	VSS	104	VSS	153	DQ43	154	DQ47
5	DQ0	6	DQ4	55	DQ24	56	DQ28	105	A7	106	A6	155	VDD	156	VDD
7	DQ1	8	DQ5	57	VDD	58	VDD	107	A5	108	A4	157	VDD	158	CK1
9	VDD	10	VDD	59	DQ25	60	DQ29	109	A3	110	A2	159	VSS	160	CK1
11	DQS0	12	DM0	61	DQS3	62	DM3	111	A1	112	A0	161	VSS	162	VSS
13	DQ2	14	DQ6	63	VSS	64	VSS	113	VDD	114	VDD	163	DQ48	164	DQ52
15	VSS	16	VSS	65	DQ26	66	DQ30	115	A10/AP	116	BA1	165	DQ49	166	DQ53
17	DQ3	18	DQ7	67	DQ27	68	DQ31	117	BA0	118	RAS	167	VDD	168	VDD
19	DQ8	20	DQ12	69	VDD	70	VDD	119	WE	120	CAS	169	DQS6	170	DM6
21	VDD	22	VDD	71	(CB0)	72	(CB4)	121	CS0	122	CS1	171	DQ50	172	DQ54
23	DQ9	24	DQ13	73	(CB1)	74	(CB5)	123	DU	124	DU	173	VSS	174	VSS
25	DQS1	26	DM1	75	VSS	76	VSS	125	VSS	126	VSS	175	DQ51	176	DQ55
27	VSS	28	VSS	77	(DQS8)	78	(DM8)	127	DQ32	128	DQ36	177	DQ56	178	DQ60
29	DQ10	30	DQ14	79	(CB2)	80	(CB6)	129	DQ33	130	DQ37	179	VDD	180	VDD
31	DQ11	32	DQ15	81	VDD	82	VDD	131	VDD	132	VDD	181	DQ57	182	DQ61
33	VDD	34	VDD	83	(CB3)	84	(CB7)	133	DQS4	134	DM4	183	DQS7	184	DM7
35	CK0	36	VDD	85	DU	86	DU	135	DQ34	136	DQ38	185	VSS	186	VSS
37	CK0	38	VSS	87	VSS	88	VSS	137	VSS	138	VSS	187	DQ58	188	DQ62
39	VSS	40	VSS	89	(CK2)	90	VSS	139	DQ35	140	DQ39	189	DQ59	190	DQ63
41	DQ16	42	DQ20	91	(CK2)	92	VDD	141	DQ40	142	DQ44	191	VDD	192	VDD
43	DQ17	44	DQ21	93	VDD	94	VDD	143	VDD	144	VDD	193	SDA	194	SA0
45	VDD	46	VDD	95	CKE1	96	CKE0	145	DQ41	146	DQ45	195	SCL	196	SA1
47	DQS2	48	DM2	97	DU	98	DU	147	DQS5	148	DM5	197	Vddspd	198	SA2
49	DQ18	50	DQ22	99	A12	100	A11	149	VSS	150	VSS	199	Vddid	200	DU

Note: Pins 71, 72, 73, 74, 77, 78, 79, 80, 83, 84, 89 and 91 are reserved for x72 variants of this module and are not used on the x64 versions. Pin 86 is reserved for a registered variant of this module and is not used on the unbuffered version





Block Diagram: Two Bank 64M x 64 DDR-SDRAM SO-DIMM Modules using x16 Organized SDRAMs on Raw Card Version A

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input / Output voltage relative to V_{SS}	V_{IN}, V_{OUT}	- 0.5	3.6	V
Power supply voltage on V_{DD}/V_{DDQ} to V_{SS}	V_{DD}, V_{DDQ}	- 0.5	3.6	V
Storage temperature range	T_{STG}	-55	+150	°C
Power dissipation (per SDRAM component)	P_D	-	1	W
Data out current (short circuit)	I_{OS}	-	50	mA

Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded.

Functional operation should be restricted to recommended operation conditions.

Exposure to higher than recommended voltage for extended periods of time affect device reliability

Supply Voltage Levels

Parameter	Symbol	Limit Values			Unit	Notes
		min.	nom.	max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	-
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	1)
Input Reference Voltage	V_{REF}	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2)
Termination Voltage	V_{TT}	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V	3)
EEPROM supply voltage	V_{DDSPD}	2.3	2.5	3.6	V	

1 Under all conditions, V_{DDQ} must be less than or equal to V_{DD}

2 Peak to peak AC noise on V_{REF} may not exceed $\pm 2\% V_{REF(DC)}$.

V_{REF} is also expected to track noise variations in V_{DDQ} .

3 V_{TT} of the transmitting device must track V_{REF} of the receiving device.

DC Operating Conditions (SSTL_2 Inputs)

($V_{DDQ} = 2.5$ V, $T_A = 70$ °C, Voltage Referenced to V_{SS})

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
DC Input Logic High	$V_{IH(DC)}$	$V_{REF} + 0.15$	$V_{DDQ} + 0.3$	V	1)
DC Input Logic Low	$V_{IL(DC)}$	- 0.30	$V_{REF} - 0.15$	V	-
Input Leakage Current	I_{IL}	- 5	5	μA	1)
Output Leakage Current	I_{OL}	- 5	5	μA	2)

1) The relationship between the V_{DDQ} of the driving device and the V_{REF} of the receiving device is what determines noise margins. However, in the case of $V_{IH(max)}$ (input overdrive), it is the V_{DDQ} of the receiving device that is referenced. In the case where a device is implemented such that it supports SSTL_2 inputs but has no SSTL_2 outputs (such as a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 3.0 V (High corner $V_{DDQ} + 300$ mV).

2) For any pin under test input of $0 \text{ V} \leq V_{IN} \leq V_{DDQ} + 0.3 \text{ V}$. Values are shown per DDR-SDRAM component.

Operating, Standby and Refresh Currents (PC2700, PC2100, PC1600)

Symbol	Parameter/Condition	512MB x64 2bank -6	512MB x64 2bank -7	512MB x64 2bank -8	Unit	Notes
		MAX	MAX	MAX		4
IDD0	Operating Current: one bank; active / precharge; tRC = tRC MIN; tCK = tCK MIN; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles	1080	920	840	mA	1
IDD1	Operating Current: one bank; active/read/precharge; Burst = 4; Refer to the following page for detailed test conditions.	1140	960	880	mA	1, 3
IDD2P	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE <= VIL MAX; tCK = tCK MIN	144	112	96	mA	2
IDD2F	Precharge Floating Standby Current: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; tCK = tCK MIN, address and other control inputs changing once per clock cycle, VIN = VREF for DQ, DQS and DM.	480	400	320	mA	2
IDD2Q	Precharge Quiet Standby Current: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; tCK = tCK MIN, address and other control inputs stable at >= VIH MIN or <= VIL MAX; VIN = VREF for DQ, DQS and DM.	320	224	200	mA	2
IDD3P	Active Power-Down Standby Current: one bank active; power-down mode; CKE <= VIL MAX; tCK = tCK MIN; VIN = VREF for DQ, DQS and DM.	184	144	128	mA	2
IDD3N	Active Standby Current: one bank active; active / precharge; CS >= VIH MIN; CKE >= VIH MIN; tRC = tRAS MAX; tCK = tCK MIN; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	600	560	400	mA	2
IDD4R	Operating Current: one bank active; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200, and DDR266A, CL=3 for DDR333; tCK = tCK MIN; IOUT = 0mA	1260	1040	860	mA	1, 3
IDD4W	Operating Current: one bank active; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200, and DDR266A, CL=3 for DDR333; tCK = tCK MIN	1220	1020	840	mA	1
IDD5	Auto-Refresh Current: tRC = tRFC MIN, distributed refresh	1620	1480	1360	mA	1
IDD6	Self-Refresh Current: CKE <= 0.2V; external clock on; tCK = tCK MIN	20	20	20	mA	
IDD7	Operating Current: four bank; four bank interleaving with BL=4; Refer to the following page for detailed test conditions.	1900	1760	1600	mA	1, 3

- The module IDD values are calculated from the component IDD datasheet values as:
 $n * IDDx[\text{component}]$ for single bank modules (n: number of components per module bank)
 $n * IDDx[\text{component}] + n * IDD3N[\text{component}]$ for two bank modules (n: number of components per module bank)
- The module IDD values are calculated from the component IDD datasheet values as:
 $n * IDDx[\text{component}]$ for single bank modules (n: number of components per module bank)
 $2 * n * IDDx[\text{component}]$ for two bank modules (n: number of components per module bank)
- DQ I/O (IDDQ) currents are not included into calculations: module IDD values will be measured differently depending on load conditions
- Test condition for maximum values: VDD = 2.7V, Ta = 10°C

Electrical Characteristics & AC Timing for DDR-I components

(for reference only)

(0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V)

Symbol	Parameter		DDR333 -6		DDR266A -7		DDR200 -8		Unit	Notes
			Min	Max	Min	Max	Min	Max		
t _{AC}	DQ output access time from CK/CK̄		- 0.7	+ 0.7	- 0.75	+ 0.75	- 0.8	+ 0.8	ns	1-4
t _{DQSK}	DQS output access time from CK/CK̄		- 0.6	+ 0.6	- 0.75	+ 0.75	- 0.8	+ 0.8	ns	1-4
t _{CH}	CK high-level width		0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	1-4
t _{CL}	CK low-level width		0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	1-4
t _{HP}	Clock Half Period		min (t _{CL} , t _{CH})		min (t _{CL} , t _{CH})		min (t _{CL} , t _{CH})		ns	1-4
t _{CK}	Clock cycle time	CL = 2.5	6	12	7	12	8	12	ns	1-4
t _{CK}		CL = 2.0	7.5	12	7.5	12	10	12	ns	1-4
t _{DH}	DQ and DM input hold time		0.45		0.5		0.6		ns	1-4
t _{DS}	DQ and DM input setup time		0.45		0.5		0.6		ns	1-4
t _{IPW}	Control and Addr. input pulse width (each input)		2.2		2.2		2.5		ns	1, 10
t _{DIPW}	DQ and DM input pulse width (each input)		1.75		1.75		2		ns	1-4, 11
t _{HZ}	Data-out high-impedence time from CK/CK̄		- 0.7	+ 0.7	- 0.75	+ 0.75	- 0.8	+ 0.8	ns	1-4, 5
t _{LZ}	Data-out low-impedence time from CK/CK̄		- 0.7	+ 0.7	- 0.75	+ 0.75	- 0.8	+ 0.8	ns	1-4, 5
t _{DQSS}	Write command to 1st DQS latching transition		0.75	1.25	0.75	1.25	0.75	1.25	t _{CK}	1-4
t _{DOSO}	DQS-DQ skew (for DQS & associated DQ signals)			+ 0.45		+ 0.5		+ 0.6	ns	1-4
t _{OHS}	Data hold skew factor			+ 0.55		+ 0.75		+ 1.0	ns	1-4
t _{OH}	Data Output hold time from DQS		t _{HP} -t _{OHS}		t _{HP} -t _{OHS}		t _{HP} -t _{OHS}		ns	1-4
t _{DQSLH}	DQS input low (high) pulse width (write cycle)		0.35		0.35		0.35		t _{CK}	1-4
t _{DSS}	DQS falling edge to CK setup time (write cycle)		0.2		0.2		0.2		t _{CK}	1-4
t _{DSH}	DQS falling edge hold time from CK (write cycle)		0.2		0.2		0.2		t _{CK}	1-4
t _{MRD}	Mode register set command cycle time		2		2		2		t _{CK}	1-4
t _{WPRES}	Write preamble setup time		0		0		0		ns	1-4, 7
t _{WPST}	Write postamble		0.40	0.60	0.40	0.60	0.40	0.60	t _{CK}	1-4, 6
t _{WPRE}	Write preamble		0.25		0.25		0.25		t _{CK}	1-4
t _{IS}	Address and control input setup time	fast slew rate	0.75		0.9		1.1		ns	2-4, 10,11
		slow slew rate	0.8		1.0		1.1		ns	
t _{IH}	Address and control input hold time	fast slew rate	0.75		0.9		1.1		ns	
		slow slew rate	0.8		1.0		1.1		ns	
t _{RPRE}	Read preamble		0.9	1.1	0.9	1.1	0.9	1.1	t _{CK}	1-4
t _{RPST}	Read postamble		0.40	0.60	0.40	0.60	0.40	0.60	t _{CK}	1-4
t _{RAS}	Active to Precharge command		42	70,000	45	120,000	50	120,000	ns	1-4
t _{RC}	Active to Active/Auto-refresh command period		60		65		70		ns	1-4
t _{RFC}	Auto-refresh to Active/Auto-refresh command period		72		75		80		ns	1-4

Electrical Characteristics & AC Timing for DDR-I components

(for reference only)

(0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V)

Symbol	Parameter	DDR333 -6		DDR266A -7		DDR200 -8		Unit	Notes	
		Min	Max	Min	Max	Min	Max			
t _{RCD}	Active to Read or Write delay	18		20		20		ns	1-4	
t _{RP}	Precharge command period	18		20		20		ns	1-4	
t _{RRD}	Active bank A to Active bank B command	12		15		15		ns	1-4	
t _{WR}	Write recovery time	15		15		15		ns	1-4	
t _{DAL}	Auto precharge write recovery + precharge time	(twr/tck) + (trp/tck)						t _{CK}	1-4,9	
t _{WTR}	Internal write to read command delay	1		1		1		t _{CK}	1-4	
t _{XSNR}	Exit self-refresh to non-read command	75		75		80		ns	1-4	
t _{XSRD}	Exit self-refresh to read command	200		200		200		t _{CK}	1-4	
t _{REFI}	Average Periodic Refresh Interval	512Mb based		7.8		7.8		7.8	µs	1-4, 8

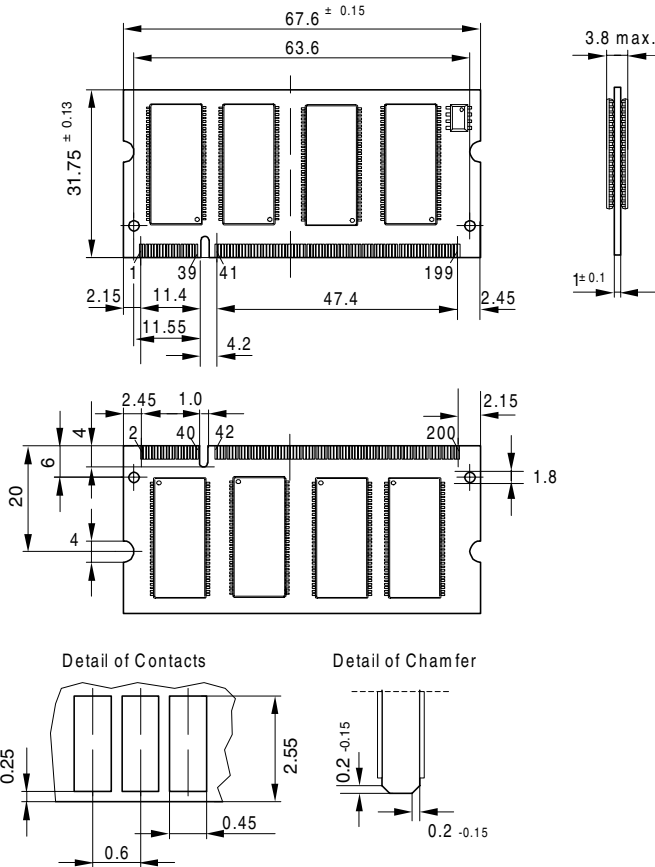
1. Input slew rate ≥ 1V/ns for DDR266 & DDR333 and = 1V/ns for DDR200.
2. The CK/CK input reference level (for timing reference to CK/CK) is the point at which CK and \overline{CK} cross: the input reference level for signals other than CK/CK, is V_{REF}. CK/CK slew rate are ≥ 1.0 V/ns.
3. Inputs are not recognized as valid until V_{REF} stabilizes.
4. The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is V_{TP}.
5. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
6. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
7. The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{BOSS}.
8. A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.
9. For each of the terms, if not already an integer, round to the next highest integer. tCK is equal to the actual system clock cycle time.
10. These parameters guarantee device timing, but they are not necessarily tested on each device
11. Fast slew rate ≥ 1.0 V/ns, slow slew rate ≥ 0.5 V/ns and < 1V/ns for command/address and CK & \overline{CK} slew rate > 1.0 V/ns, measured between VOH(ac) and VOL(ac)

SPD Codes for PC2700, PC2100 & PC1600

Byte#	Description		512MB	512MB	512MB
			x64 2bank -6	x64 2bank -7	x64 2bank -8
			HEX	HEX	HEX
0	Number of SPD Bytes	128	80	80	80
1	Total Bytes in Serial PD	256	08	08	08
2	Memory Type	DDR-SDRAM	07	07	07
3	Number of Row Addresses	13	0D	0D	0D
4	Number of Column Addresses	9	0A	0A	0A
5	Number of DIMM Banks	1 / 2	02	02	02
6	Module Data Width	x64	40	40	40
7	Module Data Width (cont'd)	0	00	00	00
8	Module Interface Levels	SSTL_2.5	04	04	04
9	SDRAM Cycle Time at CL = 2.5	6ns / 7ns / 8ns	60	70	80
10	Access Time from Clock at CL = 2.5	0.7ns / 0.75ns / 0.8ns	70	75	80
11	DIMM Config	non-ECC / ECC	00	00	00
12	Refresh Rate/Type	Self-Refresh,15.6ms	82	82	82
13	SDRAM Width, Primary	x16	10	10	10
14	Error Checking SDRAM Data Width	na	00	00	00
15	Minimum Clock Delay for Back-to-Back Random Column Address	tccd = 1 CLK	01	01	01
16	Burst Length Supported	2, 4 & 8	0E	0E	0E
17	Number of SDRAM Banks	4	04	04	04
18	Supported CAS Latencies	CAS latency = 2 & 2.5	0C	0C	0C
19	CS Latencies	CS latency = 0	01	01	01
20	WE Latencies	Write latency = 1	02	02	02
21	SDRAM DIMM Module Attributes	unbuffered	20	20	20
22	SDRAM Device Attributes: General	Concurrent Auto Precharge, weak driver	C1	C1	C1
23	Min. Clock Cycle Time at CAS Latency = 2	7.5ns / 7.5ns / 10ns	75	75	A0
24	Access Time from Clock for CL = 2	0.7ns / 0.75ns / 0.8ns	70	75	80
25	Minimum Clock Cycle Time at CL = 1.5	not supported	00	00	00
26	Access Time from Clock at CL = 1.5	not supported	00	00	00
27	Minimum Row Precharge Time	18ns / 20ns / 20ns	48	50	50
28	Minimum Row Act. to Row Act. Delay tRRD	12ns / 15ns / 15ns	30	3C	3C
29	Minimum RAS to CAS Delay tRCD	18ns / 20ns / 20ns	48	50	50
30	Minimum RAS Pulse Width tRAS	42ns / 45ns / 50ns	2A	2D	32
31	Module Bank Density (per bank)	64MByte	40	40	40
32	Addr. and Command Setup Time	0.75ns / 0.9ns / 1.1 ns	75	90	B0
33	Addr. and Command Hold Time	0.75ns / 0.9ns / 1.1 ns	75	90	B0
34	Data Input Setup Time	0.45ns / 0.5ns / 0.6ns	45	50	60
35	Data Input Hold Time	0.45ns / 0.5ns / 0.6ns	45	50	60
36-40	Superset Information	-	00	00	00
41	Minimum Core Cycle Time tRC	60ns / 65ns / 70ns	3C	41	46
42	Min. Auto Refresh Cmd Cycle Time tRFC	72ns / 75ns / 80ns	48	4B	50
43	Maximum Clock Cycle Time tck	12ns	30	30	30
44	Max. DQS-DQ Skew tDQSQ	0.45ns / 0.5ns / 0.6ns	2D	32	3C
45	X-Factor tQHS	0.55ns / 0.75ns / 1.0ns	55	75	A0
46-61	Superset Information	-	00	00	00
62	SPD Revision	Revision 0.0	00	00	00
63	Checksum for Bytes 0 - 62	-	0A	BC	B1
64	Manufacturers JEDEC ID Code	-	C1	C1	C1
65-71	Manufacturer	-	INFINEON	INFINEON	INFINEON
72	Module Assembly Location	-			
73-90	Module Part Number	-			
91-92	Module Revision Code	-			
93-94	Module Manufacturing Date	-			
95-98	Module Serial Number	-			
99-127	-	-			
128-255	open for Customer use	-			

Package Outlines Raw Card A

DDR-SDRAM SO-DIMM Modules Raw Card A



L-DIM-200-6