AP-752

APPLICATION NOTE

The Advantages of Using the 82371SB PCI ISA IDE Xcelerator (PIIX3) with the Intel 430HX PCIset in Embedded Designs

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1.0 Introduction

This application note explains the advantages of using the 82371SB PCI ISA IDE Xcelerator (PIIX3) in embedded designs that use the Intel 430HX PCIset. It highlights some of the important functions and features of the PIIX3 and addresses some of the design considerations when eliminating the PIIX3 from an embedded design.

2.0 Intel 430HX PCIset Overview

The Intel 430HX PCIset consists of the 82439HX System Controller (TXC) and the 82371SB PCI ISA IDE Xcelerator (PIIX3). The TXC is a single-chip host-to-PCI bridge and provides the second-level cache control and DRAM control functions. The second-level (L2) cache controller supports a write-back cache policy for cache sizes of 256 Kbytes and 512 Kbytes. The cache controller also supports cacheless designs. The cache memory is implemented with synchronous pipelined burst SRAMs. An external Tag RAM is used for the address tag and an internal Tag RAM is used for the cache line status bits.

The TXC provides a 64/72-bit data path to main memory and memory sizes up to 512 Mbytes. The DRAM controller provides eight rows and optional DRAM error detection/correction or parity.

The TXC's optimized PCI interface allows the processor to sustain the highest possible bandwidth to the graphics frame buffer at all frequencies. Using the snoop ahead feature, the TXC allows PCI masters to achieve full PCI bandwidth. For increased system performance, the TXC contains read prefetch and posted write buffers.

The PIIX3 is a multi-function PCI device that implements a PCI-to-ISA bridge function and a PCI IDE function. The PIIX3 also implements a Universal Serial Bus host/hub function.

3.0 PIIX3 Features

As a PCI-to-ISA bridge, the PIIX3 integrates many common I/O functions found in ISA-based PC systems. These include a seven-channel DMA controller, two 82C59 interrupt controllers, an 8254 timer counter, and power management support.

In addition to compatible transfers, each DMA channel supports type F transfers. Edge/Level interrupts and interrupt steering are supported for PCI plug-and-play compatibility. The PIIX3 can be programmed to allow the PCI active low interrupts (PIRQ[D:A]#) to be internally routed to one of 11 interrupts (IRQ[15,14,12:9,7:3]). In addition, the motherboard interrupt (MIRQ0) can be routed to any of the 11 interrupts.

The PIIX3 supports two IDE connectors for up to four IDE devices, providing an interface for IDE hard disks and CD ROMs.

The PIIX3 contains a Universal Serial Bus (USB) host controller that is UHCI compatible. The host controller's root hub has two programmable UBS ports. The PIIX3 can support a stand-alone I/O APIC device on the ISA X-Bus. It provides the chip select signal (APICCS#) for the I/O APIC and the handshake signals to maintain buffer coherency in the I/O APIC environment.

The PIIX3 contains three counters that are equivalent to those found in the 82C54 programmable interval timer. The three counters are contained in one PIIX3 timer unit, referred to as *Timer-1*. Each counter output provides a key system timer interrupt for a time-of-day, diskette time-out, or other system timing function. Counter 1 generates a refresh request signal and Counter 2 generates the tone for the speaker.

The PIIX3 has extensive power management capability, permitting a system to operate in a low power state without being powered down. The PIIX3 can put the processor in a low power state by asserting the STPCLK# signal, which is an interrupt to the processor. Once the STPCLK# interrupt is executed, the processor enters the stop grant state. In this state, the processor's internal clocks are disabled and instruction execution is stopped.

The PIIX3 provides positive decode (chip selects) and X-Bus buffer control for a real time clock, a keyboard controller, and BIOS for PCI ISA initiated cycles. In addition, the PIIX3 integrates the system reset logic for the system. It generates CPURST, PCIRST#, and RSTDRV during power up (PWROK) and whenever a hard reset is initiated through the RC register. It also generates the NMI and SMI# signals to the processor.

All of these features of the PIIX3 are integrated in a single 208-lead QFP package. This is very important in embedded designs where board space is at a premium. Intel, at this time, does not sell the PIIX3 separate from the TXC. Therefore, the PIIX3, and related technical support, will be available as long as the 430HX PCIset is available.

4.0 Designing without the PIIX3

If the PIIX3 is not implemented with the 430HX PCIset, several features that are typically supported by the PIIX3 and that are required in certain embedded designs must be provided by other means. This section discusses some design considerations with two alternatives: using the Super I/O* Controller and using another PCI-to-ISA bridge.

4.1 Using a Super I/O Controller

Using a Super I/O Controller is not new to the design world, but using the Super I/O Controller in a design that does not have an ISA bus interface is new. Using a Super I/O Controller in this type of design raises many issues:

- The Super I/O Controller must be interfaced with the PCI bus. This type of Super I/O Controller is not common in the market. A standard ISA Super I/O Controller can be used but requires additional logic to interface to the PCI bus.
- Most of the Super I/O Controllers do not have the interrupt, DMA, and IDE controllers and/or a timer counter. Separate devices may have to be added to the design.
- A PCI-to-Flash controller must be provided to access boot ROM code.
- A special software interface must be implemented for utilizing the processor's power management capabilities and handling the processor interface signals, such as different types of resets, NMI, and SMI# signals.

These considerations complicate and add more cost to the design, including the components cost and the non-recurring-engineering (NRE) cost. They also increase the board space. Additional devices on the PCI bus may cause electrical loading problems. In addition, the availability of these components may not be guaranteed for long-term embedded support.

4.2 Using Another PCI-to-ISA Bridge

A second workaround method is to use a PCI-to-ISA bridge other than the PIIX3. Considerations in implementing this type of design include:

- The PCI-to-ISA bridge timing specifications must be compatible with those of the PIIX3 to enable interfacing with the TXC.
- The availability of the new bridge may not be guaranteed for long-term embedded support.
- Intel cannot be responsible for the technical support of these types of designs.

5.0 Conclusion

Using the PIIX3 in embedded designs that use the 430HX PCIset makes the embedded design much easier to implement. Designing with the PIIX3 reduces the cost and embedded total number of components in the design. The PIIX3 will be available in the embedded market as long as the 430HX PCIset is available. Intel recommends and supports using the complete 430HX PCIset.

6.0 Related Information

Intel offers a variety of information through the World Wide Web at http://www.intel.com.

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Document Name	Intel Order Number
Intel 430HX PCIset: 82439HX System Controller (TXC) datasheet	290551
Intel 430HX PCIset: 82439HX System Controller (TXC) Timing Specification	272945
Intel 430HX PCIset: 82439HX System Controller (TXC) Specification Update	297652
82371FB (PIIX) and 82371SB (PIIX3) PCI ISA IDE Xcelerator datasheet	290550
Intel 430HX PCIset: 82371SB PCI ISA IDE Xcelerator (PIIX3) Timing Specification	272963
Intel 82371SB (PIIX3) PCI ISA IDE Xcelerator Specification Update	297658
Intel 430HX PCIset Design Guide	297467