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Status	Product Specification
FAST Products	

FAST 74F723A/723-1, 74F725A/725-1

Multiplexers

74F723A Quad 3-to-1 Data Selector Multiplexer (3-State)

74F723-1 Quad 3-to-1 Data Selector Multiplexer With 30 ohm Equivalent Output Termination Impedance (3-State)

74F725A Quad 4-to-1 Data Selector Multiplexer

74F725-1 Quad 4-to-1 Data Selector Multiplexer With 30 ohm Equivalent Output Termination Impedance

FEATURES for 74F723A/723-1

- Consists of four 3-to-1 Multiplexers
- High impedance PNP base inputs for reduced loading (20µA in High and Low states)
- Inverting or non-inverting data path capability by an Inverting (INV) input
- Designed for address multiplexing of dynamic RAM and other applications
- Multiple side pins for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)
- 3-State outputs sink 64mA ('F723A only)
- 30 ohm termination impedance on each output-74F723-1

FEATURES for 74F725A/725-1

- Consists of four 4-to-1 Multiplexers
- High impedance PNP base inputs for reduced loading (20µA in High and Low states)
- Equivalent to two 'F253s without 3-state
- Outputs sink 48mA ('F725A only)
- 30 ohm termination impedance on each output-74F725-1

DESCRIPTION

The 74F723A/723-1 consist of four 3-to-1 multiplexers designed for address multiplexing of dynamic RAMs and other multiplexing applications. Select (S₀, S₁) inputs control which line is to be selected, as defined in the Function Table for 'F723A/723-1. When the inverting input (INV) is Low, the input data path is inverted.

To improve speed and noise immunity, V_{CC} and GND side pins are used. The 3-state outputs source 15mA and sink

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F723A	5.5ns	25mA
74F723-1	7.0ns	26mA
74F725A	5.5ns	20mA
74F725-1	6.5ns	20mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V _{CC} = 5V±10%; T _A = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F723AN, N74F723-1N, N74F725AN, N74F725-1N
24-Pin Plastic SOI	N74F723AD, N74F723-1D, N74F725AD, N74F725-1D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

TYPE	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F723A/ 'F723-1	D _{na} , D _{nb} , D _{nc}	Data inputs	1.0/0.066	20µA/40µA
	S ₀ , S ₁	Select inputs	1.0/0.033	20µA/20µA
	INV	Output Inverting input	1.0/0.033	20µA/20µA
	OE	Output Enable input	1.0/0.033	20µA/20µA
'F723A	Q ₀ - Q ₃	Data outputs	750/106.7	15mA/64mA
'F723-1	Q ₀ - Q ₃	Data outputs	750/8.33	15mA/5mA
'F725A/ 'F725-1	D _{na} , D _{nb} , D _{nc} , D _{nd}	Data inputs	1.0/0.066	20µA/40µA
	S ₀ , S ₁	Select inputs	1.0/0.033	20µA/20µA
'F725A	Q ₀ - Q ₃	Data outputs	750/106.7	15mA/64mA
'F725-1	Q ₀ - Q ₃	Data outputs	750/8.33	15mA/5mA

NOTE:

One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

64mA. The 74F723-1 is the same as 74F723A except that it has a 30 ohm termination impedance on each output to reduce line noise and the 3-state outputs sink 5mA.

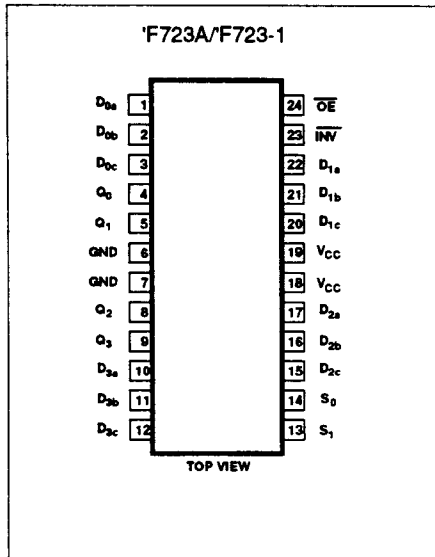
The 74F725A/725-1 consist of four 4-to-1 multiplexers designed for general multiplexing purpose. The select (S₀, S₁) in-

puts control which line is to be selected, as defined in the Function Table for 'F725A/725-1. The outputs source 15mA and sink 64mA. The 74F725-1 is the same as the 74F725A except that it has a 30 ohm termination impedance on each output to reduce line noise and the outputs sink 5mA.

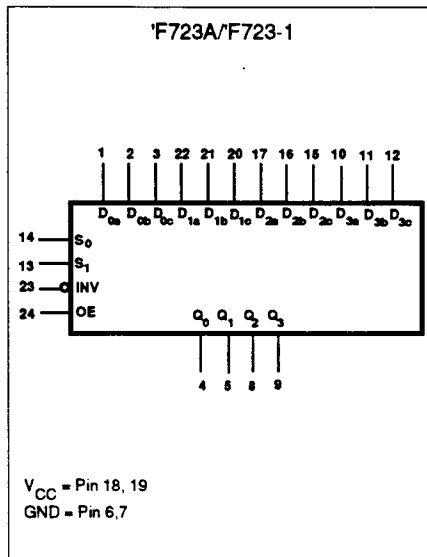
Multiplexers

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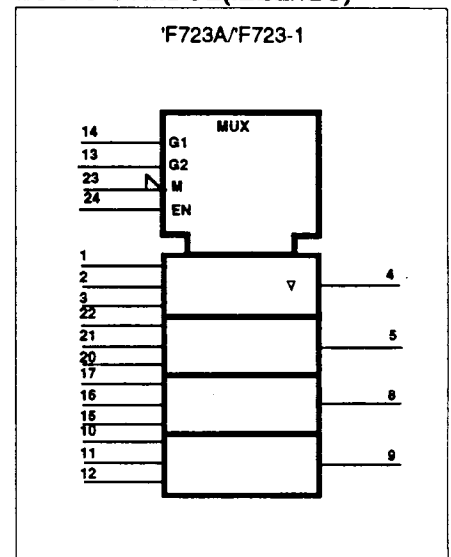
PIN CONFIGURATION



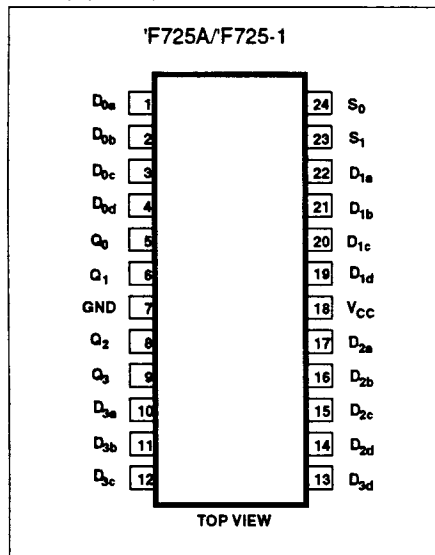
LOGIC SYMBOL



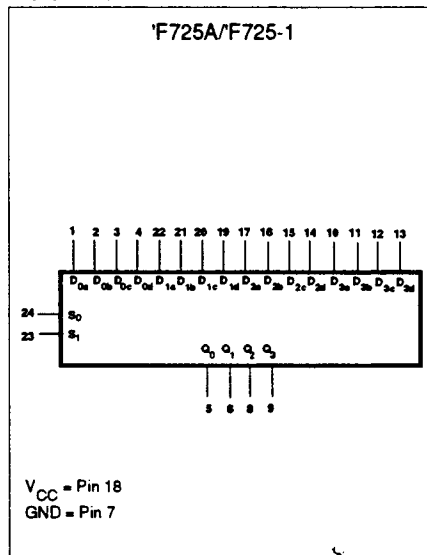
LOGIC SYMBOL (IEEE/IEC)



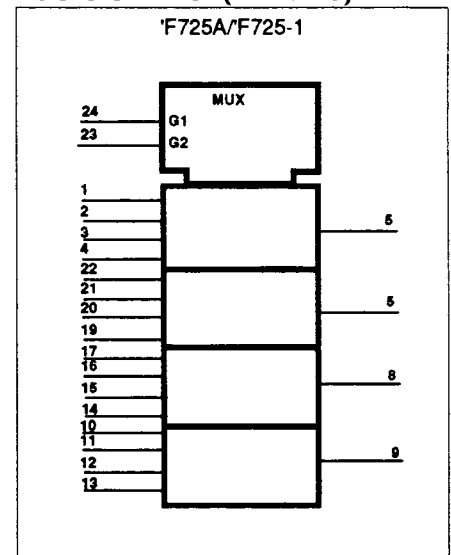
PIN CONFIGURATION



LOGIC SYMBOL



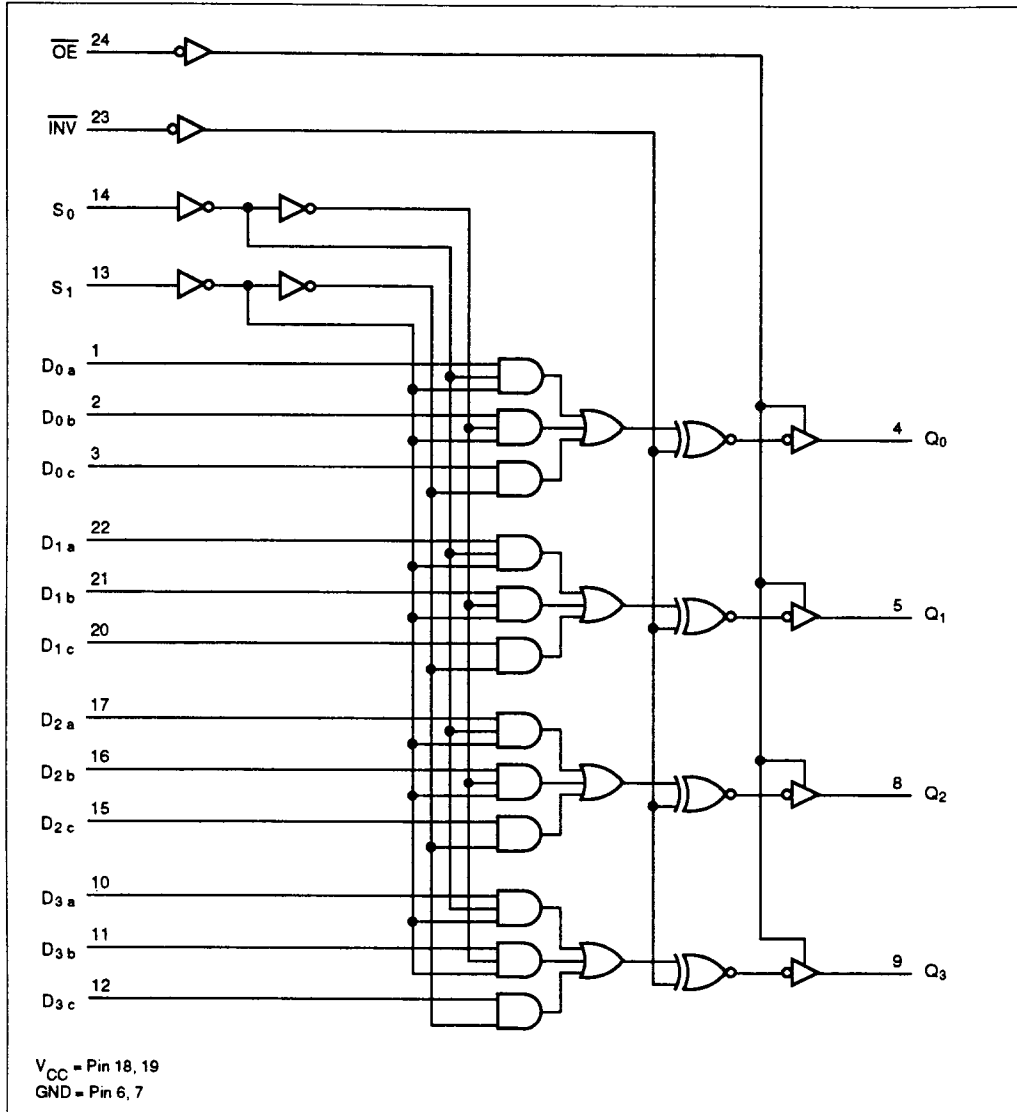
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM for 'F723A/'F723-1



FUNCTION TABLE for 'F723A/'F723-1

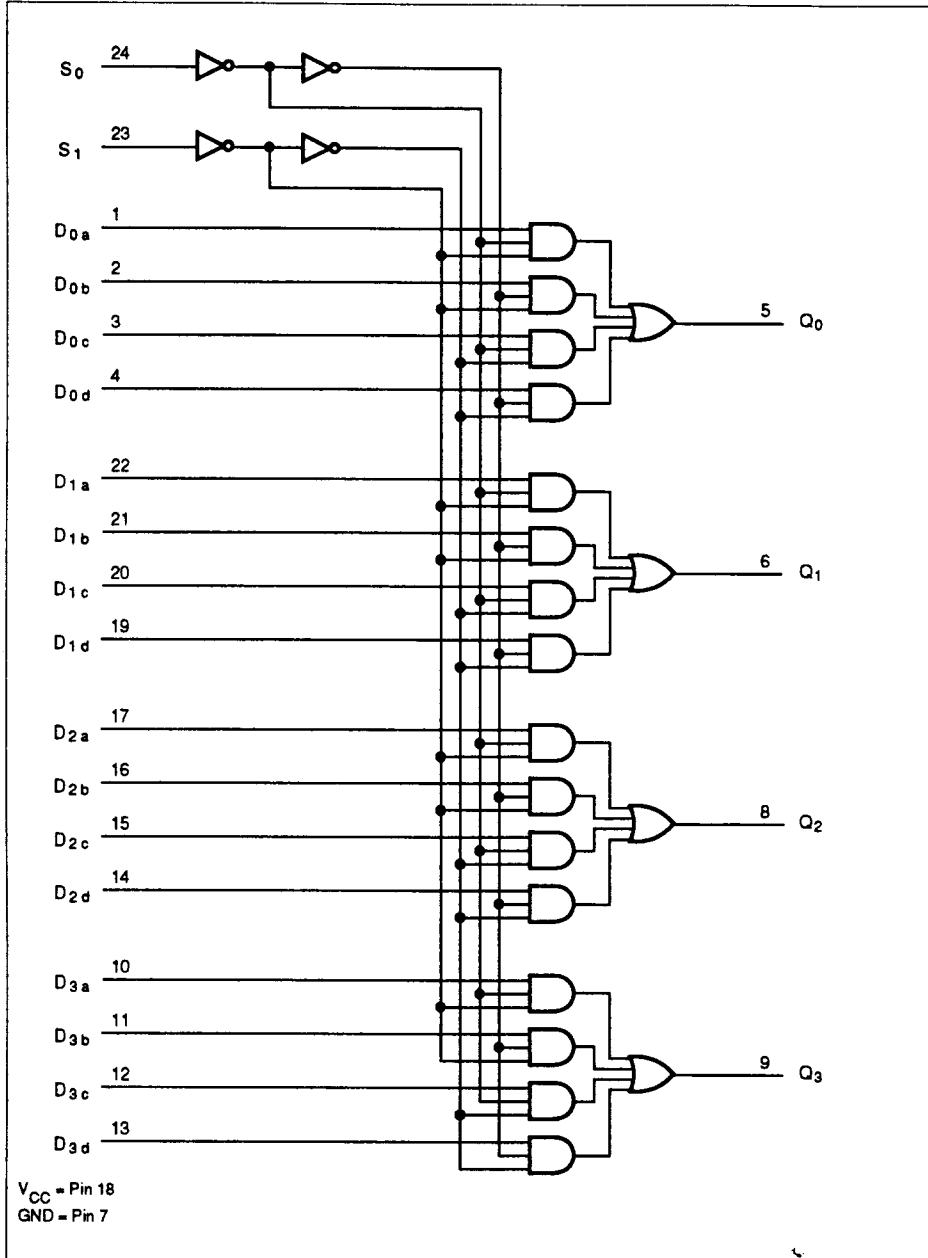
INPUTS							OUTPUT
S_0	S_1	\overline{INV}	\overline{OE}	D_{na}	D_{nb}	D_{nc}	Q_n
L	L	L	L	data a	data b	data c	<u>data a</u>
L	L	H	L	data a	data b	data c	data a
H	L	L	L	data a	data b	data c	<u>data b</u>
H	L	H	L	data a	data b	data c	data b
X	H	L	L	data a	data b	data c	<u>data c</u>
X	H	H	L	data a	data b	data c	data c
X	X	X	H	X	X	X	Z

H = High voltage level
 L = Low voltage level
 X = Don't care
 Z = High impedance "off" state

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LOGIC DIAGRAM for 'F725A/'F725-1



FUNCTION TABLE for 'F725A/'F725-1

INPUTS						OUTPUT
S_0	S_1	D_{na}	D_{nb}	D_{nc}	D_{nd}	Q_n
L	L	data a	data b	data c	data d	data a
H	L	data a	data b	data c	data d	data b
L	H	data a	data b	data c	data d	data c
H	H	data a	data b	data c	data d	data d

H = High voltage level
 L = Low voltage level

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ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT	
V _{CC}	Supply voltage	-0.5 to +7.0	V	
V _{IN}	Input voltage	-0.5 to +7.0	V	
I _{IN}	Input current	-30 to +5	mA	
V _{OUT}	Voltage applied to output in High output state	-0.5 to +V _{CC}	V	
I _{OUT}	Current applied to output in Low output state	'F723-1, 'F725-1	10	mA
		'F723A, 'F725A	96	mA
T _A	Operating free-air temperature range	0 to +70	°C	
T _{STG}	Storage temperature	-65 to +150	°C	

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-15	mA
I _{OL}	Low-level output current	'F723-1, 'F725-1		5	mA
		'F723A, 'F725A		64	mA
T _A	Operating free-air temperature range	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹		LIMITS			UNIT	
					Min	Typ ²	Max		
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = -3mA	±10%V _{CC}	2.4		V	
					±5%V _{CC}	2.7	3.4	V	
				I _{OH} = -15mA	±10%V _{CC}	2.0		V	
					±5%V _{CC}	2.0		V	
V _{OL}	Low-level output voltage	'F723-1/ 'F725-1	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = 5mA	±10%V _{CC}		0.38	0.50	V
					±5%V _{CC}		0.38	0.50	V
	'F723A/ 'F725A	I _{OL} = MAX		±10%V _{CC}		0.38	0.55	V	
				±5%V _{CC}		0.42	0.55	V	
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}			-0.73	-1.2	V	
I _I	Input current at maximum input voltage		V _{CC} = MAX, V _I = 7.0V				100	μA	
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7V				20	μA	
I _{IL}	Low-level input current	others	V _{CC} = MAX, V _I = 0.5V				-20	μA	
		D _n only					-40	μA	
I _{OZH}	Off-state output current High-level voltage applied	'F723/ 'F723-1 only	V _{CC} = MAX, V _O = 2.7V				50	μA	
I _{OZL}	Off-state output current Low-level voltage applied		V _{CC} = MAX, V _O = 0.5V				-50	μA	
I _{OS}	Short circuit output current ³	'F723-1/ 'F725-1	V _{CC} = MAX		-60		-150	mA	
I _O	Output current ⁴	'F723A/ 'F725A	V _{CC} = MAX, V _O = 2.25V		-60		-150	mA	
I _{CC}	Supply current (total)	'F723A	V _{CC} = MAX	I _{CCH}		23	30	mA	
				I _{CCL}		29	40	mA	
				I _{CCZ}		25	40	mA	
		'F723-1		I _{CCH}		23	35	mA	
				I _{CCL}		29	40	mA	
				I _{CCZ}		26	40	mA	
		'F725A		I _{CCH}		16	25	mA	
				I _{CCL}		24	35	mA	
		'F725-1		I _{CCH}		17	25	mA	
				I _{CCL}		25	35	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT	
			T _A = +25°C V _{CC} = 5V C _L = 50pF R _L = 500Ω			T _A = 0°C to +70°C V _{CC} = 5V ±10% C _L = 50pF R _L = 500Ω			
			Min	Typ	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation delay D _{na} , D _{nb} , D _{nc} to Q _n	'F723A	Waveform 1, 2	2.5 2.0	5.0 4.5	8.0 7.0	2.0 2.0	8.5 7.5	ns
t _{PLH} t _{PHL}	Propagation delay S ₀ , S ₁ , <u>INV</u> to Q _n		Waveform 1, 2	6.5 4.0	9.0 7.5	12.5 11.0	4.0 3.5	14.0 12.0	ns
t _{PZH} t _{PZL}	Output Enable time <u>OE</u> -to Q _n		Waveform 4 Waveform 5	2.0 2.5	4.0 4.5	6.5 7.0	2.0 2.0	7.5 7.5	ns
t _{PHZ} t _{PLZ}	Output Disable time <u>OE</u> -to Q _n		Waveform 4 Waveform 5	2.5 3.0	4.0 5.0	7.0 7.5	2.0 2.5	7.5 8.5	ns
t _{PLH} t _{PHL}	Propagation delay D _{na} , D _{nb} , D _{nc} to Q _n	'F723-1	Waveform 1, 2	2.5 2.5	6.0 5.0	8.5 8.0	2.5 2.0	9.5 8.0	ns
t _{PLH} t _{PHL}	Propagation delay S ₀ , S ₁ , <u>INV</u> to Q _n		Waveform 1, 2	7.0 5.0	10.0 9.0	14.0 12.5	6.0 4.5	16.0 13.5	ns
t _{PZH} t _{PZL}	Output Enable time <u>OE</u> -to Q _n		Waveform 4 Waveform 5	3.0 3.0	4.5 5.0	7.5 7.5	2.5 3.0	8.0 8.0	ns
t _{PHZ} t _{PLZ}	Output Disable time <u>OE</u> -to Q _n		Waveform 4 Waveform 5	2.5 4.0	4.5 6.0	7.0 8.5	2.0 3.0	8.0 9.5	ns

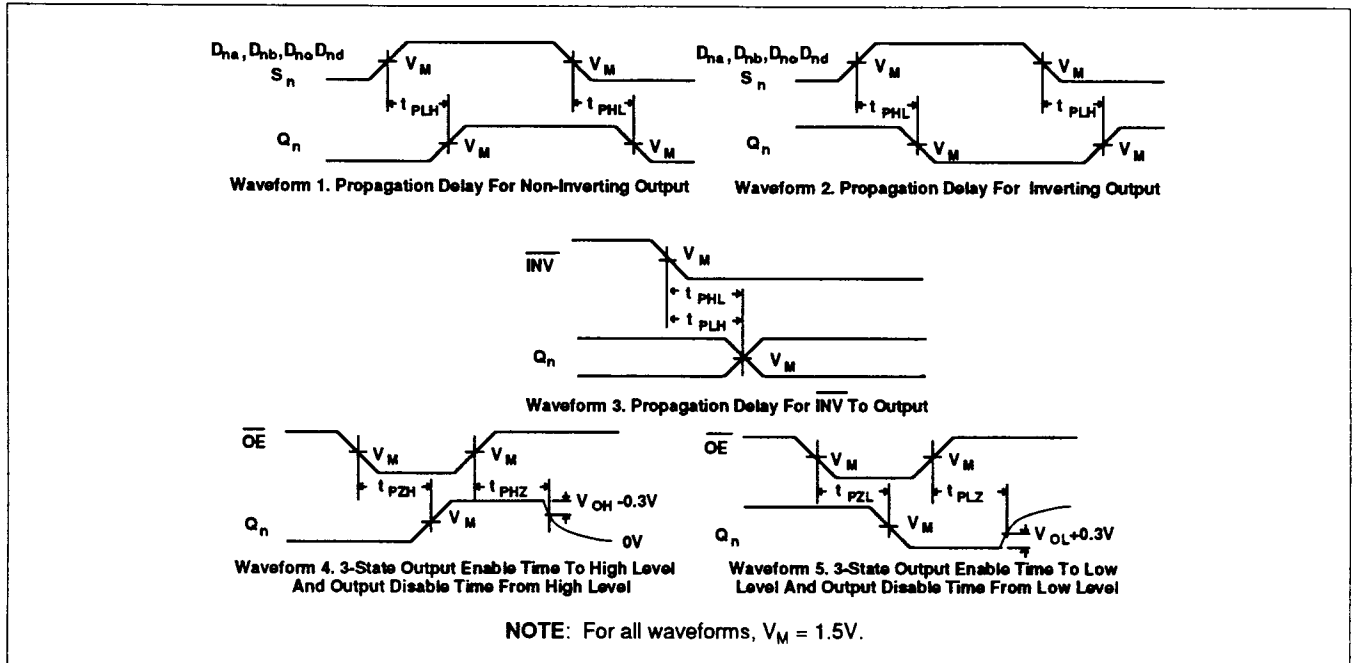
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT	
			T _A = +25°C V _{CC} = 5V C _L = 50pF R _L = 500Ω			T _A = 0°C to +70°C V _{CC} = 5V ±10% C _L = 50pF R _L = 500Ω			
			Min	Typ	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation delay D _{na} , D _{nb} , D _{nc} , D _{nd} to Q _n	'F725A	Waveform 1, 2	2.0 2.0	3.5 3.5	6.5 6.5	2.0 2.0	7.0 6.5	ns
t _{PLH} t _{PHL}	Propagation delay S ₀ , S ₁ to Q _n		Waveform 1	6.0 5.0	8.5 7.0	11.5 10.0	5.5 4.5	13.5 10.5	ns
t _{PLH} t _{PHL}	Propagation delay D _{na} , D _{nb} , D _{nc} , D _{nd} to Q _n	'F725-1	Waveform 1, 2	2.0 2.0	4.0 4.0	7.0 6.5	2.0 2.0	7.5 7.5	ns
t _{PLH} t _{PHL}	Propagation delay S ₀ , S ₁ to Q _n		Waveform 1	6.5 5.0	9.0 8.5	12.0 10.5	5.5 5.0	14.0 11.0	ns

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AC WAVEFORMS



TEST CIRCUIT AND WAVEFORMS

