HARRIS SEMICONDUCTOR

HA-2444

50MHz, Selectable, Four Channel Video Operational Amplifier

November 1996

Features

- **Digital Selection of Input Channel**
- **Unity Gain Stability**
- **Gain Flatness to 10MHz. 0.1dB**
- **Differential Gain 0.03%**
- **Differential Phase. . . . . 0.03 Degrees**
- **Fast Channel Selection 60ns**
- **Crosstalk Rejection 60dB**

Applications

- **Video Multiplexer**
- **Programmable Gain Amplifier**
- **Special Effects Processors**
- **Video Distribution Systems**
- **Heads-up/Night Vision Displays**
- **Medical Imaging Systems**
- **Radar Video**

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HA3-2444-5	0 to 75	16 Ld PDIP	E16.3
HA3-2444-9	-40 to 85	16 Ld PDIP	E16.3
HA9P2444-5	0 to 75	16 Ld SOIC	M16.3
HA9P2444-9	-40 to 85	16 Ld SOIC	M16.3

Description

The HA-2444 is a channel-selectable video op amp consisting of four differential inputs, a single-ended output, and digital control circuitry allowing two digital inputs to activate one of the four differential inputs. The HA-2444 also includes a high impedance output state allowing the outputs of multiple HA-2444s to be wire-OR'd. Functionally, the HA-2444 is equivalent to four wideband video op amps and a wideband multiplexer.

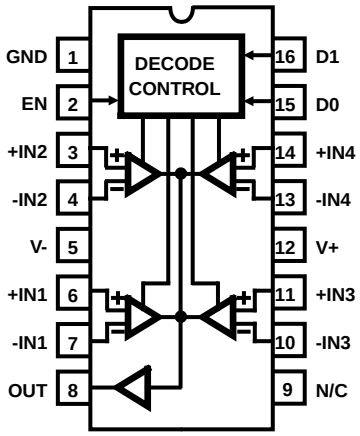
Unlike similar competitor devices, the HA-2444 is not restricted to multiplexing. Any op amp configuration can be used with any of the inputs. Signal amplification, addition, integration, and more can be put under digital control with broadcast quality performance.

The key video parameters of the HA-2444 have been optimized without compromising DC performance. Gain Flatness to 10MHz is only 0.1dB. Differential gain and phase are typically 0.03% and 0.03 degrees, respectively. Laser trimming allows offset voltages in the 4.0mV range and a unique common current source design assures minimal channel-to-channel mismatch, while maintaining 60dB of crosstalk rejection at 5MHz. Open loop gain of 76dB and low input offset and bias currents enhance the performance of this versatile device.

For information about military grade devices, please refer to the HA-2444/883 data sheet.

Pinout

HA-2444
(PDIP, SOIC)
TOP VIEW



Logic Operation

TRUTH TABLE

EN	D1	D0	SELECTED CHANNEL
H	L	L	1
H	L	H	2
H	H	L	3
H	H	H	4
L	X	X	NONE-OUT is set to a high impedance state.

L = Low State (0.8V Max)
H = High State (2.4V Min)
X = Don't Care

File Number **2490.6**

Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals . . . . . 35V (±17.5V)
Differential Input Voltage. 6V
Input Voltage. . . . . $\pm V_S$
Digital Input Voltage . . . . . GND +7.5V to GND -0.5V
Peak (Short Duration) Output Current . . . . . ±40mA

Operating Conditions

Temperature Range
HA-2444-5. . . . . 0^oC to 75^oC
HA-2444-9. . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PDIP Package	80
SOIC Package	96

Maximum Junction Temperature (Die Only). . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_S = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, $V_{IL} = 0.8V$, $V_{IH} = 2.4V$. Unless Otherwise Specified
Specifications Apply to All Channels

PARAMETER	TEST CONDITIONS	TEMP. (^oC)	HA-2444-5, -9			UNITS
			MIN	TYP	MAX	
INPUT CHARACTERISTICS						
Input Offset Voltage		25	-	4	7	mV
		Full	-	-	15	mV
Average Input Offset Voltage Drift		Full	-	10	-	$\mu V/^oC$
Channel to Channel Offset Voltage Mismatch		25	-	-	5	mV
		Full	-	-	8	mV
Input Bias Current		25	-	9	15	µA
		Full	-	-	20	µA
Average Input Bias Current Drift		Full	-	0.04	-	$\mu A/^oC$
Input Offset Current		25	-	2	4	µA
		Full	-	-	6	µA
Average Input Offset Current Drift		Full	-	10	-	$nA/^oC$
Common Mode Range		Full	-	±11.5	-	V
Differential Input Resistance (Note 2)		25	50	90	-	kΩ
Differential Input Capacitance		25	-	3	-	pF
Input Noise Voltage Density	f = 1000Hz	25	-	26	-	$nV/\sqrt{Hz}$
Input Noise Current Density	f = 1000Hz	25	-	4	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain	$V_{OUT} = \pm5V$	25	71	76	-	dB
		Full	68	-	-	dB
Common Mode Rejection Ratio	$V_{CM} = \pm5V$	Full	70	80	-	dB
Minimum Stable Gain		25	+1	-	-	V/V
Unity Gain Bandwidth	$A_V = +1$, $V_{OUT} = \pm100mV$	25	-	45	-	MHz
Gain Bandwidth Product	$V_{OUT} = \pm100mV$	25	-	50	-	MHz
Phase Margin	$A_V = +1$	25	-	65	-	Degrees
Gain Margin	$A_V = +1$	25	-	8.0	-	dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing	$R_L = 1k\Omega$	Full	±10	±11	-	V
Output Voltage Swing (Note 2)	$R_L = 75\Omega$	25	±2	-	-	V
Full Power Bandwidth (Note 3)		Full	3.8	5.1	-	MHz

Electrical Specifications $V_S = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, $V_{IL} = 0.8V$, $V_{IH} = 2.4V$. Unless Otherwise Specified Specifications Apply to All Channels **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (^oC)	HA-2444-5, -9			UNITS
			MIN	TYP	MAX	
Output Current (Note 12)		Full	±25	-	-	mA
Disabled Output Current (Note 13)		Full	-	-	860	µA
Output Resistance		25	-	20	-	Ω
TRANSIENT RESPONSE						
Rise Time (Note 4)	$A_V = +1$	25	-	7	-	ns
Overshoot (Note 4)	$A_V = +1$	25	-	10	-	%
Slew Rate (Note 6)	$A_V = +1$	Full	120	160	-	V/µs
Settling Time		25	-	120	-	ns
SWITCHING CHARACTERISTICS						
Channel Select Time	Note 7	0 to 85	-	60	100	ns
		-40 to 0	-	80	125	ns
Output Enable Time	Note 8	Full	-	40	100	ns
Digital Input Voltages	V_{IH}	Full	2.4	-	-	V
	V_{IL}	Full	-	-	0.8	V
D0/D1 Input Current	$V_{IL} = 0.0V$	Full	-	0.7	1	mA
	$V_{IH} = 5.0V$	Full	-	-	1.2	µA
EN Input Current	$V_{IL} = 0.0V$	Full	-	-	50	µA
	$V_{IH} = 5.0V$	Full	-	-	1.2	µA
Crosstalk Rejection	Note 9	25	-	60	-	dB
VIDEO PARAMETERS						
Differential Phase	Note 11	25	-	0.03	-	Degrees
Differential Gain	Note 11	25	-	0.03	-	%
Gain Flatness (Note 10)	10MHz, $A_V = +1$	25	-	0.1	-	dB
Chrominance to Luminance Gain	Note 11	25	-	0.1	-	dB
Chrominance to Luminance Delay	Note 11	25	-	7	-	ns
POWER SUPPLY						
I_{CC}		Full	-	20	25	mA
I_{EE}		Full	-	20	25	mA
Supply Current (Output Disabled)	Note 14	Full	-	-	10	mA
PSRR	$V_S = \pm15V$ to ±20V	Full	65	80	-	dB
Supply Voltage Range			±8.5	-	±17.0	V

NOTES:

2. These parameters are not tested. The limits are guaranteed based on lab characterization and reflect lot to lot variation.
3. Full Power Bandwidth is calculated by: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; $V_{PEAK} = 5V$.
4. $V_{OUT} = 0$ to ±200mV.
5. Settling time to 0.1% with a 10V step. Specified with the channel pre-selected and the output stage enabled. $A_V = -1$.
6. $V_{OUT} = -5V$ to +5V or +5V to -5V.
7. The time required for an enabled HA-2444 to switch from one input channel to another. Measured from the 50% point of the digital input to 50% of the output. $A_V = +1$ for all channels. V_{OUT} switches from 0V to 5V.
8. The time required to enable the output with a channel preselected. Measured from the 50% point of the Enable input to 4V on the output. $A_V = +1$ for all channels. $V_{IN} = 5V$ for the selected channel.
9. $V_{IN} = 5V_{P-P}$, f = 5MHz, for one of the 3 unselected channels. $V_{IN} = 0$ for the selected channel. $A_V = +1$ for all channels.
10. $V_{IN} = 200mV_{RMS}$.
11. Tested with a VM700A video tester using a NTC-7 Composite input signal.
12. $V_{OUT} = \pm10V$, $V_{EN} = 2.4V$, 50% Duty Cycle Max.
13. $V_{OUT} = \pm5V$, $V_{EN} = 0.8V$.
14. Applies to I_{CC} and I_{EE}. $V_{OUT} = 0V$, $V_{EN} = 0.8V$.

Die Characteristics

DIE DIMENSIONS:

74 mils x 103 mils x 19 mils
1880µm x 2620µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

PASSIVATION:

Type: Nitride over Silox
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

TRANSISTOR COUNT:

129

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout