iT2005

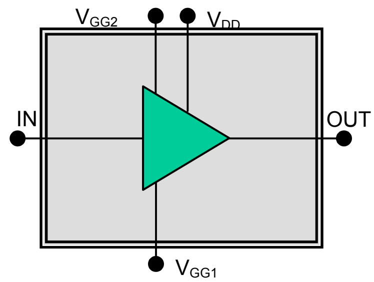
30 kHz – 26.5 GHz Power Amplifier

Description

The iT2005 is a broadband GaAs MMIC traveling wave amplifier designed for medium output power applications where low-frequency extension capabilities are also required. The iT2005 provides a saturated output power of 0.5 W up to 8 GHz, greater than 25 dBm up to 16 GHz, and greater than 20 dBm at 26.5 GHz. Average gain is 16 dB. DC power consumption is as low as 1.76 W. Input and output ports are DC coupled.

Features

- Frequency range: 2 GHz – 26.5 GHz with low-frequency extension capability down to 30 KHz
- Psat (2 GHz – 8 GHz): 27 dBm
- Psat (8 GHz – 16 GHz): 25 dBm
- Psat at 26.5 GHz: >20 dBm
- Average gain: 16 dB
- DC power consumption: 1.76 W
- DC bias conditions: 8 V at 220 mA
- Full chip passivation for high reliability



Absolute Maximum Ratings

Symbol	Parameters/conditions	Min.	Max.	Units
V_{DD}	Positive supply voltage		10	V
V_{GG1}	Negative supply voltage	-2	0	V
I_{DQ}	Positive supply current		600	mA
I_{GG1}	Negative supply current		1.8	mA
Pin	RF input power		23	dBm
Pdiss_DC	DC power dissipation (no RF)		4	W
Tch	Operating channel temperature		150	°C
Tm	Mounting temperature (30 s)		320	°C
Tst	Storage temperature	-65	150	°C

Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
Tb	Operating temperature range (back side)	-40		85	^{o}C
V_{DD}	Positive bias supply		8	9	V
V_{GG1}	Negative bias supply	-0.4	-0.6	-0.9	V
I_{DQ}	DC supply drain current		220	260	mA

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Electrical Characteristics

(at 25 °C)
50-ohm system
V_{DD} = +8 V
Quiescent current
(I_{DQ}) = 220 mA
V_{GG2} = +3.4 V

*Low frequency extension available.

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
BW	Frequency range*	2		26.5	GHz
S21	Small signal gain	10	16		dB
S11	Input return loss	12	15		dB
S22	Output return loss	12	15		dB
S12	Isolation	30			dB
Psat	Saturated output power (3 dB gain compression)				
	2 - 10GHz	24	26		dBm
	2- 20 GHz	21.5	23.5		dBm
	2 - 26.5 GHz	19	21		dBm
P_{1dB}	Output power (1 dB gain compression)				
	2 - 10 GHz	23	25		dBm
	2 - 20 GHz	20	22		dBm
	2 - 26.5 GHz	18	20		dBm

Thermal Characteristics

Symbol	Parameters/conditions	Rth_jb (°C/W)	Tch (°C)	MTTF (h)
Rth_jb	Thermal resistance junction-back side of die No RF: DC bias V_{DD} = 8 V, I_{DQ} = 220mA , P_{DC} = 1.76 W Tbase = 70 C	18.5	99.0	>> +1E7
Rth_jb	Thermal resistance junction-back side of die RF applied: Saturated power 0.5W, V_{DD} = 8 V, Pdiss = 2.15 W Tbase = 70 C	18.5	113.0	>> +1E7

Chip Layout and Bond Pad Locations

Pinout and pad dimensions:

P1: RF input (100 x 150 µm²)

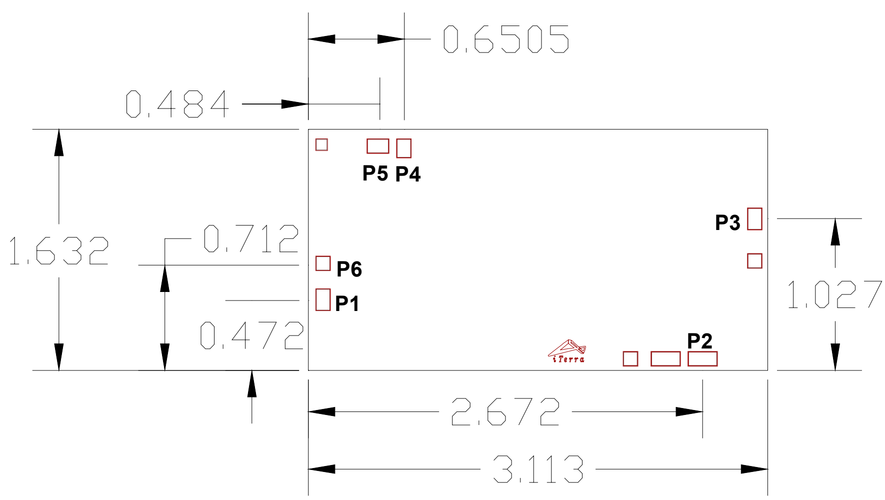
P2: VGG1, negative voltage (200 x 100 µm²)

P3: RF output and Vdd bias (option 2) by means of bias-tee (100 x 150 µm²)

P4: VDD positive voltage (option 1) by means of choke (100 x 130 µm²)

P5: Drain low-frequency extension (150 x 100 µm²)

P6: VGG2, second gate voltage (100 x 100 µm2)



Note: All dimensions are in millimeters

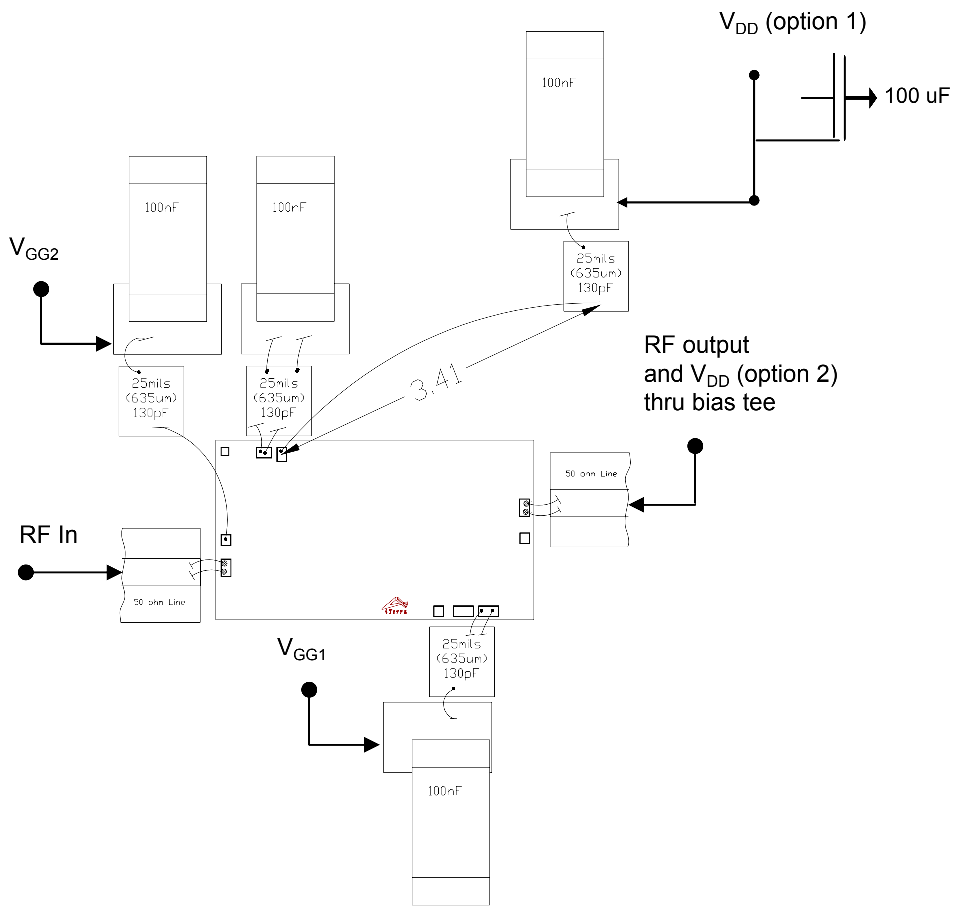
Chip size tolerance: ± 20 µm
Chip thickness: 4 mil with tolerance of ± 0.4 mil

Back of chip is RF and DC ground

Recommended Assembly Diagram for 2 to 26.5 GHz Applications

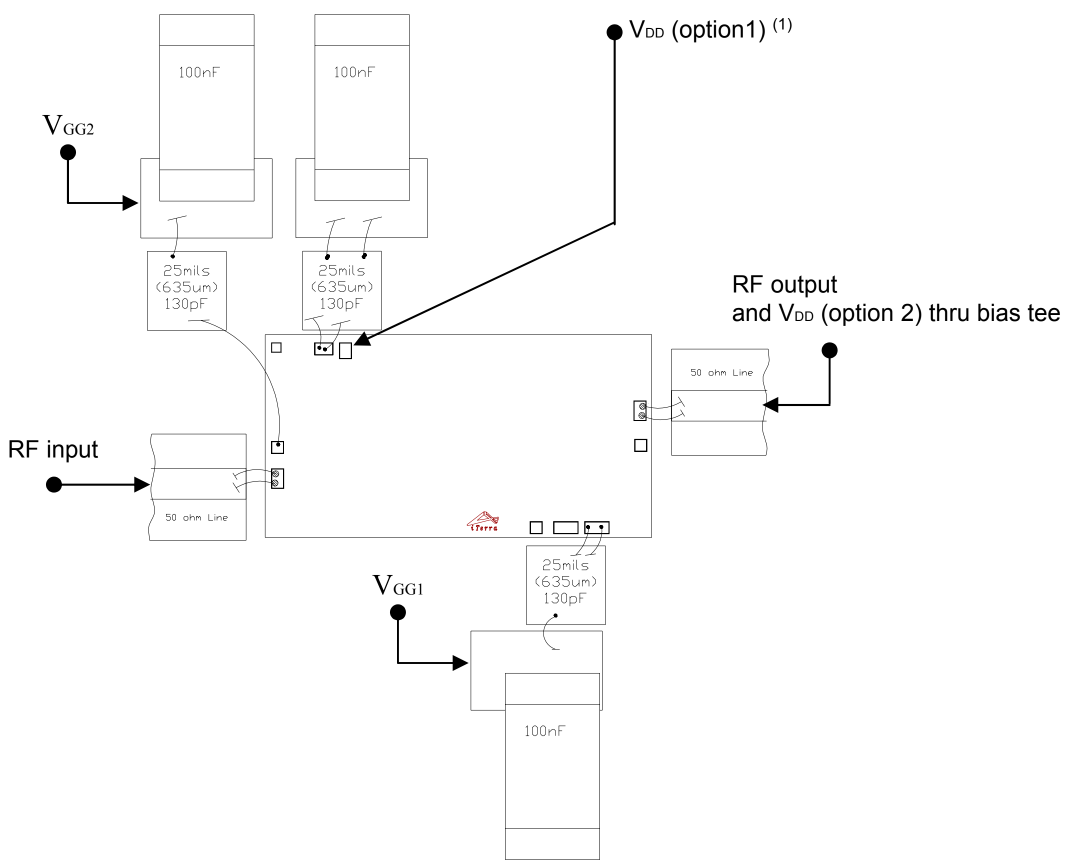
1. For applications at 2 GHz and above, an inductor of Lc> = 3 nH (1 mil long bond wire >3 mm) is necessary to provide drain bias.

2. Bypass capacitor must be large enough to isolate bias supply (> = 10 μF)



Recommended Assembly Diagram for 30 kHz to 26.5 GHz Applications

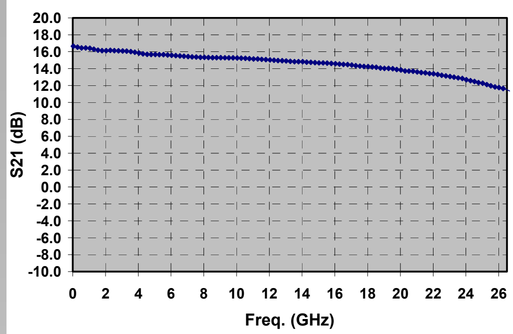
Appropriate low-frequency choke must be applied for 30 KHz application.



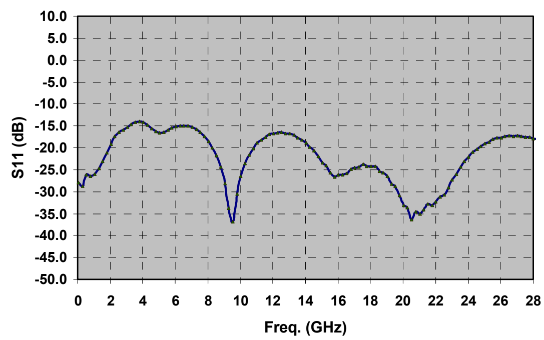
Performance Data

T = 25 °C

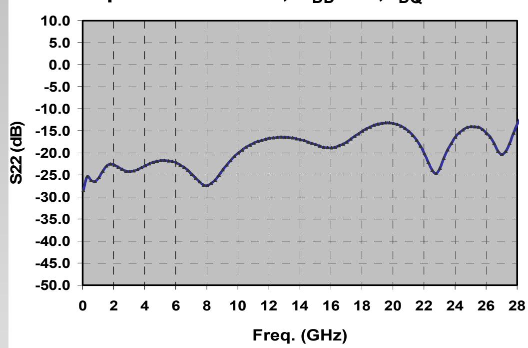
Small Signal Gain, V_{DD}=8V, I_{DQ}=220mA



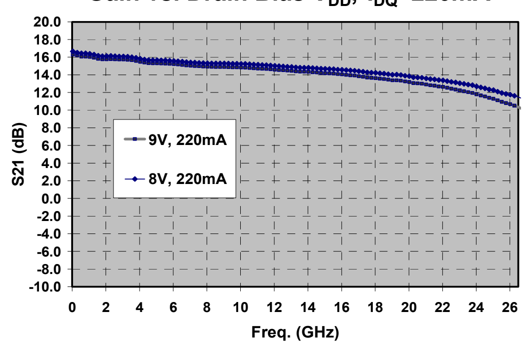
Input Return loss, V_{DD}=8V, I_{DQ}=220mA



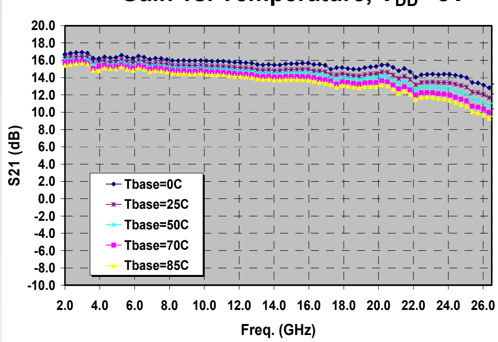
Output Return loss, V_{DD}=8V, I_{DQ}=220mA



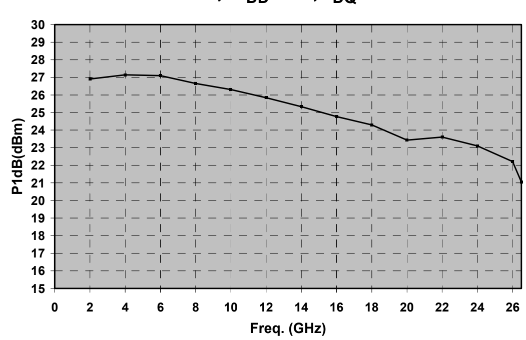
Gain vs. Drain Bias V_{DD}, I_{DQ}=220mA



Gain vs. Temperature, V_{DD} =8V



Saturated Power, V_{DD}=8V, I_{DQ}=220mA



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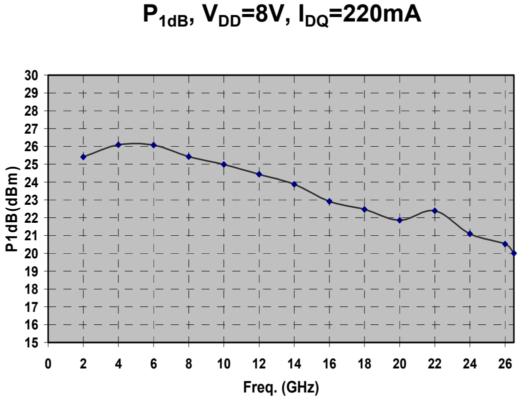
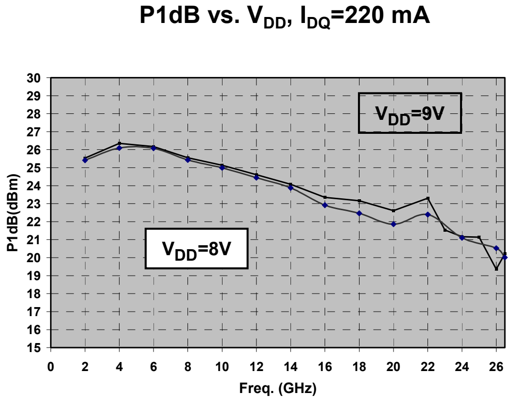
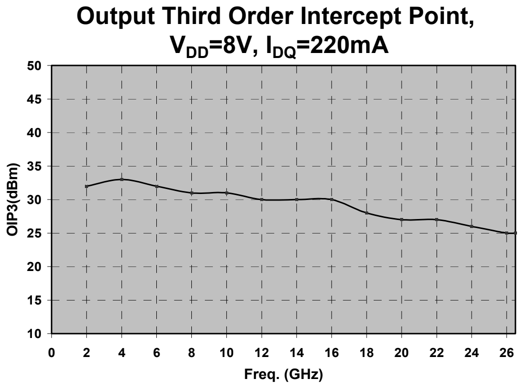
Performance Data

T = 25 °C







Recommended Procedure for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE (V_{GG1}) WHILE CORRESPONDING DRAIN VOLTAGE (V_{DD}) IS PRESENT CAN DAMAGE THE AMPLIFIER.

The following procedure must be considered to properly test the amplifier.

The iT2005 amplifier is biased with a positive drain supply (V_{DD}) and one negative gate supply (V_{GG1}). The recommended bias conditions for the iT2005 is V_{DD}= 8.0V, I_{DQ} = 220mA. To achieve this drain current level, V_{GG1} is typically biased between –0.5 V and –0.9 V. The gate voltage (V_{GG1}) MUST be applied prior to the drain voltage (V_{DD}) during power up and removed after the drain voltage is removed during the power down. Drain bias V_{DD} can be applied to the drain pad (pad 4), or the positive power supply can be applied through an external bias tee to the RF output pad.

For the second gate V_{GG2}, a voltage of about 3.4 V is required (V_{DD} = 8 V, V_{GG1} = -0.6 V). In general, $V_{GG2}=V_{DD}/2 – |V_{G1}|$. For example, when V_{DD} = 8 V and V_{GG1} = -0.6, the voltage recommended is: V_{GG2} =(8V/2)-0.6V=3.4V. V_{GG2} should be biased before or at the same time as V_{DD}.

Low Frequency Operation

External coupling capacitors are needed at the RF_IN (P1) and RF_OUT (P3) ports. Two options are allowed to provide the positive drain voltage V_{DD}. Option 1 uses an on-chip pad (P4) with an appropriate value of inductance (choke) used to maintain good matching over the operating bandwidth, as reported in the assembly diagram. Option 2 uses an external bias-tee directly from the pad at the RF output. For application as low as 30 KHz, a large value of inductance must be used in parallel with appropriate resistors in order to optimize gain flatness.

Application Information

CAUTION: THIS IS AN ESD-SENSITIVE DEVICE

Chip carrier material should be selected to have a GaAs-compatible thermal coefficient of expansion and high thermal conductivity, such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325° C for 15 min.

Die attachment for power devices should utilize gold/tin (80/20) eutectic alloy solder and should avoid a hydrogen environment for PHEMT devices. Note that the back side of the chip is gold plated and is used as RF and DC ground.

These GaAs devices should be handled with care and stored in a dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD-sensitive devices and should be handled with care, including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3-mil-wide and 0.5-mil-thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 12 mil long corresponding to a typical 2 mil gap between the chip and the substrate material.