PRELIMINARY

CY8CNP102B, CY8CNP102E

Nonvolatile Programmable System-on-Chip (PSoC® NV)

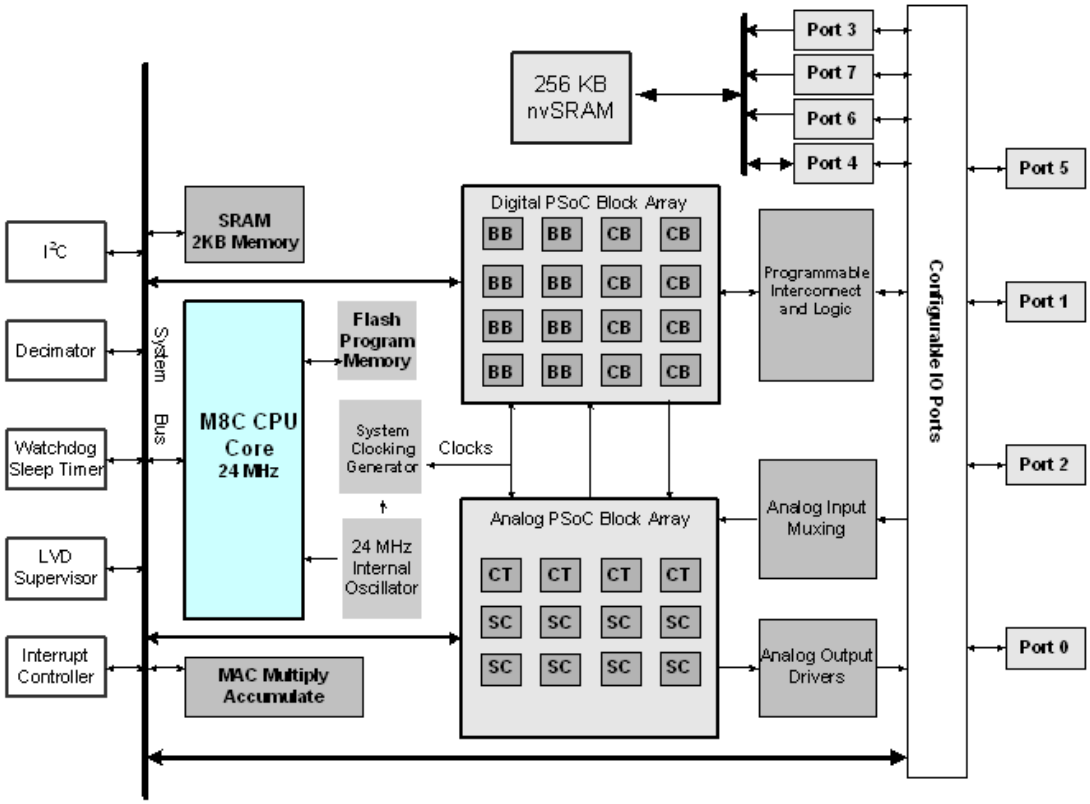
Overview

The Cypress nonvolatile Programmable System-on-Chip (PSoC® NV) processor combines a versatile Programmable System-on-Chip™ (PSoC) core with an infinite endurance nvSRAM in a single package. The PSoC NV combines an 8-bit MCU core (M8C), configurable analog and digital functions, a uniquely flexible IO interface, and a high density nvSRAM. This creates versatile data logging solutions that provide value through component integration and programmability. The flexible core and a powerful development environment work to reduce design complexity, component count, and development time.

Features

- Powerful Harvard Architecture Processor
  - M8C processor speeds
    - Up to 12 MHz for 3.3V operation
    - Up to 24 MHz for 5V operation
  - Two 8x8 multiply, 32 bit accumulate
  - Low power at high speed
- Operating Voltage
  - 3.3V (CY8CNP102B)
  - 5V (CY8CNP102E)
- Advanced Peripherals
  - 12 Rail-to-Rail Analog PSoC blocks provide:
    - Up to 14 bit ADCs
    - Up to 9 bit DACs
    - Programmable Gain Amplifiers
    - Programmable Filters and Comparators
    - 8 Analog channels for simultaneous sampling
    - Up to 820 SPS for each channel with 8 channel sampling and logging
  - 16 Digital PSoC Blocks provide:
    - 8 to 32 bit timers, counters, and PWMs
    - CRC and PRS Modules
    - Up to 4 Full Duplex UARTs
    - Multiple SPI™ Masters and Slaves
  - Complex Peripherals by Combining Blocks
- Precision, Programmable Clocking
  - Internal ±2.5% 24 and 48 MHz Oscillator
  - 24 and 48 MHz with optional 32.768 kHz Crystal
  - Optional External Oscillator, up to 24 MHz
  - Internal Oscillator for Watchdog and Sleep
- Flexible On-Chip Memory
  - 32K Bytes Flash Program Storage
  - 2K Bytes SRAM Data Storage
  - 256K Bytes secure store nvSRAM with data throughput between 100 KBPS and 1 MBPS
  - In-System Serial Programming (ISSP)
  - Partial Flash Updates
  - Flexible Protection Modes
  - EEPROM Emulation in Flash
- Programmable Pin Configurations
  - 33 GPIOs
  - 25 mA Sink on all GPIO
  - Pull up, Pull down, High Z, Strong, or Open Drain Drive Modes on all GPIO
  - Up to 12 Analog Inputs on GPIOs
  - Analog Outputs with 40 mA on 4 GPIOs
  - Configurable Interrupt on all GPIOs
- Additional System Resources
  - I^2C Slave, Master, and MultiMaster to 100 Kbps and 400 Kbps
  - Watchdog and Sleep Timers
  - Integrated Supervisory Circuit
  - On-Chip Precision Voltage Reference
- Complete Development Tools
  - Free Development Software (PSoC Designer™)
  - Full Featured, In Circuit Emulator and Programmer
  - Full Speed Emulation
  - C Compilers, Assembler, and Linker
- Temperature and Packaging
  - Industrial Temperature Range: -40°C to +85°C
  - Packaging: 100-pin TQFP

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - 100-Pin TQFP Package (14 x 14 x 1.4 mm)

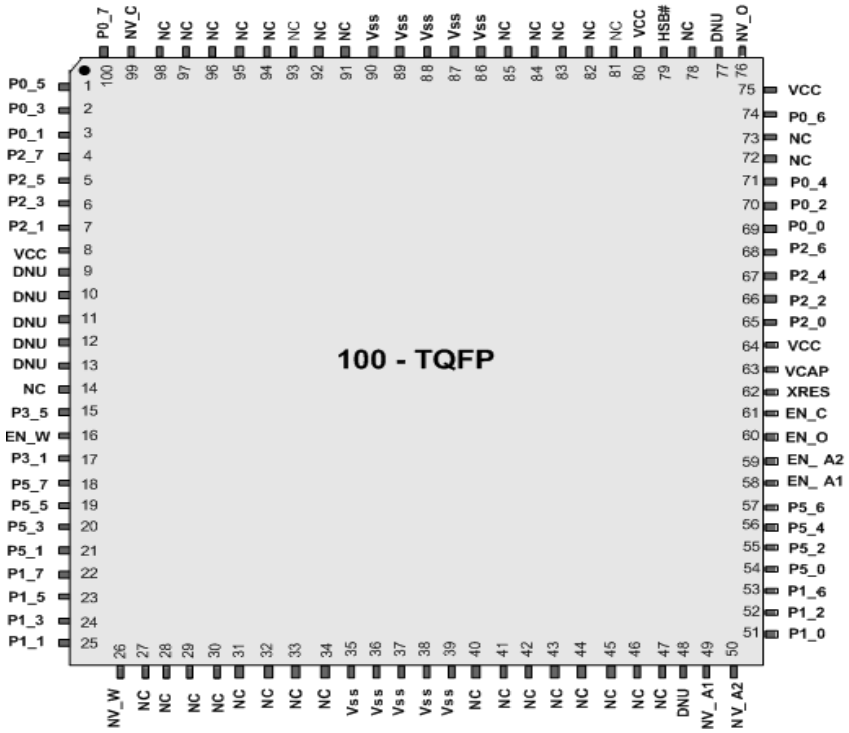


Table 1. Pin Definitions - 100-Pin TQFP

Pin Number	Pin Name	Type		Pin Definition
		Digital	Analog	
1	P0_5	IO	IO	Analog Column Mux Input and Column Output
2	P0_3	IO	IO	Analog Column Mux Input and Column Output
3	P0_1	IO	I	Analog Column Mux Input, GPIO
4	P2_7	IO		GPIO
5	P2_5	IO		GPIO
6	P2_3	IO	I	Direct Switched Capacitor Block Input
7	P2_1	IO	I	Direct Switched Capacitor Block Input
8	Vcc	Power		Supply Voltage
9	DNU			Reserved for test modes - Do Not Use
10	DNU			Reserved for test modes - Do Not Use
11	DNU			Reserved for test modes - Do Not Use
12	DNU			Reserved for test modes - Do Not Use
13	DNU			Reserved for test modes - Do Not Use
14	NC			Not connected on the die
15	P3_5	IO		GPIO
16	EN_W			Connect to Pin 26 (EN_W to NV_W)
17	P3_1	IO		GPIO

Table 1. Pin Definitions - 100-Pin TQFP (continued)

Pin Number	Pin Name	Type		Pin Definition
		Digital	Analog	
18	P5_7	IO		GPIO
19	P5_5	IO		GPIO
20	P5_3	IO		GPIO
21	P5_1	IO		GPIO
22	P1_7	IO		I2C Serial Clock (SCL), GPIO
23	P1_5	IO		I2C Serial Data (SDA), GPIO
24	P1_3	IO		GPIO
25	P1_1	IO		Serial Clock (SCL), Crystal (XTALin), GPIO
26	NV_W			Connect to pin 16 (NV_W to EN_W)
27 - 34	NC			Not connected on the die
35 - 39	Vss	Power		Ground
40 - 47	NC			Not connected on the die
48	DNU			Reserved for test modes - Do Not Use
49	NV_A1			Connect to pin 58 (NV_A1 to EN_A1)
50	NV_A2			Connect to pin 59 (NV_A2 to EN_A2)
51	P1_0	IO		Serial Data (SDA), Crystal (XTALout), GPIO
52	P1_2	IO		GPIO
53	P1_6	IO		GPIO
54	P5_0	IO		GPIO
55	P5_2	IO		GPIO
56	P5_4	IO		GPIO
57	P5_6	IO		GPIO
58	EN_A1			Connect to Pin 49 (EN_A1 to NV_A1)
59	EN_A2			Connect to Pin 50 (EN_A2 to NV_A2)
60	EN_O			Connect to Pin 76 (EN_O to NV_O)
61	EN_C			Connect to Pin 99 (EN_C to NV_C)
62	XRES	Input		Active high external reset (Internal Pull down)
63	VCAP	Power		External Capacitor connection for nvSRAM
64	Vcc	Power		Supply Voltage
65	P2_0	IO	I	Direct Switched Capacitor Block Input, GPIO
66	P2_2	IO	I	Direct Switched Capacitor Block Input, GPIO
67	P2_4	IO		External Analog GND, GPIO
68	P2_6	IO		External Voltage Ref, GPIO
69	P0_0	IO	I	Analog Column Mux Input, GPIO
70	P0_2	IO	IO	Analog Column Mux Input and Column Output
71	P0_4	IO	IO	Analog Column Mux Input and Column Output
72-73	NC			Not connected on the die
74	P0_6	IO	I	Analog Column Mux Input, GPIO
75	Vcc	Power		Supply Voltage
76	NV_O			Connect to Pin 60 (NV_O to EN_O)
77	DNU			Reserved for test modes - Do Not Use
78	NC			Not connected on the die

Table 1. Pin Definitions - 100-Pin TQFP (continued)

Pin Number	Pin Name	Type		Pin Definition
		Digital	Analog	
79	HSB#			Weak Pull up. Connect 10kΩ to Vcc.
80	Vcc	Power		Supply Voltage
81 - 85	NC			Not connected on the die
86 - 90	Vss	Power		Ground
91 - 98	NC			Not connected on the die
99	NV_C			Connect to Pin 61 (NV_C to EN_C).Weak Pull up. Connect 10kΩ to Vcc.
100	P0_7	IO	I	Analog Column Mux Input, GPIO

PSoC NV Functional Overview

The PSoC NV provides a versatile microcontroller core (M8C), Flash program memory, nvSRAM data memory, and configurable analog and digital peripheral blocks in a single package. The flexible digital and analog IOs and routing matrix create a powerful embedded and flexible mixed signal System-on-Chip (SoC).

The device incorporates configurable analog and digital blocks, interconnect circuitry around an MCU subsystem, and an infinite endurance nvSRAM. This enables high level integration in consumer, industrial, and automotive applications, where preventing data loss under all conditions is vital.

PSoC NV Core

The PSoC NV core is a powerful PSoC engine that supports a rich feature set. The core includes a M8C CPU, memory, clocks, and configurable GPIO (General Purpose IO). The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with 25 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

On-chip memory encompasses 32 KB Flash for program storage, 2 KB SRAM for data storage, 256 KB nvSRAM for data logging, and up to 2 KB EEPROM emulated using Flash. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection. The nvSRAM combines a static RAM cell and a SONOS cell to provide an infinite endurance nonvolatile memory block. The memory is random access and is accessed using a user module provided with the device.

The device incorporates flexible internal clock generators, including a 24 MHz Internal Main Oscillator (IMO) accurate to 2.5 percent over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz Internal Low speed Oscillator (ILO) is provided for the Sleep timer and WDT. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC NV device.

GPIOs provide connection to the CPU, and digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

nvSRAM Data Memory

The nvSRAM memory block is byte addressable fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap® technology producing the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, when independent nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down, and data is restored to the SRAM (the RECALL operation) from the nonvolatile memory on power up. All cells store and recall data in parallel.

Both the STORE and RECALL operations may be initiated under software control. The PSoC NV user module embedded in the PSoC Designer Tool provides all necessary APIs to initiate software STORE and RECALL function from the user program.

nvSRAM Operation

The nvSRAM is made up of an SRAM memory cell, and a nonvolatile QuantumTrap cell paired in the same physical cell. The SRAM memory cell operates as a standard fast static, and all READ and WRITE takes place from the SRAM during normal operation.

During the STORE and RECALL operations, SRAM READ and WRITE operations are inhibited, and internal operations transfer data between the SRAM and nonvolatile cells. The nvSRAM provides infinite RECALL operations from the nonvolatile cells and up to 200,000 STORE operations.

To reduce unnecessary nonvolatile stores, AutoStore® is ignored unless at least one WRITE operation is complete after the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. Embedded APIs provide a seamless interface to the nvSRAM.

During normal operation, the embedded nvSRAM draws current from Vcc to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a STORE operation. If the voltage on the Vcc pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from Vcc and STORE operation is initiated.

Programmable Digital System

The digital system contains 16 digital PSoC blocks. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references. The digital peripheral configurations are:

- PWMs (8 to 32 bit)
- PWMs with dead band (8 to 32 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity (up to 4)
- SPI master and slave (up to 4 each)
- I^2C slave and multimaster (1 available as a System Resource)
- Cyclical Redundancy Checker and Generator (8 to 32 bit)
- IrDA (up to 4)
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks connect to any GPIO through a series of global buses that route any signal to any pin. The buses also enable signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies with PSoC device family. This gives you the optimum choice of system resources for your application.

Programmable Analog System

The analog system consists 12 configurable blocks, each having an opamp circuit enabling the creation of complex analog signal flows. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the more common analog functions (most available as user modules) are:

- Analog-to-digital converters (up to 4, with 6 to 14 bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (2, 4, 6, or 8 pole band pass, low pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 4, with 16 selectable thresholds)
- DACs (up to 4, with 6 to 9 bit resolution)
- Multiplying DACs (up to 4, with 6 to 9 bit resolution)
- High current output drivers (four with 40 mA drive as a Core Resource)
- 1.3V reference (as a System Resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak Detectors
- Other possible topologies
- Analog blocks are provided in columns of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks.

Additional System Resources

System Resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Resources include a multiplier, decimator, switch mode pump, low voltage detection, and power on reset. The merits of each system resource are:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks may be routed to both the digital and analog systems. Additional clocks are generated using digital PSoC blocks as clock dividers.
- Multiply Accumulate (MAC) provides fast 8-bit multiplier with 32-bit accumulate, to assist in general math and digital filters.
- The decimator provides a custom hardware filter for digital signal, and processing applications including the creation of Delta Sigma ADCs.
- The I^2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.

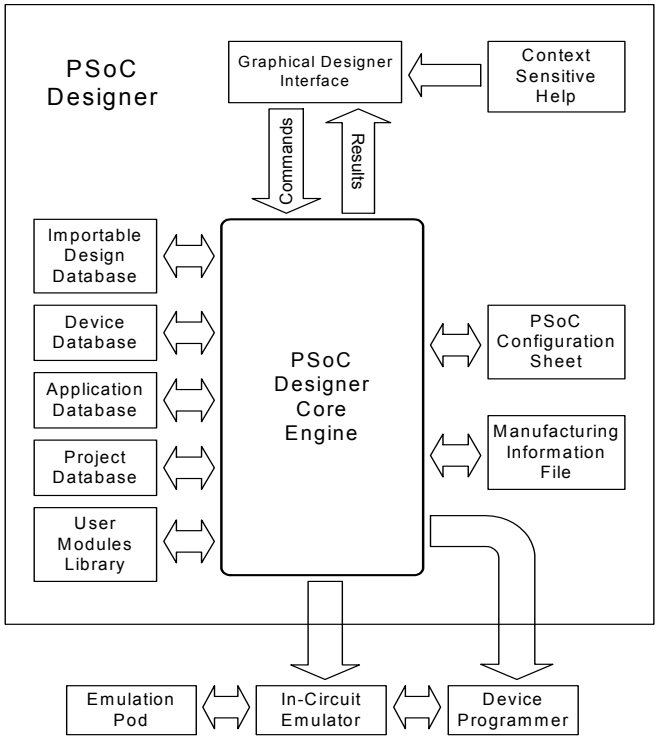
Development Tools

PSoC Designer is a Microsoft® Windows based, integrated development environment for Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application run on Windows NT 4.0, Windows 2000, Windows Millennium (Me), Microsoft Vista, and Windows XP.

PSoC Designer helps the customer to select an operating configuration for the PSoC, write application code that uses the PSoC, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high level C language compiler developed specifically for the devices in this family.

Figure 2. PSoC Designer Subsystem



PSoC Designer Software Subsystems

Device Editor

The Device Editor subsystem enables the user to select different onboard analog and digital components called user modules, using the PSoC blocks. Examples of user modules are ADCs, DACs, nvSRAM, Amplifiers, and Filters.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration enables changing configurations at run time.

PSoC Designer sets up power on initialization tables for selected PSoC block configurations and creates source code for an application framework. The framework contains software to operate the selected components. Also, if the project uses more than one operating configuration, the framework contains routines to switch between different sets of PSoC block configurations at run time. PSoC Designer can print out a configuration sheet for a given project configuration, for use during application programming in conjunction with the Device Data Sheet. After the framework is generated, the user can add application specific code to flesh out the framework. It is also possible to change the selected components and regenerate the framework.

Design Browser

The Design Browser enables users to select and import preconfigured designs into their project. Users can easily browse a catalog of preconfigured designs to facilitate time to design. Examples provided in the tools include a 300 baud modem, LIN Bus master and slave, fan controller, and magnetic card reader.

Application Editor

In the Application Editor you can edit C language and Assembly language source code. You can also assemble, compile, link, and build.

Assembler. The macro assembler seamlessly merges the assembly code with C code. The link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compiler. A C language compiler that supports Cypress PSoC family devices is available. Even if you have never worked in the C language before, the product quickly enables you to create complete C programs for the PSoC family devices.

The embedded, optimizing C compiler provides all the features of C tailored to the PSoC architecture. It is complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, which enables the designer to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands enable the designer to read and program, read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also enables the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC through the USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

Designing with User Modules

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that manages specification change during development and lowers inventory costs. These configurable resources, called PSoC Blocks, implement a wide variety of user-selectable functions. Each block has several registers that determine its function and connectivity to other blocks, multiplexers, buses, and to the IO pins. Iterative development cycles permit you to adapt the hardware and the software. This substantially lowers the risk of selecting a different part to meet the final design requirements.

To speed the development process, the PSoC Designer IDE provides a library of prebuilt, pretested hardware peripheral functions, called “User Modules.” User modules simplify selecting and implementing peripheral devices, and come in analog, digital, and mixed signal varieties. The standard User Module library contains over 50 peripherals such as ADCs, DACs, Timers, Counters, UARTs, nvSRAM, DTMF Generators, and Bi-Quad analog filter sections.

Each user module establishes the basic register settings that implement the selected function. It also provides parameters that enable you to tailor its precise configuration to your particular application. For example, a Pulse Width Modulator User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. User modules also provide tested software to cut your development time. The user module Application Programming Interface (API) provides high level functions to control and respond to hardware events at run time. The API also provides optional interrupt service routines that you can adapt as needed.

The API functions are documented in user module data sheets that are viewed directly in the PSoC Designer IDE. These data sheets explain the internal operation of the user module and provide performance specifications. Each data sheet describes the use of each user module parameter and documents the setting of each register controlled by the user module.

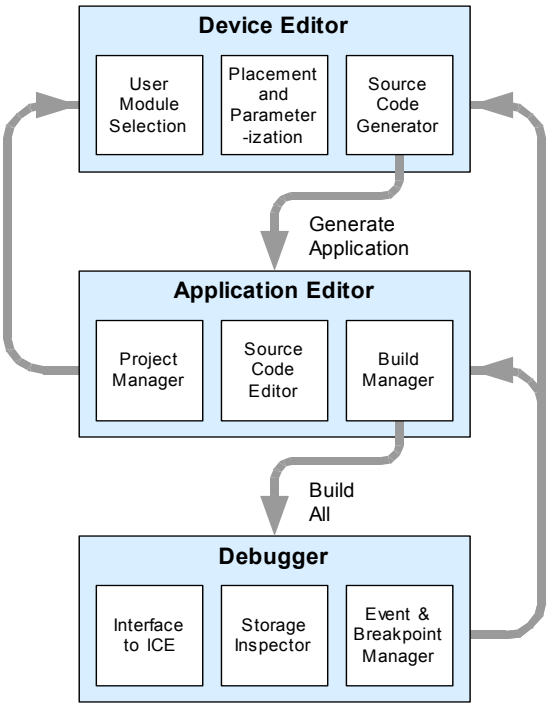
The development process starts when you open a new project and bring up the Device Editor, which is a graphical user interface (GUI) for configuring the hardware. Pick the user modules required for your project and map them onto the PSoC blocks with point and click simplicity. Next, build signal chains by interconnecting user modules to each other and to the IO pins. At this stage, configure the clock source connections and enter parameter values directly or by selecting values from drop down menus. When you are ready to test the hardware configuration or develop code for the project, perform the “Generate Application” step. PSoC Designer generates source code that automatically configures the device to your specification and provides high level user module API functions.

User Module and Source Code Development Flows

The next step is to write the main program, and any subroutine using PSoC Designer’s Application Editor subsystem. The Application Editor includes a Project Manager that enables you to open the project source code files (including all generated code files) from a hierarchal view. The source code editor provides syntax coloring and advanced edit features for C and assembly language. File search capabilities include simple string searches and recursive “grep-style” patterns. A single mouse click invokes the Build Manager.

It employs a professional strength “makefile” system to automatically analyze all file dependencies and run the compiler and assembler as necessary. Project level options control optimization strategies used by the compiler and linker. Syntax errors are displayed in a console window. Double clicking the error message takes you directly to the offending line of source code. After correction, the linker builds a HEX file image suitable for programming.

Figure 3. User Module and Source Code Development Flows



The last step in the development process takes place inside the PSoC Designer's Debugger subsystem. The Debugger downloads the HEX image to the In-Circuit Emulator (ICE) where it runs at full speed. The Debugger capabilities rival those of systems costing much more. In addition to traditional single step, run to breakpoint, and watch variable features, the Debugger provides a large trace buffer enabling you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Cypress nvSRAM user Module

The nvSRAM user module is integrated with the PSoC Designer tool and contains APIs that facilitate nvSRAM access and control. The user module provides high level access to the nvSRAM without user developed code. The user module API also provides the ability to read and write arbitrary data structures to or from the nvSRAM, and initiate nvSRAM Store or Recall operations.

Electrical Specifications

This section lists the PSoC NV device DC and AC electrical specifications.

Specifications are valid for -40°C ≤ T_A ≤ 85°C, and T_J ≤ 100°C, except where noted.

Refer Table 14 on page 17 for electrical specifications on the Internal Main Oscillator (IMO) using SLIMO mode.

Figure 4. Voltage versus CPU Frequency

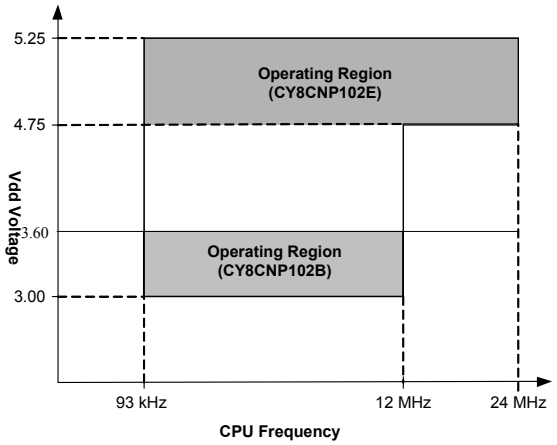
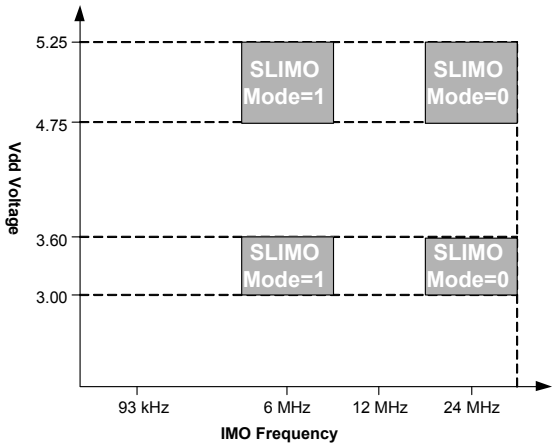


Figure 5. IMO Frequency Trim Options



The following table lists the units of measure that are used in this data sheet.

Table 2. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	microwatts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
µA	microampere	pp	peak-to-peak
µF	microfarad	ppm	parts per million
µH	microhenry	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolts	σ	sigma: one standard deviation
µVrms	microvolts root-mean-square	V	volts

3.3V Operation

Absolute Maximum Ratings

Table 3. 3.3V Absolute Maximum Ratings (CY8CNP102B)

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is ± 25°C. Extended duration storage temperatures above 65°C degrade reliability.
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	
Vcc	Supply Voltage on Vcc Relative to Vss	-0.5	–	+4.1	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vcc + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vcc + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch-up Current	–	–	200	mA	

Operating Temperature

Table 4. 3.3V Operating Temperature (CY8CNP102B)

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	°C	
T_J	Junction Temperature	-40	–	+100	°C	

DC Electrical Characteristics

The following DC electrical specifications list the guaranteed maximum and minimum specifications for the voltage and temperature range: 3.0V to 3.6V over the Temperature range of -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 3.3V at 25°C and are for design guidance only.

DC Chip Level Specifications

Table 5. 3.3V DC Chip Level Specifications (CY8CNP102B)

Symbol	Description	Min	Typ	Max	Units	Notes
Vcc	Supply Voltage	3.00	–	3.6	V	
I_{DD}	Supply Current	–	36	40	mA	T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz, continuous nvSRAM access
I_{DDP}	Supply current when IMO = 6 MHz using SLIMO mode.	–	27	28	mA	T_A = 25 °C, CPU = 0.75 MHz, SYSCLK doubler disabled, VC1=0.375 MHz, VC2=23.44 kHz, VC3 = 0.09 kHz, continuous nvSRAM access
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active.	–	–	5	mA	nvSRAM in standby.
V_{REF}	Reference Voltage (Bandgap)	1.28	1.3	1.32	V	Trimmed for appropriate Vcc.
V_{cap}	Storage Capacitor between Vcap and Vss	61	68	82	uF	5V rated (minimum)

DC General Purpose IO Specifications

Table 6. 3.3V DC GPIO Specifications (CY8CNP102B)

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull up Resistor	4	5.6	8	KΩ	
R_{PD}	Pull down Resistor	4	5.6	8	KΩ	
V_{OH}	High Output Level	Vcc - 1.0	–	–	V	IOH = 10 mA, Vcc = 3.0 to 3.6V. 8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5]). 80 mA maximum combined IOH budget.
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vcc = 3.0 to 3.6V 8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5]). 150 mA maximum combined IOL budget.
V_{IL}	Input Low Level	–	–	0.8	V	Vcc = 3.0 to 3.6
V_{IH}	Input High Level	1.6	–		V	Vcc = 3.0 to 3.6
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Pin dependent. Temp = 25°C.

DC Operational Amplifier Specifications

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 7. 3.3V DC Operational Amplifier Specifications (CY8CNP102B)

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value)					High Power is 5 Volts Only
	Power = Low, Opamp Bias = High	–	1.65	10	mV	
	Power = Medium, Opamp Bias = High	–	1.32	8	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Pin dependent. Temp = 25 °C.
V_{CMOA}	Common Mode Voltage Range	0	–	Vcc	V	
$CMRR_{OA}$	Common Mode Rejection Ratio	60	–	–	dB	
G_{OLOA}	Open Loop Gain	80	–	–	dB	
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals)	Vcc - 0.01	–	–	V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals)	–	–	0.01	V	
I_{SOA}	Supply Current (including associated AGND buffer)					
	Power = Low, Opamp Bias = Low	–	150	200	µA	
	Power = Low, Opamp Bias = High	–	300	400	µA	
	Power = Medium, Opamp Bias = Low	–	600	800	µA	
	Power = Medium, Opamp Bias = High	–	1200	1600	µA	
	Power = High, Opamp Bias = Low	–	2400	3200	µA	
	Power = High, Opamp Bias = High	–	–	–	µA	Not Allowed for 3.3V operation
$PSRR_{OA}$	Supply Voltage Rejection Ratio	54	80	–	dB	Vss ≤ VIN ≤ (Vcc - 2.25) or (Vcc - 1.25V) ≤ VIN ≤ Vcc

DC Low Power Comparator Specifications

Table 8. 3.3V DC Low Power Comparator Specifications (CY8CNP102B)

Symbol	Description	Min	Typ	Max	Units
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	Vcc - 1.0	V
I_{SLPC}	LPC supply current	–	10	40	µA
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV

DC Analog Output Buffer Specifications

Table 9. 3.3V DC Analog Output Buffer Specifications (CY8CNP102B)

Symbol	Description	Min	Typ	Max	Units
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C
V_{CMOB}	Common-Mode Input Voltage Range	0.5	-	Vcc - 1.0	V
R_{OUTOB}	Output Resistance				
	Power = Low	–	–	10	Ω
	Power = High	–	–	10	Ω
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1KΩ to Vcc/2)				
	Power = Low	0.5 x Vcc + 1.0	–	–	V
	Power = High	0.5 x Vcc + 1.0	–	–	V
V_{OLOWOB}	Low Output Voltage Swing (Load = 1KΩ to Vcc/2)				
	Power = Low	–	–	0.5 x Vcc - 1.0	V
	Power = High	–	–	0.5 x Vcc - 1.0	V
I_{SOB}	Supply Current Including Bias Cell (No Load)				
	Power = Low	–	0.8	1	mA
	Power = High	–	2.0	5	mA
$PSRR_{OB}$	Supply Voltage Rejection Ratio	60	64	–	dB

DC Analog Reference Specifications

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 10. 3.3V DC Analog Reference Specifications (CY8CNP102B)

Symbol	Description	Min	Typ	Max	Units
V_{BG33}	Bandgap Voltage Reference 3.3V	1.28	1.30	1.32	V
–	AGND = Vcc/2[1]	Vcc/2 - 0.02	Vcc/2	Vcc/2 + 0.02	V
–	AGND = 2 x BandGap[1]	Not Allowed			
–	AGND = P2[4] (P2[4] = Vcc/2)	P2[4] - 0.009	P2[4]	P2[4] + 0.009	V
–	AGND = BandGap[1]	1.27	1.30	1.34	V
–	AGND = 1.6 x BandGap[1]	2.03	2.08	2.13	V
–	AGND Block to Block Variation (AGND = Vcc/2)[1]	-0.034	0.000	0.034	mV
–	RefHi = Vcc/2 + BandGap	Not Allowed			
–	RefHi = 3 x BandGap	Not Allowed			
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefHi = P2[4] + BandGap (P2[4] = Vcc/2)	Not Allowed			
–	RefHi = P2[4] + P2[6] (P2[4] = Vcc/2, P2[6] = 0.5V)	P2[4] + P2[6] - 0.042	P2[4] + P2[6]	P2[4] + P2[6] + 0.042	V
–	RefHi = 2 x BandGap	2.50	2.60	2.70	V
–	RefHi = 3.2 x BandGap	Not Allowed			
–	RefLo = Vcc/2 - BandGap	Not Allowed			
–	RefLo = BandGap	Not Allowed			
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefLo = P2[4] – BandGap (P2[4] = Vcc/2)	Not Allowed			
–	RefLo = P2[4]-P2[6] (P2[4] = Vcc/2, P2[6] = 0.5V)	P2[4] - P2[6] - 0.036	P2[4] - P2[6]	P2[4] - P2[6] + 0.036	V

DC Analog PSoC NV Block Specifications

Table 11. 3.3V DC Analog PSoC NV Block Specifications (CY8CNP102B)

Symbol	Description	Min	Typ	Max	Units
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ
C_{SC}	Capacitor Unit Value (Switch Cap)	–	80	–	fF

Note
1. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 0.02V.

DC POR, SMP, and LVD Specifications

Table 12. 3.3V DC POR, SMP, and LVD Specifications (CY8CNP102B)

Symbol	Description	Min	Typ	Max	Units
	Vdd Value for PPOR Trip (positive ramp)				
V_{PPOR0R}	PORLEV[1:0] = 00b		2.91		V
	Vdd Value for PPOR Trip (negative ramp)				
V_{PPOR0}	PORLEV[1:0] = 00b		2.82		V
	PPOR Hysteresis				
V_{PH0}	PORLEV[1:0] = 00b		92		mV
V_{PH1}	PORLEV[1:0] = 01b		0		mV
V_{PH2}	PORLEV[1:0] = 10b		0		mV
	Vdd Value for LVD Trip				
V_{LVD0}	VM[2:0] = 000b	2.86	2.92	2.98[2]	V
V_{LVD1}	VM[2:0] = 001b	2.96	3.02	3.08	V
V_{LVD2}	VM[2:0] = 010b	3.07	3.13	3.20	V
	Vdd Value for SMP Trip				
V_{PUMP0}	VM[2:0] = 000b	2.96	3.02	3.08	V
V_{PUMP1}	VM[2:0] = 001b	3.03	3.10	3.16	V
V_{PUMP2}	VM[2:0] = 010b	3.18	3.25	3.32	V

Note
2. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.

DC Programming Specifications

Table 13. 3.3V DC Programming Specifications (CY8CNP102B)

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDPV}	Supply Current During Programming or Verify	–	10	30	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vcc - 1.0	–	Vcc	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[3]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

Note
3. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single lock ever sees more than 50,000 cycles). For the full industrial range, the user must employ a temperature sensor user module (Flash Temp) and feed the result to the temperature argument before timing. Refer to the Flash APIs Application Note AN2015 at http//www.cypress.com under Application Notes for more information.

AC Electrical Characteristics

The following AC electrical specifications list the guaranteed maximum and minimum specifications for the voltage and temperature range: 3.0V to 3.6V over the temperature range of -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 3.3V at 25°C and are for design guidance only.

AC Chip Level Specifications

Table 14. 3.3V AC Chip Level Specifications (CY8CNP102B)

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	23.4	24	24.6[4, 5, 6]	MHz	Trimmed for 3.3V operation using factory trim values. See the figure on page 10. SLIMO Mode = 0.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.75	6	6.35[4 , 5, 6]	MHz	Trimmed for 3.3V operation using factory trim values. See the figure on page 10. SLIMO Mode = 1.
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.3[5, 6]	MHz	
F_{48M}	Digital PSoC Block Frequency	0	48	49.2[4, 5, 7]	MHz	Refer to section AC Digital Block Specifications on page 19.
F_{24M}	Digital PSoC Block Frequency	0	24	24.6[5, 7]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	A multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	–	–	600	ps	
$T_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	
$T_{PLLSLEWLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	–	250	500	ms	
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	300	600	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal.
Jitter32k	32 kHz Period Jitter	–	100		ns	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2[4,6]	MHz	Trimmed. Using factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO)	–	600		ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

Notes
4. 4.75V < Vcc < 5.25V.
5. Accuracy derived from Internal Main Oscillator with appropriate trim for Vcc range.
6. 3.0V < Vcc < 3.6V. See Application Note AN2012 “Adjusting PSoC Micro controller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.
7. See individual user module data sheets for information on maximum frequencies for user modules.

In the following table, $t_{HRECALL}$ starts from the time Vcc rises above V_{SWITCH}. If an SRAM WRITE has not taken place since the last nonvolatile cycle, no STORE occurs. Industrial grade devices require 15 ms maximum.

Table 15.3.3V nvSRAM AutoStore/Power Up RECALL (CY8CNP102B)

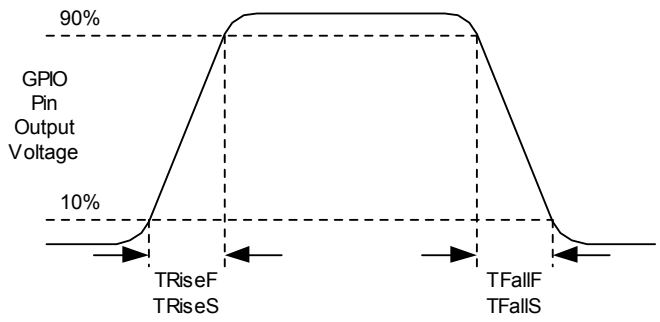
Parameter	Description	nvSRAM		Unit
		Min	Max	
$t_{HRECALL}$	Power Up RECALL Duration		20	ms
t_{STORE}	STORE Cycle Duration		12.5	ms
V_{SWITCH}	Low Voltage Trigger Level		2.65	V
$t_{VccRISE}$	VCC Rise Time	150		µs

AC General Purpose IO Specifications

Table 16. 3.3V AC GPIO Specifications (CY8CNP102B)

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12.3	MHz	Normal Strong Mode
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	Vcc = 3V to 3.6V 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	Vcc = 3V to 3.6V 10% - 90%

Figure 6. GPIO Timing Diagram



AC Operational Amplifier Specifications

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Table 17. 3.3V AC Operational Amplifier Specifications (CY8CNP102B)

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time to 0.1% of a 1V Step (10 pF load, Unity Gain)					Power = High and Opamp Bias = High is not supported at 3.3V.
	Power = Low, Opamp Bias = Low	–	–	3.92	µs	
	Power = Medium, Opamp Bias = High	–	–	0.72	µs	
T_{SOA}	Falling Settling Time to 0.1% of a 1V Step (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	–	–	5.41	µs	
	Power = Medium, Opamp Bias = High	–	–	0.72	µs	
SR_{ROA}	Rising Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.31	–	–	V/µs	
	Power = Medium, Opamp Bias = High	2.7	–	–	V/µs	
SR_{FOA}	Falling Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.24	–	–	V/µs	
	Power = Medium, Opamp Bias = High	1.8	–	–	V/µs	
BW_{OA}	Gain Bandwidth Product					
	Power = Low, Opamp Bias = Low	0.67	–	–	MHz	
	Power = Medium, Opamp Bias = High	2.8	–	–	MHz	
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz	

AC Digital Block Specifications

Table 18. 3.3V AC Digital Block Specifications (CY8CNP102B)

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Maximum Block Clocking Frequency			24.6	MHz	3.0V ≤ Vcc ≤ 3.6V
Timer	Capture Pulse Width	50[8]	–	–	ns	
	Maximum Frequency, No Capture	–	–	24.6	MHz	3.0V ≤ Vcc ≤ 3.6V.
	Maximum Frequency, With Capture	–	–	24.6	MHz	3.0V ≤ Vcc ≤ 3.6V.
Counter	Enable Pulse Width	50[8]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	24.6	MHz	3.0V ≤ Vcc ≤3.6V.
	Maximum Frequency, Enable Input	–	–	24.6	MHz	3.0V ≤ Vcc ≤ 3.6V.
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[8]	–	–	ns	
	Disable Mode	50[8]	–	–	ns	
	Maximum Frequency	–	–	24.6	MHz	3.0V ≤ Vcc ≤ 3.6V

Note
8. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Table 18. 3.3V AC Digital Block Specifications (CY8CNP102B) (continued)

Function	Description	Min	Typ	Max	Units	Notes
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	3.0V ≤ Vcc ≤ 3.6V
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	3.0V ≤ Vcc ≤ 3.6V.
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	ns	
	Width of SS_ Negated Between Transmissions	50[8]	–	–	ns	
Transmitter	Maximum Input Clock Frequency Vcc ≥ 3.0V, 2 Stop Bits	– –	– –	24.6 49.2	MHz MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking. Maximum data rate at 6.15 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
	Vcc ≥ 3.0V, 2 Stop Bits	–	–	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.

AC Analog Output Buffer Specifications

Table 19. 3.3V AC Analog Output Buffer Specifications (CY8CNP102B)

Symbol	Description	Min	Typ	Max	Units
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100pF Load				
	Power = Low	–	–	4.7	µs
	Power = High	–	–	4.7	µs
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100pF Load				
	Power = Low	–	–	4	µs
	Power = High	–	–	4	µs
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load				
	Power = Low	0.36	–	–	V/µs
	Power = High	0.36	–	–	V/µs
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load				
	Power = Low	0.4	–	–	V/µs
	Power = High	0.4	–	–	V/µs
BW_{OB}	Small Signal Bandwidth, 20mV$_{pp}$, 3dB BW, 100pF Load				
	Power = Low	0.7	–	–	MHz
	Power = High	0.7	–	–	MHz
BW_{OB}	Large Signal Bandwidth, 1V$_{pp}$, 3dB BW, 100pF Load				
	Power = Low	200	–	–	kHz
	Power = High	200	–	–	kHz

AC Programming Specifications

Table 20. 3.3V AC Programming Specifications (CY8CNP102B)

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
T_{WRITE}	Flash Block Write Time	–	10	–	ms	
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.0V ≤ Vcc ≤ 3.6V

AC I^2C Specifications

Table 21. 3.3V AC Characteristics of the I^2C SDA and SCL Pins (CY8CNP102B)

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs
$T_{SUDATI2C}$	Data Setup Time	250	–	100[9]	–	ns
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns

Note
9. A Fast Mode I2C-bus device may be used in a Standard-Mode I2C-bus system, but the requirement tSUDAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line trmax + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard Mode I2C bus specification) before the SCL line is released.

5V Operation

Absolute Maximum Ratings

Table 22. 5V Absolute Maximum Ratings (CY8CNP102E)

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is ± 25°C. Extended duration storage temperatures above 65°C degrade reliability.
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	
Vcc	Supply Voltage on Vcc Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vcc + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vcc + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch-up Current	–	–	200	mA	

Operating Temperature

Table 23. 5V Operating Temperature (CY8CNP102E)

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	°C	
T_J	Junction Temperature	-40	–	+100	°C	

DC Electrical Characteristics

The following DC electrical specifications lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V over the Temperature range of -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

DC Chip Level Specifications

Table 24. 5V DC Chip-Level Specifications (CY8CNP102E)

Symbol	Description	Min	Typ	Max	Units	Notes
Vcc	Supply Voltage	4.75	–	5.25	V	
I_{DD}	Supply Current	–	39	45	mA	T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz, continuous nvSRAM access
I_{DDP}	Supply current when IMO = 6 MHz using SLIMO mode.	–	27	28	mA	T_A = 25 °C, CPU = 0.75 MHz, SYSCLK doubler disabled, VC1=0.375 MHz, VC2=23.44 kHz, VC3 = 0.09 kHz, continuous nvSRAM access
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active.	–	–	5	mA	nvSRAM in standby.
V_{REF}	Reference Voltage (Bandgap)	1.28	1.3	1.32	V	Trimmed for appropriate Vcc.
V_{cap}	Storage Capacitor between Vcap and Vss	61	68	82	uF	5V rated (minimum)

DC General Purpose IO Specifications

Table 25. 5V DC GPIO Specifications (CY8CNP102E)

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vcc - 1.0	–	–	V	IOH = 10 mA, Vcc = 4.75 to 5.25V. 8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5]). 80 mA maximum combined IOH budget.
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vcc = 4.75 to 5.25V 8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5]). 150 mA maximum combined IOL budget.
V_{IL}	Input Low Level	–	–	0.8	V	4.75 to 5.25.
V_{IH}	Input High Level	2.1	–		V	4.75 to 5.25.
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Pin dependent. Temp = 25°C.

DC Operational Amplifier Specifications

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 26. 5V DC Operational Amplifier Specifications (CY8CNP102E)

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value)					
	Power = Low, Opamp Bias = High	–	1.6	10	mV	
	Power = Medium, Opamp Bias = High	–	1.3	8	mV	
	Power = High, Opamp Bias = High	–	1.2	7.5	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Pin dependent. Temp = 25 °C.
V_{CMOA}	Common Mode Voltage Range. All Cases, except highest.	0.0	–	Vcc	V	
	Power = High, Opamp Bias = High	0.5	–	Vcc - 0.5	V	
$CMRR_{OA}$	Common Mode Rejection Ratio	60	–	–	dB	
G_{OLOA}	Open Loop Gain	80	–	–	dB	
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals)	Vcc - 0.01	–	–	V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals)	–	–	0.1	V	
I_{SOA}	Supply Current (including associated AGND buffer)					
	Power = Low, Opamp Bias = Low	–	150	200	µA	
	Power = Low, Opamp Bias = High	–	300	400	µA	
	Power = Medium, Opamp Bias = Low	–	600	800	µA	
	Power = Medium, Opamp Bias = High	–	1200	1600	µA	
	Power = High, Opamp Bias = Low	–	2400	3200	µA	
	Power = High, Opamp Bias = High	–	4600	6400	µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	67	80	–	dB	Vss ≤ VIN ≤ (Vcc - 2.25) or (Vcc - 1.25V) ≤ VIN ≤ Vcc.

DC Low Power Comparator Specifications

Table 27. 5V DC Low Power Comparator Specifications (CY8CNP102E)

Symbol	Description	Min	Typ	Max	Units
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	Vcc - 1.0	V
I_{SLPC}	LPC supply current	–	10	40	µA
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV

DC Analog Output Buffer Specifications

Table 28. 5V DC Analog Output Buffer Specifications (CY8CNP102E)

Symbol	Description	Min	Typ	Max	Units
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	Vcc - 1.0	V
R_{OUTOB}	Output Resistance				
	Power = Low	–	–	1	Ω
	Power = High	–	–	1	Ω
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32 ohms to Vcc/2)				
	Power = Low	0.5 x Vcc + 1.3	–	–	V
	Power = High	0.5 x Vcc + 1.3	–	–	V
V_{OLOWOB}	Low Output Voltage Swing (Load = 32 ohms to Vcc/2)				
	Power = Low	–	–	0.5 x Vcc - 1.3	V
	Power = High	–	–	0.5 x Vcc - 1.3	V
I_{SOB}	Supply Current Including Bias Cell (No Load)				
	Power = Low	–	1.1	2	mA
	Power = High	–	2.6	5	mA
$PSRR_{OB}$	Supply Voltage Rejection Ratio	40	64	–	dB

DC Analog Reference Specifications

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 29. 5V DC Analog Reference Specifications (CY8CNP102E)

Symbol	Description	Min	Typ	Max	Units
V_{BG5}	Bandgap Voltage Reference 5V	1.28	1.30	1.32	V
–	AGND = Vcc/2[1]	Vcc/2 - 0.02	Vcc/2	Vcc/2 + 0.02	V
–	AGND = 2 x BandGap[1]	2.52	2.60	2.72	V
–	AGND = P2[4] (P2[4] = Vcc/2)[1]	P2[4] - 0.013	P2[4]	P2[4] + 0.013	V
–	AGND = BandGap[1]	1.27	1.3	1.34	V
–	AGND = 1.6 x BandGap[1]	2.03	2.08	2.13	V
–	AGND Block to Block Variation (AGND = Vcc/2)[1]	-0.034	0.000	0.034	V
–	RefHi = Vcc/2 + BandGap	Vcc/2 + 1.21	Vcc/2 + 1.3	Vcc/2 + 1.382	V
–	RefHi = 3 x BandGap	3.75	3.9	4.05	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V)	P2[6] + 2.478	P2[6] + 2.6	P2[6] + 2.722	V
–	RefHi = P2[4] + BandGap (P2[4] = Vcc/2)	P2[4] + 1.218	P2[4] + 1.3	P2[4] + 1.382	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vcc/2, P2[6] = 1.3V)	P2[4] + P2[6] - 0.058	P2[4] + P2[6]	P2[4] + P2[6] + 0.058	V
–	RefHi = 2 x BandGap	2.50	2.60	2.70	V
–	RefHi = 3.2 x BandGap	4.02	4.16	4.29	V
–	RefLo = Vcc/2 – BandGap	Vcc/2 - 1.369	Vcc/2 - 1.30	Vcc/2 - 1.231	V
–	RefLo = BandGap	1.20	1.30	1.40	V
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V)	2.489 - P2[6]	2.6 - P2[6]	2.711 - P2[6]	V
–	RefLo = P2[4] – BandGap (P2[4] = Vcc/2)	P2[4] - 1.368	P2[4] - 1.30	P2[4] - 1.232	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vcc/2, P2[6] = 1.3V)	P2[4] - P2[6] - 0.042	P2[4] - P2[6]	P2[4] - P2[6] + 0.042	V

DC Analog PSoC NV Block Specifications

Table 30. 5V DC Analog PSoC NV Block Specifications (CY8CNP102E)

Symbol	Description	Min	Typ	Max	Units
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ
C_{SC}	Capacitor Unit Value (Switch Cap)	–	80	–	fF

DC POR, SMP, and LVD Specifications

Table 31. 5V DC POR, SMP, and LVD Specifications (CY8CNP102E)

Symbol	Description	Min	Typ	Max	Units
	Vdd Value for PPOR Trip (positive ramp)				
V_{PPOR0R}	PORLEV[1:0] = 00b		2.91		V
V_{PPOR1R}	PORLEV[1:0] = 01b		4.39		V
V_{PPOR2R}	PORLEV[1:0] = 10b		4.55		V
	Vdd Value for PPOR Trip (negative ramp)				
V_{PPOR0}	PORLEV[1:0] = 00b		2.82		V
V_{PPOR1}	PORLEV[1:0] = 01b		4.39		V
V_{PPOR2}	PORLEV[1:0] = 10b		4.55		V
	PPOR Hysteresis				
V_{PH0}	PORLEV[1:0] = 00b		92		mV
V_{PH1}	PORLEV[1:0] = 01b		0		mV
V_{PH2}	PORLEV[1:0] = 10b		0		mV
	Vdd Value for LVD Trip				
V_{LVD0}	VM[2:0] = 000b	2.86	2.92	2.98[2]	V
V_{LVD1}	VM[2:0] = 001b	2.96	3.02	3.08	V
V_{LVD2}	VM[2:0] = 010b	3.07	3.13	3.20	V
V_{LVD3}	VM[2:0] = 011b	3.92	4.00	4.08	V
V_{LVD4}	VM[2:0] = 100b	4.39	4.48	4.57	V
V_{LVD5}	VM[2:0] = 101b	4.55	4.64	4.74	V
V_{LVD6}	VM[2:0] = 110b	4.63	4.73	4.82	V
V_{LVD7}	VM[2:0] = 111b	4.72	4.81	4.91	V
	Vdd Value for SMP Trip				
V_{PUMP0}	VM[2:0] = 000b	2.96	3.02	3.08	V
V_{PUMP1}	VM[2:0] = 001b	3.03	3.10	3.16	V
V_{PUMP2}	VM[2:0] = 010b	3.18	3.25	3.32	V
V_{PUMP3}	VM[2:0] = 011b	4.11	4.19	4.28	V
V_{PUMP4}	VM[2:0] = 100b	4.55	4.64	4.74	V
V_{PUMP5}	VM[2:0] = 101b	4.63	4.73	4.82	V
V_{PUMP6}	VM[2:0] = 110b	4.72	4.82	4.91	V
V_{PUMP7}	VM[2:0] = 111b	4.90	5.00	5.10	V

DC Programming Specifications

Table 32. 5V DC Programming Specifications (CY8CNP102E)

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDPV}	Supply Current During Programming or Verify	–	10	30	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vcc - 1.0	–	Vcc	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[3]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

AC Electrical Characteristics

The following AC electrical specifications lists the guaranteed maximum and minimum specifications for the voltage and temperature range: 4.75V to 5.25V over the Temperature range of -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

AC Chip Level Specifications

Table 33. 5V AC Chip Level Specifications (CY8CNP102E)

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	23.4	24	24.6[4, 5, 6]	MHz	Trimmed for 5V operation using factory trim values. See Figure 5 on page 9. SLIMO Mode = 0.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.75	6	6.35[4 , 5, 6]	MHz	Trimmed for 5V operation using factory trim values. See Figure 5 on page 9. SLIMO Mode = 1.
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.6[4, 5]	MHz	
F_{48M}	Digital PSoC Block Frequency	0	48	49.2[4, 5, 7]	MHz	Refer to AC Digital Block Specifications on page 30.
F_{24M}	Digital PSoC Block Frequency	0	24	24.6[5, 7]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	A multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	–	–	600	ps	
$T_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	
$T_{PLLSLEWLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	–	250	500	ms	
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	300	600	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal.
Jitter32k	32 kHz Period Jitter	–	100		ns	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2[4,6]	MHz	Trimmed. Using factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO)	–	600		ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

In the following table, $t_{HRECALL}$ starts from the time Vcc rises above V_{SWITCH}. If an SRAM WRITE has not taken place since the last nonvolatile cycle, no STORE takes place. Industrial grade devices require 15 ms maximum.

Table 34. 5V nvSRAM AutoStore/Power Up RECALL (CY8CNP102E)

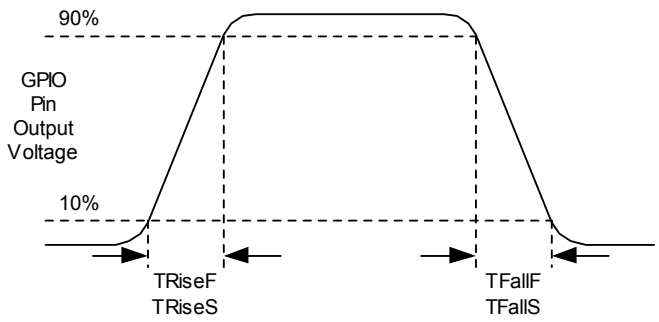
Parameter	Description	nvSRAM		Unit
		Min	Max	
$t_{HRECALL}$	Power Up RECALL Duration		20	ms
t_{STORE}	STORE Cycle Duration		12.5	ms
V_{SWITCH}	Low Voltage Trigger Level		4.4	V
$t_{VccRISE}$	VCC Rise Time	150		µs

AC General Purpose IO Specifications

Table 35. 5V AC GPIO Specifications (CY8CNP102E)

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12.3	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vcc = 4.75V to 5.25V 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vcc = 4.75V to 5.25V 10% - 90%

Figure 7. GPIO Timing Diagram



AC Operational Amplifier Specifications

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Table 36. 5V AC Operational Amplifier Specifications (CY8CNP102E)

Symbol	Description	Min	Typ	Max	Units
T_{ROA}	Rising Settling Time to 0.1% for a 1V Step (10 pF load, Unity Gain)				
	Power = Low, Opamp Bias = Low	–	–	3.9	µs
	Power = Medium, Opamp Bias = High	–	–	0.72	µs
	Power = High, Opamp Bias = High	–	–	0.62	µs
T_{SOA}	Falling Settling Time to 0.1% for a 1V Step (10 pF load, Unity Gain)				
	Power = Low, Opamp Bias = Low	–	–	5.9	µs
	Power = Medium, Opamp Bias = High	–	–	0.92	µs
	Power = High, Opamp Bias = High	–	–	0.72	µs
SR_{ROA}	Rising Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain)				
	Power = Low, Opamp Bias = Low	0.15	–	–	V/µs
	Power = Medium, Opamp Bias = High	1.7	–	–	V/µs
	Power = High, Opamp Bias = High	6.5	–	–	V/µs
SR_{FOA}	Falling Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain)				
	Power = Low, Opamp Bias = Low	0.01	–	–	V/µs
	Power = Medium, Opamp Bias = High	0.5	–	–	V/µs
	Power = High, Opamp Bias = High	4.0	–	–	V/µs
BW_{OA}	Gain Bandwidth Product				
	Power = Low, Opamp Bias = Low	0.75	–	–	MHz
	Power = Medium, Opamp Bias = High	3.1	–	–	MHz
	Power = High, Opamp Bias = High	5.4	–	–	MHz
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz

AC Digital Block Specifications

Table 37. 5V AC Digital Block Specifications (CY8CNP102E)

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Maximum Block Clocking Frequency			49.2	MHz	4.75V ≤ Vcc ≤ 5.25V.
Timer	Capture Pulse Width	50[8]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.2	MHz	4.75V ≤ Vcc ≤ 5.25V.
	Maximum Frequency, With Capture	–	–	24.6	MHz	4.75V ≤ Vcc ≤ 5.25V.
Counter	Enable Pulse Width	50[8]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.2	MHz	4.75V ≤ Vcc ≤ 5.25V.
	Maximum Frequency, Enable Input	–	–	24.6	MHz	4.75V ≤ Vcc ≤ 5.25V.
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[8]	–	–	ns	
	Disable Mode	50[8]	–	–	ns	
	Maximum Frequency	–	–	49.2	MHz	4.75V ≤ Vcc ≤ 5.25V
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.2	MHz	4.75V ≤ Vcc ≤ 5.25V

Table 37. 5V AC Digital Block Specifications (CY8CNP102E) (continued)

Function	Description	Min	Typ	Max	Units	Notes
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	4.75V ≤ Vcc ≤ 5.25V.
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	ns	
	Width of SS_ Negated Between Transmissions	50[8]	–	–	ns	
Transmitter	Maximum Input Clock Frequency Vcc ≥ 4.75V, 2 Stop Bits	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
		–	–	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency Vcc ≥ 4.75V, 2 Stop Bits	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
		–	–	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.

AC Analog Output Buffer Specifications

Table 38. 5V AC Analog Output Buffer Specifications (CY8CNP102E)

Symbol	Description	Min	Typ	Max	Units
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100 pF Load				
	Power = Low	–	–	4	µs
	Power = High	–	–	4	µs
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100 pF Load				
	Power = Low	–	–	3.4	µs
	Power = High	–	–	3.4	µs
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load				
	Power = Low	0.5	–	–	V/µs
	Power = High	0.5	–	–	V/µs
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load				
	Power = Low	0.55	–	–	V/µs
	Power = High	0.55	–	–	V/µs
BW_{OB}	Small Signal Bandwidth, 20mV$_{pp}$, 3dB BW, 100 pF Load				
	Power = Low	0.8	–	–	MHz
	Power = High	0.8	–	–	MHz
BW_{OB}	Large Signal Bandwidth, 1V$_{pp}$, 3dB BW, 100 pF Load				
	Power = Low	300	–	–	kHz
	Power = High	300	–	–	kHz

AC Programming Specifications

Table 39. 5V AC Programming Specifications (CY8CNP102E)

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
T_{WRITE}	Flash Block Write Time	–	10	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	4.75V ≤ Vcc ≤ 5.25V

AC I^2C Specifications

Table 40. 5V AC Characteristics of the I^2C SDA and SCL Pins (CY8CNP102E)

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs
$T_{SUDATI2C}$	Data Setup Time	250	–	100[9]	–	ns
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns

Switching Waveforms

Figure 8. AutoStore/Power Up RECALL

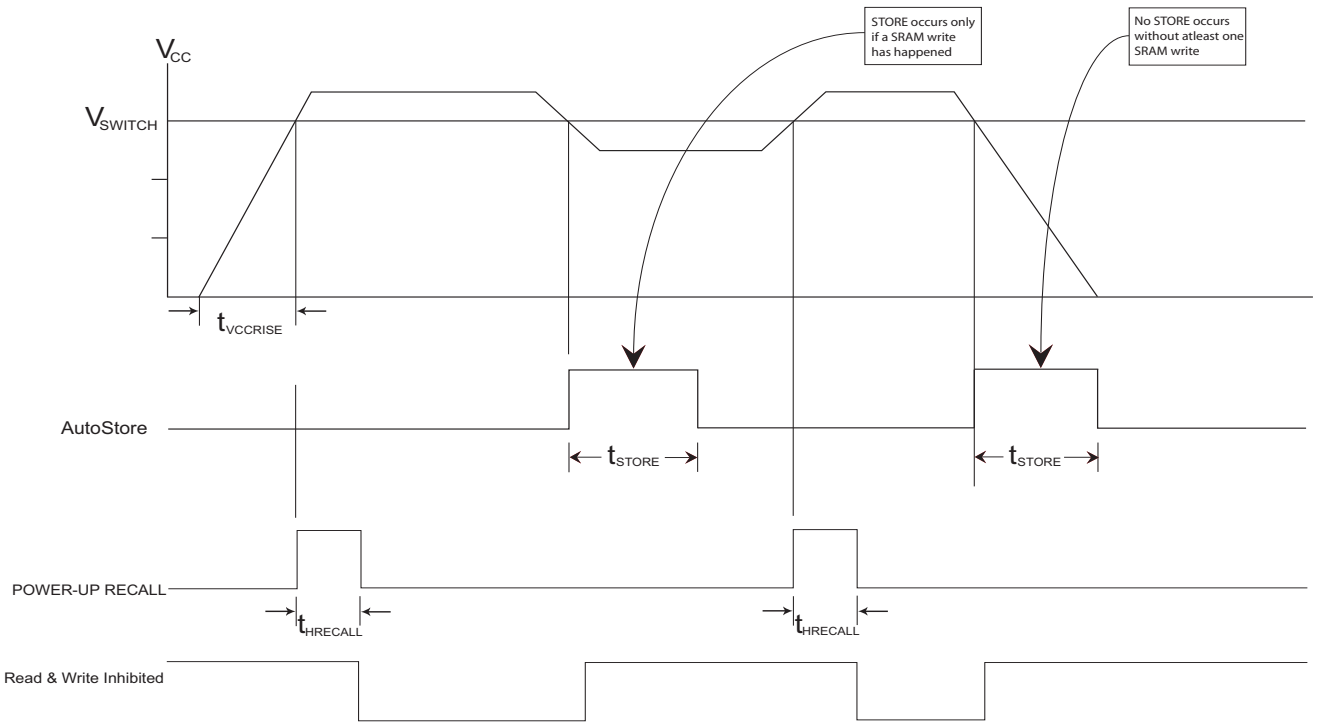


Figure 9. PLL Lock Timing Diagram

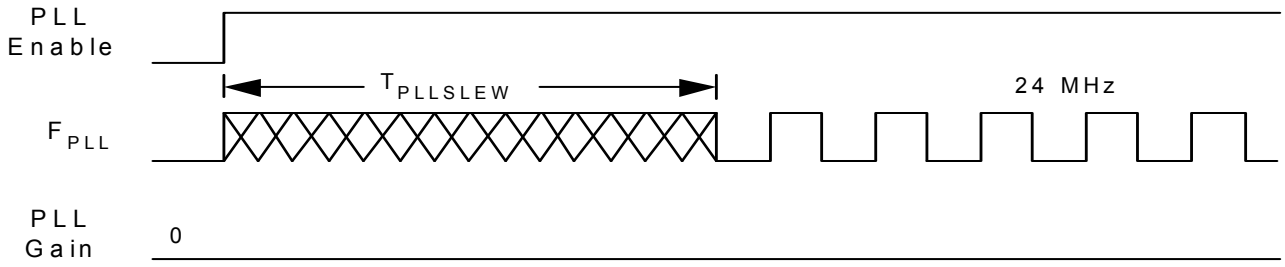
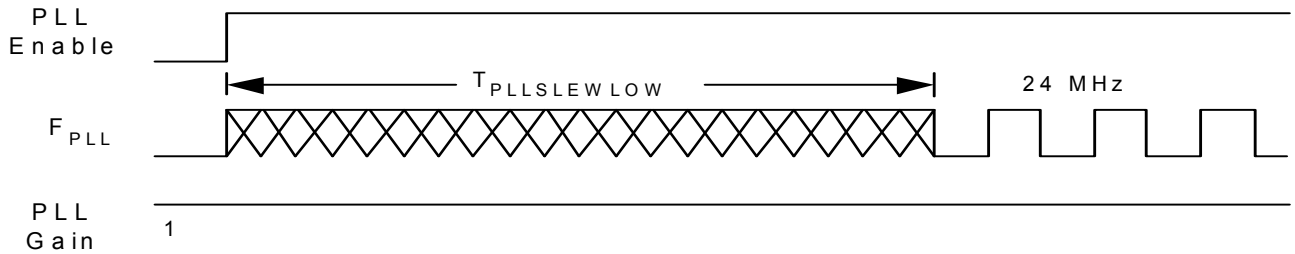


Figure 10. PLL Lock for Low Gain Setting Timing Diagram



Switching Waveforms (continued)

Figure 11. External Crystal Oscillator Startup Timing Diagram

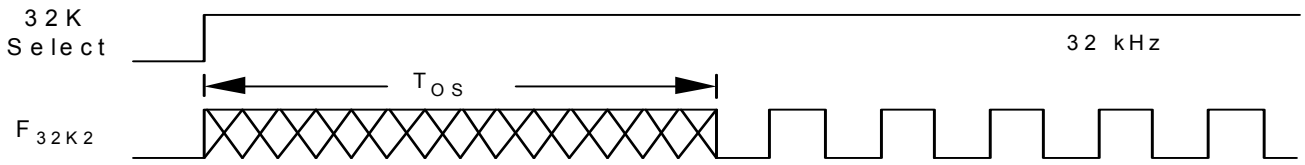


Figure 12. 24 MHz Period Jitter (IMO) Timing Diagram

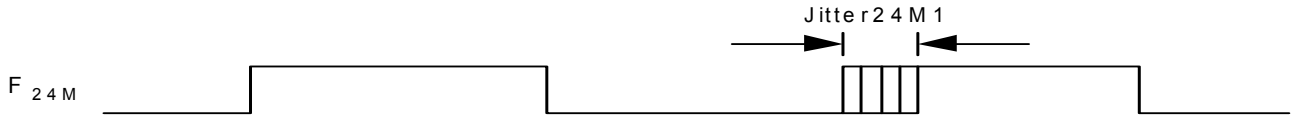
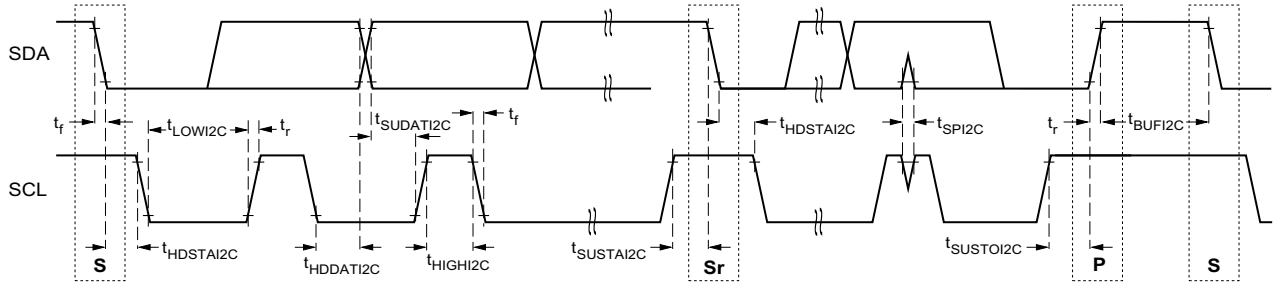
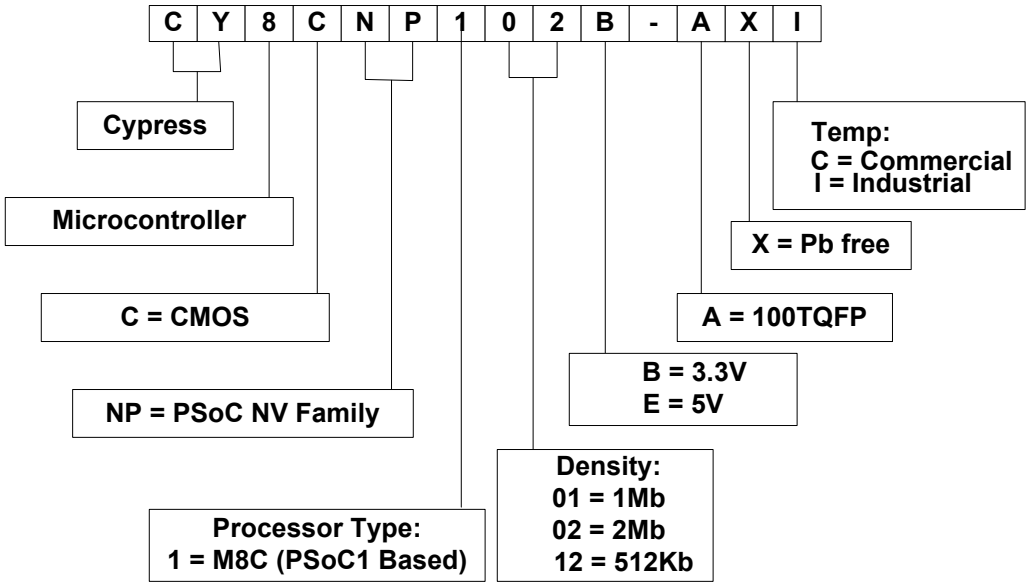


Figure 13. 32 kHz Period Jitter (ECO) Timing Diagram

Figure 14. Definition of Timing for Fast/Standard Mode on the I²C Bus



Part Numbering Nomenclature



Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
CY8CNP102B-AXI	51 - 85048	100-pin TQFP	Industrial
CY8CNP102E-AXI	51 - 85048	100-pin TQFP	

All the above mentioned parts are of “Pb-free” type and contain preliminary information. Please contact your local Cypress sales representative for availability of these parts.

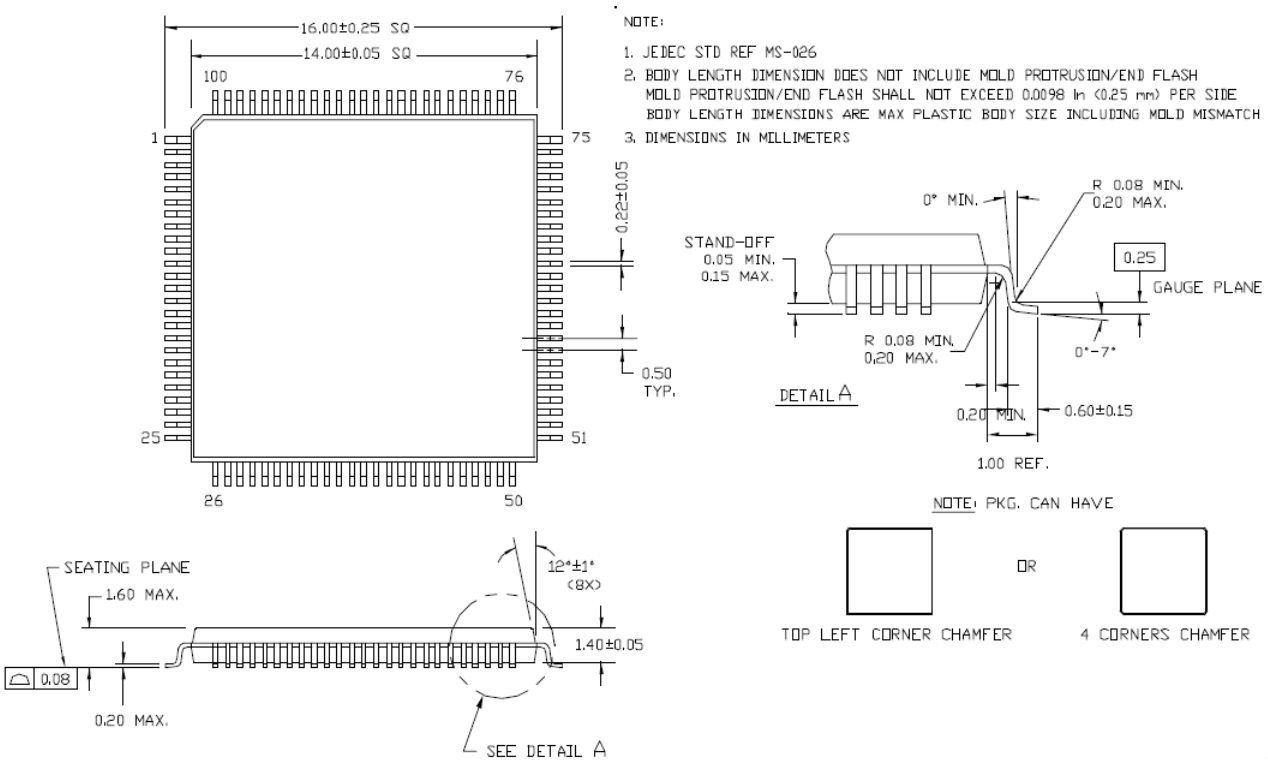
Packaging Information

This section describes the packaging specifications for the PSoC NV device and the thermal impedances for TQFP package.

Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tool dimensions, refer to the document "PSoC Emulator Pod Dimensions" at http://www.cypress.com/design/MR10161.

Package Diagrams

Figure 15. 100-Pin TQFP - 14 x 14 x 1.4 mm



51-85048 *C

Thermal Impedance

Table 41. Thermal Impedance

Package[10]	Typical θ_{JA} *	Typical θ_{JC} *
100 TQFP	26.14 °C/W	5.81 °C/W

Note
10. * $T_J = T_A + POWER \times \theta_{JA}$

Document History Page

Document Title: CY8CNP102B/CY8CNP102E Nonvolatile Programmable System-on-Chip (PSoC® NV) Document Number: 001-43991				
REV.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	1941108	vsutmp8/AESA	See ECN	New Data Sheet
*A	2378513	PYRS	See ECN	Move to external web
*B	2512803	GVCH/PYRS	06/05/2008	Features: Added total no. of GPIO information in Programmable Pin configurations Changed Pin no.14 from P3_7 to NC in the Pin diagram Table 1: Updated Pin definitions Table 5: Changed Typ and max value of I_{DD} from 25 mA and 29mA to 36 mA and 40 mA resp. Table 5: Changed Typ and max value of I_{DDP} from 15 mA and 16 mA to 27 mA and 28 mA respectively. Table 5: Changed Min and Max value of V_{CAP} from 56 uF and 100 uF to 61 uF and 82 uF resp. Table 6: Changed V_{IH} min value from 2.1 mV to 1.6 mV Added Table 12: DC POR,SMP, and LVD specifications Table 13: Changed I_{DDP} naming convention to I_{DDPV} Table 14: Updated note references Table 17: Updated Timer, Counter, deadband and CRCPS (PRS mode) values Table 23: Changed Typ and max value of I_{DD} from 28 mA and 34 mA to 39 mA and 45 mA resp. Table 23: Changed Typ and max value of I_{DDP} from 15 mA and 16 mA to 27 mA and 28 mA resp. Table 23: Changed Min and Max value of V_{CAP} from 56 uF and 100 uF to 61 uF and 82 uF resp. Added Table 30: DC POR,SMP, and LVD specifications Table 31: Changed I_{DDP} naming convention to I_{DDPV} table 32: Updated note references Updated Figure 14: Definition for Timing for Fast/Standard Mode on the I2C bus Updated part Numbering Nomenclature Updated Thermal Impedance table Updated data sheet template
*C	2571208	GVCH/PYRS	09/23/08	Changed Title from nvPSoC to PSoC NV Updated “Features”
*D	2594976	GVCH/PYRS	10/22/08	Added M8C processor speeds for 3.3V and 5V operation in “Features” Updated Logic block diagram Changed total GPIOs from 27 to 33 Changed pin number 53 name from P1_4 to P1_6 Changed pin definition of pin 79 and 99 Table 5: Changed I_{SB} from 3 mA to 5 mA Updated Table 12 Table 24: Changed I_{SB} from 3 mA to 5 mA

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