

# DATA SHEET



## **TDA8261TW** Satellite Zero-IF QPSK/8PSK downconverter with PLL synthesizer

Product specification  
Supersedes data of 2004 Oct 25

2004 Dec 02

## Satellite Zero-IF QPSK/8PSK downconverter with PLL synthesizer

### TDA8261TW

#### FEATURES

- Direct conversion Quadrature Phase Shift Keying (QPSK) and 8PSK demodulation (Zero-IF)
- 950 to 2175 MHz frequency range
- High-level asymmetrical RF input
- 0 to 50 dB variable gain on RF input
- Loop-controlled 0° to 90° phase shifter
- High AGC linearity (<1 dB per bit with an 8-bit DAC), AGC between 0 and 3 V
- External baseband filters for In-phase (I) and Quadrature (Q) signal paths
- I<sup>2</sup>C-bus controlled PLL frequency synthesizer
- Low phase noise
- Operation from a 4 MHz crystal (allowing the use of an SMD crystal)
- Five frequency steps from 125 kHz to 2 MHz
- Crystal frequency output to drive demodulator IC
- Compatible with 5, 3.3 and 2.5 V I<sup>2</sup>C-bus
- Fully compatible and easy to interface with digital satellite demodulators of the Philips Semiconductors family
- 5 V DC supply voltage
- 32-pin high heat-dissipation package.

#### APPLICATIONS

- Direct Broadcasting Satellite (DBS) QPSK demodulation
- Digital Video Broadcasting (DVB) QPSK demodulation
- BS digital 8PSK demodulation.

#### GENERAL DESCRIPTION

The direct conversion QPSK demodulator is the front-end receiver dedicated to digital TV broadcasting, satisfying both DVB and DBS TV standards. The wide range oscillator (from 950 to 2175 MHz) covers the American, European and Asian satellite bands, as well as the Satellite Master Antennae (SMA) TV US standard.

The Zero-IF concept discards traditional IF filtering and intermediate conversion techniques. It also simplifies the signal path.



Optimum signal level is guaranteed by gain controlled amplifiers in the RF path. The 0 to 50 dB variable gain is controlled by the signal returned from the Satellite Demodulator and Decoder (SDD) and applied to pin AGCIN.

The PLL synthesizer is built on a dual-loop concept. The first loop controls a fully integrated L-band oscillator, using the LC VCO as a reference which runs at a quarter of the synthesized frequency.

The second loop controls the tuning voltage of the VCO and improves the phase noise of the carrier within the loop bandwidth. The step size is equal to the comparison frequency. The input of the main divider of the PLL synthesizer is connected internally to the VCO output.

The comparison frequency of the second loop is obtained from an oscillator driven by an external 4 MHz crystal. The 4 MHz output available at pin XTOUT may be used to drive the crystal inputs of the SDD, saving an additional crystal in the application.

Both the divided and the comparison frequencies of the second loop are compared in a fast phase detector which drives the charge pump. The TDA8261TW includes a loop amplifier with an internal high-voltage transistor to drive an external 33 V tuning voltage.

Control data is entered via the I<sup>2</sup>C-bus. The I<sup>2</sup>C-bus voltage can be 5, 3.3 or 2.5 V, allowing compatibility with most of the existing microcontrollers.

A 5-byte frame is required to address the device and to program the main divider ratio, the reference divider ratio, the charge pump current and the operating mode.

A flag is set when the loop is 'in-lock'. This flag can be read during read operations, as well as the Power-On Reset (POR) flag.

The device has four selectable I<sup>2</sup>C-bus addresses. The selection is done by applying a specific voltage to pin AS. This feature gives the possibility to use up to four TDA8261TW ICs in the same system.

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## Performance summary

TDA8261TW performance:

- Noise figure at maximum gain = +18 dB
- High linearity; IP2 = +19 dBm and IP3 = +14 dBm
- Low phase noise on baseband outputs: -78 dBc/Hz ( $f_{\text{offset}} = 1$  and 10 kHz;  $f_{\text{COMP}} = 1$  MHz)
- 0 to 50 dB variable gain with AGC control
- AGC linearity <1 dB/bit with an 8-bit DAC
- Maximum I-to-Q amplitude mismatch = 1 dB
- Maximum I-to-Q phase mismatch = 3°
- Signal rates from 1 to 45 Msymbol/s (depending on the external filter).

System performance, for example, in a tuner application with the TDA8261TW placed after a low-cost discrete LNA:

- Noise figure at maximum gain = 8 dB
- High linearity; IP2 = 15 dBm and IP3 = 5 dBm
- 0 to 50 dB variable gain with AGC control.

## Specification limitation

Please note that this data sheet applies to versions C2 and above only, it does not apply to version C1. For further information, please contact your Philips Semiconductors representative.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CC}$	supply voltage		4.75	5.0	5.25	V
$I_{CC}$	supply current		–	130	–	mA
$V_{o(p-p)}$	output voltage (peak-to-peak value)		–	750	–	mV
$\Delta\Phi$	quadrature error		–	–	3	deg
$f_{osc}$	oscillator frequency		950	–	2175	MHz
$\varphi_n$	phase noise on baseband outputs	$f_{\text{offset}} = 1$ and 10 kHz; $f_{\text{COMP}} = 1$ MHz with appropriate loop filter and charge pump	–	–	-78	dBc/Hz
$\Delta G_v$	dynamic range of voltage gain	from pins RFA or RFB to pins IBBOUT or QBBOUT	48	50	–	dB
$V_{XTOUT(p-p)}$	crystal oscillator output voltage on pin XTOUT (peak-to-peak value)	T2 = 1; T1 = 0; T0 = 0; driving a load of $C_L = 10$ pF; $R_L = 1$ M $\Omega$	500	650	–	mV
$T_{amb}$	ambient temperature		-20	–	+85	°C

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8261TW	HTSSOP32	plastic, thermal enhanced thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm; exposed die pad	SOT549-3

# Satellite Zero-IF QPSK/8PSK downconverter with PLL synthesizer

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## BLOCK DIAGRAM

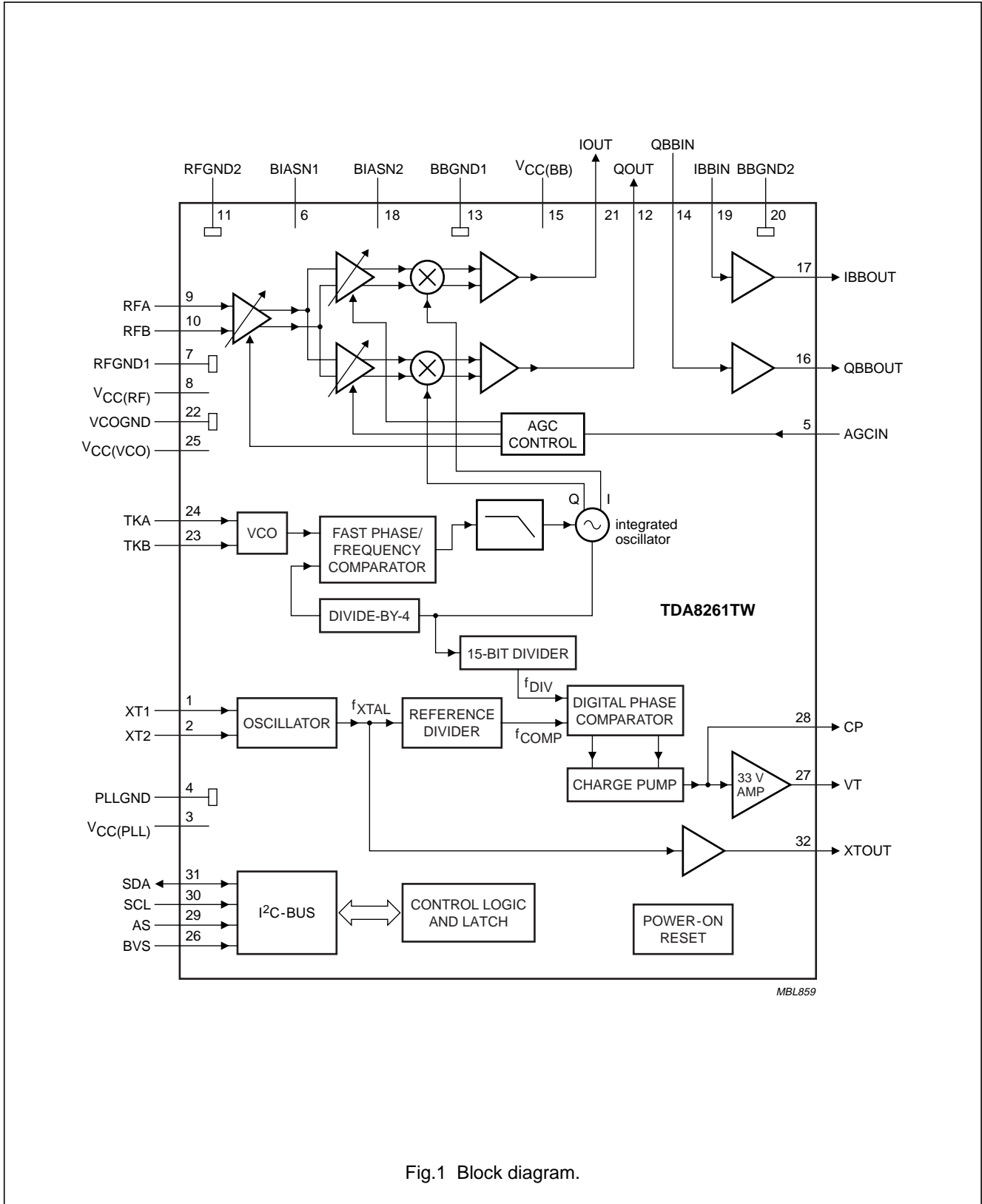


Fig.1 Block diagram.

# Satellite Zero-IF QPSK/8PSK downconverter with PLL synthesizer

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**PINNING**

SYMBOL	PIN	DESCRIPTION
XT1	1	4 MHz crystal oscillator input 1
XT2	2	4 MHz crystal oscillator input 2
V <sub>CC(PLL)</sub>	3	supply voltage for PLL circuit (5 V)
PLLGND	4	ground for PLL circuit
AGCIN	5	AGC input from satellite demodulator and decoder
BIASN1	6	RF isolation input 1 (5 V)
RFGND1	7	ground 1 for RF circuit
V <sub>CC(RF)</sub>	8	supply voltage for RF stage (5 V)
RFA	9	RF signal input A
RFB	10	RF signal input B
RFGND2	11	ground 2 for RF circuit
QOUT	12	quadrature output for external filtering
BBGND1	13	ground 1 for baseband stage
QBBIN	14	quadrature baseband input after external filtering
V <sub>CC(BB)</sub>	15	supply voltage for baseband stage (5 V)
QBBOUT	16	quadrature baseband output to satellite demodulator and decoder
IBBOUT	17	in-phase baseband output to satellite demodulator and decoder
BIASN2	18	RF isolation input 2 (5 V)
IBBIN	19	in-phase baseband input after external filtering
BBGND2	20	ground 2 for baseband stage
IOUT	21	in-phase output for external filtering
VCOGND	22	ground for VCO circuit
TKB	23	VCO tank circuit input B
TKA	24	VCO tank circuit input A
V <sub>CC(VCO)</sub>	25	supply voltage for VCO circuit (5 V)
BVS	26	bus voltage select input
VT	27	tuning voltage output for VCO
CP	28	charge pump output
AS	29	address selection input
SCL	30	I <sup>2</sup> C-bus clock input
SDA	31	I <sup>2</sup> C-bus data input and output
XTOUT	32	4 MHz crystal oscillator output to satellite demodulator and decoder

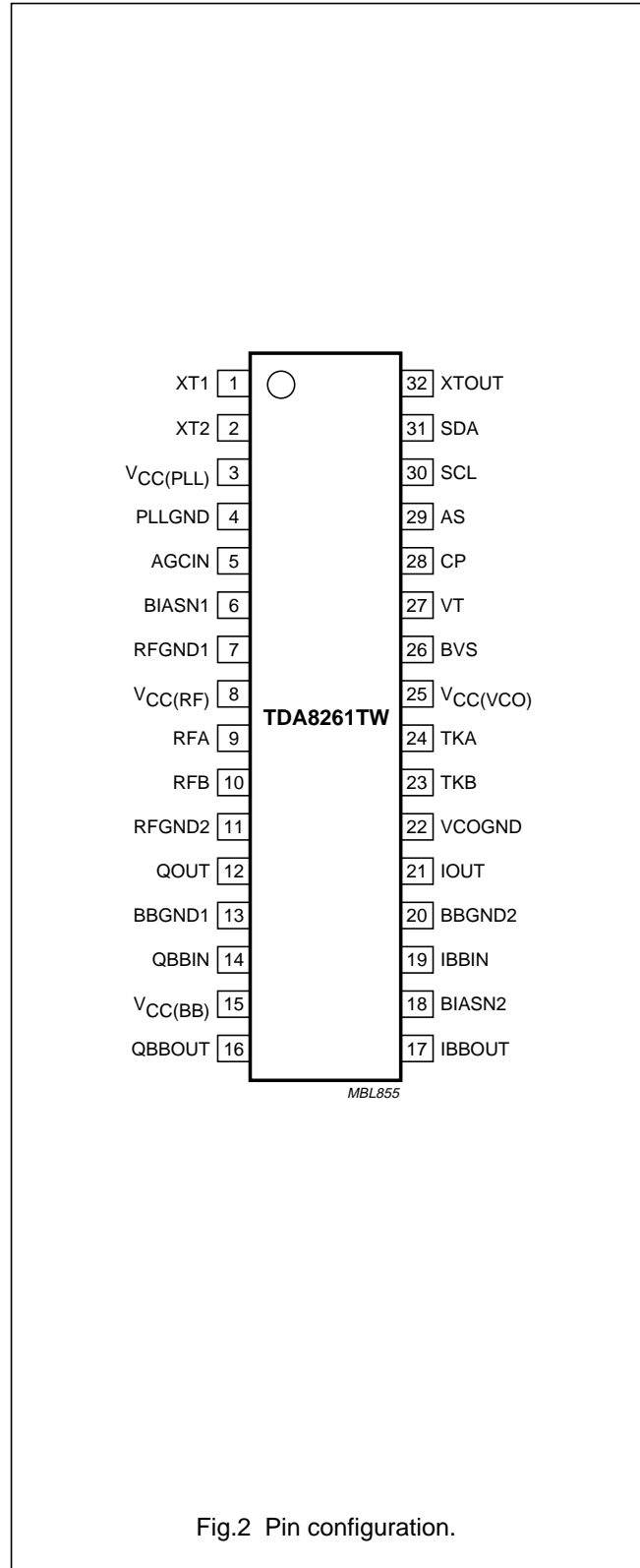


Fig.2 Pin configuration.

# Satellite Zero-IF QPSK/8PSK downconverter with PLL synthesizer

## TDA8261TW

### FUNCTIONAL DESCRIPTION

The TDA8261TW contains the core of the RF analog part of a digital satellite receiver. The signal coming from the Low Noise Block (LNB) is coupled through a Low Noise Amplifier (LNA) to the RF inputs. The circuitry in the TDA8261TW performs the Zero-IF quadrature frequency conversion and the two in-phase (IBBOUT) and quadrature (QBBOUT) output signals can be used directly to feed a SDD circuit.

The relative phase of I and Q signals is measured on the baseband outputs, when a sine wave unmodulated carrier at  $f_{lo} + 1$  MHz is present at the RF input of the TDA8261TW (see Fig.3).

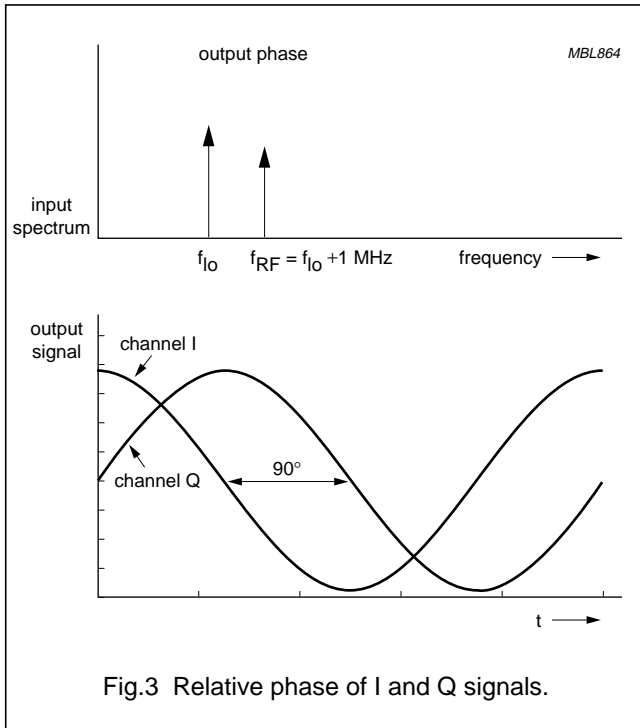


Fig.3 Relative phase of I and Q signals.

The TDA8261TW has a gain controlled amplifier which is controlled by the SDD.

An external VCO tank circuit is connected between pins TKA and TKB. The main elements of the external tank circuit are an SMD coil and a varactor diode. The tuning voltage of 0 to 30 V covers the whole frequency range from 237.5 to 543.75 MHz. The internal loop controls a fully integrated VCO to cover the range 950 to 2175 MHz. The VCO provides both in-phase and quadrature signals to drive the two mixers.

The TDA8261TW integrates all elements necessary to control the varactor tuned oscillator except a 4 MHz crystal and a loop filter. It includes a fast phase detector with high comparison frequency to get the lowest phase noise level in the local oscillator.

The  $f_{DIV}$  output of the 15-bit programmable divider passes through the fast phase comparator where it is compared in both phase and frequency with the comparison frequency ( $f_{COMP}$ ).  $f_{COMP}$  is derived from the signal present at the pins XT1 and XT2 ( $f_{XTAL}$ ) divided-down by the reference divider. The buffered XTOUT signal can drive the crystal frequency input of the SDD, saving a crystal in the application.

The output of the phase comparator drives the charge pump and loop amplifier section. The loop amplifier includes a high voltage transistor to handle the 30 V tuning voltage at pin VT, this drives a variable capacitance diode in the external circuit of the voltage controlled oscillator. Pin CP is the output of the charge pump. The loop filter is connected between pins CP and VT and the post-filter section is connected between pin VT and the variable capacitance diode.

For test and alignment purposes, it is possible to release the tuning voltage output and apply an external voltage on pin VT and to select the charge pump function to sink current, source current or to be switched off.

# Satellite Zero-IF QPSK/8PSK downconverter with PLL synthesizer

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## PROGRAMMING

Programming of the TDA8261TW is performed via the I<sup>2</sup>C-bus. The read or write selection is made with bit  $R/\overline{W}$  (address LSB). The TDA8261TW fulfils the I<sup>2</sup>C-bus fast mode, according to the Philips I<sup>2</sup>C-bus specification.

### I<sup>2</sup>C-bus voltage

The I<sup>2</sup>C-bus lines SCL and SDA can be connected to an I<sup>2</sup>C-bus system tied to either 2.5, 3.3 or 5.0 V, that will allow direct connection to most of the existing microcontrollers. The choice of the threshold voltage for the I<sup>2</sup>C-bus lines is made with pin BVS that needs to be connected to the supply voltage, to ground or needs an open-circuit; see Table 1.

**Table 1** I<sup>2</sup>C-bus voltage selection

PIN BVS	I <sup>2</sup> C-BUS VOLTAGE
GND	2.5 V
Open-circuit	3.3 V
V <sub>CC</sub>	5 V

**Table 2** I<sup>2</sup>C-bus write data format

BYTE	MSB <sup>(1)</sup>		BITS <sup>(2)</sup>					LSB	ACK <sup>(3)</sup>
Programmable address	1	1	0	0	0	MA1	MA0	0	A
Programmable Divider 1 (PD1)	0	N14	N13	N12	N11	N10	N9	N8	A
Programmable Divider 2 (PD2)	N7	N6	N5	N4	N3	N2	N1	N0	A
Control Data 1 (CD1)	1	T2	T1	T0	R2	R1	R0	X	A
Control Data 2 (CD2)	C1	C0	X	X	X	X	X	X	A

### Notes

- MSB is transmitted first.
- X = undefined.
- Acknowledge bit (A).

### I<sup>2</sup>C-bus write mode

I<sup>2</sup>C-bus write mode: bit  $R/\overline{W} = 0$ ; see Table 2.

After the transmission of the address (first byte), four data bytes can be sent to fully program the TDA8261TW. The bus transceiver has an auto-increment facility that permits to program the TDA8261TW with a single transmission: one address byte followed by four data bytes (PD1, PD2, CD1 and CD2).

The TDA8261TW can be partly programmed provided that the first data byte following the address is PD1 or CD1. The first bit of the first data byte transmitted indicates whether PD1 (first bit = 0) or CD1 (first bit = 1) will follow. Until an I<sup>2</sup>C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. Each byte is loaded after the corresponding 8th clock pulse. Programmable divider data (contents of PD1 and PD2) becomes valid only after the 8th clock pulse of PD2, or after a STOP condition if only PD1 needs to be programmed.

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## PROGRAMMABLE ADDRESS

The programmable address bits MA1 and MA0 offer the possibility of having up to four TDA8260TW devices in the same system. The relationship between the voltage applied on pin AS and the value of bits MA1 and MA0 is given in Table 3.

**Table 3** I<sup>2</sup>C-bus address selection

V <sub>AS</sub>	MA1	MA0
0 to 0.1V <sub>CC</sub>	0	0
open-circuit	0	1
0.4V <sub>CC</sub> to 0.6V <sub>CC</sub>	1	0
0.9V <sub>CC</sub> to V <sub>CC</sub>	1	1

## PROGRAMMABLE MAIN DIVIDER RATIO

Program bytes PD1 and PD2 contain the fifteen bits N14 to N0 that set the main divider ratio. The ratio  $N = N14 \times 2^{14} + N13 \times 2^{13} + \dots + N1 \times 2 + N0$ .

## OPERATING AND TEST MODES

The mode of operation is set using bits T2, T1 and T0 in control byte CD1; see Table 4.

**Table 4** Mode selection

T2	T1	T0	TEST MODE	XTOUT
0	0	0	normal operation	off
0	0	1	POR state = CP sink <sup>(1)</sup>	f <sub>XTAL</sub>
0	1	0	$\frac{1}{2} \times f_{DIV}$	$\frac{1}{2} \times f_{DIV}$
0	1	1	CP sink	f <sub>XTAL</sub>
1	0	0	normal operation	f <sub>XTAL</sub>
1	0	1	$2 \times f_{ref}$	$2 \times f_{ref}$
1	1	0	CP off	f <sub>XTAL</sub>
1	1	1	CP source	f <sub>XTAL</sub>

### Note

- Status at power-on: the tuning voltage output is released and pin VT is in the high-impedance mode.

## REFERENCE DIVIDER

Five reference divider ratios allow to adjust the comparison frequency to different values, depending on the compromise which has to be found between step size and phase noise. The reference divider ratios and the corresponding comparison frequencies are programmed using bits R2, R1 and R0, as described in Table 5.

**Table 5** Reference divider ratio

R2	R1	R0	DIVIDER RATIO	COMPARISON FREQUENCY
0	0	0	2	2 MHz
0	0	1	4	1 MHz
0	1	0	8	500 kHz
0	1	1	not allowed	not allowed
1	0	0	not allowed	not allowed
1	0	1	16	250 kHz
1	1	0	not allowed	not allowed
1	1	1	32	125 kHz

## CHARGE PUMP CURRENT

Four values of charge pump current can be chosen using bits C1 and C0, according to Table 6.

**Table 6** Typical charge pump current

C1	C0	I <sub>CP</sub> (ABSOLUTE VALUE)
0	0	420 μA
0	1	900 μA
1	0	1320 μA
1	1	2320 μA



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### I<sup>2</sup>C-bus read mode

If bit R/W = 1 the data can be read from the TDA8261TW (see Table 7). After recognition of its slave address, the TDA8261TW generates an acknowledge pulse and transfers the status byte onto the SDA line (MSB first). Data is valid on the SDA line when the SCL clock signal is HIGH.

A second data byte can be read from the TDA8261TW if the microcontroller generates an acknowledge on the SDA line. End of transmission will occur if no acknowledge is received from the microcontroller. The TDA8261TW will

then release the data line to allow the microcontroller to generate a STOP condition.

The POR flag is set to logic 1 at power-on and when  $V_{CC} < 2.7$  V. It is reset to logic 0 when an end-of-data condition is detected by the TDA8261TW (end of a read sequence).

The in-lock flag FL indicates that the loop is phase-locked when set to logic 1.

When a read sequence is started, all eight bits of the status byte must be read.

**Table 7** I<sup>2</sup>C-bus read data format

BYTE	MSB						BITS <sup>(1)</sup>		LSB	ACK <sup>(2)</sup>
Address	1	1	0	0	0	MA1	MA0	1	A	
Status byte	POR	FL <sup>(3)</sup>	X	X	X	X	X	X	–	

### Notes

1. X can be 1 or 0 and needs to be masked in the microcontrollers' software; MSB is transmitted first.
2. Acknowledge bit (A).
3. FL is valid only in normal mode.

### POWER-ON RESET

At power-on (bit POR = 1) or when the supply voltage drops below 2.7 V, internal registers are set according to Table 8.

**Table 8** Status at POR

BYTE	MSB			BITS <sup>(1)</sup>				LSB
Programmable divider 1 (PD1)	0	N14 = X	N13 = X	N12 = X	N11 = X	N10 = X	N9 = X	N8 = X
Programmable divider 2 (PD2)	N7 = X	N6 = X	N5 = X	N4 = X	N3 = X	N12 = X	N1 = X	N0 = X
Control data 1 (CD1)	1	T2 = 0	T1 = 0	T0 = 1	R2 = X	R1 = X	R0 = X	X
Control data 1 (CD2)	C1 = X	C0 = X	X	X	X	X	X	X

### Note

1. X = not set.

# Satellite Zero-IF QPSK/8PSK downconverter with PLL synthesizer

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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		-0.3	+6.0	V
$V_i$	input voltage	pin SDA	-0.3	+6.0	V
		pin SCL	-0.3	+6.0	V
		all other pins	-0.3	$V_{CC} + 0.3$	V
$V_o$	output voltage	pin SDA	-0.3	+6.0	V
		pin VT	-0.3	+35	V
		all other pins	-0.3	$V_{CC} + 0.3$	V
$T_{amb}$	ambient temperature		-20	+85	°C
$T_{stg}$	storage temperature		-40	+150	°C
$T_j$	junction temperature		-	150	°C
$t_{sc}$	short-circuit time	each pin short-circuited to $V_{CC}$ or GND	-	10	s

### Note

1. Maximum ratings cannot be exceeded, not even momentarily without causing irreversible damages to the TDA8261TW. Maximum ratings cannot be accumulated.

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	41.4	K/W

## HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe, it is desirable to take normal precautions appropriate to handle integrated circuits. Every pin withstands 2000 V in the ESD test in accordance with "JEDEC Specification EIA/JESD22-A114A", HBM model (category 1c), except for pin 1 (XT1) which withstands 500 V, pin 2 (XT2) which withstands 1000 V and pin 8 ( $V_{CC(RF)}$ ) which withstands 1500 V. Identically, every pin withstands 200 V in the ESD test in accordance with "JEDEC Specification EIA/JESD22-A115A", MM model (category A).

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## CHARACTERISTICS

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $V_{CC} = 5\text{ V}$ ; unless otherwise specified;  $R_L = 1\text{ k}\Omega$  on base band output IBBOUT and QBBOUT;  
 $V_{o(p-p)} = 750\text{ mV}$  on IBBOUT and QBBOUT.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
$V_{CC}$	supply voltage		4.75	5.00	5.25	V
$I_{CC}$	supply current		–	130	–	mA
$V_{POR}$	voltage limit where POR active		–	2.7	–	V
<b>Performances from pins RFA or RFB to pins IBBOUT or QBBOUT</b>						
$LO_{leak}$	LO leakage through pins RFA and RFB		–	–75	–	dBm
$\Delta G_V$	dynamic voltage gain range	$V_{AGC} = 0\text{ to }3\text{ V}$	48	50	–	dB
$G_{V(max)}$	maximum voltage gain	$V_{AGC} = 3\text{ V}$ ; see Figs 4 and 5	55	57	–	dB
$V_{o(p-p)}$	output voltage (peak-to-peak)	recommended value	–	750	–	mV
IP2i	2nd-order interception point	at RF input; $V_{AGC} = 0\text{ V}$	–	19	–	dBm
IP3i	3rd-order interception point	at RF input; $V_{AGC} = 0\text{ V}$	–	14	–	dBm
F	noise figure	at maximum gain; $V_{AGC} = 3\text{ V}$ ; see Fig.6	–	18	–	dB
$Z_o$	output impedance on pin IOOUT and QOOUT		–	35	–	$\Omega$
$Z_i$	input impedance on pin IBBIN and QBBIN		–	1.0	–	k $\Omega$
$G_{V(I-Q)}$	voltage gain mismatch between I and Q	in 22.5 MHz band with bypass capacity 100 nF between IOOUT and IBBIN, QOOUT and QBBIN	–	–	1	dB
$ \Delta\Phi $	absolute quadrature error	$V_{AGC} = 1.5\text{ V}$ ; $V_o = 750\text{ mV}$ (peak to peak value); measured in baseband	–	0	3	deg
<b>Pulling sensitivity</b>						
3/4LO	sensitivity to pulling on the third harmonic of the external VCO	see Table 9 and Fig.8	–	–40	–35	dBc
5/4LO	sensitivity to pulling on the fifth harmonic of the external VCO	see Table 9 and Fig.8	–	–40	–35	dBc
<b>VCO and synthesizer</b>						
$f_{osc}$	oscillator frequency		950	–	2175	MHz
$\Phi_{n(osc)}$	oscillator phase noise in the satellite band	$f_{offset} = 100\text{ kHz}$ ; out of PLL loop bandwidth	–	–100	–94	dBc/Hz
$\Phi_n$	phase noise on baseband outputs	$f_{offset} = 1\text{ and }10\text{ kHz}$ ; $f_{COMP} = 1\text{ MHz}$ ; see Fig.7	–	–	–78	dBc/Hz
MDR	main divider ratio		64	–	32767	

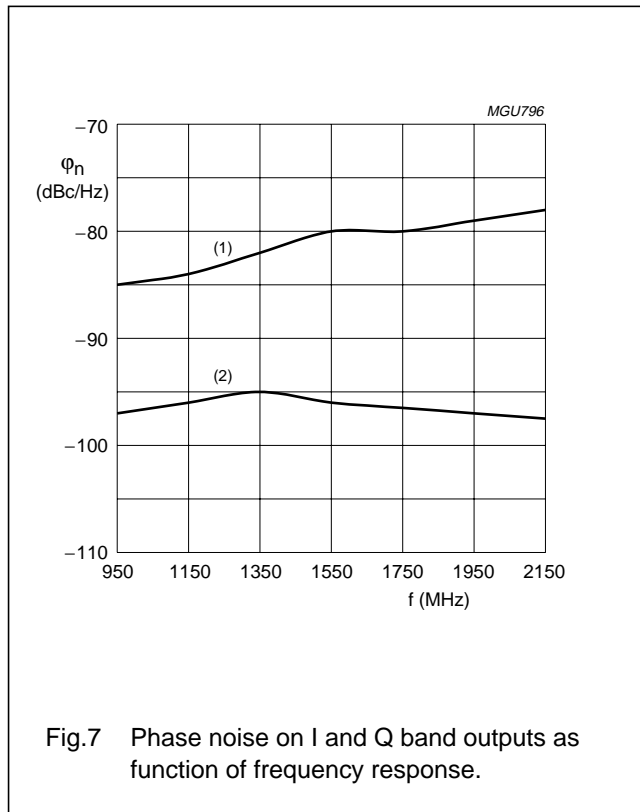
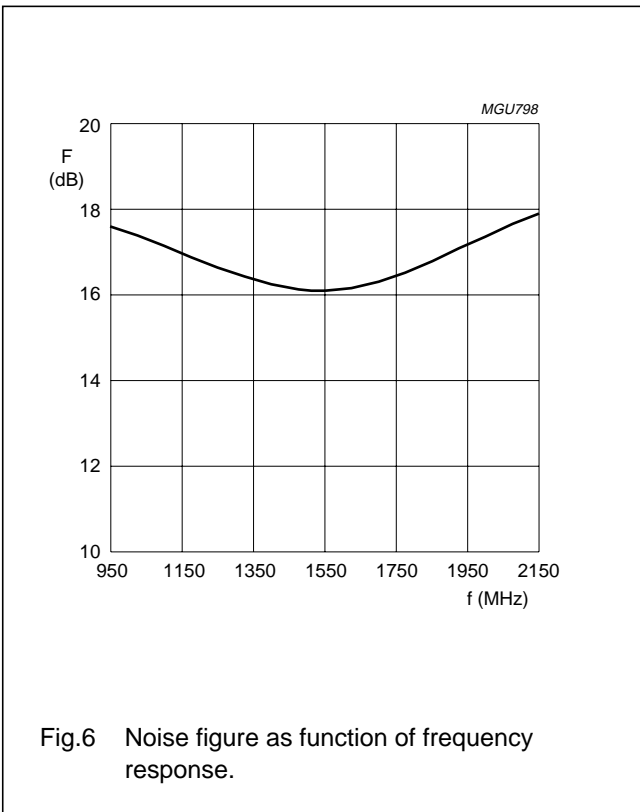
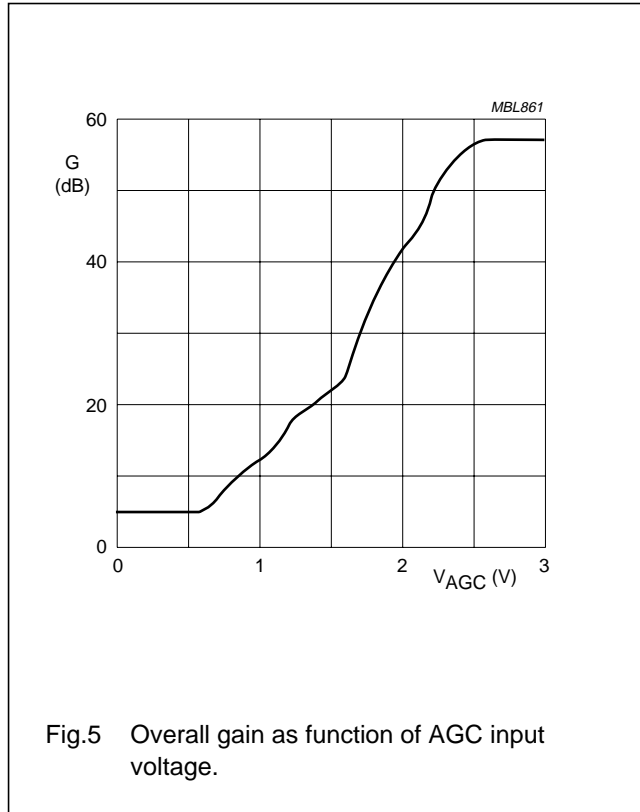
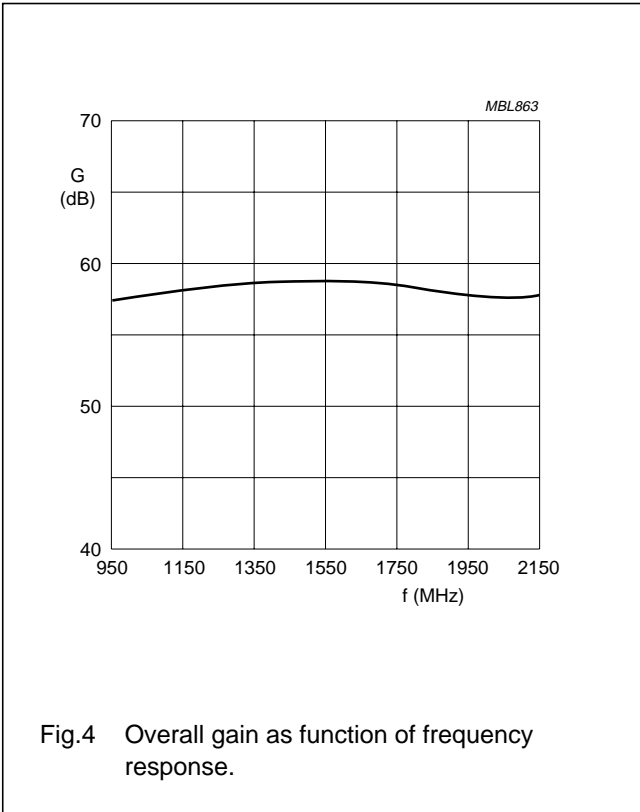
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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ Z_{osc} $	crystal oscillator negative impedance (absolute value)		1.0	1.5	–	k $\Omega$
$f_{xtal}$	crystal frequency		–	4	–	MHz
$Z_{xtal}$	crystal series resistance	recommended value	–	–	200	$\Omega$
$V_{XTOUT(p-p)}$	crystal oscillator output voltage on pin XTOUT (peak-to-peak value)	T2 = 1; T1 = 0; T0 = 0; driving a load of CL = 10 pF; R <sub>L</sub> = 1 M $\Omega$	500	650	–	mV
<b>Charge pump output; pin CP</b>						
$I_L$	leakage current	T2 = 1; T1 = 1; T0 = 0	–10	0	+10	nA
<b>Tuning voltage output; pin VT</b>						
$I_{L(off)}$	leakage current when switch off	T2 = 0; T1 = 0; T0 = 1; V <sub>tune</sub> = 33 V	–	–	10	$\mu$ A
$V_{o(VT)}$	output voltage when the loop is locked	normal mode; V <sub>tune</sub> = 33 V	0.2	–	32.7	V
<b>Bus voltage select input; pin BVS</b>						
$I_{LIH}$	HIGH-level leakage current	V <sub>BVS</sub> = V <sub>CC</sub>	–	–	100	$\mu$ A
$I_{LIL}$	LOW-level leakage current	V <sub>BVS</sub> = 0 V	–100	–	–	$\mu$ A
<b>SCL and SDA inputs</b>						
$V_{IL}$	LOW-level input voltage	V <sub>BVS</sub> = open	–	–	0.2V <sub>CC</sub>	V
		V <sub>BVS</sub> = 0 V	–	–	0.15V <sub>CC</sub>	V
		V <sub>BVS</sub> = 5 V	–	–	0.3V <sub>CC</sub>	V
$V_{IH}$	HIGH-level input voltage	V <sub>BVS</sub> = open	0.46V <sub>CC</sub>	–	–	V
		V <sub>BVS</sub> = 0 V	0.35V <sub>CC</sub>	–	–	V
		V <sub>BVS</sub> = 5 V	0.6V <sub>CC</sub>	–	–	V
$I_{LIH}$	HIGH-level leakage current	V <sub>IH</sub> = 5.5 V; V <sub>CC</sub> = 5.5 V	–	–	10	$\mu$ A
		V <sub>IH</sub> = 5.5 V; V <sub>CC</sub> = 0 V	–	–	10	$\mu$ A
$I_{LIL}$	LOW-level leakage current	V <sub>IL</sub> = 0 V; V <sub>CC</sub> = 5.5 V	–10	–	–	$\mu$ A
$f_{SCL}$	SCL input frequency		–	–	400	kHz
<b>SDA output</b>						
$V_{ACK}$	output voltage during acknowledge	I <sub>sink</sub> = 3 mA	–	–	0.4	V
<b>AS input</b>						
$I_{IH}$	HIGH-level input current	V <sub>AS</sub> = V <sub>CC</sub>	–	–	10	$\mu$ A
$I_{IL}$	LOW-level input current	V <sub>AS</sub> = 0 V	–10	–	–	$\mu$ A

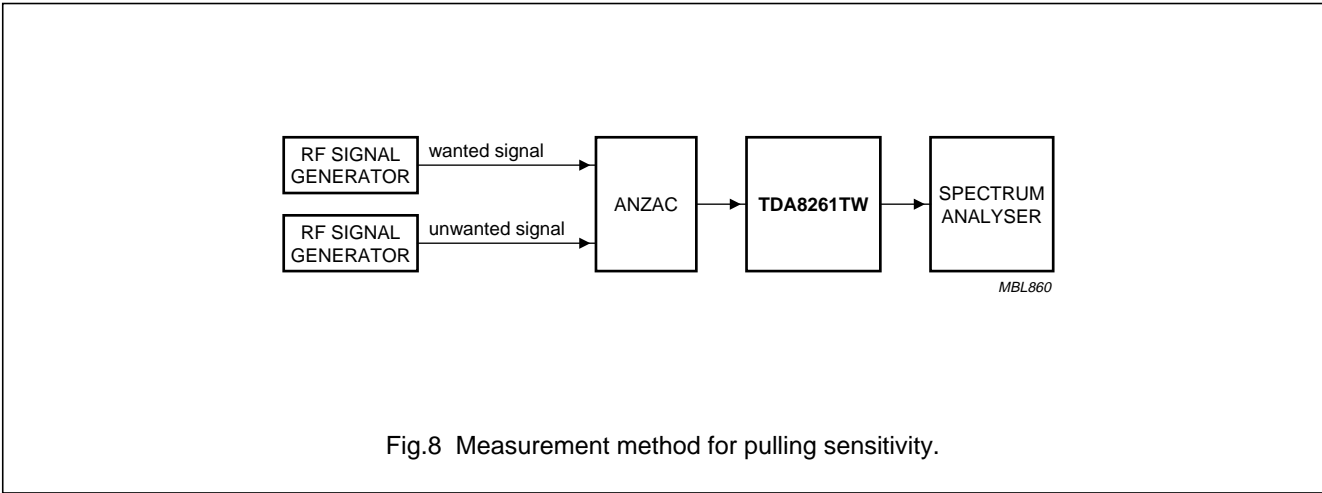
# Satellite Zero-IF QPSK/8PSK downconverter with PLL synthesizer

TDA8261TW



Satellite Zero-IF QPSK/8PSK  
downconverter with PLL synthesizer

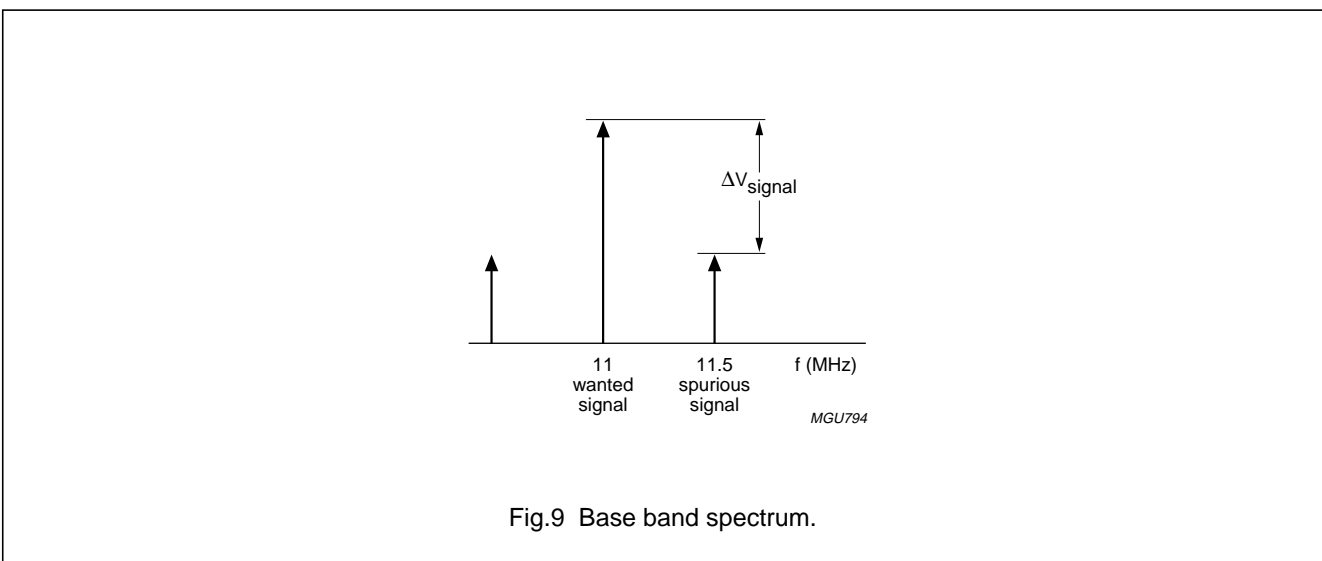
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**Table 9** Test signal conditions for pulling measurements

SIGNAL		FREQUENCY	LEVEL	REMARK
3/4LO test	wanted	$f_w = 2161 \text{ MHz}$	-10 dBm	$f_w = f_{lo} + 11 \text{ MHz}$
	unwanted	$f_{uw} = 1613 \text{ MHz}$	-2 dBm	$f_{uw} = f_{lo} \times 3/4 + 500 \text{ kHz}$
	local oscillator	$f_{lo} = 2150 \text{ MHz}$	-	-
5/4LO test	wanted	$f_w = 1761 \text{ MHz}$	-10 dBm	$f_w = f_{lo} + 11 \text{ MHz}$
	unwanted	$f_{uw} = 2188 \text{ MHz}$	-2 dBm	$f_{uw} = f_{lo} \times 5/4 + 500 \text{ kHz}$
	local oscillator	$f_{lo} = 1750 \text{ MHz}$	-	-

The level of the wanted and unwanted signal mentioned in the table are measured at the outputs of the RF signal generators. The sensitivity to pulling is measured in baseband by the difference expressed in dB ( $\Delta$ ) between the level of the wanted signal and the spurious generated by pulling. The ANZAC reference is HH128.



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## APPLICATION INFORMATION

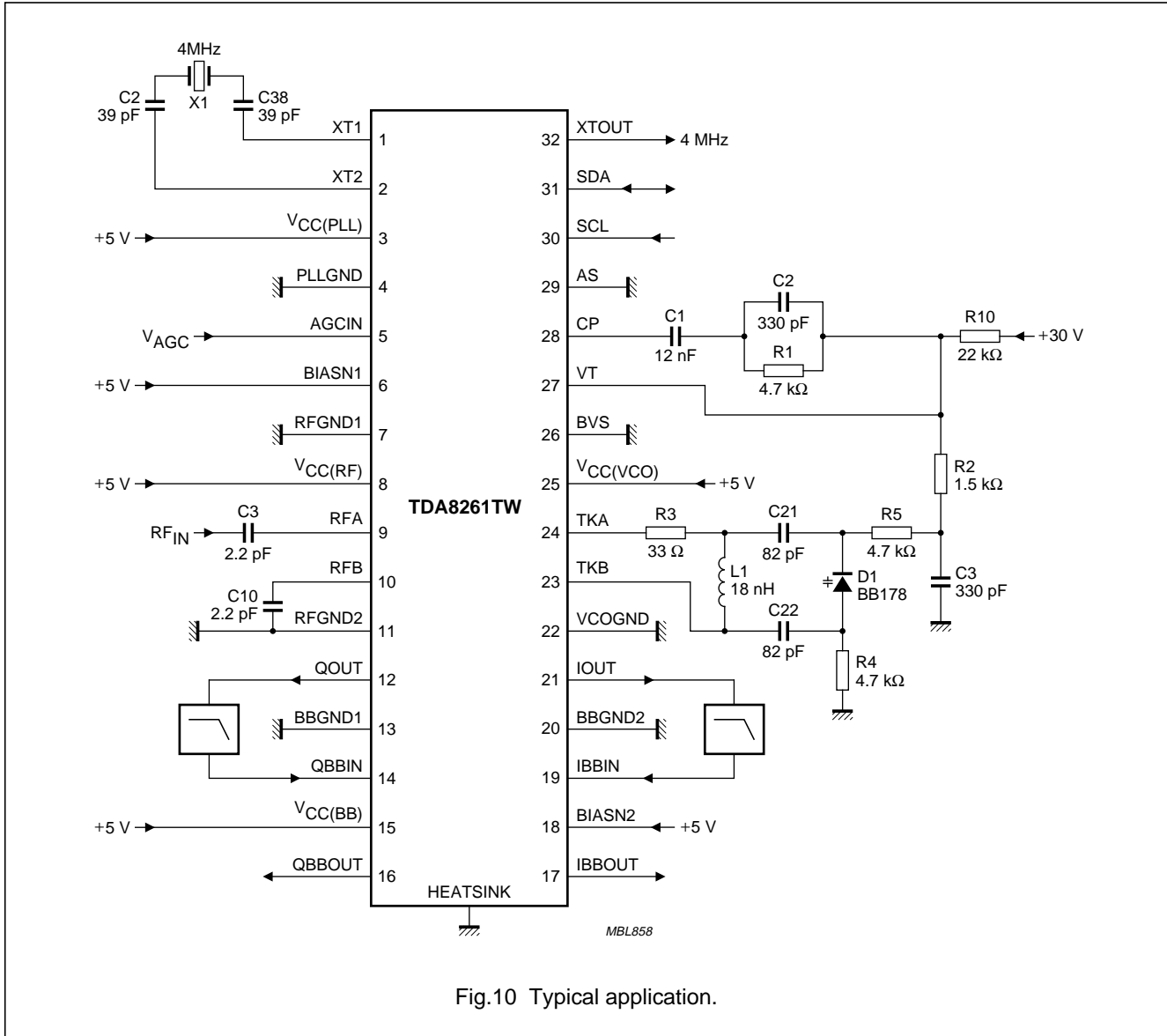


Fig.10 Typical application.

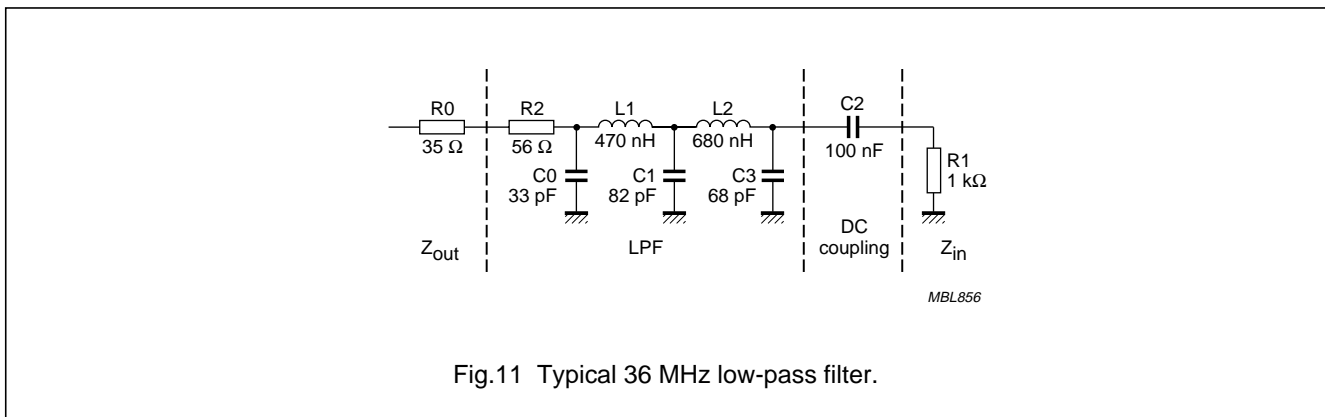


Fig.11 Typical 36 MHz low-pass filter.

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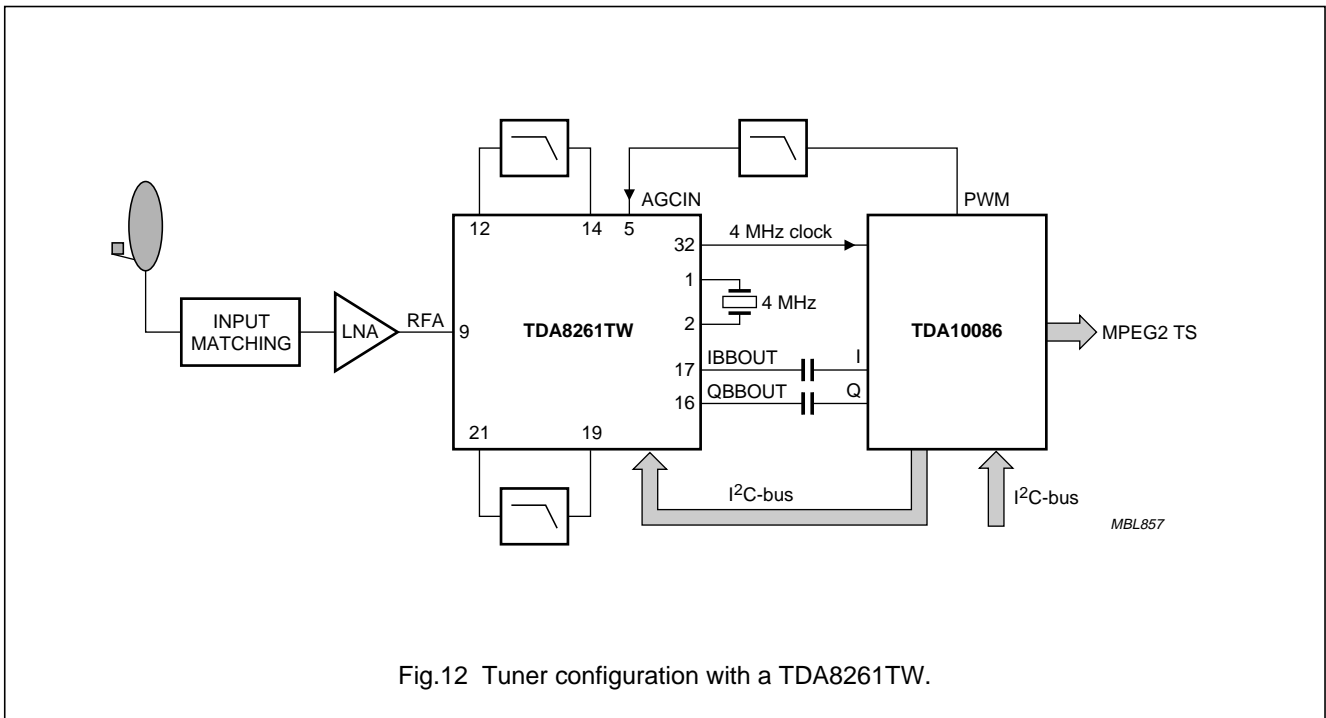


Fig.12 Tuner configuration with a TDA8261TW.

**Application design**

The performance of the application using the TDA8261TW strongly depends on the application design itself. Furthermore the printed-circuit board design and the soldering conditions should take into account the exposed die pad underneath the device, as this requires an optimum electrical ground path for electrical performance, together with the capability to dissipate into the application the heat created in the device. Philips Semiconductors can provide support through reference designs and application

notes for TDA8261TW together with associated channel decoders. Please contact your local Philips Semiconductors sales office for more information.

Wave soldering is not suitable for the TDA8261TW package. This is because the heatsink needs to be soldered to the printed-circuit board underneath the package but with wave soldering the solder cannot penetrate between the printed-circuit board and the heatsink.



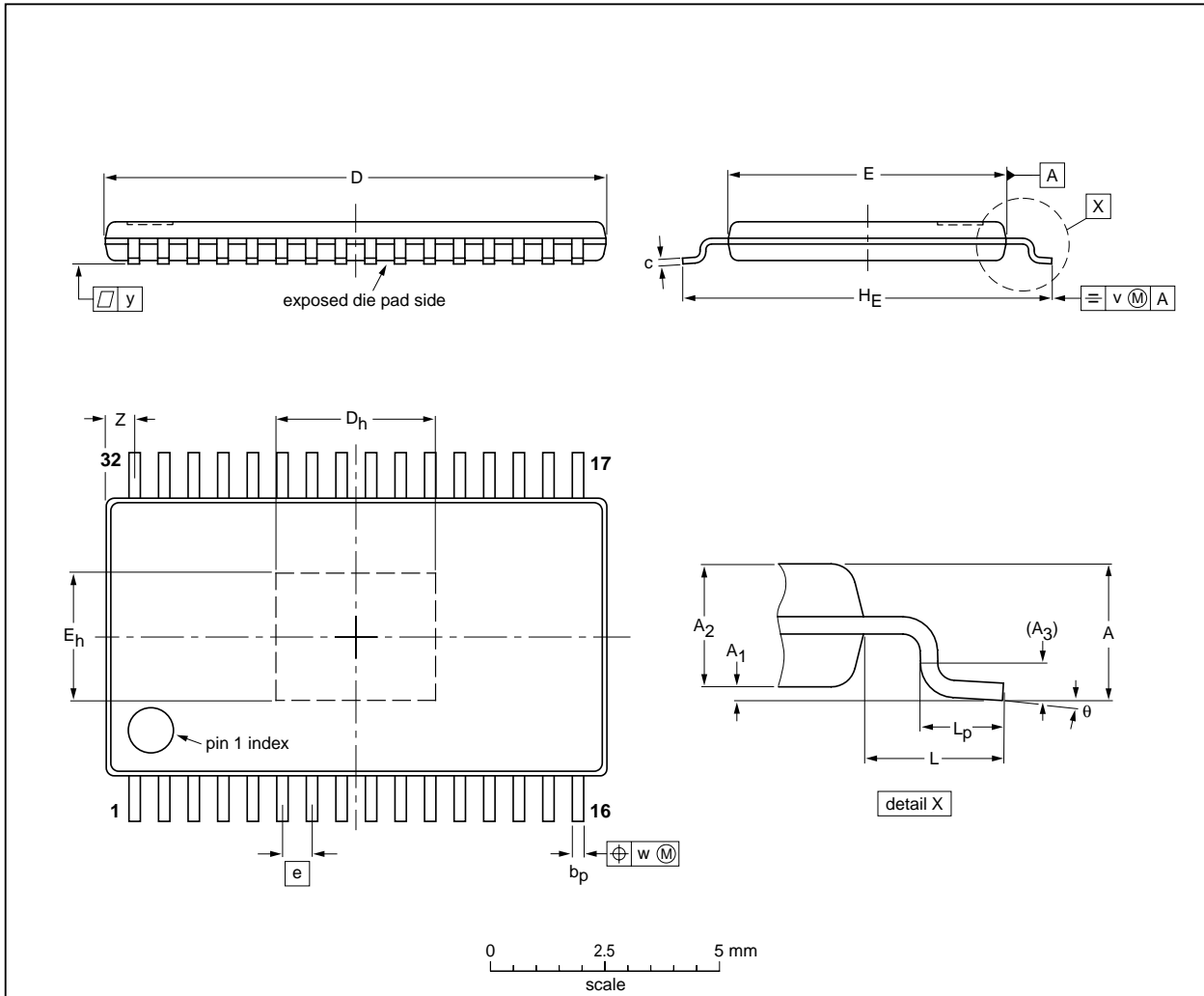
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PACKAGE OUTLINE

HTSSOP32: plastic thermal enhanced thin shrink small outline package; 32 leads;  
body width 6.1 mm; lead pitch 0.65 mm; exposed die pad

SOT549-3



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A1	A2	A3	bp	c	D <sup>(1)</sup>	Dh	E <sup>(2)</sup>	Eh	e	HE	L	Lp	v	w	y	Z	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.30 0.19	0.20 0.09	11.1 10.9	3.65 3.45	6.2 6.0	2.85 2.65	0.65	8.3 7.9	1	0.75 0.50	0.2	0.1	0.1	0.78 0.48	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT549-3						04-01-22

## Satellite Zero-IF QPSK/8PSK downconverter with PLL synthesizer

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### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness  $\geq 2.5$  mm
  - for packages with a thickness  $< 2.5$  mm and a volume  $\geq 350$  mm<sup>3</sup> so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness  $< 2.5$  mm and a volume  $< 350$  mm<sup>3</sup> so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

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## Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE <sup>(1)</sup>	SOLDERING METHOD	
	WAVE	REFLOW <sup>(2)</sup>
BGA, HTSSON..T <sup>(3)</sup> , LBGA, LFBGA, SQFP, SSOP..T <sup>(3)</sup> , TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable <sup>(4)</sup>	suitable
PLCC <sup>(5)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(5)(6)</sup>	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended <sup>(7)</sup>	suitable
CWQCCN..L <sup>(8)</sup> , PMFP <sup>(9)</sup> , WQCCN..L <sup>(8)</sup>	not suitable	not suitable

### Notes

- For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
- These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding  $217\text{ °C} \pm 10\text{ °C}$  measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
- These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- If wave soldering is considered, then the package must be placed at a  $45^\circ$  angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- Hot bar soldering or manual soldering is suitable for PMFP packages.

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## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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### Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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