

Features

- Temperature Ranges
 - Commercial: 0 °C to +70 °C
 - Industrial: -40 °C to +85 °C
 - Automotive-A: -40 °C to +85 °C
 - Automotive-E: -40 °C to +125 °C
- High Speed: 55 ns
- Voltage Range: 4.5 V to 5.5 V Operation
- Low Active Power
 - 275 mW (max)
- Low Standby Power (LL version)
 - 82.5 μW (max)
- Easy Memory Expansion with \overline{CE} and \overline{OE} Features
- TTL-Compatible Inputs and Outputs
- Automatic Power Down when Deselected
- CMOS for Optimum Speed and Power
- Available in Pb-free and non Pb-free 28-pin (600-mil) PDIP, 28-pin (300-mil) Narrow SOIC, 28-pin TSOP-I, and 28-pin Reverse TSOP-I Packages

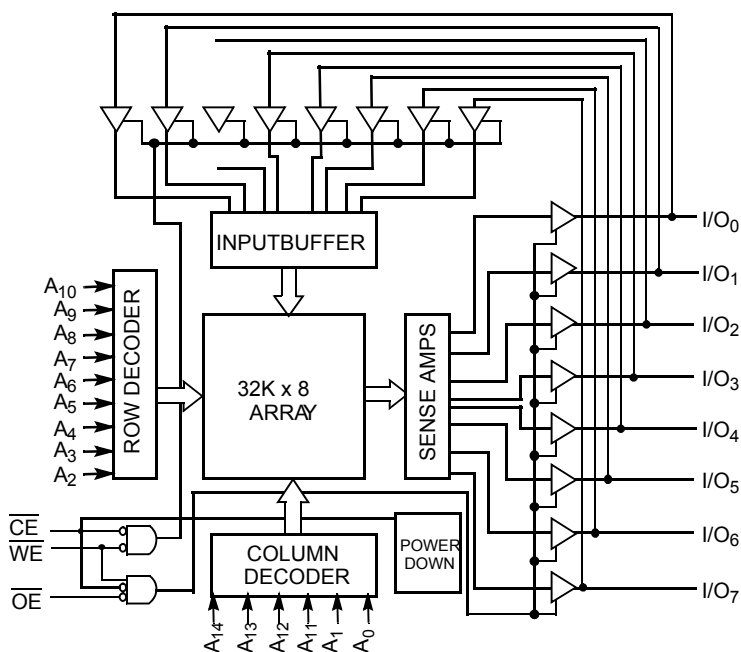
Functional Description

The CY62256N^[1] is a high performance CMOS static RAM organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}) and active LOW output enable (\overline{OE}) and tristate drivers. This device has an automatic power down feature, reducing the power consumption by 99.9 percent when deselected.

An active LOW write enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE} and \overline{WE} inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE} and \overline{OE} active LOW, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH.

Logic Block Diagram



Note

1. For best practice recommendations, do refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

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Product Portfolio

Product		V _{CC} Range (V)			Speed (ns)	Power Dissipation			
						Operating, I _{CC} (mA)		Standby, I _{SB2} (μA)	
		Min	Typ ^[2]	Max		Typ ^[2]	Max	Typ ^[2]	Max
CY62256NLL	Commercial	4.5	5.0	5.5	70	25	50	0.1	5
CY62256NLL	Industrial				55/70	25	50	0.1	10
CY62256NLL	Automotive-A				55/70	25	50	0.1	10
CY62256NLL	Automotive-E				55	25	50	0.1	15

Pin Configurations

Figure 1. 28-pin DIP and Narrow SOIC

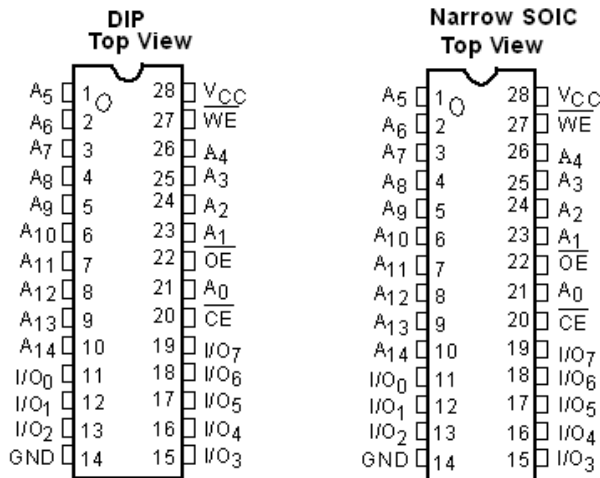


Figure 2. 28-pin TSOP I and Reverse TSOP I

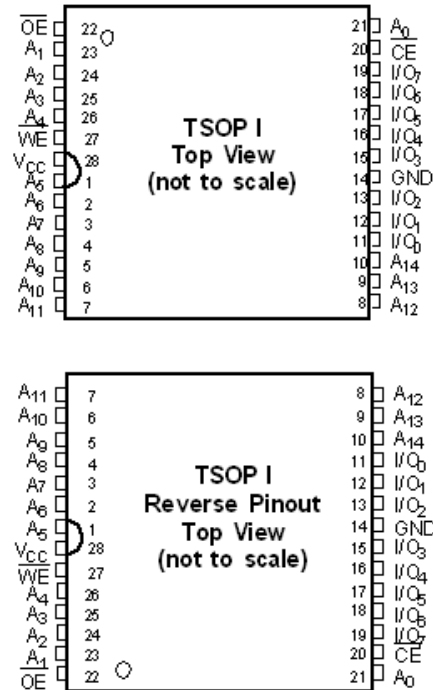


Table 1. Pin Definitions

Pin Number	Type	Description
1–10, 21, 23–26	Input	A₀–A₁₄ . Address Inputs
11–13, 15–19,	Input/Output	I/O₀–I/O₇ . Data lines. Used as input or output lines depending on operation
27	Input/Control	WE . When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted
20	Input/Control	CE . When LOW, selects the chip. When HIGH, deselects the chip
22	Input/Control	OE . Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins
14	Ground	GND . Ground for the device
28	Power Supply	V_{CC} . Power supply for the device

Note

2. Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions (T_A = 25 °C, V_{CC}). Parameters are guaranteed by design and characterization, and not 100% tested.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied	-55 °C to +125 °C
Supply voltage to ground potential (pin 28 to pin 14).....	-0.5 V to +7.0 V
DC voltage applied to outputs in high Z State ^[3]	-0.5 V to V _{CC} + 0.5 V
DC input voltage ^[3]	-0.5 V to V _{CC} + 0.5 V
Output current into outputs (LOW)	20 mA

Static discharge voltage..... > 2001 V (per MIL-STD-883, method 3015)

Latch up current..... > 200 mA

Operating Range

Range	Ambient Temperature (T _A) ^[4]	V _{CC}
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial	-40 °C to +85 °C	5 V ± 10%
Automotive-A	-40 °C to +85 °C	5 V ± 10%
Automotive-E	-40 °C to +125 °C	5 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-55			-70			Unit	
			Min	Typ ^[5]	Max	Min	Typ ^[5]	Max		
V _{OH}	Output HIGH voltage	V _{CC} = Min, I _{OH} = -1.0 mA	2.4	-	-	2.4	-	-	V	
V _{OL}	Output LOW voltage	V _{CC} = Min, I _{OL} = 2.1 mA	-	-	0.4	-	-	0.4	V	
V _{IH}	Input HIGH voltage		2.2	-	V _{CC} + 0.5 V	2.2	-	V _{CC} + 0.5 V	V	
V _{IL}	Input LOW voltage		-0.5	-	0.8	-0.5	-	0.8	V	
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}	-0.5	-	+0.5	-0.5	-	+0.5	μA	
I _{OZ}	Output leakage current	GND ≤ V _O ≤ V _{CC} , output disabled	-0.5	-	+0.5	-0.5	-	+0.5	μA	
I _{CC}	V _{CC} operating supply current	V _{CC} = Max, I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	LL-Commercial	-	-	-	-	25	50	mA
			LL - Industrial	-	25	50	-	25	50	mA
			LL - Auto-A	-	25	50	-	25	50	mA
			LL - Auto-E	-	25	50	-	-	-	mA
I _{SB1}	Automatic CE power down current—TTL inputs	Max. V _{CC} , CE ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	LL-Commercial	-	-	-	-	0.3	0.5	mA
			LL - Industrial	-	0.3	0.5	-	0.3	0.5	mA
			LL - Auto-A	-	0.3	0.5	-	0.3	0.5	mA
			LL - Auto-E	-	0.3	0.5	-	-	-	mA
I _{SB2}	Automatic CE power down current—CMOS inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3 V, V _{IN} ≥ V _{CC} - 0.3 V, or V _{IN} ≤ 0.3 V, f = 0	LL-Commercial	-	-	-	-	0.1	5	μA
			LL - Industrial	-	0.1	10	-	0.1	10	μA
			LL - Auto-A	-	0.1	10	-	0.1	10	μA
			LL - Auto-E	-	0.1	15	-	-	-	μA

Capacitance

Parameter ^[6]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 5.0 V	6	pF
C _{OUT}	Output capacitance		8	pF

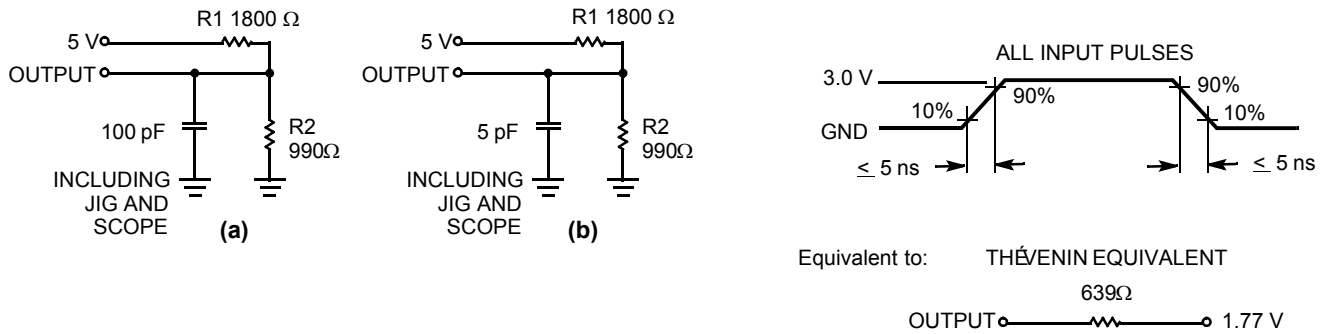
Notes

- V_{IL} (min) = -2.0 V for pulse durations of less than 20 ns.
- T_A is the "Instant-On" case temperature.
- Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions (T_A = 25 °C, V_{CC}). Parameters are guaranteed by design and characterization, and not 100% tested.
- Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance

Parameter ^[7]	Description	Test Conditions	DIP	SOIC	TSOP	RTSOP	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 4.25 × 1.125 inch, 4-layer printed circuit board	75.61	76.56	93.89	93.89	°C/W
Θ_{JC}	Thermal resistance (junction to case)		43.12	36.07	24.64	24.64	°C/W

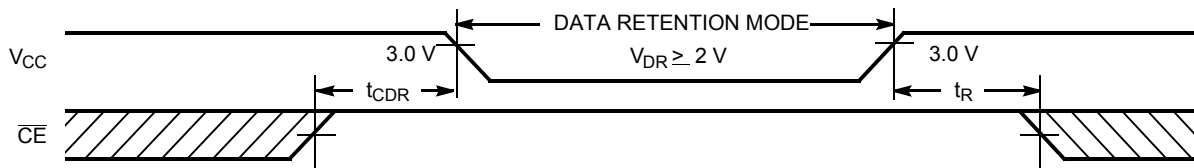
Figure 3. AC Test Loads and Waveforms



Data Retention Characteristics

Parameter	Description	Conditions ^[8]	Min	Typ ^[9]	Max	Unit	
V_{DR}	V_{CC} for data retention		2.0	–	–	V	
I_{CCDR}	Data retention current	LL - Commercial	$V_{CC} = 2.0V, CE \geq V_{CC} - 0.3V,$ $V_{IN} \geq V_{CC} - 0.3V, \text{ or } V_{IN} \leq 0.3V$	–	0.1	5	μA
		LL - Industrial/Auto-A		–	0.1	10	μA
		LL - Auto-E		–	0.1	10	μA
$t_{CDR}^{[7]}$	Chip deselect to data retention time		0	–	–	ns	
$t_R^{[7]}$	Operation recovery time		t_{RC}	–	–	ns	

Figure 4. Data Retention Waveform



Notes

- 7. Tested initially and after any design or process changes that may affect these parameters.
- 8. No input may exceed $V_{CC} + 0.5V$.
- 9. Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions ($T_A = 25^\circ C, V_{CC}$). Parameters are guaranteed by design and characterization, and not 100% tested.

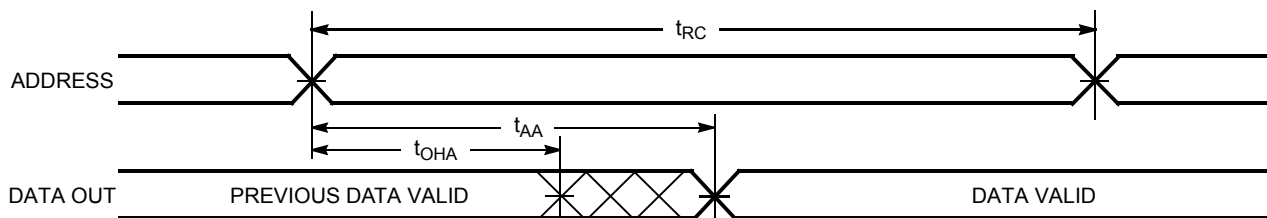
Switching Characteristics

Over the Operating Range^[10]

Parameter	Description	CY62256N-55		CY62256N-70		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	55	–	70	–	ns
t_{AA}	Address to data valid	–	55	–	70	ns
t_{OHA}	Data hold from address change	5	–	5	–	ns
t_{ACE}	\overline{CE} LOW to data valid	–	55	–	70	ns
t_{DOE}	\overline{OE} LOW to data valid	–	25	–	35	ns
t_{LZOE}	\overline{OE} LOW to low Z ^[11]	5	–	5	–	ns
t_{HZOE}	\overline{OE} HIGH to high Z ^[11, 12]	–	20	–	25	ns
t_{LZCE}	\overline{CE} LOW to low Z ^[11]	5	–	5	–	ns
t_{HZCE}	\overline{CE} HIGH to high Z ^[11, 12]	–	20	–	25	ns
t_{PU}	\overline{CE} LOW to power up	0	–	0	–	ns
t_{PD}	\overline{CE} HIGH to power down	–	55	–	70	ns
Write Cycle^[13, 14]						
t_{WC}	Write cycle time	55	–	70	–	ns
t_{SCE}	\overline{CE} LOW to write end	45	–	60	–	ns
t_{AW}	Address setup to write end	45	–	60	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	\overline{WE} pulse width	40	–	50	–	ns
t_{SD}	Data setup to write end	25	–	30	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	\overline{WE} LOW to high Z ^[11, 12]	–	20	–	25	ns
t_{LZWE}	\overline{WE} HIGH to low Z ^[11]	5	–	5	–	ns

Switching Waveforms

Figure 5. Read Cycle No. 1^[15, 16]



Notes

10. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
11. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
12. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
13. The internal Write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a Write and either signal can terminate a Write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the Write.
14. The minimum Write cycle time for Write Cycle #3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .
15. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
16. \overline{WE} is HIGH for Read cycle.

Switching Waveforms (continued)

Figure 6. Read Cycle No. 2^[17, 18]

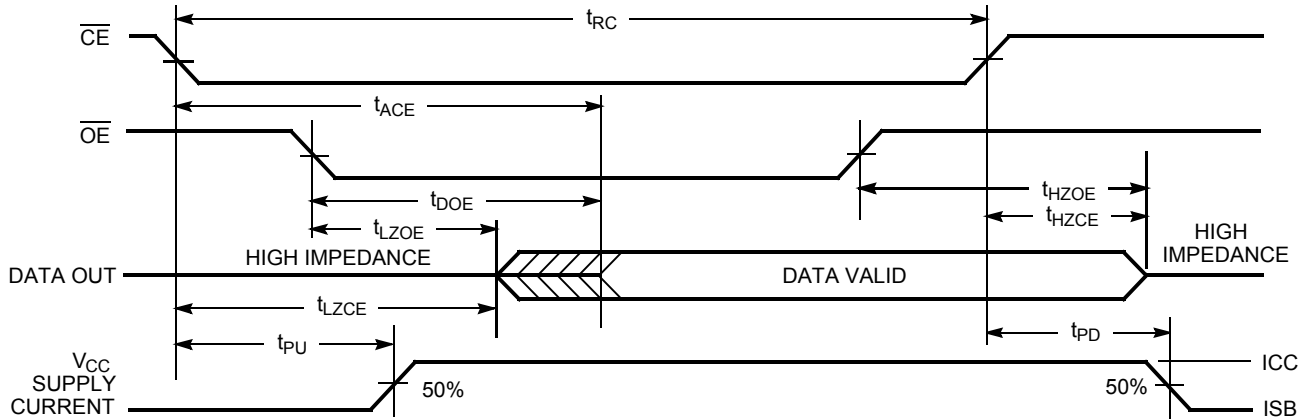


Figure 7. Write Cycle No. 1 (\overline{WE} Controlled)^[19, 20, 21]

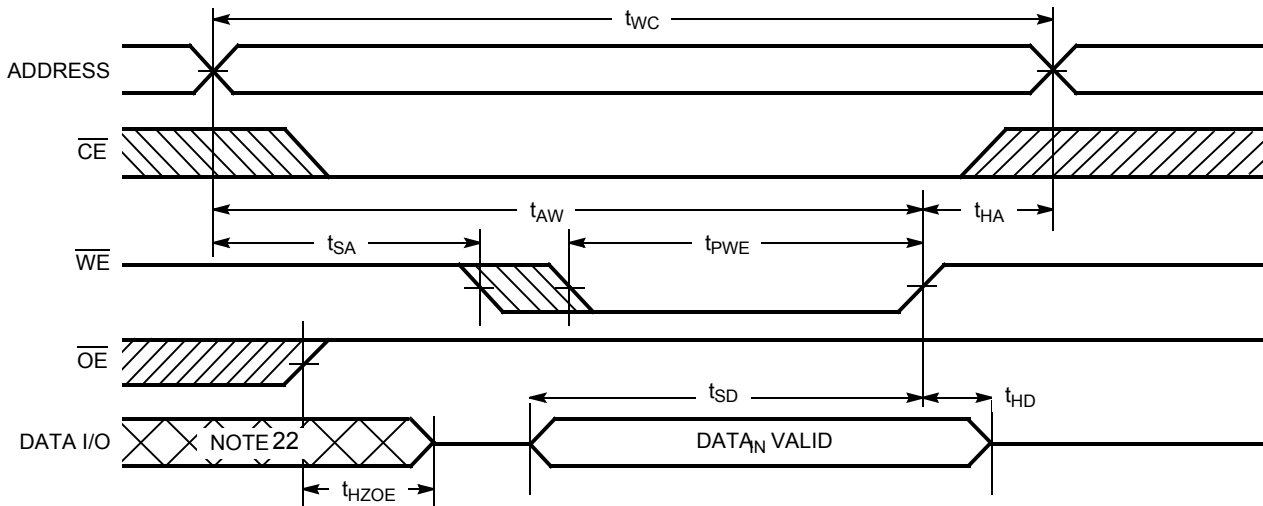
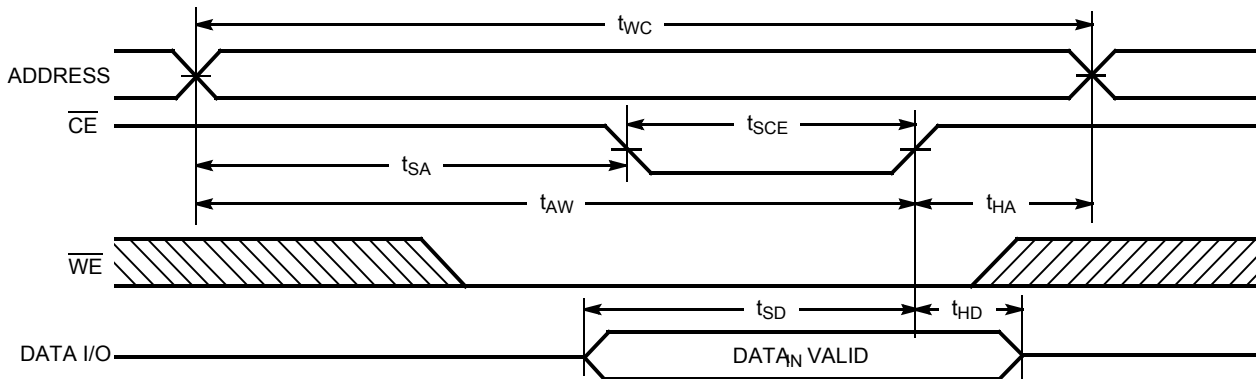


Figure 8. Write Cycle No. 2 (\overline{CE} Controlled)^[19, 20, 21]

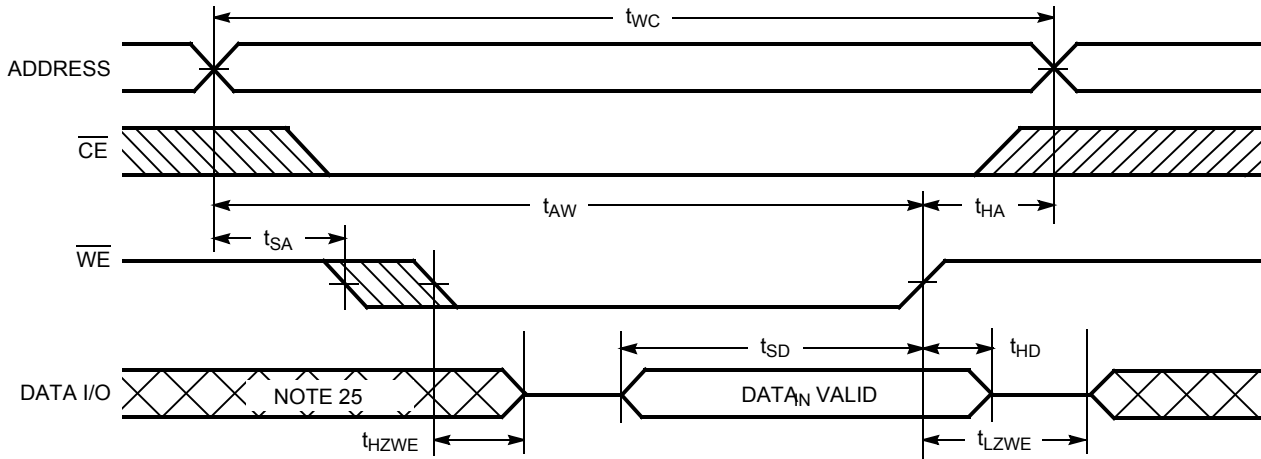


Notes

- 17. \overline{WE} is HIGH for Read cycle.
- 18. Address valid prior to or coincident with \overline{CE} transition LOW.
- 19. The internal Write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a Write and either signal can terminate a Write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the Write.
- 20. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 21. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
- 22. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

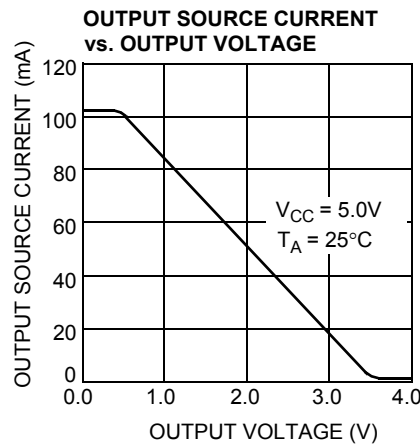
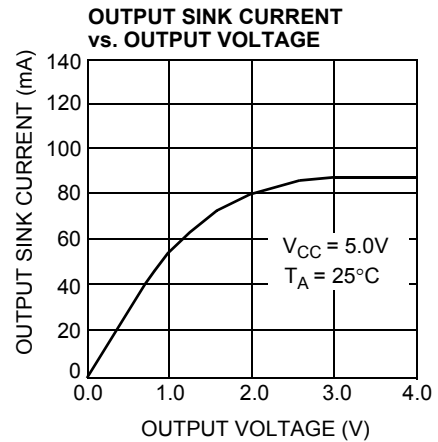
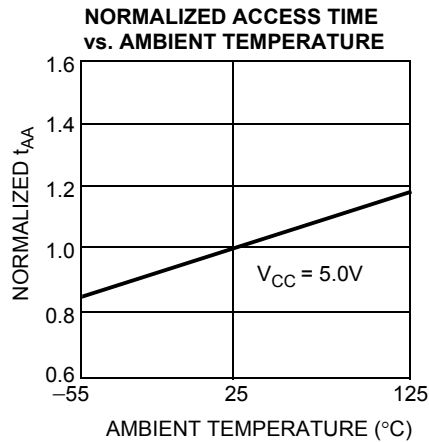
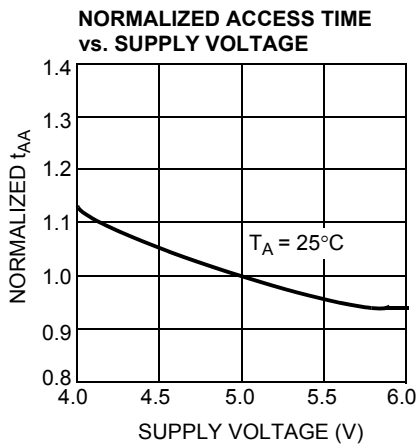
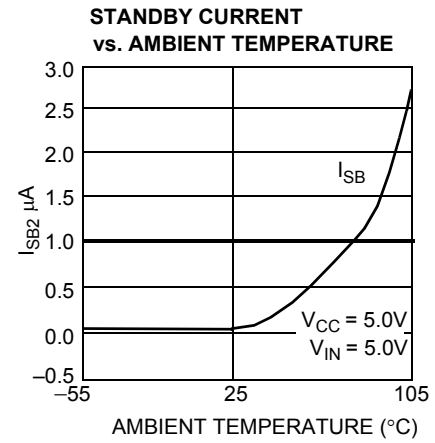
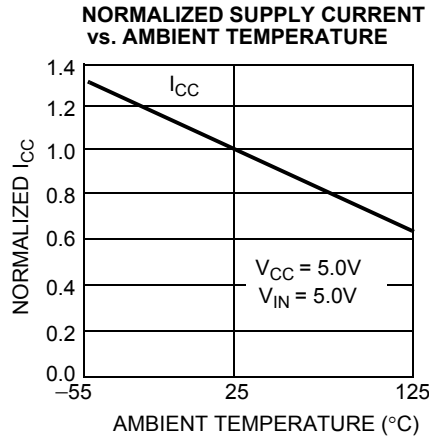
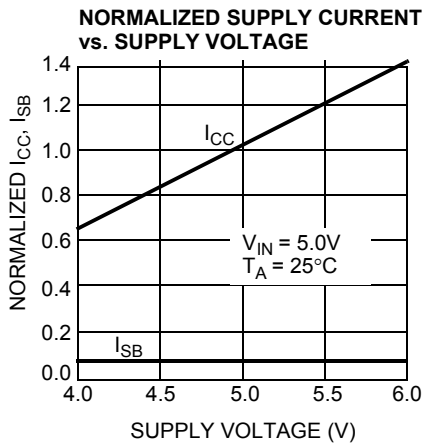
Figure 9. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[23, 24]



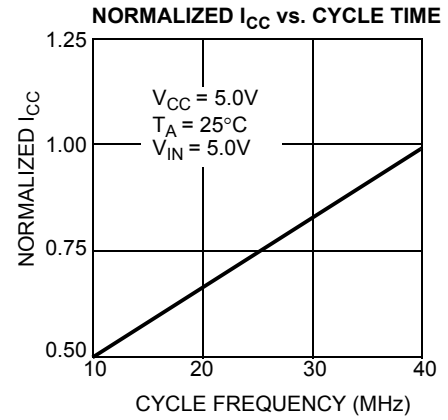
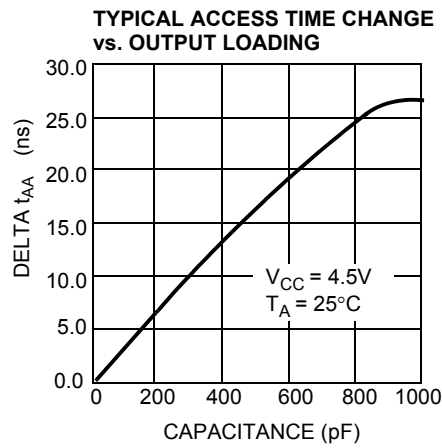
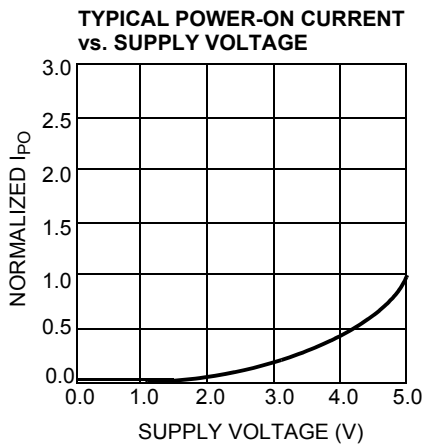
Notes

- 23. The minimum Write cycle time for Write Cycle #3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .
- 24. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
- 25. During this period, the I/Os are in output state and input signals should not be applied.

Typical DC and AC Characteristics



Typical DC and AC Characteristics (continued)



Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power down	Standby (I _{SB})
L	H	L	Data Out	Read	Active (I _{CC})
L	L	X	Data In	Write	Active (I _{CC})
L	H	H	High Z	Output Disabled	Active (I _{CC})

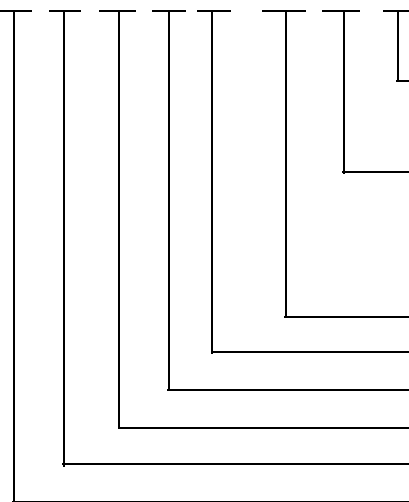
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62256NLL-55SNXI	51-85092	28-pin (300-Mil) Narrow SOIC (Pb-free)	Industrial
	CY62256NLL-55ZXI	51-85071	28-pin TSOP I (Pb-free)	
	CY62256NLL-55ZXA	51-85071	28-pin TSOP I (Pb-free)	Automotive-A
	CY62256NLL-55SNXE	51-85092	28-pin (300-Mil) Narrow SOIC (Pb-free)	Automotive-E
	CY62256NLL-55ZXE	51-85071	28-pin TSOP I (Pb-free)	
70	CY62256NLL-70PXC	51-85017	28-pin (600-Mil) Molded DIP (Pb-free)	Commercial
	CY62256NLL-70SNXC	51-85092	28-pin (300-Mil) Narrow SOIC (Pb-free)	
	CY62256NLL-70ZRXI	51-85074	28-pin Reverse TSOP I (Pb-free)	Industrial
	CY62256NLL-70SNXA	51-85092	28-pin (300-Mil) Narrow SOIC (Pb-free)	Automotive-A

Do contact your local Cypress sales representative for availability of these parts

Ordering Code Definitions

CY 62 256 N LL - XX XXX X



Temperature Grade: X = C or I or A or E

C = Commercial = 0 °C to +70 °C; I = Industrial = -40 °C to +85 °C;

A = Automotive-A = -40 °C to +85 °C; E = Automotive-E = -40 °C to +125 °C

Package Type: XXX = SNX or ZX or PX or ZRX

SNX = 28-pin Narrow SOIC (Pb-free)

ZX = 28-pin TSOP I (Pb-free)

PX = 28-pin Molded DIP (Pb-free)

ZRX = 28-pin Reverse TSOP I (Pb-free)

Speed Grade: XX = 55 ns or 70 ns

Low Power

Nitride Seal Mask fix

Density: 256 Kbit

MoBL SRAM family

Company ID: CY = Cypress

Package Diagrams

Figure 10. 28-pin (600-Mil) Molded DIP, 51-85017

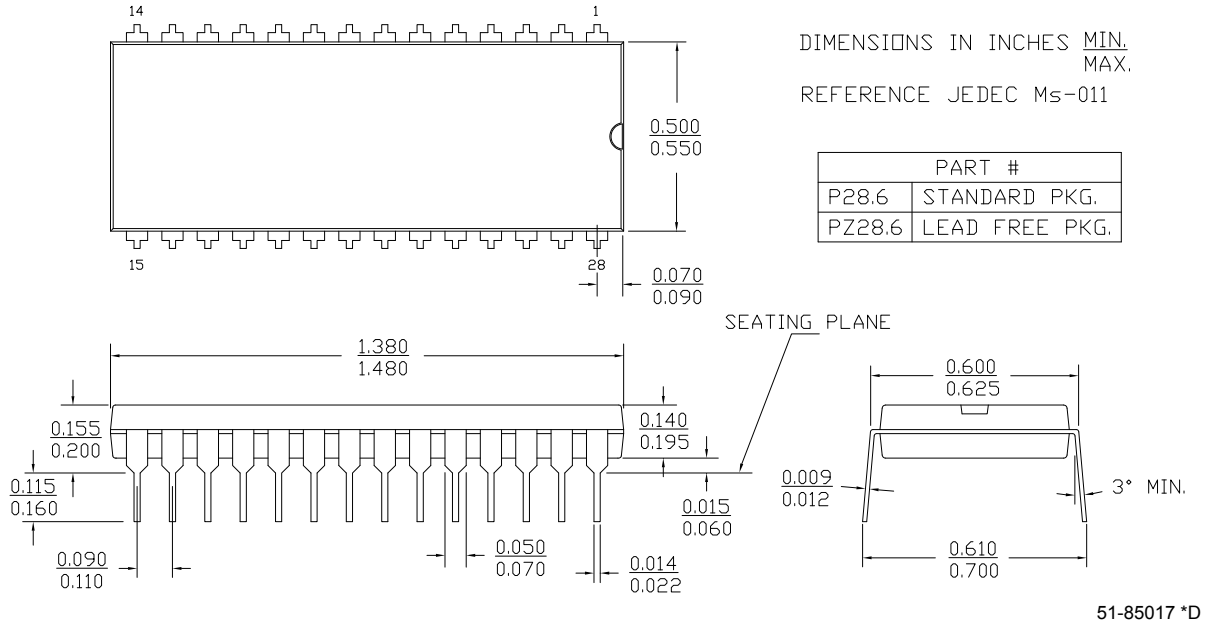


Figure 11. 28-pin (300-mil) SNC (Narrow Body), 51-85092

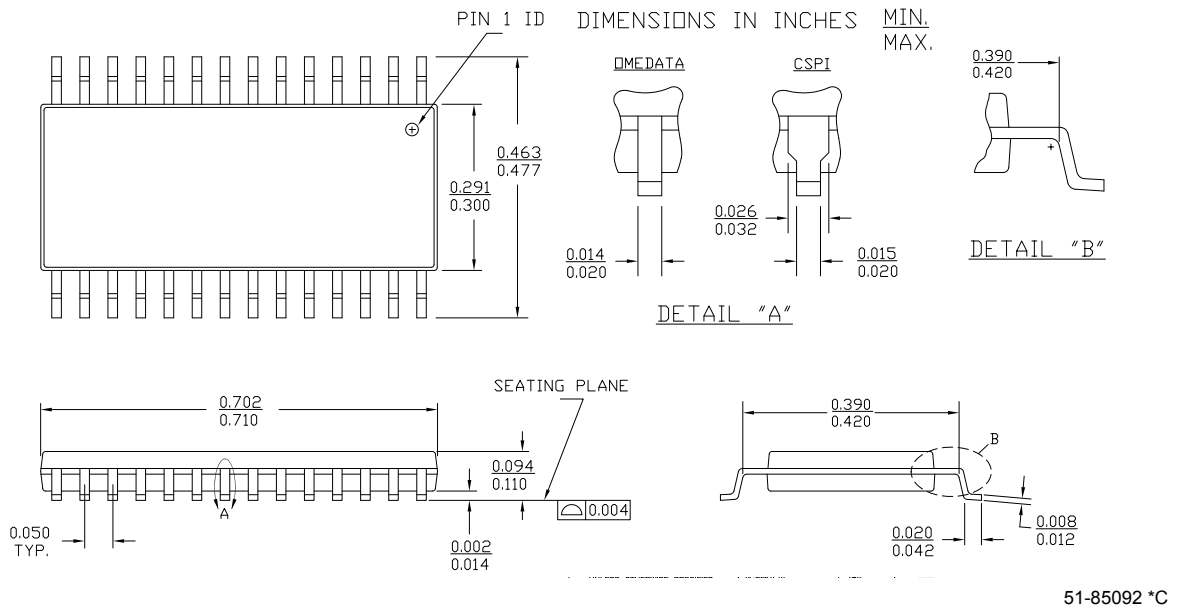


Figure 12. 28-pin TSOP I (8 × 13.4 mm), 51-85071

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2

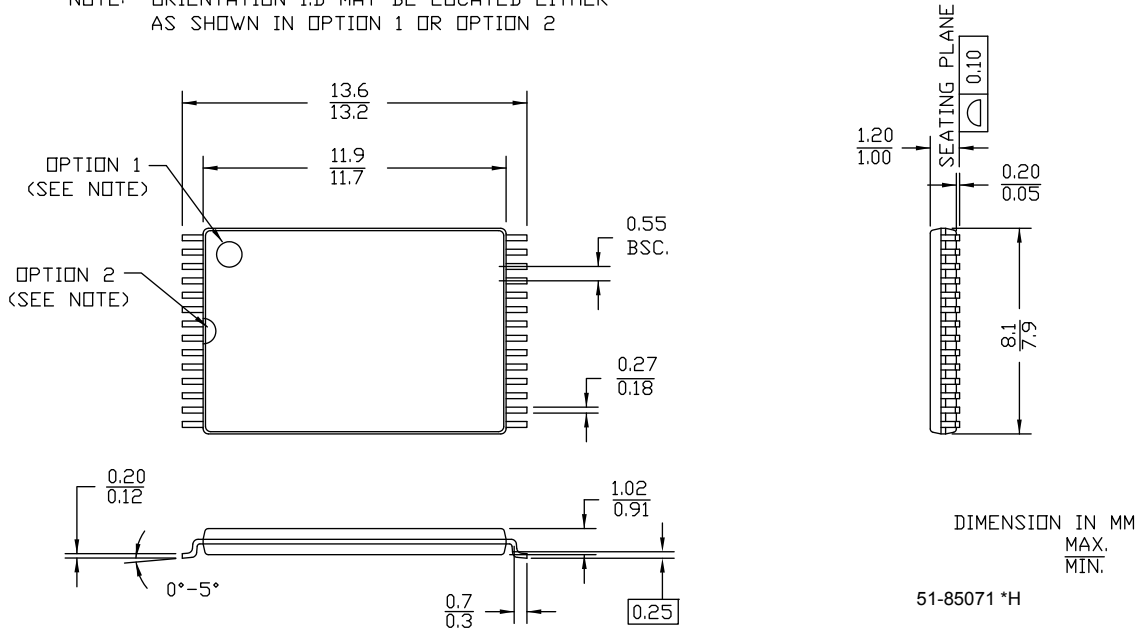
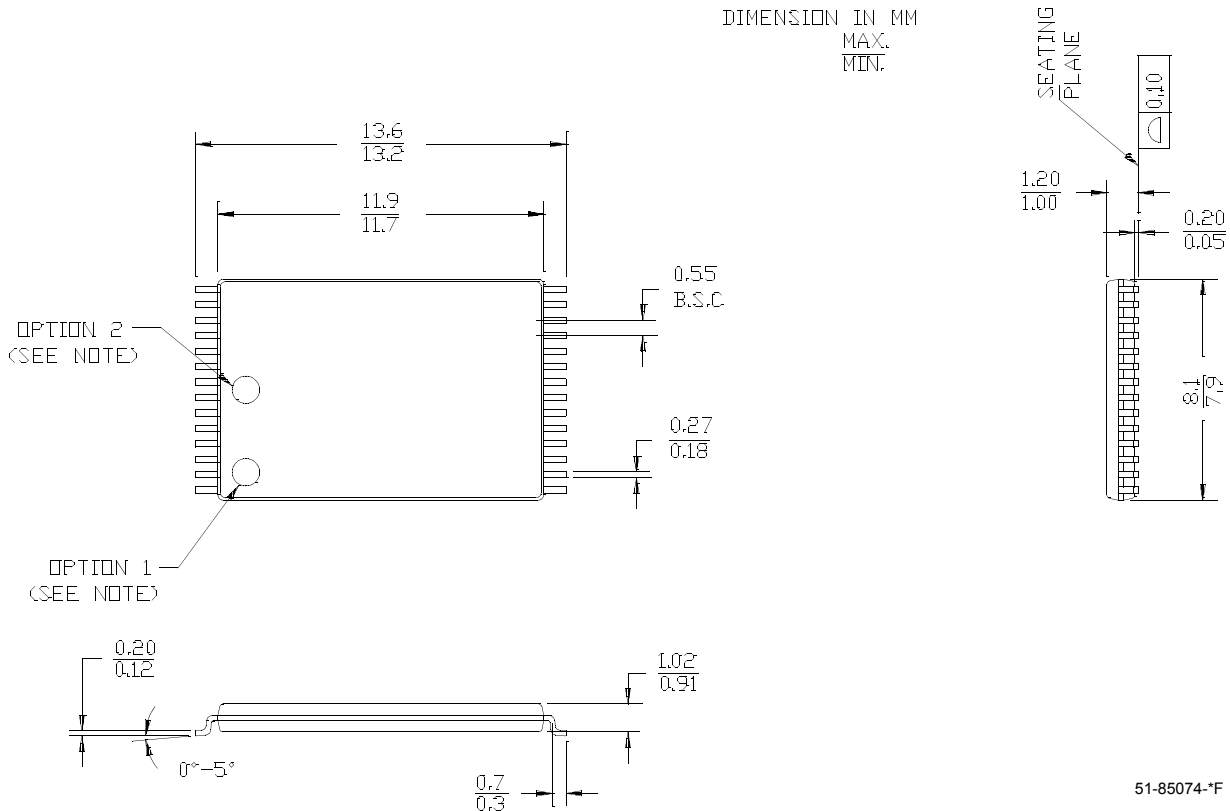


Figure 13. 28-pin TSOP I (8 × 13.4 mm), 51-85074

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



Document History Page

Document Title: CY62256N 256K (32K × 8) Static RAM Document Number: 001-06511				
REV.	ECN NO.	Submission Date	Orig. of Change	Description of Change
**	426504	See ECN	NXR	New Data Sheet
*A	488954	See ECN	NXR	Added Automotive product Updated ordering Information table
*B	2715270	06/05/2009	VKN/AESA	Updated POD of 28-Pin (600-Mil) Molded DIP package (Spec# 51-85017)
*C	2891344	03/12/2010	VKN	Added Table of Contents Removed "L" product information Updated Ordering Information table Updated Package Diagrams (Figure 10, Figure 11, and Figure 12) Updated Sales, Solutions, and Legal Information
*D	3119519	01/04/2011	AJU	Updated Ordering Information . Added Ordering Code Definitions .

Sales, Solutions, and Legal Information

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