R1Q5A3636B/R1Q5A3618B

36-Mbit DDRII SRAM
4-word Burst

REJ03C0344-0003
Preliminary
Rev. 0.03
Apr.11, 2008

Description

The R1Q5A3636B is a 1,048,576-word by 36-bit, the R1Q5A3618B is a 2,097,152-word by 18-bit synchronous double data rate static RAM fabricated with advanced CMOS technology using full CMOS six-transistor memory cell. It integrates unique synchronous peripheral circuitry and a burst counter. All input registers controlled by an input clock pair (K and /K) and are latched on the positive edge of K and /K. These products are suitable for applications which require synchronous operation, high speed, low voltage, high density and wide bit configuration. These products are packaged in 165-pin plastic FBGA package.

Features

- 1.8 V ± 0.1 V power supply for core (V_{DD})
- 1.4 V to V_{DD} power supply for I/O (V_{DDQ})
- DLL circuitry for wide output data valid window and future frequency scaling
- Pipelined double data rate operation
- Common data input/output bus
- Four-tick burst for reduced address frequency
- Two input clocks (K and /K) for precise DDR timing at clock rising edges only
- Two output clocks (C and /C) for precise flight time and clock skew matching-clock and data delivered together to receiving device
- Internally self-timed write control
- Clock-stop capability with µs restart
- User programmable impedance output
- Fast clock cycle time: 3.3 ns (300 MHz)/4.0 ns (250 MHz)/ 5.0 ns (200 MHz)/6.0 ns (167 MHz)
- Simple control logic for easy depth expansion
- JTAG boundary scan

Preliminary: The specifications of this device are subject to change without notice. Please contact your nearest Renesas Technology's Sales Dept. regarding specifications

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Ordering Information

Part Number	Organization	Cycle time	Clock frequency	Package	Notes
R1Q5A3636BBG-33R	1-M word × 36-bit	3.3 ns	300 MHz	Plastic FBGA 165-pin PLBG0165FB-A	
R1Q5A3636BBG-40R		4.0 ns	250 MHz		
R1Q5A3636BBG-50R		5.0 ns	200 MHz		
R1Q5A3636BBG-60R		6.0 ns	167 MHz		
R1Q5A3618BBG-33R	2-M word × 18-bit	3.3 ns	300 MHz		
R1Q5A3618BBG-40R		4.0 ns	250 MHz		
R1Q5A3618BBG-50R		5.0 ns	200 MHz		
R1Q5A3618BBG-60R		6.0 ns	167 MHz		

Notes:

1. Part Number

(0:1)	R1	: Renesas Memory prefix
(2:3)	Q2	: QDRII 2-word Burst SRAM
	Q3	: QDRII 4-word Burst SRAM
	Q4	: DDRII 2-word Burst SRAM
	Q5	: DDRII 4-word Burst SRAM
	Q6	: DDRII 2-word Burst SRAM
		Separate I/O
(4)	A	: V_{DD}=1.8V
(5:6)	36	: Density = 36Mb
	72	: Density = 72Mb
(7:8)	36	: Organization = x36
	18	: Organization = x18
	09	: Organization = x9
(9)	R	: 1st Generation
	A	: 2nd Generation
	B	: 3rd Generation
(10:11)	BG	: Package type=BGA
(12:13)	60	: Cycle time=6.0 ns
	50	: Cycle time=5.0 ns
	40	: Cycle time=4.0 ns
	33	: Cycle time=3.3 ns
(14)	R	: Temperature range= 0°C~ 70°C
	I	: Temperature range= -40°C ~85°C
(15)	B	: Pb-free
	T	: Tape&Reel
	S	: Pb-free and Tape&Reel
	None	: Standard (Pb and Tray)
(16)	0 ~9 , A ~Z:Renesas internal use	

2. Marking Name

Marking Name(0:14) =Part Number (0:14) ----------Pb

Marking Name(0:16) =Part Number (0:14)+Bx----------Pb-free (x= 0 ~9 , A ~Z)

(Example) R1Q5A3618BBG-60R ----------Pb

R1Q5A3618BBG-60RB0 ----------Pb-free

Pin Arrangement

R1Q5A3636B series

	1	2	3	4	5	6	7	8	9	10	11
A	/CQ	V_{SS}	SA	R-/W	/BW2	/K	/BW1	/LD	SA	NC	CQ
B	NC	DQ27	DQ18	SA	/BW3	K	/BW0	SA	NC	NC	DQ8
C	NC	NC	DQ28	V_{SS}	SA	SA0	SA1	V_{SS}	NC	DQ17	DQ7
D	NC	DQ29	DQ19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	DQ16
E	NC	NC	DQ20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQ15	DQ6
F	NC	DQ30	DQ21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	DQ31	DQ22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ14
H	/DOFF	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	DQ32	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ13	DQ4
K	NC	NC	DQ23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ12	DQ3
L	NC	DQ33	DQ24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	DQ34	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ11	DQ1
N	NC	DQ35	DQ25	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	DQ10
P	NC	NC	DQ26	SA	SA	C	SA	SA	NC	DQ9	DQ0
R	TDO	TCK	SA	SA	SA	/C	SA	SA	SA	TMS	TDI

(Top View)

R1Q5A3618B series

	1	2	3	4	5	6	7	8	9	10	11
A	/CQ	V_{SS}	SA	R-/W	/BW1	/K	NC	/LD	SA	SA	CQ
B	NC	DQ9	NC	SA	NC	K	/BW0	SA	NC	NC	DQ8
C	NC	NC	NC	V_{SS}	SA	SA0	SA1	V_{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	/DOFF	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	DQ17	SA	SA	C	SA	SA	NC	NC	DQ0
R	TDO	TCK	SA	SA	SA	/C	SA	SA	SA	TMS	TDI

(Top View)

Notes: 1. Note that 7C is not SA1. The ×9 product does not permit random start address on the two least significant address bit. SA0, SA1 = 0 at the start of each address.

: 2. Address expansion order for future higher density SRAMs (i.e. 72Mb → 144Mb →288Mb): (9A → 3A → 10A) → 2A → 7A → 5B.

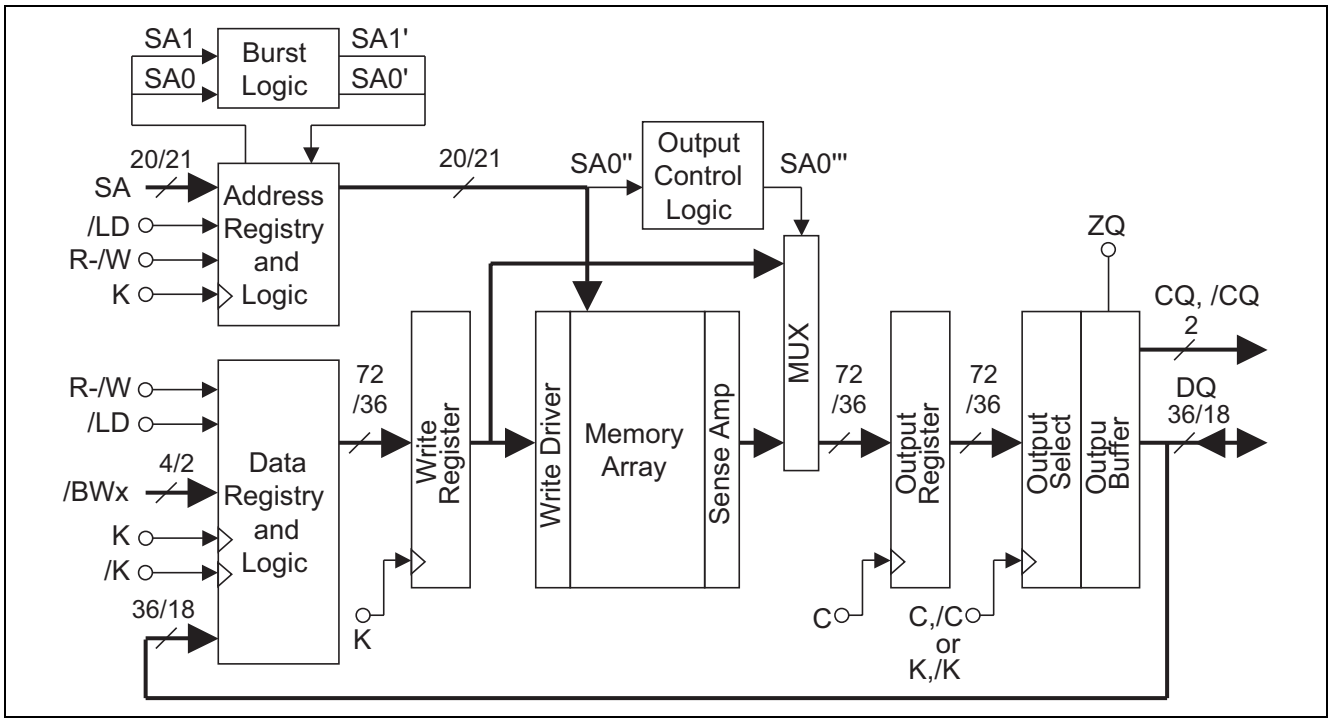
Pin Description

Name	I/O type	Descriptions	Notes
SAx	Input	Synchronous address inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. All transactions operate on a burst-of-four words (two clock periods of bus activity). SA0 and SA1 are used as the lowest two address bits for burst READ and burst WRITE operations permitting a random burst start address on ×18 and ×36 devices. These inputs are ignored when device is deselected or once burst operation is in progress.	
/LD	Input	Synchronous load: This input is brought low when a bus cycle sequence is to be defined. This definition includes address and READ / WRITE direction. All transactions operate on a burst-of-four data (two clock periods of bus activity).	
R-/W	Input	Synchronous read / write Input: When /LD is low, this input designates the access type (READ when R-/W is high, WRITE when R-/W is low) for the loaded address. R-/W must meet the setup and hold times around the rising edge of K.	
/BWx	Input	Synchronous byte writes: When low, these inputs cause their respective byte to be registered and written during WRITE cycles. These signals must meet setup and hold times around the rising edges of K and /K for each of the two rising edges comprising the WRITE cycle. See Byte Write Truth Table for signal to data relationship.	
K, /K	Input	Input clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of /K. /K is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges. These balls cannot remain V_{REF} level.	
C, /C	Input	Output clock: This clock pair provides a user-controlled means of tuning device output data. The rising edge of /C is used as the output timing reference for first and third output data. The rising edge of C is used as the output timing reference for second and fourth output data. Ideally, /C is 180 degrees out of phase with C. C and /C may be tied high to force the use of K and /K as the output reference clocks instead of having to provide C and /C clocks. If tied high, C and /C must remain high and not to be toggled during device operation. These balls cannot remain V_{REF} level.	
/DOFF	Input	DLL disable: When low, this input causes the DLL to be bypassed for stable, low frequency operation.	
ZQ	Input	Output impedance matching input: This input is used to tune the device outputs to the system data bus impedance. DQ and CQ output impedance are set to 0.2 × RQ, where RQ is a resistor from this ball to ground. This ball can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This ball cannot be connected directly to V_{SS} or left unconnected.	
TMS TDI	Input	IEEE1149.1 test inputs: 1.8 V I/O levels. These balls may be left not connected if the JTAG function is not used in the circuit.	
TCK	Input	IEEE1149.1 clock input: 1.8 V I/O levels. This ball must be tied to V_{SS} if the JTAG function is not used in the circuit.	
DQ0 to DQn	Input/ output	Synchronous data I/Os: Input data must meet setup and hold times around the rising edges of K and /K. Output data is synchronized to the respective C and /C, or to the respective K and /K if C and /C are tied high. The ×9 device uses DQ0 to DQ8. Remaining signals are not used. The ×18 device uses DQ0 to DQ17. Remaining signals are not used. The ×36 device uses DQ0 to DQ35.	
CQ, /CQ	Output	Synchronous echo clock outputs: The edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals run freely and do not stop when DQ tristates.	
TDO	Output	IEEE 1149.1 test output: 1.8 V I/O level.	
V_{DD}	Supply	Power supply: 1.8 V nominal. See DC Characteristics and Operating Conditions for range.	
V_{DDQ}	Supply	Power supply: Isolated output buffer supply. Nominally 1.5 V. 1.8 V is also permissible. See DC Characteristics and Operating Conditions for range.	
V_{SS}	Supply	Power supply: Ground.	
V_{REF}	—	HSTL input reference voltage: Nominally V_{DDQ}/2, but may be adjusted to improve system noise margin. Provides a reference voltage for the HSTL input buffers.	

Name	I/O type	Descriptions	Notes
NC	—	No connect: These signals are not internally connected. These signals can be left floating or connected to ground to improve package heat dissipation.	

Notes: 1. All power supply and ground balls must be connected for proper operation of the device.

Block Diagram (R1Q5A3636B / R1Q5A3618B series)



General Description

Power-up and Initialization Sequence

The following supply voltage application sequence is recommended: V_{SS}, V_{DD}, V_{DDQ}, V_{REF} then V_{IN}.

After the stable power, there are three possible sequences.

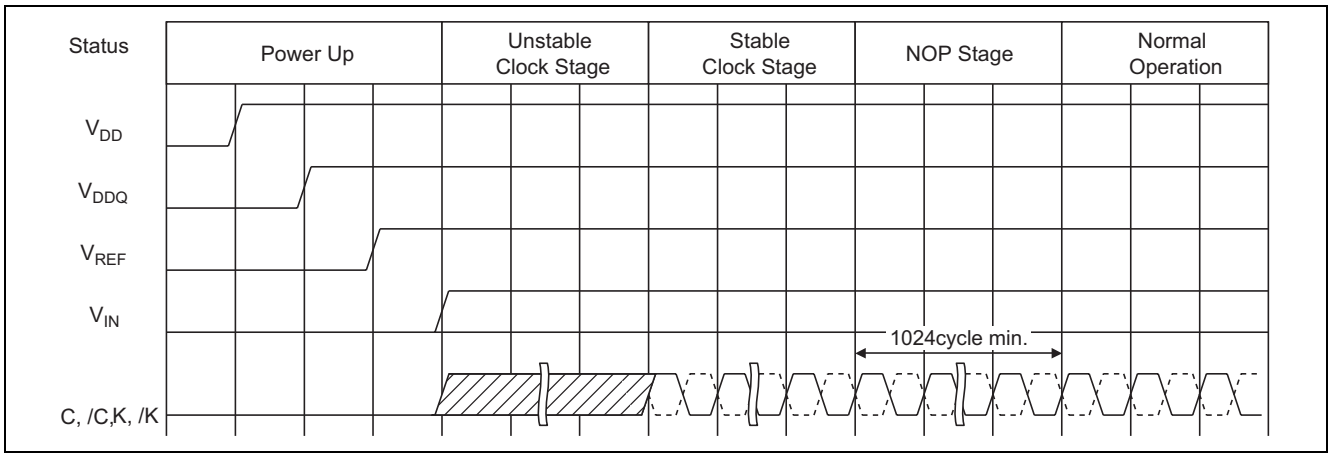
1. Sequence when DLL disable (/DOFF pin fixed low)
   Just after the stable power and clock (K, /K, C, /C), 1024 NOP cycles (min.) are required for all operations, including JTAG functions, to become normal.

2a. Sequence controlled by /DOFF pin when DLL enable Just after the stable power and clock (K, /K, C, /C), take /DOFF to be high.
   The additional 1024 NOP cycles (min.) are required to lock the DLL and for all operations to become normal.

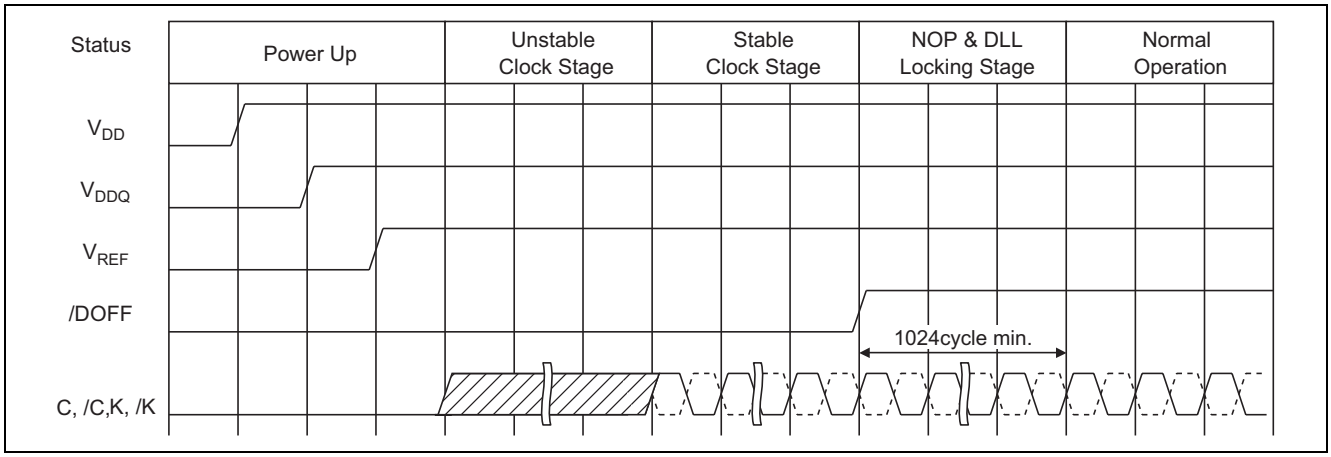
2b. Sequence controlled by Clock (/DOFF pin fixed high) when DLL enable If /DOFF pin is fixed high with unstable clock, the clock (K, /K, C, /C) must be stopped for 30ns (min.).
   During stop clock stage, C pin must tie low for 30ns (min.).C,/C,K and /K cannot remain V_{REF} level.
   The additional 1024 NOP cycles (min.) are required to lock the DLL and for all operations to become normal.

Notes: 1. After K or C clock is stopped, clock recovery cycles (1024 NOP cycles (min.)) are required for read/write operations to become normal.
2. When DLL is enable and the operating frequency is changed, DLL reset should be required again. After DLL reset again, the 1024 NOP cycles (min.) are needed to lock the DLL.

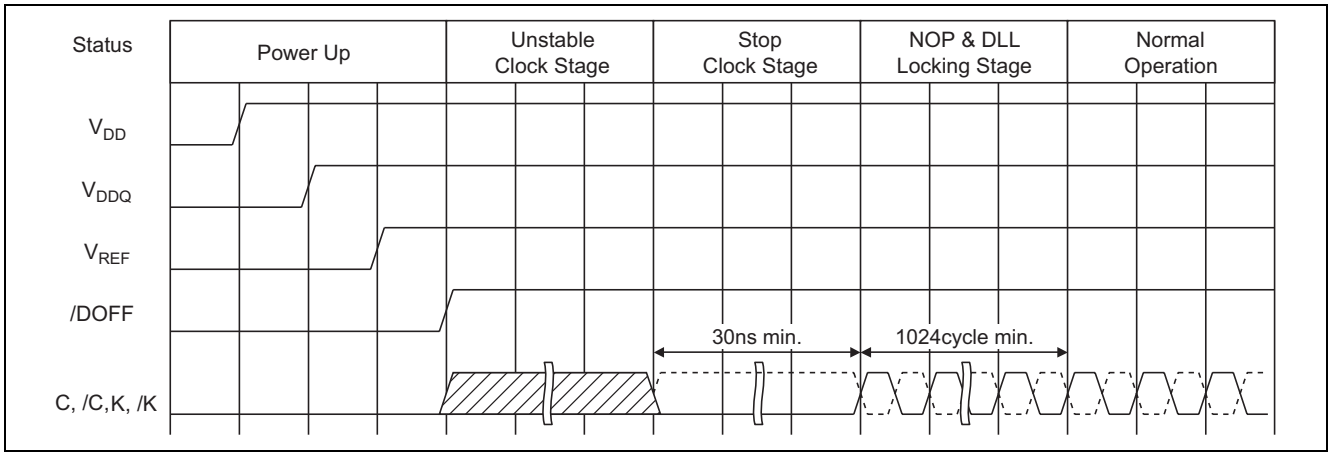
1. Sequence when DLL disable (/DOFF pin fixed low)



2a. Sequence controlled by /DOFF pin when DLL enable



2b. Sequence controlled by Clock (/DOFF pin fixed high) when DLL enable



DLL Constraints

1. DLL uses either K or C clock as its synchronizing input, the input should have low phase jitter which is specified as TKC var.
2. The lower end of the frequency at which the DLL can operate is 119MHz.

Programmable Output Impedance

1. Output buffer impedance can be programmed by terminating the ZQ ball to Vss through a precision resistor (RQ). The value of RQ is five times the output impedance desired. The allowable range of RQ to guarantee impedance matching with a tolerance of 10% is 250 Ω typical. The total external capacitance of ZQ ball must be less than 7.5 pF.

Burst Sequence
Linear Burst Sequence Table (R1Q5A3636B / R1Q5A3618B series)

	SA1, SA0	SA1, SA0	SA1, SA0	SA1, SA0	Notes
External address	0, 0	0, 1	1, 0	1, 1	
1st internal burst address	0, 1	1, 0	1, 1	0, 0	
2nd internal burst address	1, 0	1, 1	0, 0	0, 1	
3rd internal burst address	1, 1	0, 0	0, 1	1, 0	

K Truth Table

Operation	K	/R	/W	D or Q				
Write Cycle: Load address, input write data on consecutive K and /K rising edges	↑	L	L	Data in				
				Input data	D(A1)	D(A2)	D(A3)	D(A4)
				Output clock	K(t+1)↑	/K(t+1)↑	K(t+2)↑	/K(t+2)↑
Read Cycle: Load address, output read data on consecutive C and /C rising edges	↑	L	H	Data out				
				Output data	Q(A1)	Q(A2)	Q(A3)	Q(A4)
				Output clock	/C(t+1)↑	C(t+2)↑	/C(t+2)↑	C(t+3)↑
NOP (No operation)	↑	H	×	High-Z				
Standby (Clock stopped)	Stopped	×	×	Previous state				

Notes: 1. H: high level, L: low level, ×: don't care, ↑: rising edge.
2. Data inputs are registered at K and /K rising edges. Data outputs are delivered at C and /C rising edges, except if C and /C are high, then data outputs are delivered at K and /K rising edges.
3. /LD and R-/W must meet setup/hold times around the rising edges (low to high) of K and are registered at the rising edge of K.
4. This device contains circuitry that will ensure the outputs will be in high-Z during power-up.
5. Refer to state diagram and timing diagrams for clarification.
6. When clocks are stopped, the following cases are recommended; the case of K = low, /K = high, C = low and /C = high, or the case of K = high, /K = low, C = high and /C = low. This condition is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
7. A1 refers to the address input during a WRITE or READ cycle. A2, A3 and A4 refer to the 1st, 2nd and 3rd internal burst address, respectively, in accordance with the linear burst sequence.

Byte Write Truth Table (x36)

Operation	K	/K	/BW0	/BW1	/BW2	/BW3
Write D0 to D35	↑	—	L	L	L	L
	—	↑	L	L	L	L
Write D0 to D8	↑	—	L	H	H	H
	—	↑	L	H	H	H
Write D9 to D17	↑	—	H	L	H	H
	—	↑	H	L	H	H
Write D18 to D26	↑	—	H	H	L	H
	—	↑	H	H	L	H
Write D27 to D35	↑	—	H	H	H	L
	—	↑	H	H	H	L
Write nothing	↑	—	H	H	H	H
	—	↑	H	H	H	H

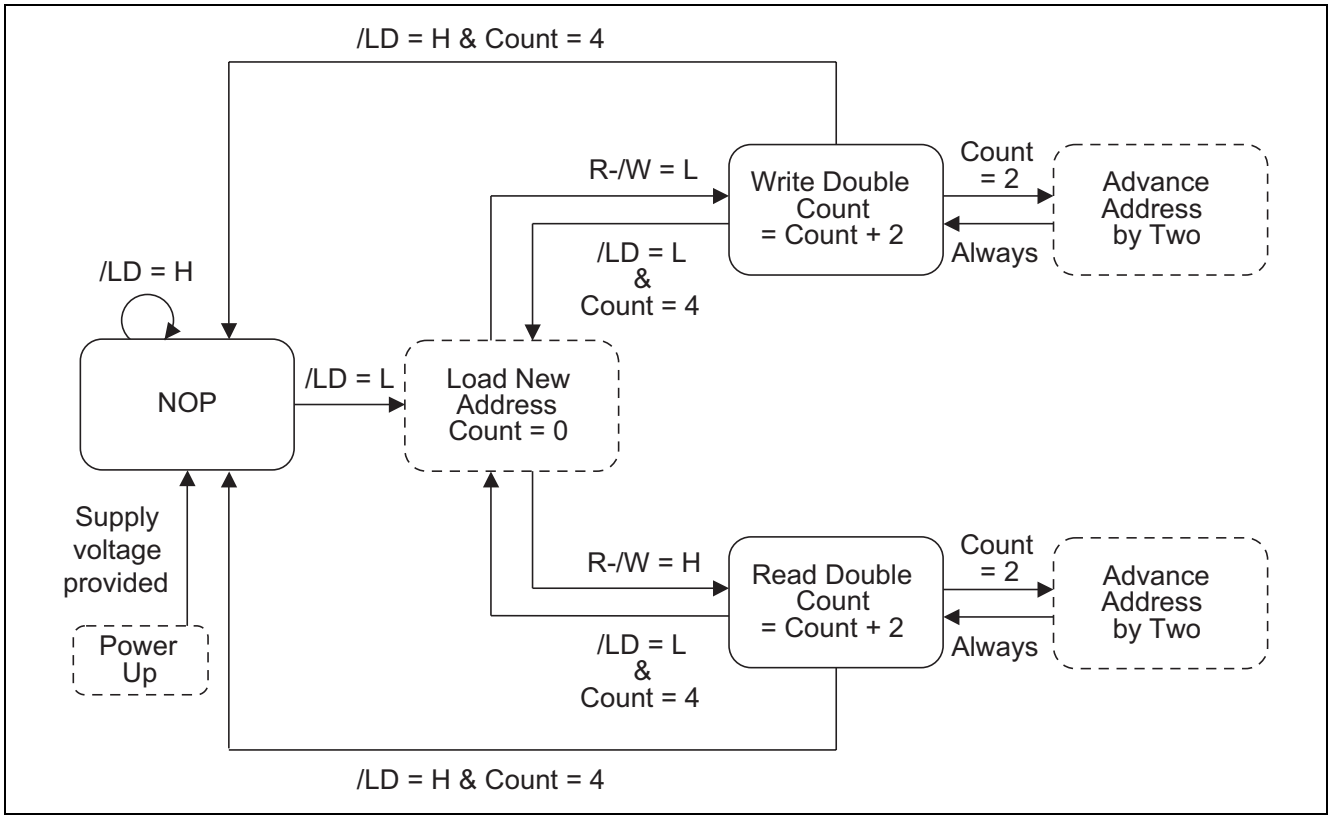
Notes: 1. H: high level, L: low level, ↑: rising edge.
2. Assumes a WRITE cycle was initiated. /BWx can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

Byte Write Truth Table (x18)

Operation	K	/K	/BW0	/BW1
Write D0 to D17	↑	—	L	L
	—	↑	L	L
Write D0 to D8	↑	—	L	H
	—	↑	L	H
Write D9 to D17	↑	—	H	L
	—	↑	H	L
Write nothing	↑	—	H	H
	—	↑	H	H

Notes: 1. H: high level, L: low level, ↑: rising edge.
2. Assumes a WRITE cycle was initiated. /BWx can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

Bus Cycle State Diagram



Notes: 1. SA0 and SA1 are internally advanced in accordance with the burst order table. Bus cycle is terminated at the end of this sequence (burst count = 4).
2. State machine control timing sequence is controlled by K.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Input voltage on any ball	V_{IN}	−0.5 to V_{DD} + 0.5 (2.5 V max.)	V	1, 4
Input/output voltage	$V_{I/O}$	−0.5 to V_{DDQ} + 0.5 (2.5 V max.)	V	1, 4
Core supply voltage	V_{DD}	−0.5 to 2.5	V	1, 4
Output supply voltage	V_{DDQ}	−0.5 to V_{DD}	V	1, 4
Junction temperature	Tj	+125 (max)	°C	
Storage temperature	T_{STG}	−55 to +125	°C	

Notes: 1. All voltage is referenced to V_{SS}.
2. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted the Operation Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
3. These CMOS memory circuits have been designed to meet the DC and AC specifications shown in the tables after thermal equilibrium has been established.
4. The following supply voltage application sequence is recommended: V_{SS}, V_{DD}, V_{DDQ}, V_{REF} then V_{IN}. Remember, according to the Absolute Maximum Ratings table, V_{DDQ} is not to exceed 2.5 V, whatever the instantaneous value of V_{DDQ}.

Recommended DC Operating Conditions

(Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Power supply voltage --core	V_{DD}	1.7	1.8	1.9	V	
Power supply voltage --I/O	V_{DDQ}	1.4	1.5	V_{DD}	V	
Input reference voltage --I/O	V_{REF}	0.68	0.75	0.95	V	1
Input high voltage	$V_{IH\ (DC)}$	V_{REF} + 0.1	—	V_{DDQ} + 0.3	V	2, 3
Input low voltage	$V_{IL\ (DC)}$	–0.3	—	V_{REF} – 0.1	V	2, 3

Notes: 1. Peak to peak AC component superimposed on V_{REF} may not exceed 5% of V_{REF}.
2. Overshoot: $V_{IH\ (AC)} \leq V_{DDQ}$ + 0.5 V for $t \leq t_{KHKH}/2$
Undershoot: $V_{IL\ (AC)} \geq$ –0.5 V for $t \leq t_{KHKH}/2$
Power-up: $V_{IH} \leq V_{DDQ}$ + 0.3 V and $V_{DD} \leq$ 1.7 V and $V_{DDQ} \leq$ 1.4 V for $t \leq$ 200 ms
During normal operation, V_{DDQ} must not exceed V_{DD}.
Control input signals may not have pulse widths less than t_{KHKL} (min) or operate at cycle rates less than t_{KHKH} (min).
During normal operation, $V_{IH(DC)}$ must not exceed V_{DDQ} and $V_{IL(DC)}$ must not be lower than V_{SS}.
3. These are DC test criteria. The AC V_{IH} / V_{IL} levels are defined separately to measure timing parameters.

DC Characteristics

(Ta = 0 to +70°C, V_{DD} = 1.8V ± 0.1V)

Parameter		Symbol	–33 Max	–40 Max	–50 Max	–60 Max	Unit	Notes
Operating supply current (READ / WRITE)	(×18)	I_{DD}	700	650	600	550	mA	1, 2, 3
	(×36)	I_{DD}	750	700	650	600	mA	1, 2, 3
Standby supply current (NOP)	×18 / ×36)	I_{SB1}	380	350	340	330	mA	2, 4, 5

Parameter	Symbol	Min	Max	Unit	Test conditions	Notes
Input leakage current	I_{LI}	–2	2	µA		10
Output leakage current	I_{LO}	–5	5	µA		11
Output high voltage	V_{OH} (Low)	V_{DDQ} –0.2	V_{DDQ}	V	$\|I_{OH}\| \le 0.1$ mA	8, 9
	V_{OH}	$V_{DDQ}/2$ –0.08	$V_{DDQ}/2$ +0.08	V	Note 6	8, 9
Output low voltage	V_{OL} (Low)	V_{SS}	0.2	V	$I_{OL} \le 0.1$ mA	8, 9
	V_{OL}	$V_{DDQ}/2$ –0.08	$V_{DDQ}/2$ +0.08	V	Note 7	8, 9

Notes: 1. All inputs (except ZQ, V_{REF}) are held at either V_{IH} or V_{IL}.
2. I_{OUT} = 0 mA. V_{DD} = V_{DD} max, t_{KHKH} = t_{KHKH} min.
3. Operating supply currents are measured at 100% bus utilization.
4. All address / data inputs are static at either $V_{IN} > V_{IH}$ or $V_{IN} < V_{IL}$.
5. Reference value (Condition=NOP currents are valid when entering NOP after all pending READ and WRITE cycles are completed.)
6. Outputs are impedance-controlled. $|I_{OH}| = (V_{DDQ}/2)/(RQ/5)$ for values of 175 Ω ≤ RQ ≤ 350 Ω.
7. Outputs are impedance-controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of 175 Ω ≤ RQ ≤ 350 Ω.
8. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
9. HSTL outputs meet JEDEC HSTL Class I standards.
10. $0 \le V_{IN} \le V_{DDQ}$ for all input balls (except V_{REF}, ZQ, TCK, TMS, TDI ball).
11. $0 \le V_{OUT} \le V_{DDQ}$ (except TDO ball), output disabled.

Thermal Resistance

Parameter	Symbol	Typ	Unit	Notes
Junction to Ambient	θ_{JA}	24.5	°C/W	
Junction to Case	θ_{JC}	5.6	°C/W	

Note: These parameters are calculated under the condition of wind velocity = 1 m/s.

Capacitance

(Ta = +25°C, f=1.0MHz, V_{DD} = 1.8V, V_{DDQ} = 1.5V)

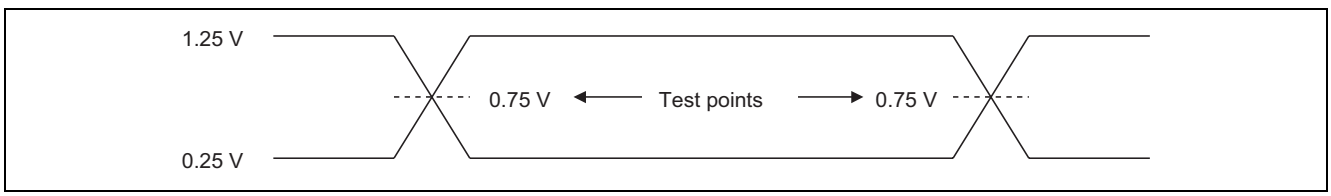
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
Input capacitance	C_{IN}	—	2	3	pF	V_{IN} = 0 V	1, 2
Clock input capacitance	C_{CLK}	—	2	3	pF	V_{CLK} = 0 V	1, 2
Input/output capacitance (D, Q, ZQ)	$C_{I/O}$	—	3	4.5	pF	$V_{I/O}$ = 0 V	1, 2

Notes: 1. These parameters are sampled and not 100% tested.
2. Except JTAG (TCK, TMS, TDI, TDO) pins.

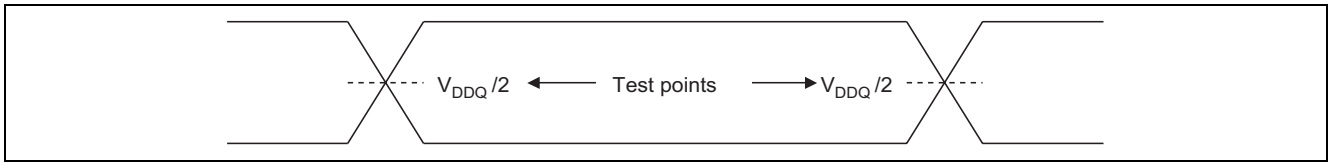
AC Test Conditions

(Ta = 0 to +70°C, V_{DD} = 1.8V ±0.1V)

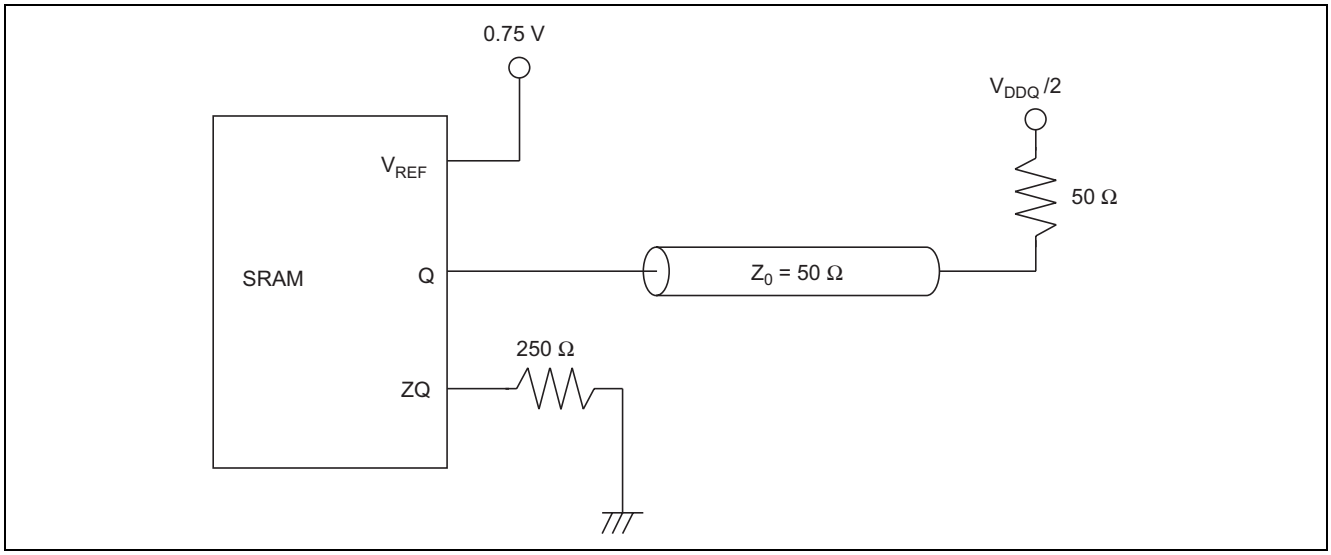
Input waveform (Rise/fall time ≤ 0.3 ns)



Output waveform



Output load condition



AC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	$V_{IH\ (AC)}$	V_{REF} + 0.2	—	—	V	1, 2, 3, 4
Input low voltage	$V_{IL\ (AC)}$	—	—	V_{REF} – 0.2	V	1, 2, 3, 4

Notes: 1. All voltages referenced to V_{SS} (GND).

2. These conditions are for AC functions only, not for AC parameter test.
3. Overshoot: $V_{IH\ (AC)} \leq V_{DDQ}$ + 0.5 V for $t \leq t_{KHKH}/2$
   Undershoot: $V_{IL\ (AC)} \geq -0.5$ V for $t \leq t_{KHKH}/2$
   Power-up: $V_{IH} \leq V_{DDQ}$ + 0.3 V and $V_{DD} \leq 1.7$ V and $V_{DDQ} \leq 1.4$ V for $t \leq 200$ ms
   During normal operation, V_{DDQ} must not exceed V_{DD}. Control input signals may not have pulse widths less than t_{KHKL} (min) or operate at cycle rates less than t_{KHKH} (min).
4. To maintain a valid level, the transitioning edge of the input must:
   a. Sustain a constant slew rate from the current AC level through the target AC level, $V_{IL\ (AC)}$ or $V_{IH\ (AC)}$.
   b. Reach at least the target AC level.
   c. After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL\ (DC)}$ or $V_{IH\ (DC)}$.

AC Characteristics

(Ta = 0 to +70°C, V_{DD} = 1.8V ± 0.1V)

Parameter	Symbol	-33		-40		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Average clock cycle time (K, /K, C, /C)	t_{KHKH}	3.30	8.40	4.00	8.40	5.00	8.40	6.00	8.40	ns	
Clock phase jitter (K, /K, C, /C)	t_{KC} var	—	0.20	—	0.20	—	0.20	—	0.20	ns	3
Clock high time (K, /K, C, /C)	t_{KHKL}	1.32	—	1.60	—	2.00	—	2.40	—	ns	
Clock low time (K, /K, C, /C)	t_{KLKH}	1.32	—	1.60	—	2.00	—	2.40	—	ns	
Clock to /clock (K to /K, C to /C)	$t_{KH/KH}$	1.49	—	1.80	—	2.20	—	2.70	—	ns	
/Clock to clock (/K to K, /C to C)	$t_{/KHKH}$	1.49	—	1.80	—	2.20	—	2.70	—	ns	
Clock to data clock (K to C, /K to /C)	t_{KHCH}	0	0.75	0	1.10	0	1.60	0	2.10	ns	
DLL lock time (K, C)	t_{KC} lock	1,024	—	1,024	—	1,024	—	1,024	—	Cycle	2
K static to DLL reset	t_{KC} reset	30	—	30	—	30	—	30	—	ns	7
C, /C high to output valid	t_{CHQV}	—	0.45	—	0.45	—	0.45	—	0.50	ns	
C, /C high to output hold	t_{CHQX}	-0.45	—	-0.45	—	-0.45	—	-0.50	—	ns	
C, /C high to echo clock valid	t_{CHCQV}	—	0.45	—	0.45	—	0.45	—	0.50	ns	
C, /C high to echo clock hold	t_{CHCQX}	-0.45	—	-0.45	—	-0.45	—	-0.50	—	ns	
CQ, /CQ high to output valid	t_{CQHQV}	—	0.27	—	0.30	—	0.35	—	0.40	ns	4, 7
CQ, /CQ high to output hold	t_{CQHQX}	-0.27	—	-0.30	—	-0.35	—	-0.40	—	ns	4, 7
C, /C high to output high-Z	t_{CHQZ}	—	0.45	—	0.45	—	0.45	—	0.50	ns	5

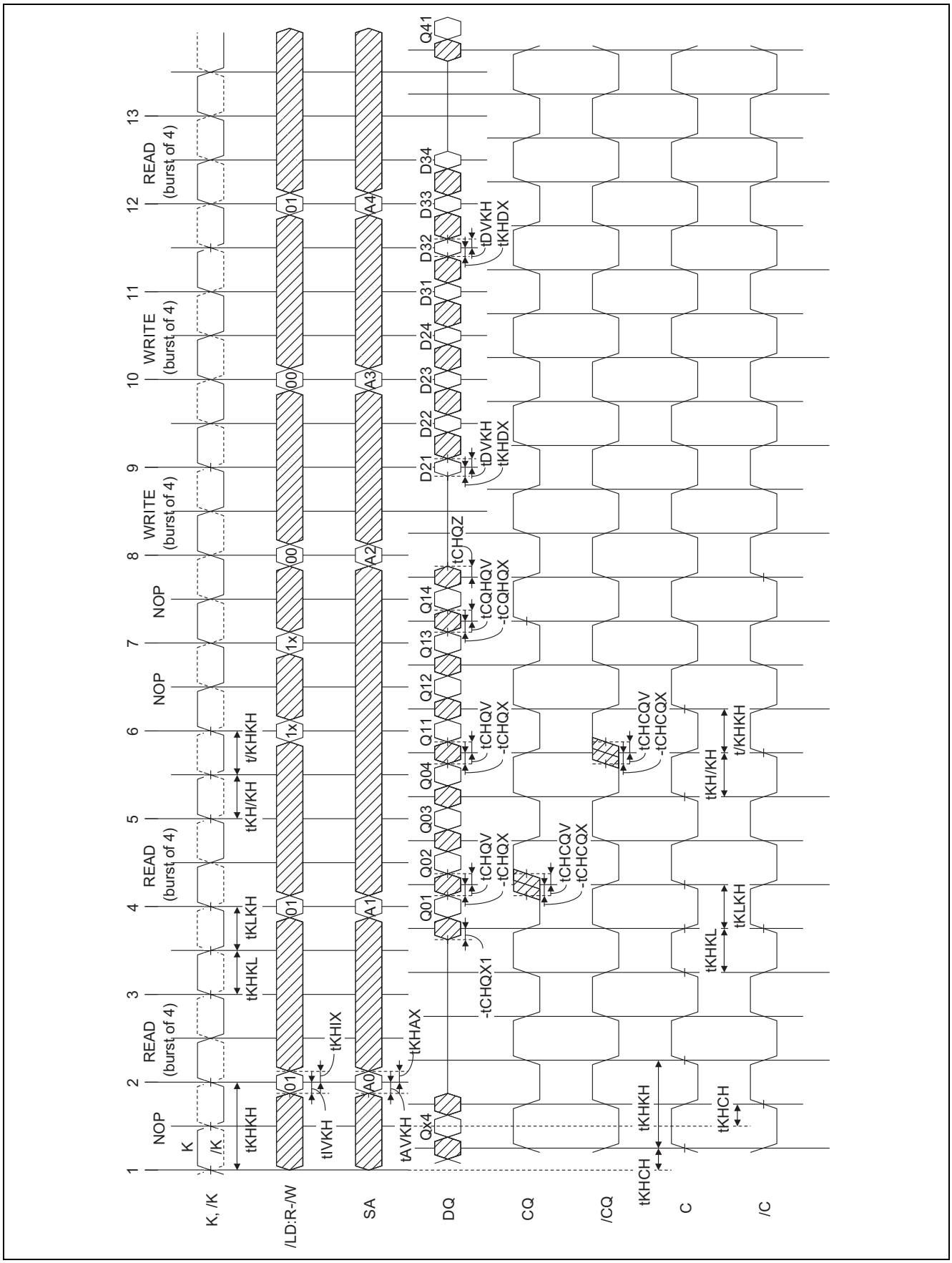
Parameter	Symbol	-33		-40		-50		-60		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
C, /C high to output low-Z	t_{CHQX1}	-0.45	—	-0.45	—	-0.45	—	-0.50	—	ns	5
Address valid to K rising edge	t_{AVKH}	0.40	—	0.50	—	0.60	—	0.70	—	ns	1
Control inputs valid to K rising edge	t_{IVKH}	0.40	—	0.50	—	0.60	—	0.70	—	ns	1
Data-in valid to K, /K rising edge	t_{DVKH}	0.30	—	0.35	—	0.40	—	0.50	—	ns	1
K rising edge to address hold	t_{KHAX}	0.40	—	0.50	—	0.60	—	0.70	—	ns	1
K rising edge to control inputs hold	t_{KHIX}	0.40	—	0.50	—	0.60	—	0.70	—	ns	1
K, /K rising edge to data-in hold	t_{KHDX}	0.30	—	0.35	—	0.40	—	0.50	—	ns	1

Notes:
1. This is a synchronous device. All addresses, data and control lines must meet the specified setup and hold times for all latching clock edges.
2. V_{DD} slew rate must be less than 0.1 V DC per 50 ns for DLL lock retention. DLL lock time begins once V_{DD} and input clock are stable. It is recommended that the device is kept inactive during these cycles.
3. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
4. Echo clock is very tightly controlled to data valid / data hold. By design, there is a ±0.1 ns variation from echo clock to data. The datasheet parameters reflect tester guardbands and test setup variations.
5. Transitions are measured ±100 mV from steady-state voltage.
6. At any given voltage and temperature t_{CHQZ} is less than t_{CHQX1} and t_{CHQZ} less than t_{CHQV}.
7. These parameters are sampled.

Remarks:
1. Test conditions as specified with the output loading as shown in AC Test Conditions unless otherwise noted.
2. Control input signals may not be operated with pulse widths less than t_{KHKL} (min).
3. If C, /C are tied high, K, /K become the references for C, /C timing parameters.
4. V_{DDQ} is +1.5 V DC.
5. Control signals are /LD, R-/W, /BW, /BW0, /BW1, /BW2 and /BW3.
   BWn signals must operate at the same timing as Data in.

Timing Waveforms

Read and Write Timing



Notes: 1. Q01 refers to output from address A0. Q02 refers to output from the next internal burst address following A0, etc.
2. Outputs are disable (high-Z) one clock cycle after a NOP.
3. In this example, if address A4 = A3, then data Q41 = D31, Q42 = D32, etc. Write data is forwarded immediately as read results.
4. To control read and write operations, /BW signals must operate at the same timing as Data in.
5. The second NOP cycle is not necessary for correct device operation; however, at high clock frequencies it may be required to prevent bus contention.

JTAG Specification

These products support a limited set of JTAG functions as in IEEE standard 1149.1.

Disabling the Test Access Port

It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1,and may be left unconnected. But they may also be tied to V_{DD} through a 1kΩ resistor.TDO should be left unconnected.

Test Access Port (TAP) Pins

Symbol I/O	Pin assignments	Description	Notes
TCK	2R	Test clock input. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.	
TMS	10R	Test mode select. This is the command input for the TAP controller state machine.	
TDI	11R	Test data input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction.	
TDO	1R	Test data output. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.	

Notes: The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held high for five rising edges of TCK. The TAP controller state is also reset on SRAM POWER-UP.

TAP DC Operating Characteristics

($Ta = 0$ to $+70°C$, $V_{DD} = 1.8V \pm 0.1V$)

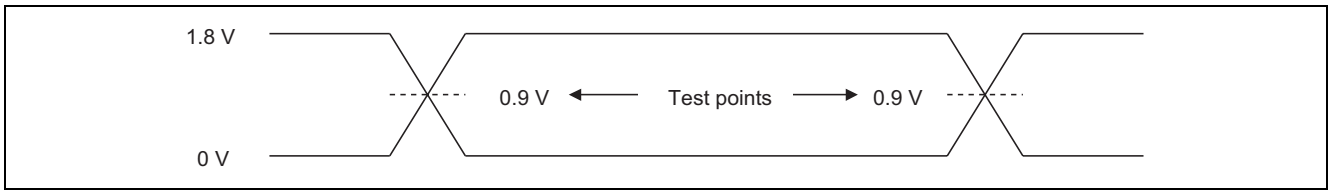
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	V_{IH}	+1.3	—	V_{DD} + 0.3	V	
Input low voltage	V_{IL}	–0.3	—	+0.5	V	
Input leakage current	I_{LI}	–5.0	—	+5.0	µA	$0 V \le V_{IN} \le V_{DD}$
Output leakage current	I_{LO}	–5.0	—	+5.0	µA	$0 V \le V_{IN} \le V_{DD}$, output disabled
Output low voltage	V_{OL1}	—	—	0.2	V	I_{OLC} = 100 µA
	V_{OL2}	—	—	0.4	V	I_{OLT} = 2 mA
Output high voltage	V_{OH1}	1.6	—	—	V	$\|I_{OHC}\|$ = 100 µA
	V_{OH2}	1.4	—	—	V	$\|I_{OHT}\|$ = 2 mA

Notes: 1. All voltages referenced to V_{SS} (GND).
2. Power-up: $V_{IH} \le V_{DDQ}$ + 0.3 V and $V_{DD} \le$ +1.7 V and $V_{DDQ} \le$ +1.4 V for $t \le 200$ ms.
3. In “EXTEST” mode and “SAMPLE” mode, V_{DDQ} is nominally 1.5 V.
4. ZQ: $V_{IH} = V_{DDQ}$.

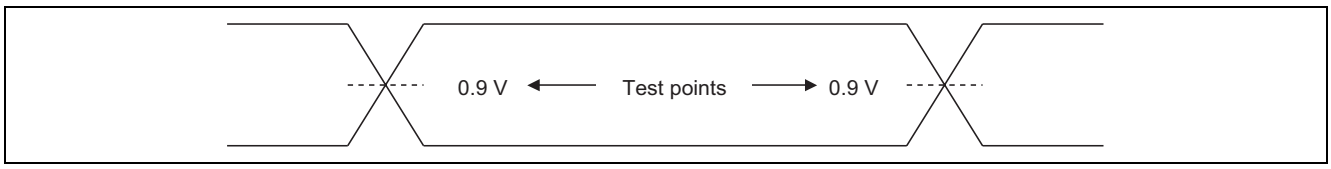
TAP AC Test Conditions

Parameter	Symbol	Conditions	Unit	Notes
Temperature	Ta	0 ≤ Ta ≤ +70	°C	
Input timing measurement reference levels	V_{REF}	0.9	V	
Input pulse levels	V_{IL}, V_{IH}	0 to 1.8	V	
Input rise/fall time	tr, tf	≤ 1.0	ns	
Output timing measurement reference levels		0.9	V	
Test load termination supply voltage (V_{TT})		0.9	V	
Output load		See figures		

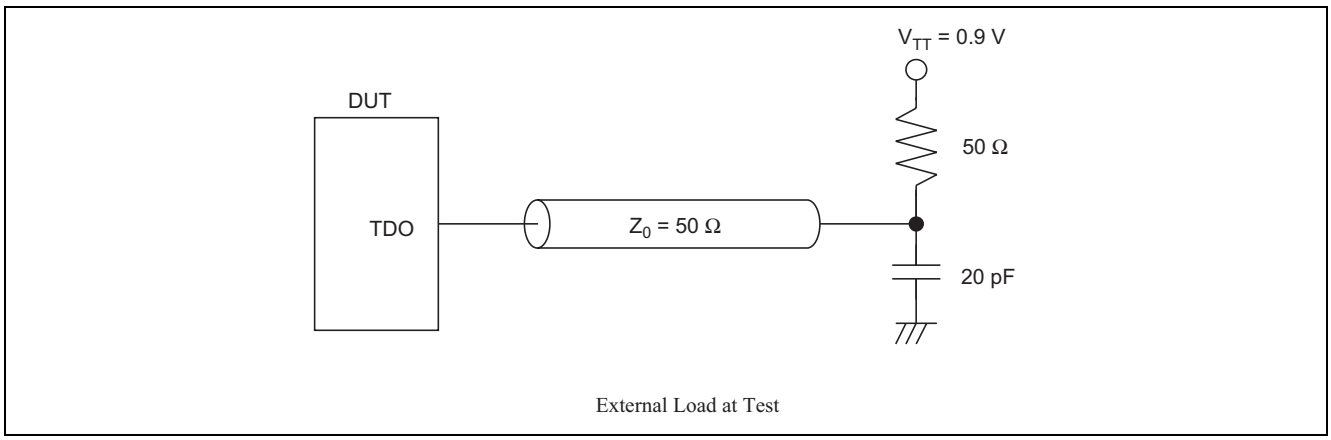
Input waveform



Output waveform



Output load condition



External Load at Test

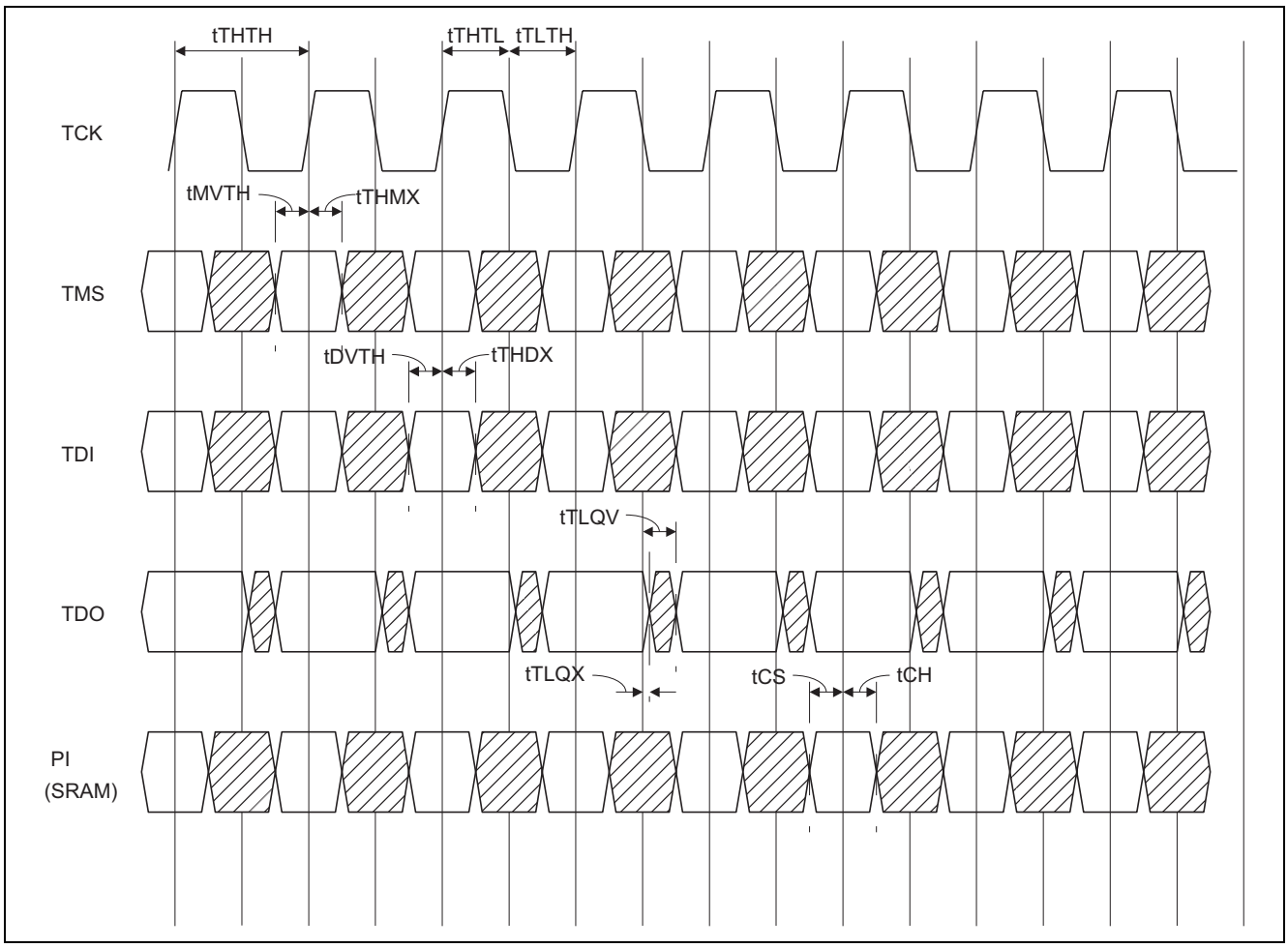
TAP AC Operating Characteristics

(Ta = 0 to +70°C, V_{DD} = 1.8V ±0.1V)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Test clock (TCK) cycle time	t_{THTH}	100	—	—	ns	
TCK high pulse width	t_{THTL}	40	—	—	ns	
TCK low pulse width	t_{TLTH}	40	—	—	ns	
Test mode select (TMS) setup	t_{MVTH}	10	—	—	ns	
TMS hold	t_{THMX}	10	—	—	ns	
Capture setup	t_{CS}	10	—	—	ns	1
Capture hold	t_{CH}	10	—	—	ns	1
TDI valid to TCK high	t_{DVTH}	10	—	—	ns	
TCK high to TDI invalid	t_{THDX}	10	—	—	ns	
TCK low to TDO unknown	t_{TLQX}	0	—	—	ns	
TCK low to TDO valid	t_{TLQV}	—	—	20	ns	

Notes: 1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure pad data capture.

TAP Controller Timing Diagram



Test Access Port Registers

Register name	Length	Symbol	Notes
Instruction register	3 bits	IR [2:0]	
Bypass register	1 bits	BP	
ID register	32 bits	ID [31:0]	
Boundary scan register	109 bits	BS [109:1]	

TAP Controller Instruction Set

IR2	IR1	IR0	Instruction	Description	Notes
0	0	0	EXTEST	The EXTEST instruction allows circuitry external to the component package to be tested. Boundary scan register cells at output balls are used to apply test vectors, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the Update-IR state of EXTEST, the output driver is turned on and the PRELOAD data is driven onto the output balls.	1, 2, 3
0	0	1	IDCODE	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO balls in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.	
0	1	0	SAMPLE-Z	If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z), moving the TAP controller into the capture-DR state loads the data in the RAMs input into the boundary scan register, and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.	3, 4
0	1	1	RESERVED	The RESERVED instructions are not implemented but are reserved for future use. Do not use these instructions.	
1	0	0	SAMPLE (/PRELOAD)	When the SAMPLE instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to SAMPLE metastable input will not harm the device, repeatable results cannot be expected. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO balls.	3
1	0	1	RESERVED		
1	1	0	RESERVED		
1	1	1	BYPASS	The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.	

Notes: 1. Data in output register is not guaranteed if EXTEST instruction is loaded.
2. After performing EXTEST, power-up conditions are required in order to return part to normal operation.
3. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.
4. Clock recovery initialization cycles are required to return from the SAMPLE-Z instruction.

Boundary Scan Order Boundary Scan Order

Bit #	Ball ID	Signal names	
		x18	x36
1	6R	/C	/C
2	6P	C	C
3	6N	SA	SA
4	7P	SA	SA
5	7N	SA	SA
6	7R	SA	SA
7	8R	SA	SA
8	8P	SA	SA
9	9R	SA	SA
10	11P	DQ0	DQ0
11	10P	DNU	DQ9
12	10N	DNU	DNU
13	9P	DNU	DNU
14	10M	DQ1	DQ11
15	11N	DNU	DQ10
16	9M	DNU	DNU
17	9N	DNU	DNU
18	11L	DQ2	DQ2
19	11M	DNU	DQ1
20	9L	DNU	DNU
21	10L	DNU	DNU
22	11K	DQ3	DQ3
23	10K	DNU	DQ12
24	9J	DNU	DNU
25	9K	DNU	DNU
26	10J	DQ4	DQ13
27	11J	DNU	DQ4
28	11H	ZQ	ZQ
29	10G	DNU	DNU
30	9G	DNU	DNU
31	11F	DQ5	DQ5
32	11G	DNU	DQ14
33	9F	DNU	DNU
34	10F	DNU	DNU
35	11E	DQ6	DQ6
36	10E	DNU	DQ15
37	10D	DNU	DNU
38	9E	DNU	DNU
39	10C	DQ7	DQ17
40	11D	DNU	DQ16
41	9C	DNU	DNU
42	9D	DNU	DNU
43	11B	DQ8	DQ8
44	11C	DNU	DQ7
45	9B	DNU	DNU
46	10B	DNU	DNU
47	11A	CQ	CQ
48	10A	SA	DNU
49	9A	SA	SA

Bit #	Ball ID	Signal names	
		x18	x36
50	8B	SA	SA
51	7C	SA1	SA1
52	6C	SA0	SA0
53	8A	/LD	/LD
54	7A	DNU	/BW1
55	7B	/BW0	/BW0
56	6B	K	K
57	6A	/K	/K
58	5B	DNU	/BW3
59	5A	/BW1	/BW2
60	4A	R-/W	R-/W
61	5C	SA	SA
62	4B	SA	SA
63	3A	SA	SA
64	2A	VSS	VSS
65	1A	/CQ	/CQ
66	2B	DQ9	DQ27
67	3B	DNU	DQ18
68	1C	DNU	DNU
69	1B	DNU	DNU
70	3D	DQ10	DQ19
71	3C	DNU	DQ28
72	1D	DNU	DNU
73	2C	DNU	DNU
74	3E	DQ11	DQ20
75	2D	DNU	DQ29
76	2E	DNU	DNU
77	1E	DNU	DNU
78	2F	DQ12	DQ30
79	3F	DNU	DQ21
80	1G	DNU	DNU
81	1F	DNU	DNU
82	3G	DQ13	DQ22
83	2G	DNU	DQ31
84	1H	/DOFF	/DOFF
85	1J	DNU	DNU
86	2J	DNU	DNU
87	3K	DQ14	DQ23
88	3J	DNU	DQ32
89	2K	DNU	DNU
90	1K	DNU	DNU
91	2L	DQ15	DQ33
92	3L	DNU	DQ24
93	1M	DNU	DNU
94	1L	DNU	DNU
95	3N	DQ16	DQ25
96	3M	DNU	DQ34
97	1N	DNU	DNU
98	2M	DNU	DNU

Bit #	Ball ID	Signal names	
		x18	x36
99	3P	DQ17	DQ26
100	2N	DNU	DQ35
101	2P	DNU	DNU
102	1P	DNU	DNU
103	3R	SA	SA
104	4R	SA	SA

Bit #	Ball ID	Signal names	
		x18	x36
105	4P	SA	SA
106	5P	SA	SA
107	5N	SA	SA
108	5R	SA	SA
109	—	INTERNAL	INTERNAL

Notes: In boundary scan mode,

1. Clock balls (K, /K, C, /C) are referenced to each other and must be at opposite logic levels for reliable operation.
2. CQ and /CQ data are synchronized to the respective C and /C (except EXTEST, SAMPLE-Z).
3. If C and /C tied high, CQ is generated with respect to K and /CQ is generated with respect to /K (except EXTEST, SAMPLE-Z).
4. ZQ must be driven to V_{DDQ} supply to ensure consistent results.

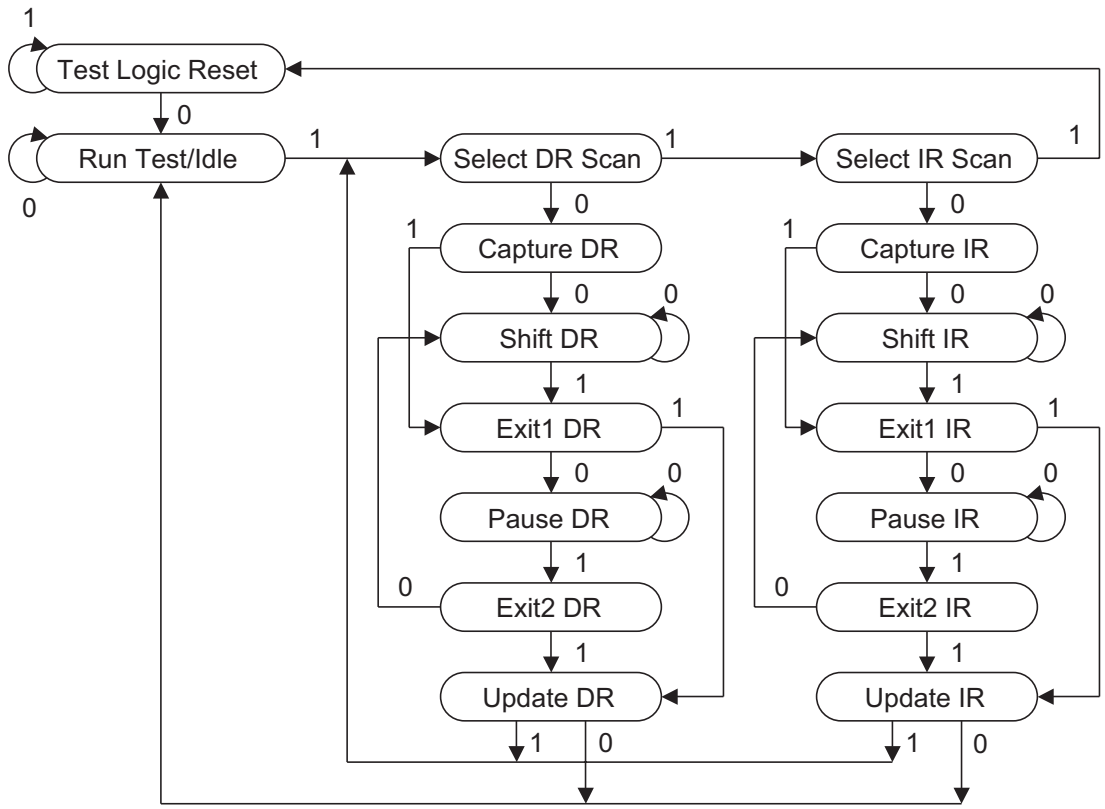
ID Register

Part	Revision number (31:29)	Type number (28:12)	Vendor JEDEC code (11:1)	Start bit (0)
—	—	0 0MMM 0WW0 10Q0 B0S0	—	—
R1Q5A3636B	000	0 0010 0110 1000 1000	0100 0100 011	1
R1Q5A3618B	000	0 0010 0100 1000 1000	0100 0100 011	1

Notes: 1. Type number

MMM	:Density	011:72Mb,	010:36Mb,	001:18Mb
WW	:Organization	11: x 36,	10: x 18,	00: x 9, 01: x 8
Q	:QDR/DDR	1: QDR,	0: DDR	
B	:Burst lengths	1: 4-word burst,	0: 2-word burst	
S	:I/O	1: Separate I/O,	0: Common I/O	

TAP Controller State Diagram Package Dimensions



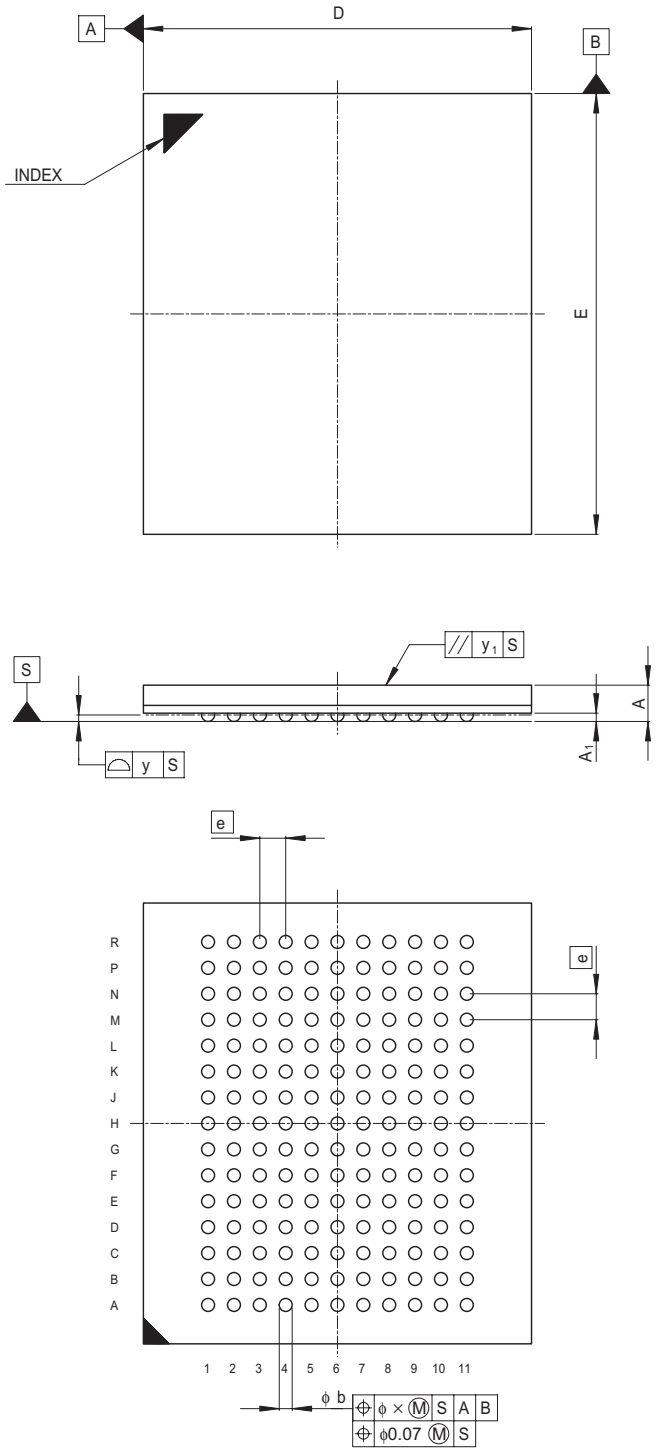
Notes: The value adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.

No matter what the original state of the controller, it will enter Test-Logic-Reset when TMS is held high for at least five rising edges of TCK.

Package Dimensions

R1Q5A3636B/R1Q5A3618B (PLBG0165FB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LBGA165-15x17-1.00	PLBG0165FB-A	BP-165A	0.7g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	14.90	15.00	15.10
E	16.90	17.00	17.10
v	——	——	——
w	——	——	——
A	1.34	1.40	1.46
A_1	0.27	0.32	0.37
e	——	1.00	——
b	0.45	0.50	0.55
x	——	——	0.20
y	——	——	0.15
y_1	——	——	0.25
S_D	——	——	——
S_E	——	——	——
Z_D	——	——	——
Z_E	——	——	——

Revision History	R1Q5A3636B/R1Q5A3618B Data Sheet

Rev.	Date	Contents of Modification	
		Page	Description
0.01	Jan.31, 2008	—	Initial issue
0.02	Mar.17,2008	P7 P13	DLL Constraints 2.the lower end of the frequency at which the DLL can operate is 119MHz AC characteristics Average clock cycle time is enlarged t_{KHKH}(-33)(max) 8.40ns, t_{KHKH}(-40)(max) 8.40ns, t_{KHKH}(-50)(max) 8.40ns, t_{KHKH}(-60)(max) 8.40ns
0.03	Apr.11,2008	P2	Ordering Infomatuon: Adding Part Number and Marking Name 1.Part Number (9) R: 1stGeneration,A: 2ndGeneration,B: 3rdGeneration (10:11) BG: Package type=BGA (12:13) 60: Cycle time=6.0 ns,50 : Cycle time=5.0 ns,40: Cycle time=4.0 ns 33: Cycle time=3.3 ns (14) R: Temperature range= 0°C ~70°C,I: Temperature range= -40°C ~85°C (15) B: Pb-free,T: Tape&Reel,S: Pb-free and Tape&Reel None: Standard (Pb and Tray) (16) 0 ~9 , A ~Z:Renesas internal use 2.Marking Name Marking Name(0:14) =Part Number (0:14) ----------Pb Marking Name(0:16) =Part Number (0:14)+Bx----------Pb-free (x=0 ~9 , A ~Z) (Example) R1Q5A3618BBG-60R ----------Pb R1Q5A3618BBG-60RB0 ----------Pb-free

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Colophon .7.2