PCS2P3805E

3.3V CMOS Dual 1-To-5 Clock Driver

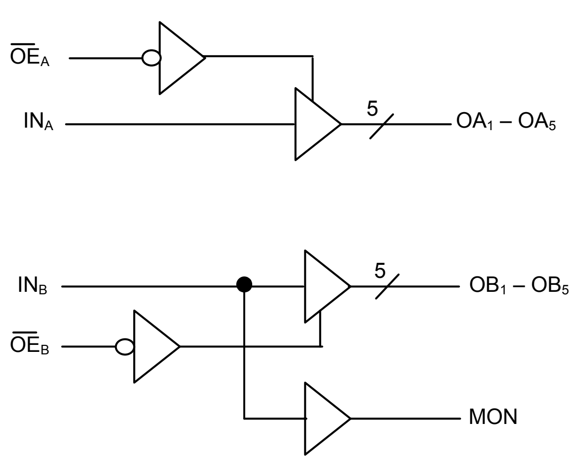
Features

- Advanced CMOS Technology
- Guaranteed low skew < 200pS (max)
- Very low propagation delay < 2.5nS (max)
- Very low duty cycle distortion < 270pS (max)
- Very low CMOS power levels
- Operating frequency up to 166MHz
- TTL compatible inputs and outputs
- Inputs can be driven from 3.3V or 5V components
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- "Heartbeat" monitor output
- V_{CC} = 3.3V ± 0.3V
- Available in SSOP and QSOP Packages

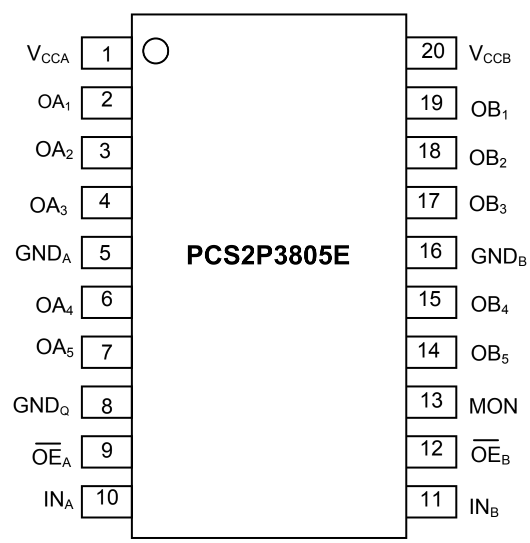
Functional Description

The PCS2P3805E is a 3.3V clock driver built using advanced CMOS technology. The device consists of two banks of drivers, each with a 1:5 fanout and its own output enable control. The device has a "heartbeat" monitor for diagnostics and PLL driving. The MON output is identical to all other outputs and complies with the output specifications in this document. The PCS2P3805E offers low capacitance inputs. The PCS2P3805E is designed for high speed clock distribution where signal quality and skew are critical. The PCS2P3805E also allows single point-to-point transmission line driving in applications such as address distribution, where one signal must be distributed to multiple receivers with low skew and high signal quality.

Block Diagram



Pin Diagram



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Pin Description

Pin #	Pin Names	Description
9,12	$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
10,11	IN_A, IN_B	Clock Inputs
2,3,4,6,7	OA_1-OA_5	Clock Outputs from Bank A
19,18,17,15,14	OB_1-OB_5	Clock Outputs from Bank B
1	V_{CCA}	Power supply for Bank A
20	V_{CCB}	Power supply for Bank B
5	GND_A	Ground for Bank A
16	GND_B	Ground for Bank B
8	GND_Q	Ground
13	MON	Monitor Output

Function Table[1]

Inputs		Outputs	
$\overline{OE}_A$, $\overline{OE}_B$	IN_A, IN_B	OA_n, OB_n	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

Note: 1 H = HIGH; L = LOW; Z = High-Impedance

Capacitance (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN}= 0V	3	4	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	-	6	pF

Note: 1 This parameter is measured at characterization but not tested.

Absolute Maximum Ratings[1]

Symbol	Description	Max	Unit
V_{CC}	Input Power Supply Voltage	-0.5 to +4.6	V
V_I	Input Voltage	-0.5 to +5.5	V
V_O	Output Voltage	-0.5 to V_{CC}+0.5	V
T_J	Junction Temperature	150	° C
T_{STG}	Storage Temperature	-65 to +165	° C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: 1 These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

DC Electrical Characteristics over Operating Range

Following Conditions Apply Unless Otherwise Specified
Industrial: T_A = -40°C to +85°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions[1]		Min	Typ[2]	Max	Unit
V_{IH}	Input HIGH Level			2	-	5.5	V
V_{IL}	Input LOW Level			-0.5	-	0.8	V
I_{IH}	Input HIGH Current	V_{CC}= Max.	V_I = 5.5V	-	-	±1	µA
I_{IL}	Input LOW Current	V_{CC}= Max.	V_I = GND	-	-	±1	µA
I_{OZH}	High Impedance Output Current (3-State Outputs Pins)	V_{CC}= Max.	V_O = V_{CC}	-	-	±1	µA
I_{OZL}	High Impedance Output Current (3-State Outputs Pins)	V_{CC}= Max.	V_O = GND	-	-	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC}= Min., I_{IN} = –18mA		-	-0.7	-1.2	V
I_{ODH}	Output HIGH Current	V_{CC}= 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3,4]		-45	-74	-180	mA
I_{ODL}	Output LOW Current	V_{CC}= 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3,4]		50	90	200	mA
I_{OS}	Short Circuit Current	V_{CC}= Max., V_O = GND[3,4]		-60	-135	-240	mA
V_{OH}	Output HIGH Voltage	V_{CC}= Min. V_{IN} = V_{IH} or V_{IL}	I_{OL}= 12mA	2.4[5]	3	-	V
			I_{OH}= –8mA	2.4[5]	3	-	V
			I_{OH}= –100µA	V_{CC} - 0.2	-	-	V
V_{OL}	Output LOW Voltage	V_{CC}= Min. V_{IN} = V_{IH} or V_{IL}	I_{OL}= 12mA	-	0.3	0.4	V
			I_{OL}= 8mA	-	0.2	0.4	V
			I_{OL}= 100µA	-	-	0.2	V

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, 25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} -0.6V at rated current.

Power Supply Characteristics

Symbol	Parameter	Test Conditions[1]		Min	Typ[2]	Max	Unit
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		-	0.1	30	µA
ΔI_{CC}	Power Supply Current per Input HIGH	V_{CC} = Max. V_{IN} = V_{CC} –0.6V		-	45	300	µA
I_{CCD}	Dynamic Power Supply Current per Output[3]	V_{CC}= Max. C_L= 15pF All Outputs Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	80	120	µA/MHz
I_C	Total Power Supply Current[4]	V_{CC}= Max. C_L= 15pF All Outputs Toggling f_i = 133MHz	V_{IN} = V_{CC} V_{IN} = GND	-	210	240	mA
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	-	210	240	
		V_{CC}= Max. C_L= 15pF All Outputs Toggling f_i = 166MHz	V_{IN} = V_{CC} V_{IN} = GND	-	260	310	
			V_{IN} = V_{CC} –0.6V V_{IN}= GND	-	260	310	

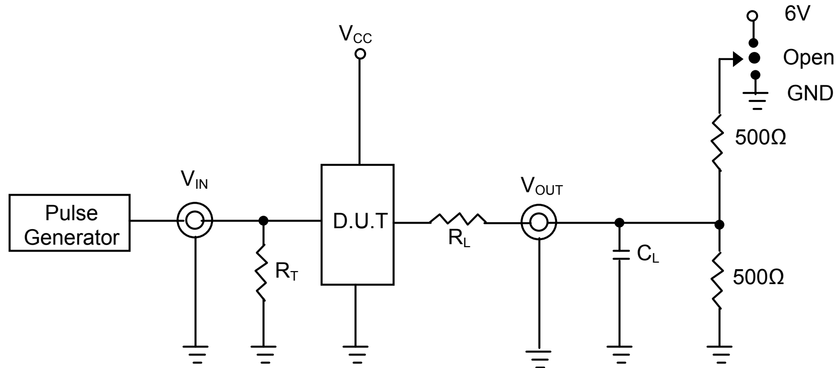
Notes:
1. For conditions shown as Max or Min, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. I_C = IQUIESCENT + IINPUTS + IDYNAMIC
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_O N_O)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = V_{CC} -0.6V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_O = Output Frequency
   NO = Number of Outputs at f_O

Switching Characteristics Over Operating Range – PCS2P3805E[3,4]

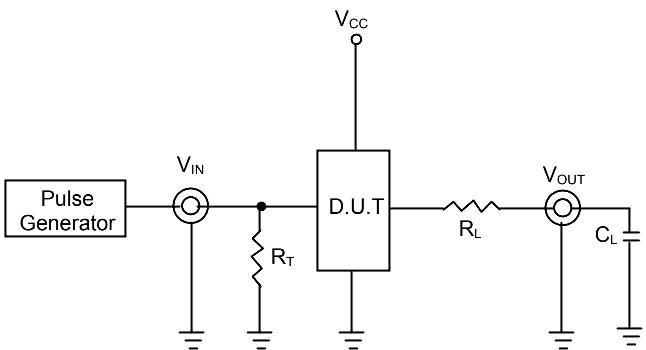
Symbol	Parameter	Conditions[1,8]	Min[2]	Max	Unit
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_n, INB to OB_n	C_L= 15pF f ≤166MHz	0.5	2.5	nS
t_R	Output Rise Time (Measured from 0.7V to 1.7V)		-	1	nS
t_F	Output Fall Time (Measured from 1.7V to 0.7V)		-	1	nS
$t_{SK(O)}$	Same device output pin to pin skew[5]		-	200	pS
$t_{SK(P)}$	Pulse skew[6,9]		-	270	pS
$t_{SK(PP)}$	Part to part skew[7]		-	550	pS
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		-	5.2	nS
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		-	5.2	nS
f_{MAX}	Input Frequency		-	166	MHz

Notes:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH} , t_{PHL} and $t_{SK(O)}$ are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min and Max limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.
5. Skew measured between all outputs under identical transitions and load conditions.
6. Skew measured is difference between propagation delay times t_{PHL} and t_{PLH} of same outputs under identical load conditions.
7. Part to part skew for all outputs given identical transitions and load conditions at identical V_{CC} levels and temperature.
8. Airflow of 1m/s is recommended for frequencies above 133MHz.
9. This parameter is measured using f = 1MHz.

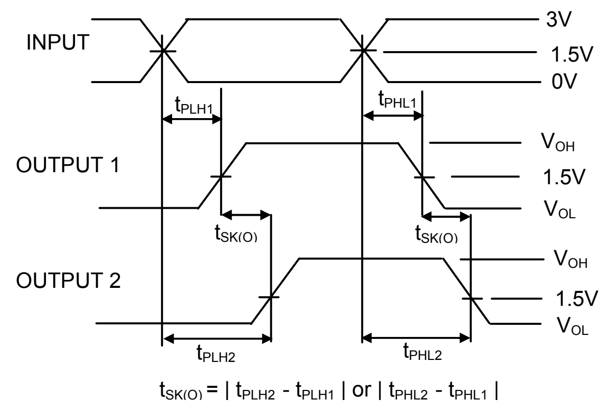
Test Circuits and Waveforms



Enable and Disable Time Circuit



C_L = 15pF Test Circuit



$t_{SK(O)} = | t_{PLH2} - t_{PLH1} |$ or $| t_{PHL2} - t_{PHL1} |$

Output Skew – $t_{SK(o)}$

Switch Position

Test	Switch
Disable Low Enable Low	6V
Disable High Enable High	GND

Test Conditions

Symbol	V_{CC} = 3.3V ±0.3V	Unit
C_L	15	pF
R_T	Z_{OUT} of pulse generator	Ω
R_L	33	Ω
t_R / t_F	1 (0V to 3V or 3V to 0V)	nS

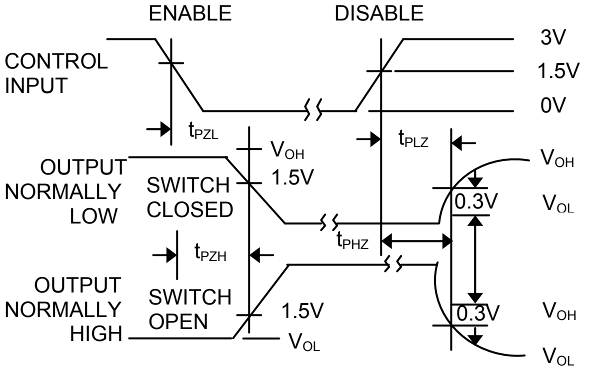
Definitions:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

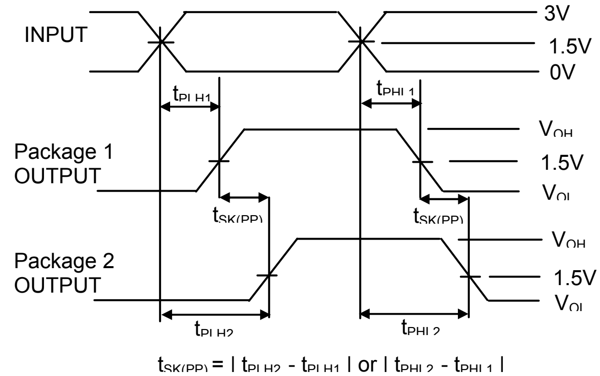
t_R / t_F = Rise/Fall time of the input stimulus from the Pulse Generator.

Test Circuits and Waveforms



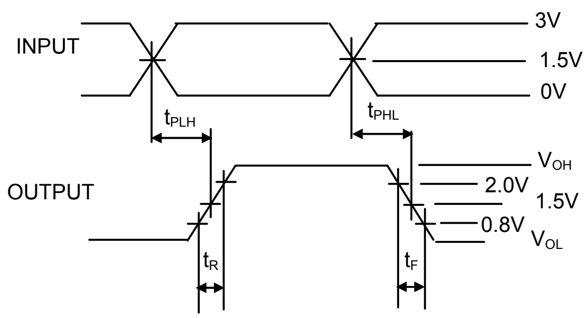
Enable and Disable Times

Note: 1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH

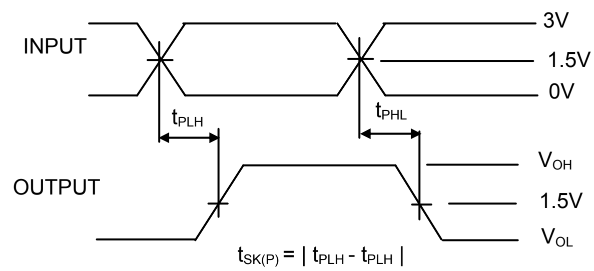


Part-to- Part Skew

Note: Part-to- Part Skew is for package and speed grade.



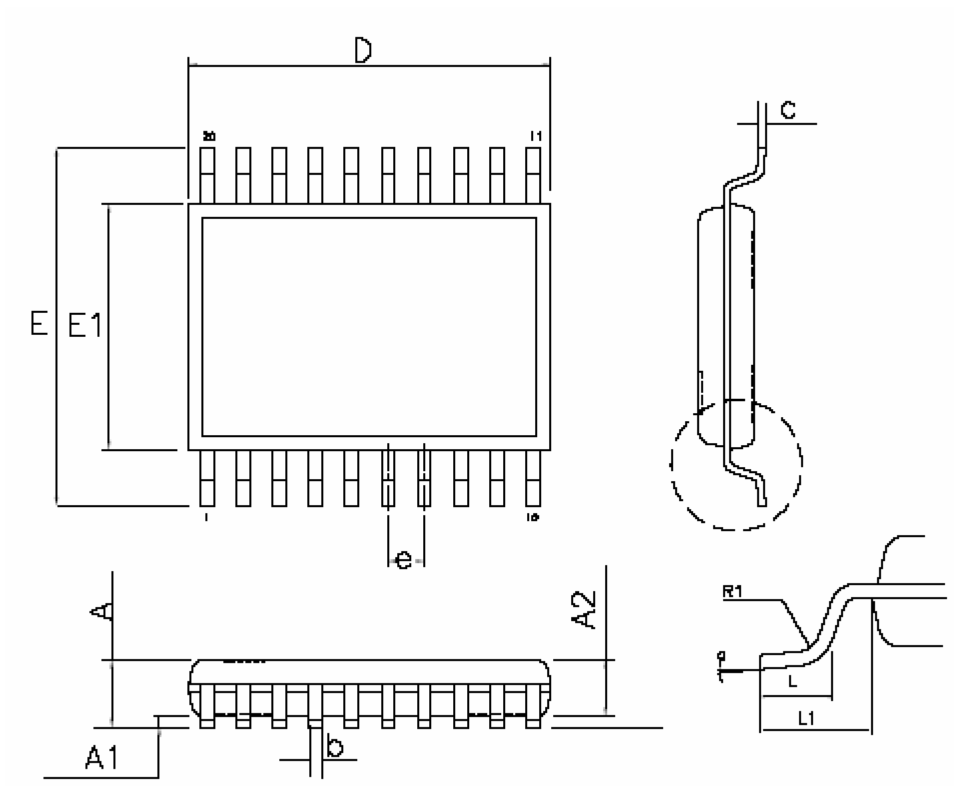
Propagation Delay



Pulse Skew

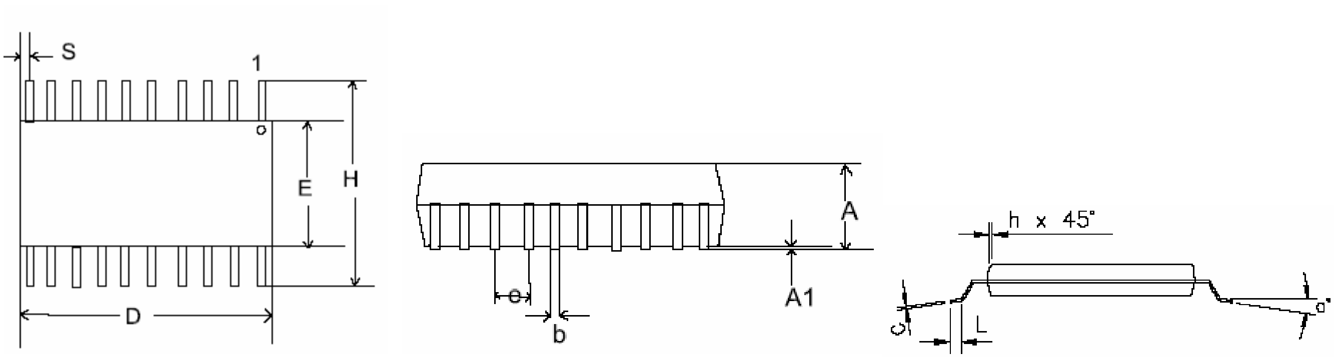
Package Information

20-lead SSOP (209 mil)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	….	0.079	…	2.0
A1	0.002	…	0.05	…..
A2	0.065	0.073	1.65	1.85
D	0.275	0.291	7.00	7.40
c	0.004	0.010	0.09	0.25
E	0.295	0.319	7.50	8.10
E1	0.197	0.220	5.00	5.60
L	0.021	0.037	0.55	0.95
L1	0.050 REF		1.25 REF	
b	0.009	0.015	0.22	0.38
R1	0.004	….	0.09	….
a	0°	8°	0°	8°
e	0.0197 BASE		0.65 BASE	

20-lead QSOP

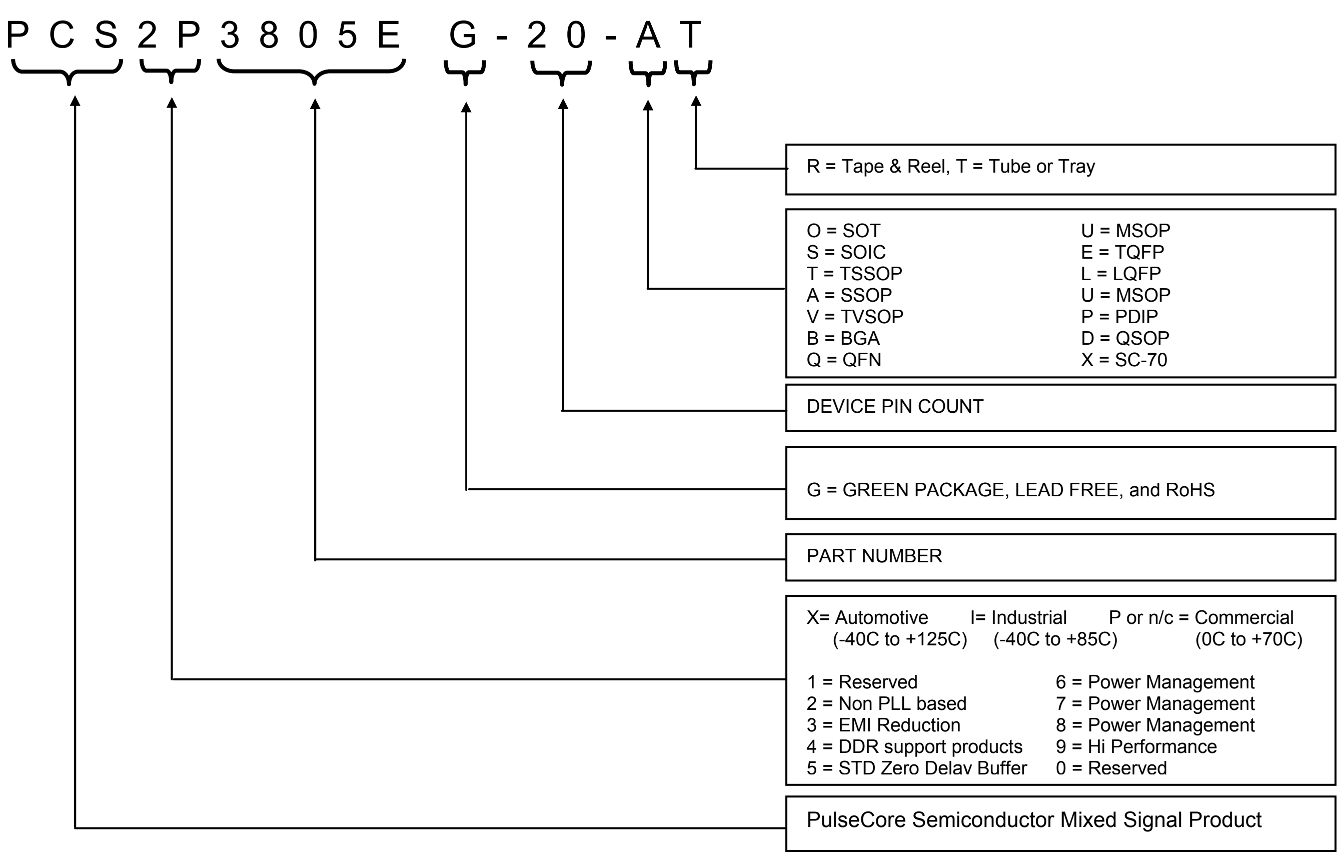


Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.060	0.068	1.52	1.73
A1	0.004	0.008	0.10	0.20
b	0.009	0.012	0.23	0.30
c	0.007	0.010	0.18	0.25
D	0.337	0.344	8.56	8.74
E	0.150	0.157	3.81	3.99
e	0.025 BSC		0.64 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
S	0.056	0.060	1.42	1.52
a	0°	8°	0°	8°

Ordering Information

Part Number	Marking	Package Type	Temperature
PCS2P3805EG-20-AR	2P3805EG	20-Pin SSOP, TAPE & REEL, Green	Commercial
PCS2P3805EG-20-AT	2P3805EG	20-Pin SSOP, TUBE, Green	Commercial
PCS2P3805EG-20-DR	2P3805EG	20-Pin QSOP, TAPE & REEL, Green	Commercial
PCS2P3805EG-20-DT	2P3805EG	20-Pin QSOP, TUBE, Green	Commercial
PCS2I3805EG-20-AR	2I3805EG	20-Pin SSOP, TAPE & REEL, Green	Industrial
PCS2I3805EG-20-AT	2I3805EG	20-Pin SSOP, TUBE, Green	Industrial
PCS2I3805EG-20-DR	2I3805EG	20-Pin QSOP, TAPE & REEL, Green	Industrial
PCS2I3805EG-20-DT	2I3805EG	20-Pin QSOP, TUBE, Green	Industrial

Device Ordering Information



Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.

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Preliminary Information
Part Number: PCS2P3805E
Document Version: 0.3

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003