Mobile SDRAM

512K x 16Bit x 2Banks
Mobile Synchronous DRAM

FEATURES

- 1.8V power supply
- LVCMOS compatible with multiplexed address
- Dual banks operation
- MRS cycle with address key programs
  - CAS Latency (2 & 3)
  - Burst Length (1, 2, 4, 8 & full page)
  - Burst Type (Sequential & Interleave)
- EMRS cycle with address key programs.
- All inputs are sampled at the positive going edge of the system clock
- Burst Read Single-bit Write operation
- Special Function Support.
  - PASR (Partial Array Self Refresh)
  - TCSR (Temperature compensated Self Refresh)
  - DS (Driver Strength)
- DQM for masking
- Auto & self refresh
- 32ms refresh period (2K cycle)

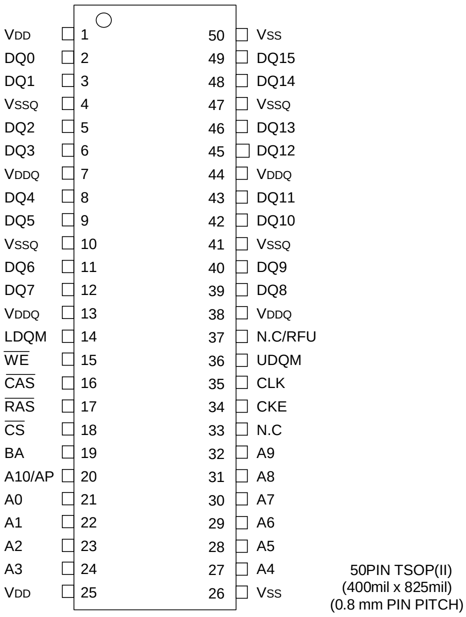
GENERAL DESCRIPTION

The M52D16161A is 16,777,216 bits synchronous high data rate Dynamic RAM organized as 2 x 524,288 words by 16 bits, fabricated with high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

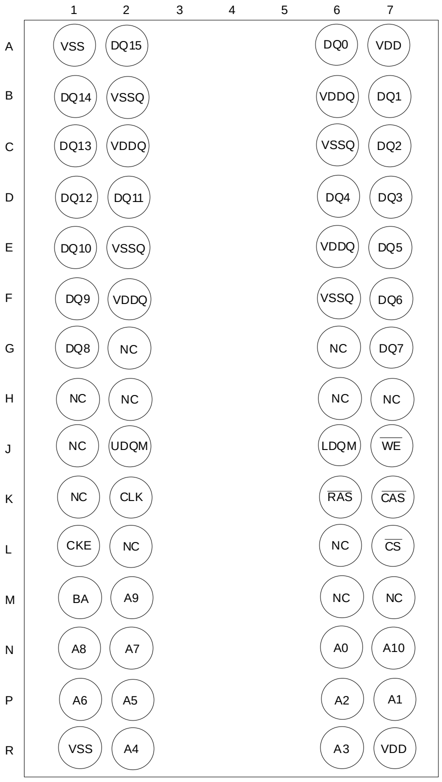
Product ID	Max Freq.	Package	Comments
M52D16161A-6TIG	166MHz	50 Pin TSOP(II)	Pb-free
M52D16161A-7.5TIG	133MHz	50 Pin TSOP(II)	Pb-free
M52D16161A-10TIG	100MHz	50 Pin TSOP(II)	Pb-free
M52D16161A-6BIG	166MHz	60 Ball VFBGA	Pb-free
M52D16161A-7.5BIG	133MHz	60 Ball VFBGA	Pb-free
M52D16161A-10BIG	100MHz	60 Ball VFBGA	Pb-free

PIN CONFIGURATION (TOP VIEW)



Signal	Pin	Pin	Signal
VDD	1	50	VSS
DQ0	2	49	DQ15
DQ1	3	48	DQ14
VSSQ	4	47	VSSQ
DQ2	5	46	DQ13
DQ3	6	45	DQ12
VDDQ	7	44	VDDQ
DQ4	8	43	DQ11
DQ5	9	42	DQ10
VSSQ	10	41	VSSQ
DQ6	11	40	DQ9
DQ7	12	39	DQ8
VDDQ	13	38	VDDQ
LDQM	14	37	N.C/RFU
$\overline{WE}$	15	36	UDQM
$\overline{CAS}$	16	35	CLK
$\overline{RAS}$	17	34	CKE
$\overline{CS}$	18	33	N.C
BA	19	32	A9
A10/AP	20	31	A8
A0	21	30	A7
A1	22	29	A6
A2	23	28	A5
A3	24	27	A4
VDD	25	26	VSS

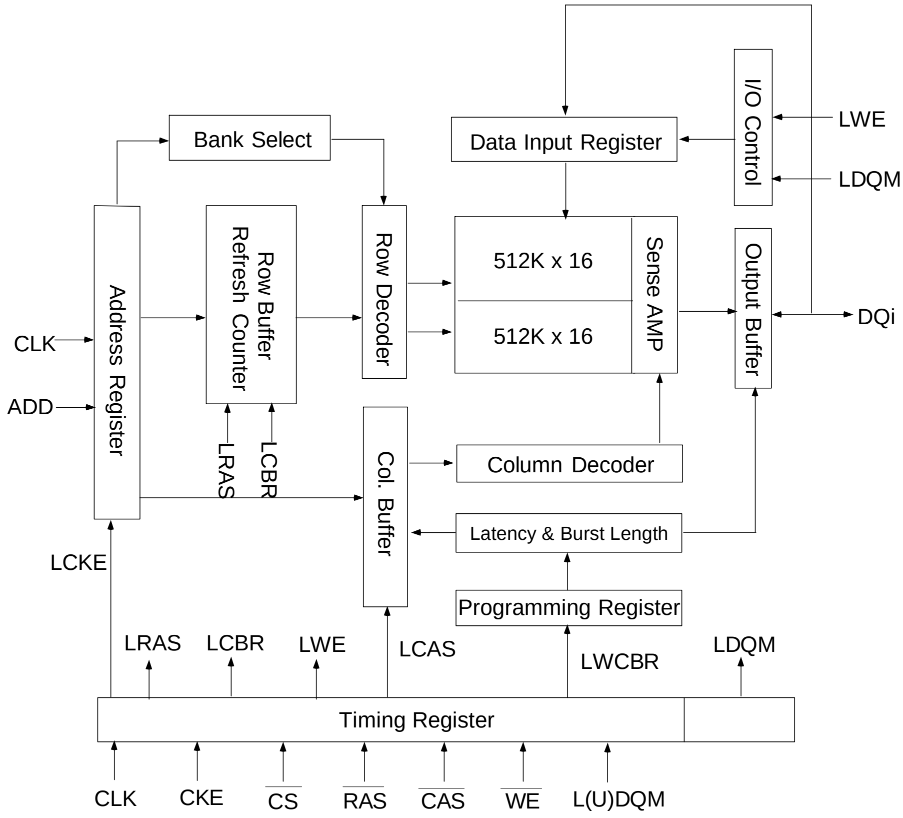
50PIN TSOP(II)
(400mil x 825mil)
(0.8 mm PIN PITCH)



	1	2	3	4	5	6	7
A	VSS	DQ15				DQ0	VDD
B	DQ14	VSSQ				VDDQ	DQ1
C	DQ13	VDDQ				VSSQ	DQ2
D	DQ12	DQ11				DQ4	DQ3
E	DQ10	VSSQ				VDDQ	DQ5
F	DQ9	VDDQ				VSSQ	DQ6
G	DQ8	NC				NC	DQ7
H	NC	NC				NC	NC
J	NC	UDQM				LDQM	$\overline{WE}$
K	NC	CLK				$\overline{RAS}$	$\overline{CAS}$
L	CKE	NC				NC	$\overline{CS}$
M	BA	A9				NC	NC
N	A8	A7				A0	A10
P	A6	A5				A2	A1
R	VSS	A4				A3	VDD

60 Ball VFBGA
(6.4x10.1mm)
(0.65mm ball pitch)

FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM.
CKE	*Clock Enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A10/AP	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, column address : CA0 ~ CA7
BA	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, $\overline{\text{WE}}$ active.
L(U)DQM	*Data Input / Output Mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when L(U)DQM active.

DQ0 ~ 15	*Data Input / Output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	*Data Output Power/Ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No Connection/ Reserved for Future Use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1.0 ~ 2.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD},V_{DDQ}	-1.0 ~ 2.6	V
Storage temperature	T_{STG}	-55 ~ + 150	°C
Power dissipation	P_D	0.7	W
Short circuit current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A= -40 °C ~ 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD},V_{DDQ}	1.7	1.8	1.9	V	
Input logic high voltage	V_{IH}	0.8 x V_{DDQ}	1.8	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.3	V	2
Output logic high voltage	V_{OH}	V_{DDQ} - 0.2	-	-	V	I_{OH} =-0.1mA
Output logic low voltage	V_{OL}	-	-	0.2	V	I_{OL} = 0.1mA
Input leakage current	I_{IL}	-10	-	10	uA	3
Output leakage current	I_{OL}	-10	-	10	uA	4

Note: 1.V_{IH} (max) = 2.2V AC for pulse width ≤ 3ns acceptable.
2.V_{IL} (min) = -1.0V AC for pulse width ≤ 3ns acceptable.
3.Any input 0V ≤ V_{IN} ≤ V_{DDQ}, all other pins are not under test = 0V.
4.Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (V_{DD} = 1.8V, T_A = 25 °C , f = 1MHz)

Pin	Symbol	Min	Max	Unit
CLOCK	C_{CLK}	2.0	4.0	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, LDQM, UDQM	C_{IN}	2.0	4.0	pF
ADDRESS	C_{ADD}	2.0	4.0	pF
DQ0 ~DQ15	C_{OUT}	3.5	6.0	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = -40 °C ~ 85 °C)

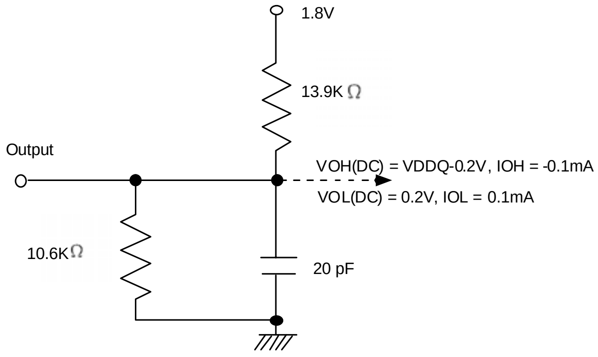
<table>
<tr><th rowspan="2">Parameter</th><th rowspan="2">Symbol</th><th rowspan="2" colspan="2">Test Condition</th><th colspan="6">Version</th><th rowspan="2">Unit</th><th rowspan="2">Note</th></tr>
<tr><th colspan="2">-6</th><th colspan="2">-7.5</th><th colspan="2">-10</th></tr>
<tr><td>Operating Current
(One Bank Active)</td><td>I_{CC1}</td><td colspan="2">Burst Length = 1
$t_{RC} \geq t_{RC}$ (min), $t_{CC} \geq t_{CC}$ (min), I_{OL}= 0mA</td><td colspan="2">50</td><td colspan="2">45</td><td colspan="2">40</td><td>mA</td><td>1</td></tr>
<tr><td rowspan="2">Precharge Standby Current in power-down mode</td><td>I_{CC2P}</td><td colspan="2">CKE ≤ V_{IL}(max), t_{CC} =15ns</td><td colspan="6">0.18</td><td>mA</td><td></td></tr>
<tr><td>I_{CC2PS}</td><td colspan="2">CKE ≤ V_{IL}(max), CLK ≤ V_{IL}(max), t_{CC} = ∞</td><td colspan="6">0.15</td><td>mA</td><td></td></tr>
<tr><td rowspan="2">Precharge Standby Current in non power-down mode</td><td>I_{CC2N}</td><td colspan="2">CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} =15ns
Input signals are changed one time during 30ns</td><td colspan="6">5.5</td><td>mA</td><td></td></tr>
<tr><td>I_{CC2NS}</td><td colspan="2">CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞
Input signals are stable</td><td colspan="6">1</td><td>mA</td><td></td></tr>
<tr><td rowspan="2">Active Standby Current in power-down mode</td><td>I_{CC3P}</td><td colspan="2">CKE ≤ V_{IL}(max), t_{CC} =15ns</td><td colspan="6">1.5</td><td rowspan="2">mA</td><td rowspan="2"></td></tr>
<tr><td>I_{CC3PS}</td><td colspan="2">CKE ≤ V_{IL}(max), CLK ≤ V_{IL}(max), t_{CC} = ∞</td><td colspan="6">1</td></tr>
<tr><td rowspan="2">Active Standby Current in non power-down mode
(One Bank Active)</td><td>I_{CC3N}</td><td colspan="2">CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC}=15ns
Input signals are changed one time during 2clks
All other pins ≥ V_{DD}-0.2V or ≤ 0.2V</td><td colspan="6">12</td><td>mA</td><td></td></tr>
<tr><td>I_{CC3NS}</td><td colspan="2">CKE ≥ V_{IH} (min), CLK ≤ V_{IL}(max), t_{CC}= ∞
Input signals are stable</td><td colspan="6">6</td><td>mA</td><td></td></tr>
<tr><td>Operating Current
(Burst Mode)</td><td>I_{CC4}</td><td colspan="2">I_{OL}= 0 mA, Page Burst
All Band Activated, t_{CCD} = t_{CCD}(min)</td><td colspan="2">70</td><td colspan="2">65</td><td colspan="2">60</td><td>mA</td><td>1</td></tr>
<tr><td>Refresh Current</td><td>I_{CC5}</td><td colspan="2">$t_{RFC} \geq t_{RFC}$(min)</td><td colspan="2">55</td><td colspan="2">50</td><td colspan="2">45</td><td>mA</td><td>2</td></tr>
<tr><td rowspan="4">Self Refresh Current</td><td rowspan="4">I_{CC6}</td><td rowspan="4">CKE ≤ 0.2V</td><td>TCSR range</td><td colspan="3">15</td><td colspan="3">85</td><td>°C</td><td rowspan="4"></td></tr>
<tr><td>2 Banks</td><td colspan="3">160</td><td colspan="3">180</td><td rowspan="3">uA</td></tr>
<tr><td>1 Bank</td><td colspan="3">140</td><td colspan="3">160</td></tr>
<tr><td>1/2 Bank</td><td colspan="3">130</td><td colspan="3">140</td></tr>
<tr><td>Deep Power Down Current</td><td>I_{CC7}</td><td colspan="2">CKE ≤ 0.2V</td><td colspan="6">10</td><td>uA</td><td></td></tr>
</table>

Note: 1.Measured with outputs open. Addresses are changed only one time during t_{CC}(min).

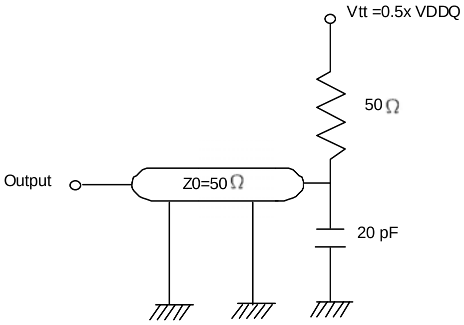
2.Refresh period is 32ms. Addresses are changed only one time during t_{CC}(min).

AC OPERATING TEST CONDITIONS (V_{DD}=1.8V ± 0.1V, T_A= -40 °C ~ 85 °C)

Parameter	Value	Unit
Input levels (Vih/Vil)	0.9 x V_{DDQ} / 0.2	V
Input timing measurement reference level	0.5 x V_{DDQ}	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	0.5 x V_{DDQ}	V
Output load condition	See Fig.2	



(Fig.1) DC Output Load circuit



(Fig.2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			-6	-7.5	-10		
Row active to row active delay		t_{RRD}(min)	12	15	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		t_{RCD}(min)	18	22.5	30	ns	1
Row precharge time		t_{RP}(min)	18	22.5	30	ns	1
Row active time		t_{RAS}(min)	30	37.5	50	ns	1
		t_{RAS}(max)	100			us	
Row cycle time	@Operating	t_{RC}(min)	60	67.5	80	ns	1
	@Auto refresh	t_{RFC}(min)	66	67.5	80	ns	1, 5
Last data in to new col. Address delay		t_{CDL}(min)	1			CLK	2
Last data in to row precharge		t_{RDL}(min)	2			CLK	2
Last data in to burst stop		t_{BDL}(min)	1			CLK	2
Col. Address to col. Address delay		t_{CCD}(min)	1			CLK	3
Number of valid output data		CAS latency=3	2			ea	4
		CAS latency=2	1				

Note: 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
The earliest a precharge command can be issued after a Read command without the loss of data is CL+BL-2 clocks.
5. A new command may be given t_{REF} after self refresh exit.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-6		-7.5		-10		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS Latency =3	t_{CC}	6	1000	7.5	1000	10	1000	ns	1
	CAS Latency =2		10		12		15			
CLK to valid output delay	CAS Latency =3	t_{SAC}	-	5.5	-	6	-	9	ns	1, 4
	CAS Latency =2		-	9	-	10	-	12		
Output data hold time		t_{OH}	2.5	-	2.5	-	2.5	-	ns	2
CLK high pulse width		t_{CH}	2.5	-	2.5	-	3	-	ns	3
CLK low pulse width		t_{CL}	2.5	-	2.5	-	3	-	ns	3
Input setup time		t_{SS}	2	-	2.5	-	3	-	ns	3
Input hold time		t_{SH}	1	-	1	-	1	-	ns	3
CLK to output in Low-Z		t_{SLZ}	1	-	1	-	1	-	ns	2
CLK to output in Hi-Z	CAS Latency =3	t_{SHZ}	-	5.5	-	6	-	9	ns	-
	CAS Latency =2		-	9	-	10	-	12		

*All AC parameters are measured from half to half.

Note: 1.Parameters depend on programmed CAS latency.

2.If clock rising time is longer than 1ns,(tr/2-0.5)ns should be added to the parameter.

3.Assumed input rise and fall time (tr & tf)=1ns.

If tr & tf is longer than 1ns, transient time compensation should be considered, i.e., [(tr+ tf)/2-1]ns should be added to the parameter.

4. t_{SAC} at CL = 3 for -6 speed grade with no load is 5.5ns and is guaranteed by design.

Mode Register

BA	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address bus
x	x	1	0	0	LTMODE			WT	BL			Burst Read and Single Write (for Write Through Cache)
0	0	0	0	0	LTMODE			WT	BL			Mode Register Set

x =Don't care

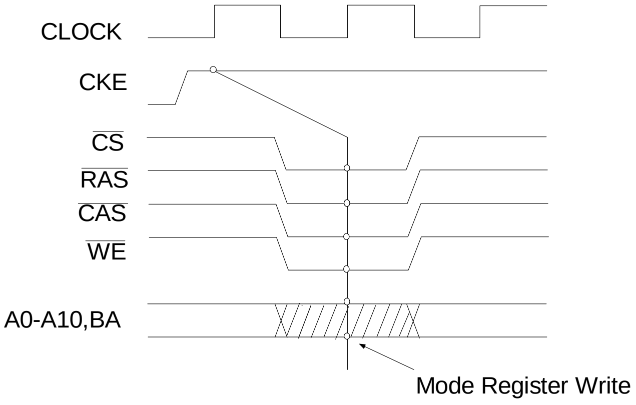
	A2-A0	WT=0	WT=1
Burst length	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	Full page	R

Wrap type	0	Sequential
	1	Interleave

	A6-A4	$\overline{\text{CAS}}$ Latency
Latency mode	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
	111	R

Remark R: Reserved

Mode Register Write Timing



Extended Mode Register

BA	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address bus	
1	0	0	0	0	DS		X	X	PASR			Extended Mode Register Set	x =Don't care

	A2-A0	Self Refresh Coverage
PASR	000	2 Banks
	001	1 Bank (Bank 0, BA=0)
	010	1/2 Bank (BA=A10=0)
	011	R
	100	R
	101	1/4 Bank (BA=A10=A9=0)
	110	R
	111	R

	A6-A5	Driver Strength
DS	00	Full Strength
	01	1/2 Strength
	10	1/4 Strength
	11	R

Remark R: Reserved

Burst Length and Sequence

(Burst of Two)

Starting Address (column address A0 binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0,1	0,1
1	1,0	1,0

(Burst of Four)

Starting Address (column address A1-A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
00	0,1,2,3	0,1,2,3
01	1,2,3,0	1,0,3,2
10	2,3,0,1	2,3,0,1
11	3,0,1,2	3,2,1,0

(Burst of Eight)

Starting Address (column address A2-A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
000	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
001	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
010	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
011	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
100	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
101	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
110	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
111	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0

Full page burst is an extension of the above tables of Sequential Addressing, with the length being 256 for 1Mx16 device.

POWER UP SEQUENCE

1.Apply power and start clock, attempt to maintain CKE= “H”, L(U)DQM = “H” and the other pin are NOP condition at the inputs.

2.Maintain stable power, stable clock and NOP input condition for a minimum of 200us.

3.Issue precharge commands for all banks of the devices.

4.Issue 2 or more auto-refresh commands.

5.Issue mode register set command to initialize the mode register.

6.Issue an extended mode register set command to define special function of the device after normal MRS.

Cf.)Sequence of 4~6 is regardless of the order.

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA	A10/AP	A9~A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
	Extended Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4,5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4,5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	4
	Both Banks									X	H		4
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
			H		L	H	H	H					
Deep Power Down Mode		Entry	H	L	L	H	H	L	X	X			
		Exit	L	H	X	X	X	X	X				

(V= Valid, X= Don't Care, H= Logic High, L = Logic Low)

Note:

1. OP Code: Operation Code

   A0~ A10/AP, BA: Program keys.(@MRS). BA=0 for MRS and BA=1 for EMRS.
2. MRS/EMRS can be issued only at both banks precharge state.

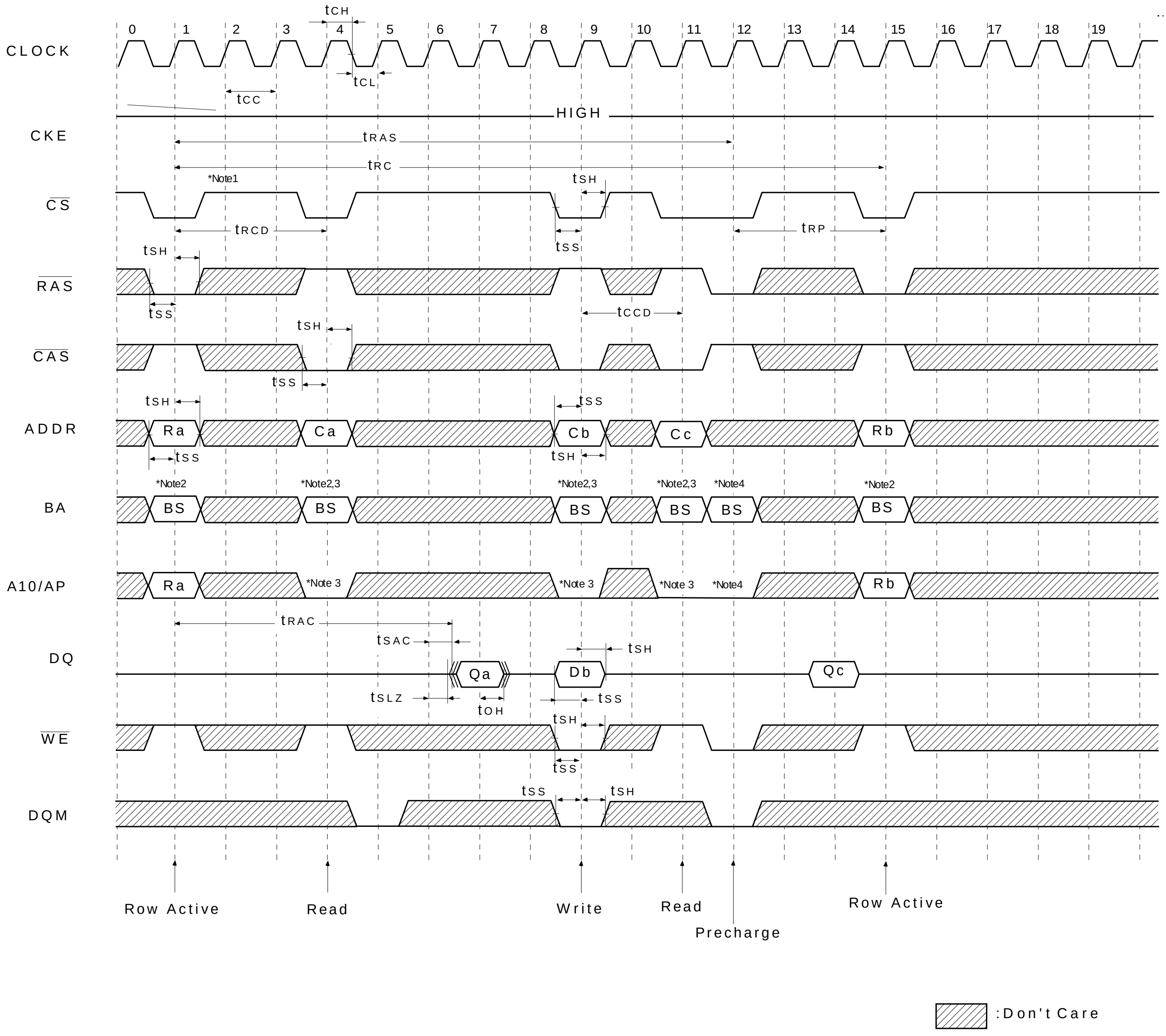
   A new command can be issued after 2 clock cycle of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.

   The automatical precharge without row precharge command is meant by "Auto".
   Auto / self refresh can be issued only at both banks precharge state.
4. BA: Bank select address.

   If "Low": at read, write, row active and precharge, bank A is selected.
   If "High": at read, write, row active and precharge, bank B is selected.
   If A10/AP is "High" at row precharge, BA ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.

   Another bank read /write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

Single Bit Read-Write-Read Cycle (Same Page) @CAS Latency=3, Burst Length=1



***Note:** 1. All inputs expect CKE & DQM can be don’t care when $\overline{CS}$ is high at the CLK high going edge.

2. Bank active & read/write are controlled by BA.

BA	Active & Read/Write
0	Bank A
1	Bank B

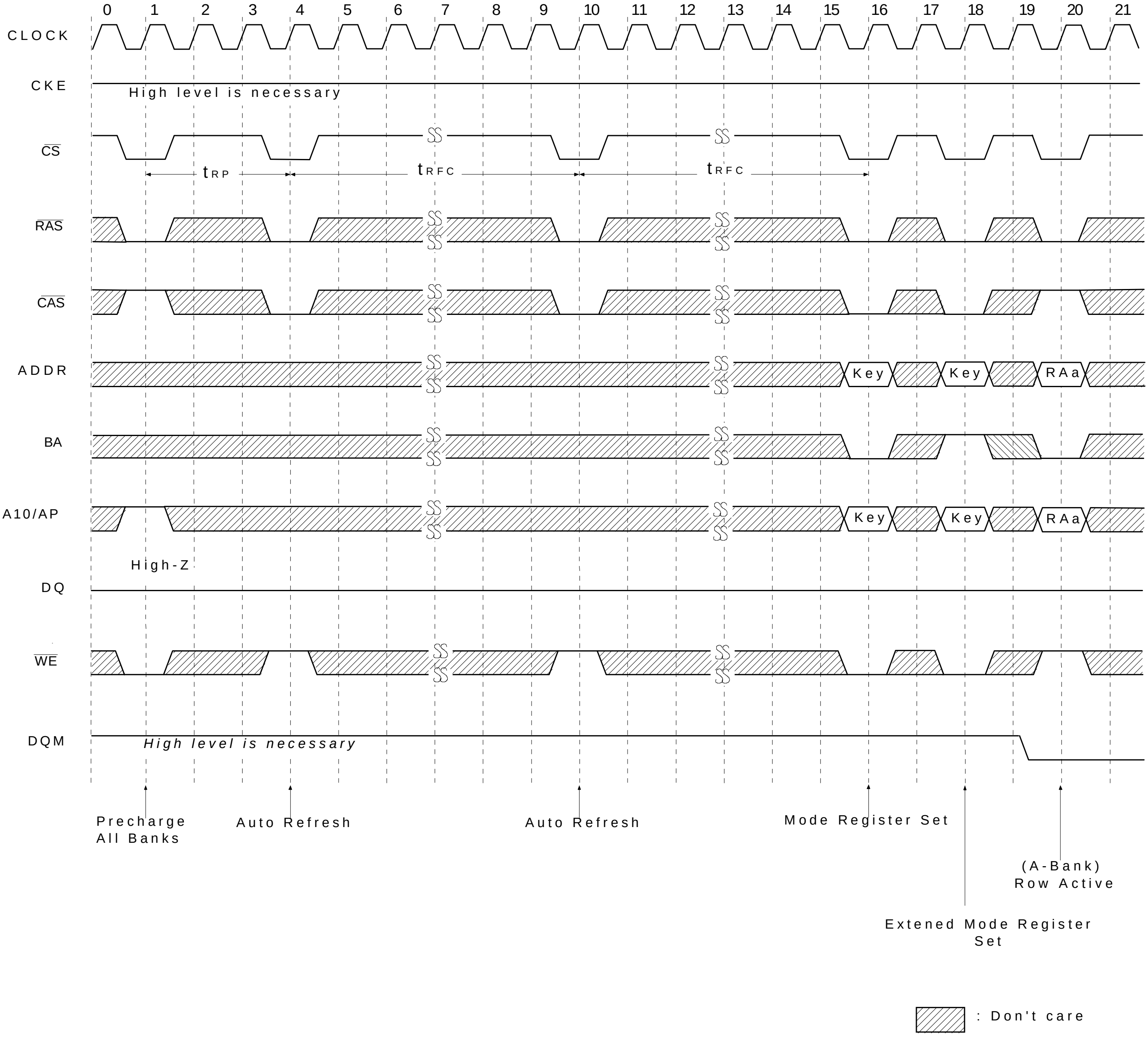
3.Enable and disable auto precharge function are controlled by A10/AP in read/write command.

A10/AP	BA	Operation
0	0	Disable auto precharge, leave bank A active at end of burst.
	1	Disable auto precharge, leave bank B active at end of burst.
1	0	Enable auto precharge, precharge bank A at end of burst.
	1	Enable auto precharge, precharge bank B at end of burst.

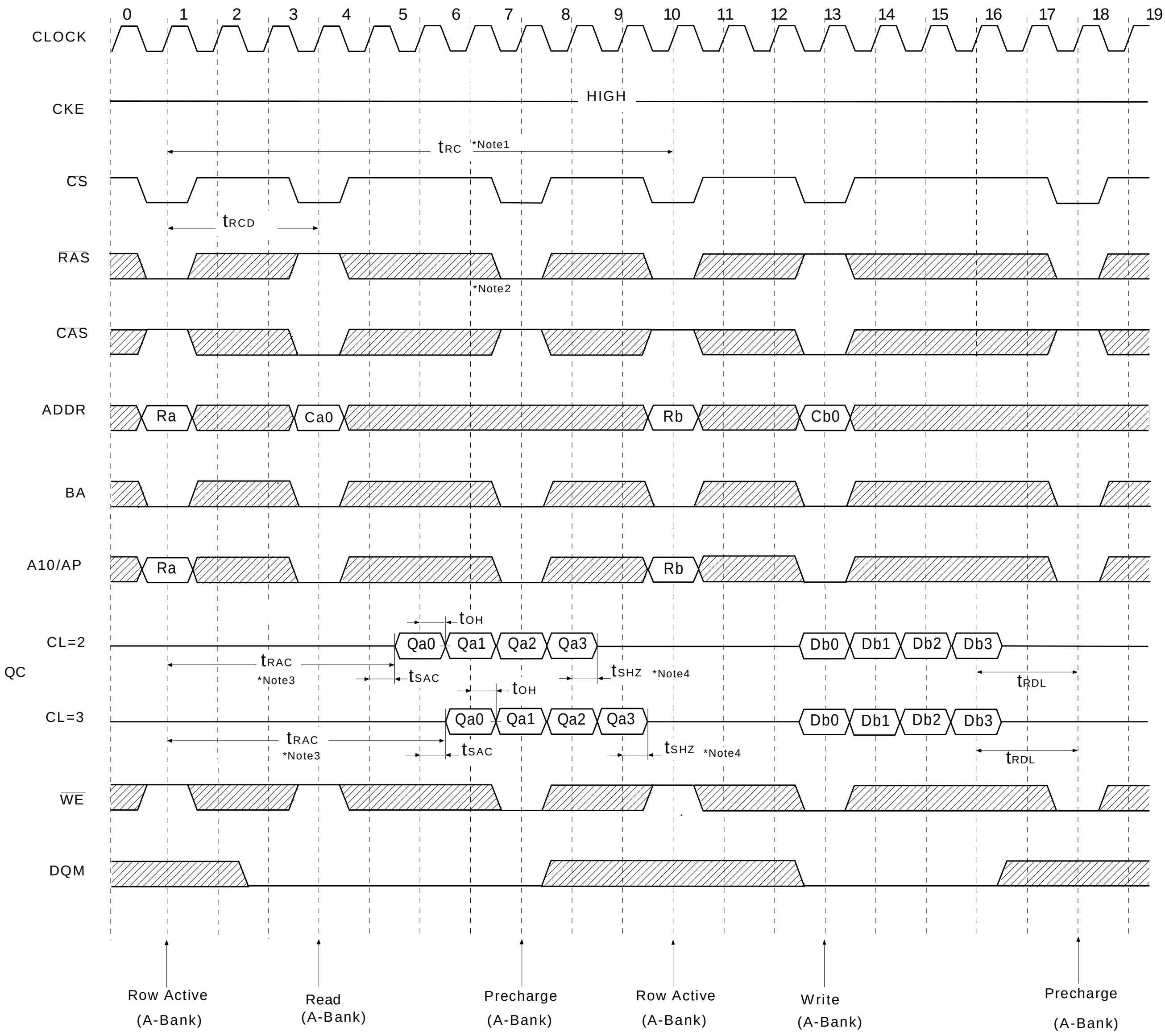
4.A10/AP and BA control bank precharge when precharge command is asserted.

A10/AP	BA	Precharge
0	0	Bank A
0	1	Bank B
1	X	Both Banks

Power Up Sequence



Read & Write Cycle at Same Bank @ Burst Length = 4



▨ : Don't care

*Note: 1.Minimum row cycle times is required to complete internal DRAM operation.

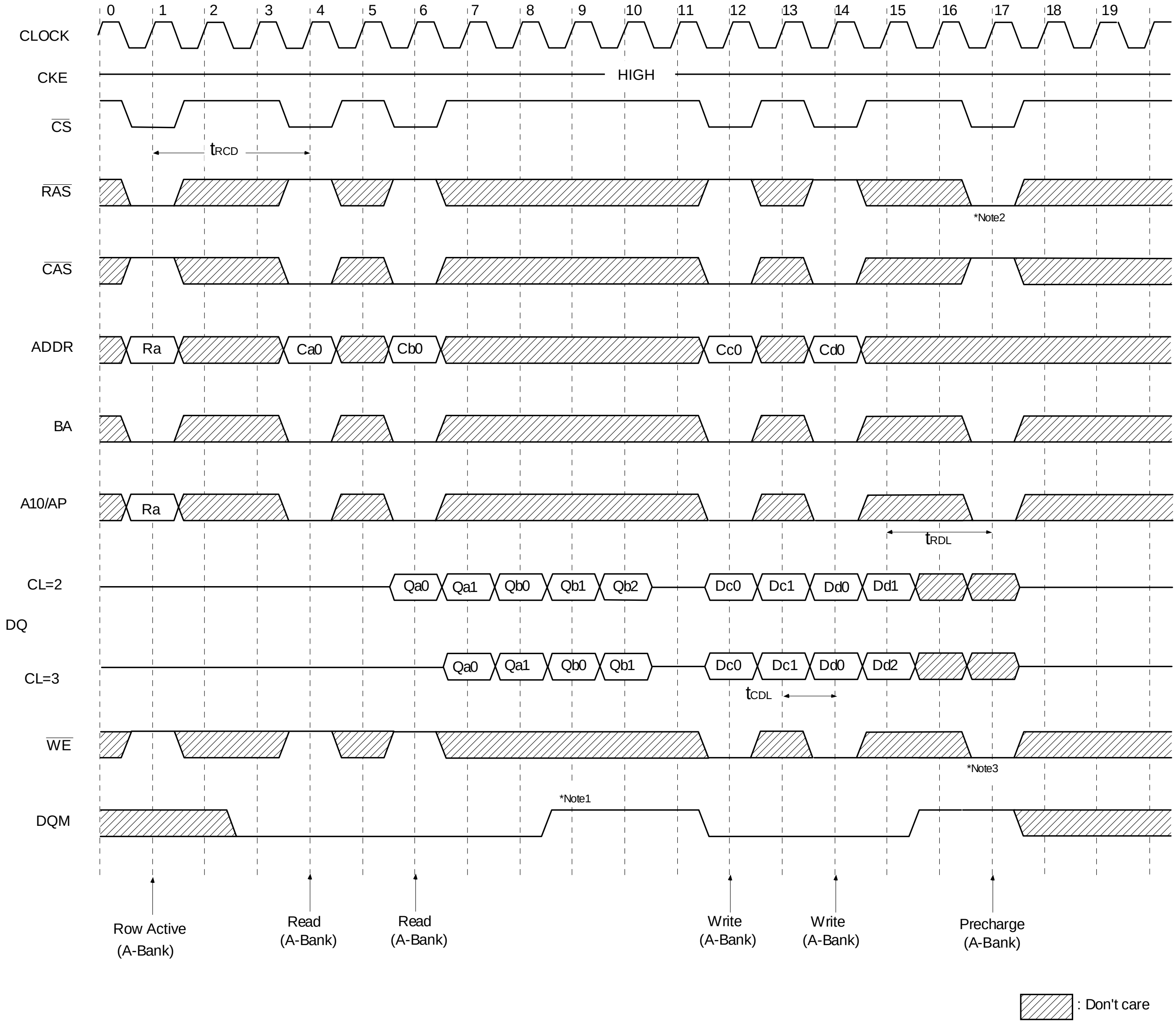
2.Row precharge can interrupt burst on any cycle. [CAS Latency-1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{SHZ}) after the clock.

3.Access time from Row active command. tcc*(t_{RCD} +CAS latency-1)+t_{SAC}

4.Ouput will be Hi-Z after the end of burst.(1,2,4,8 bit burst)

Burst can't end in Full Page Mode.

Page Read & Write Cycle at Same Bank @ Burst Length=4

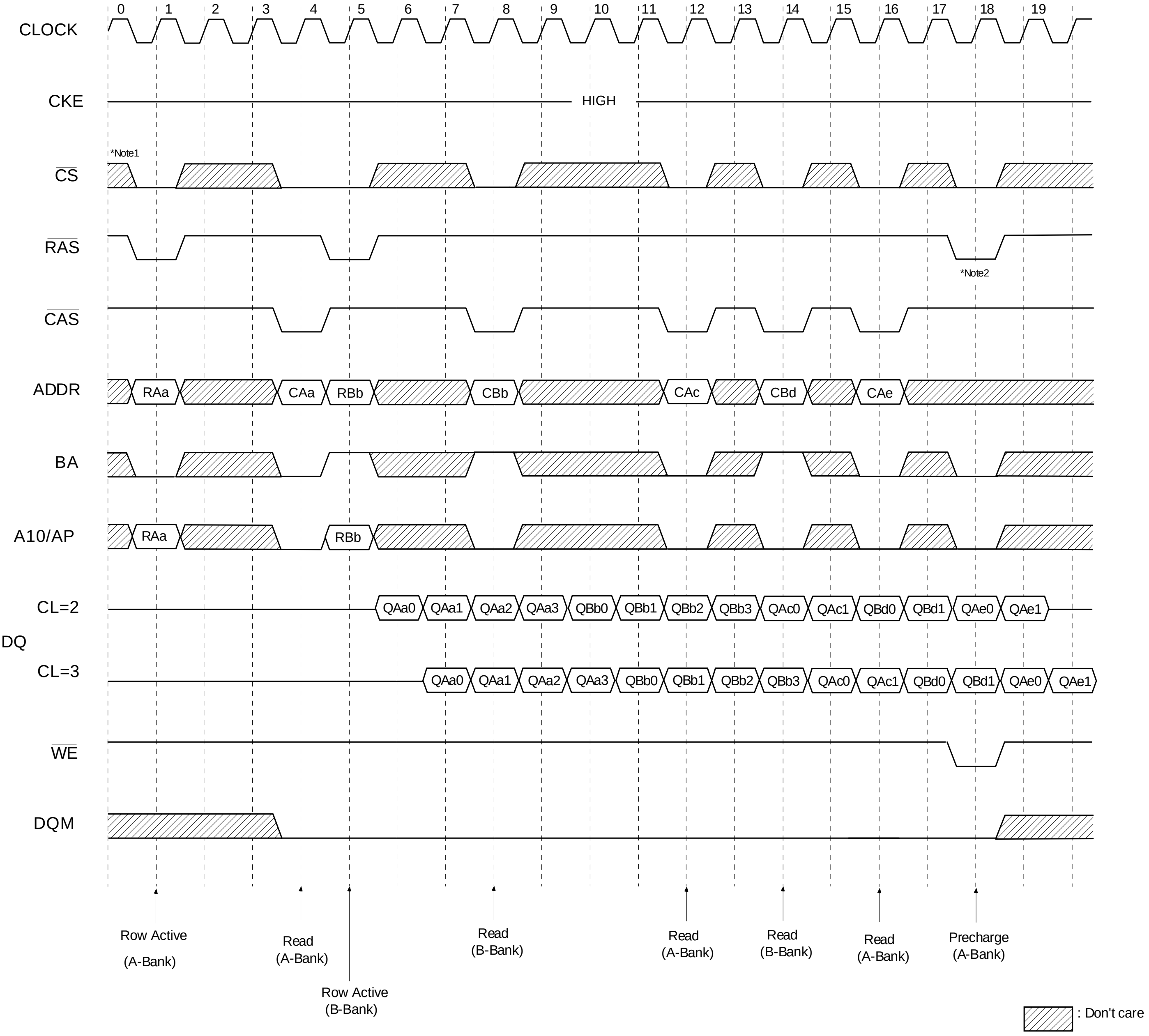


*Note: 1.To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.

2.Row precharge will interrupt writing. Last data input, t_{RDL} before Row precharge, will be written.

3.DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

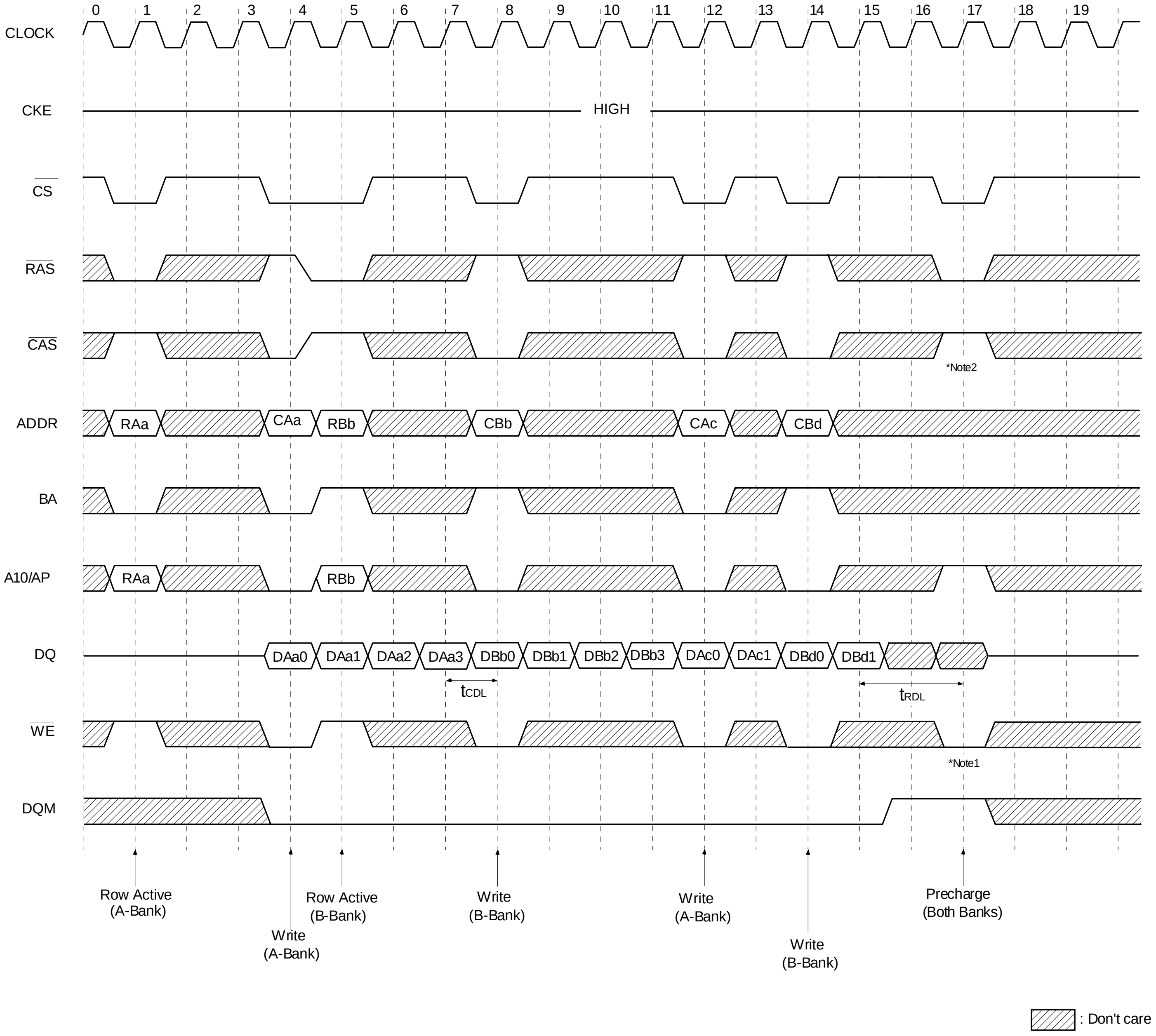
Page Read Cycle at Different Bank @ Burst Length=4



*Note: 1. $\overline{\text{CS}}$ can be don't cared when $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ are high at the clock high going dege.

2.To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

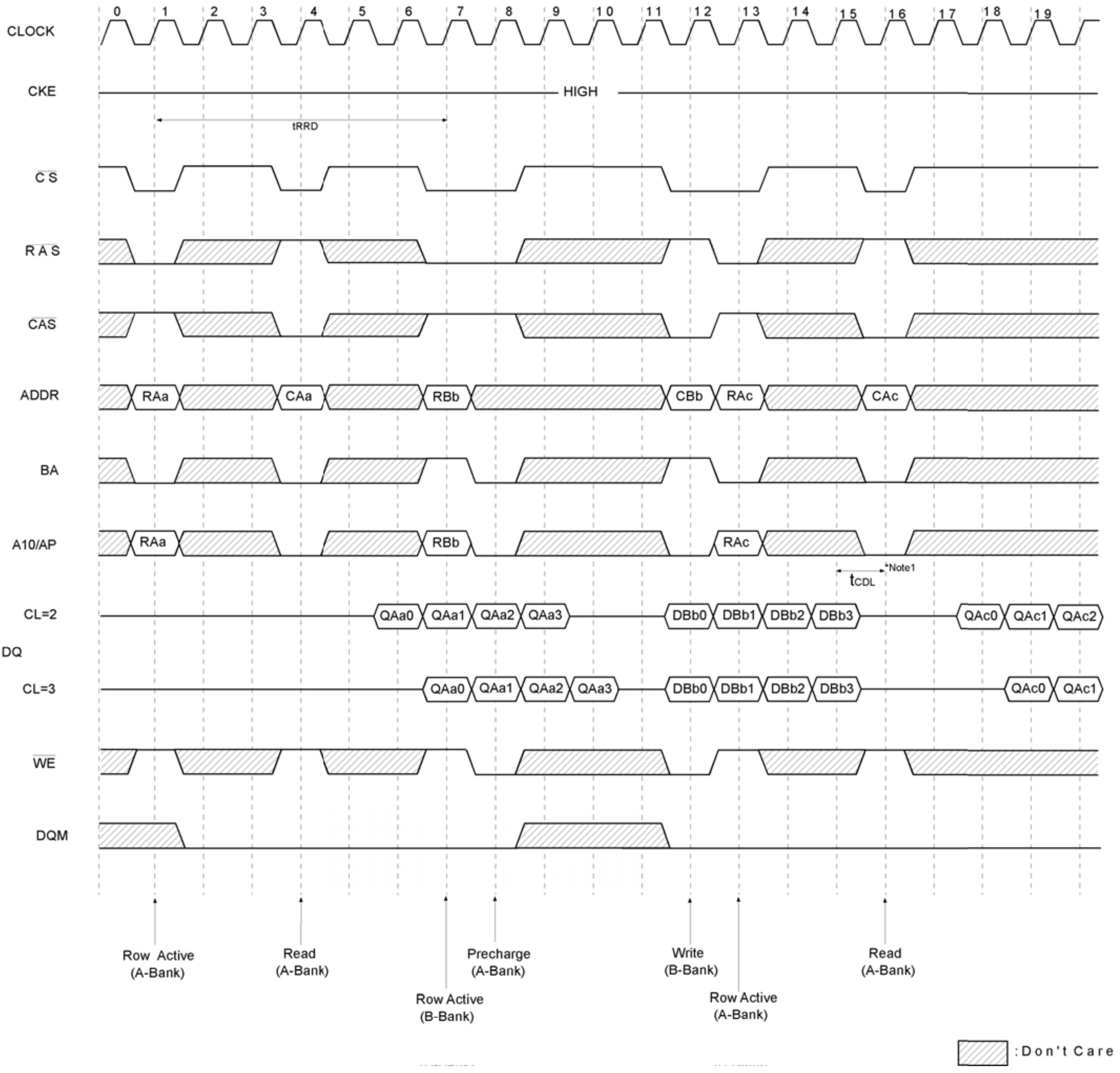
Page Write Cycle at Different Bank @ Burst Length = 4



*Note: 1.To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.

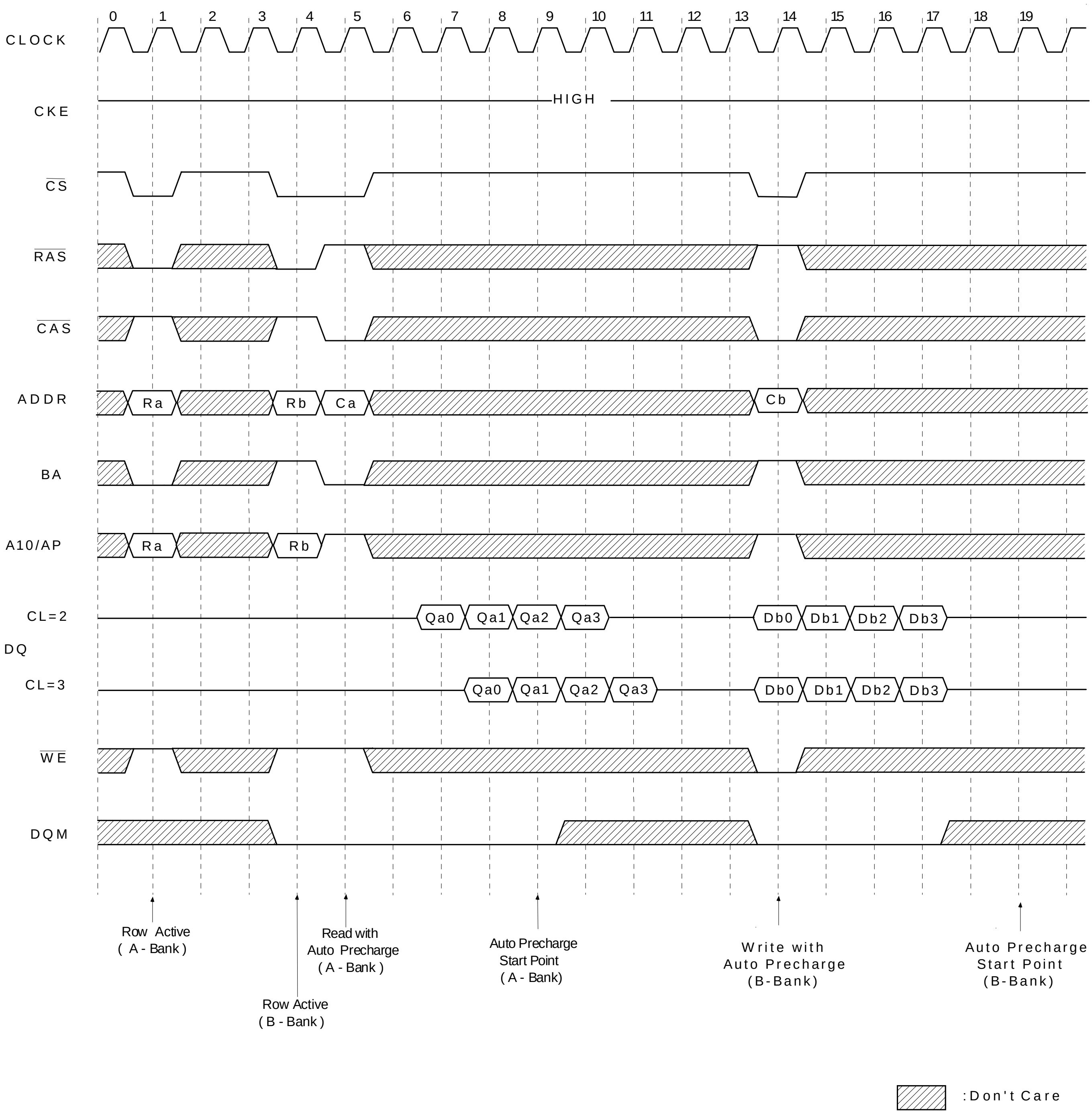
2.To interrupt burst write by row precharge, both the write and the precharge banks must be the same.

Read & Write Cycle at Different Bank @ Burst Length = 4



*Note: 1.tCDL should be met to complete write.

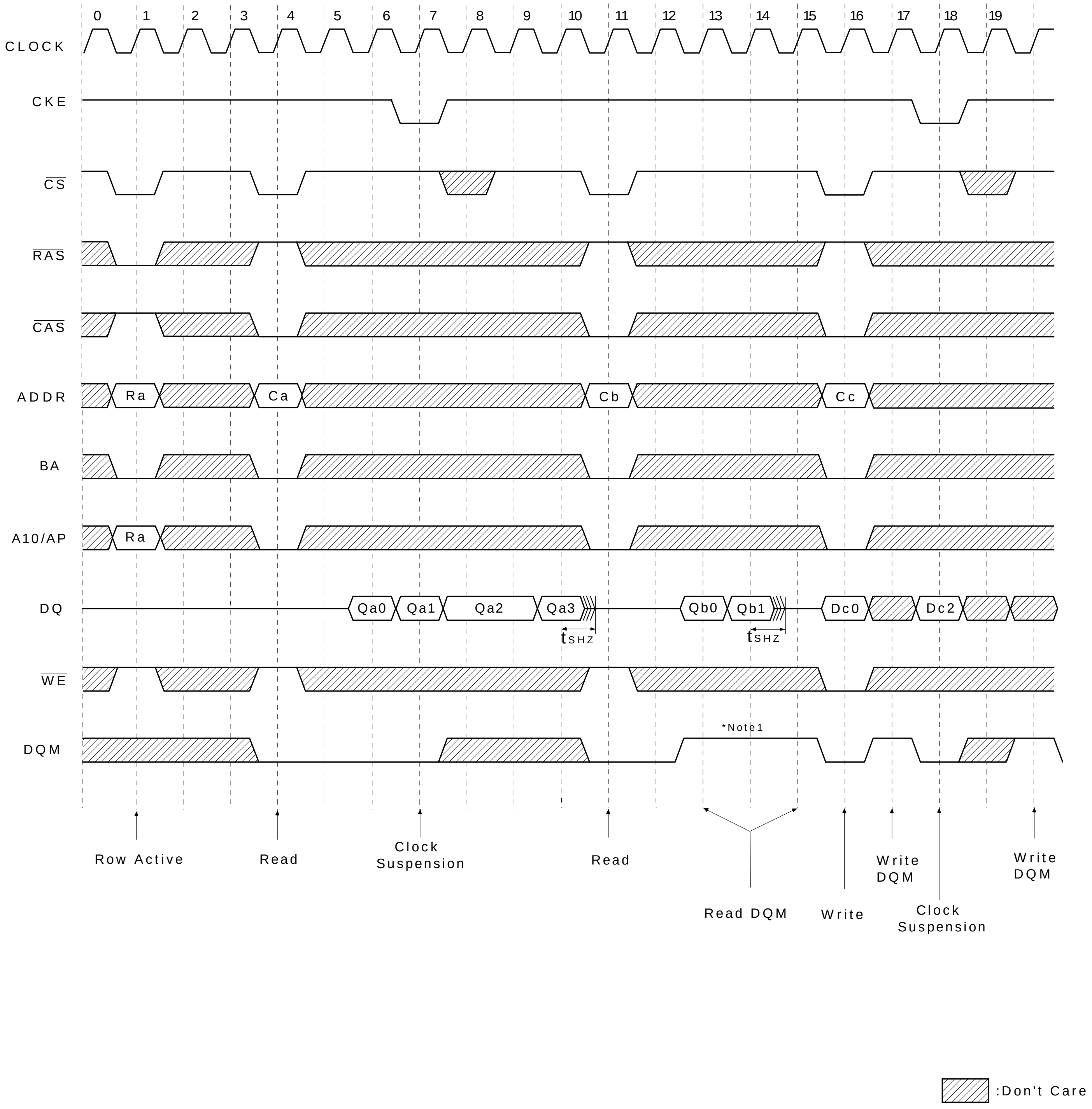
Read & Write Cycle with auto Precharge @ Burst Length =4



*Note: 1.t_{CDL} Should be controlled to meet minimum t_{RAS} before internal precharge start

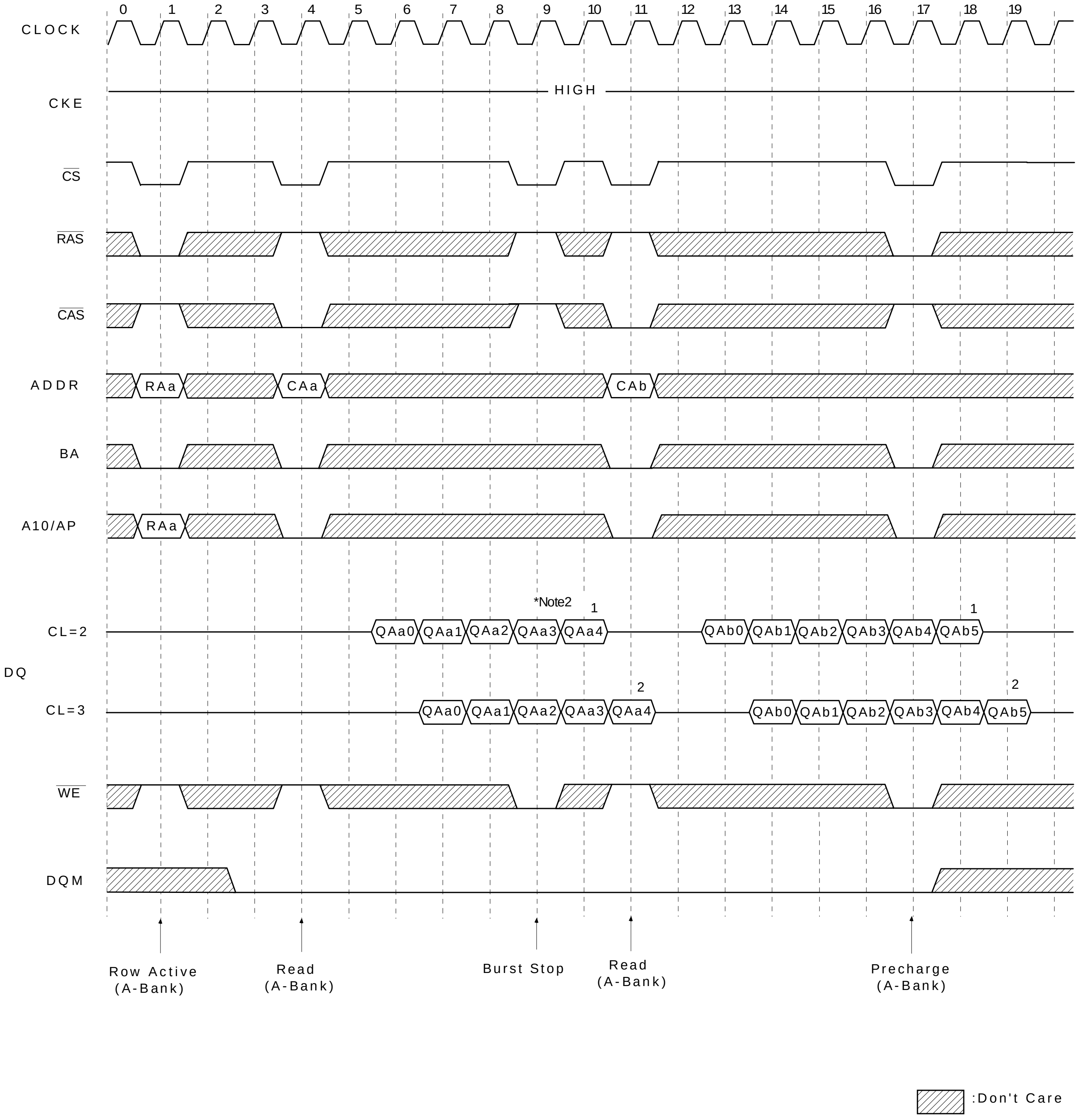
(In the case of Burst Length=1 & 2 and BRSW mode)

Clock Suspension & DQM Operation Cycle @CAS Latency=2, Burst Length=4



*Note: 1.DQM is needed to prevent bus contention.

Read Interrupted by Precharge Command & Read Burst Stop Cycle @ Burst Length =Full page



*Note: 1.Burst can't end in full page mode, so auto precharge can't issue.

2.About the valid DQs after burst stop, it is same as the case of $\overline{RAS}$ interrupt.

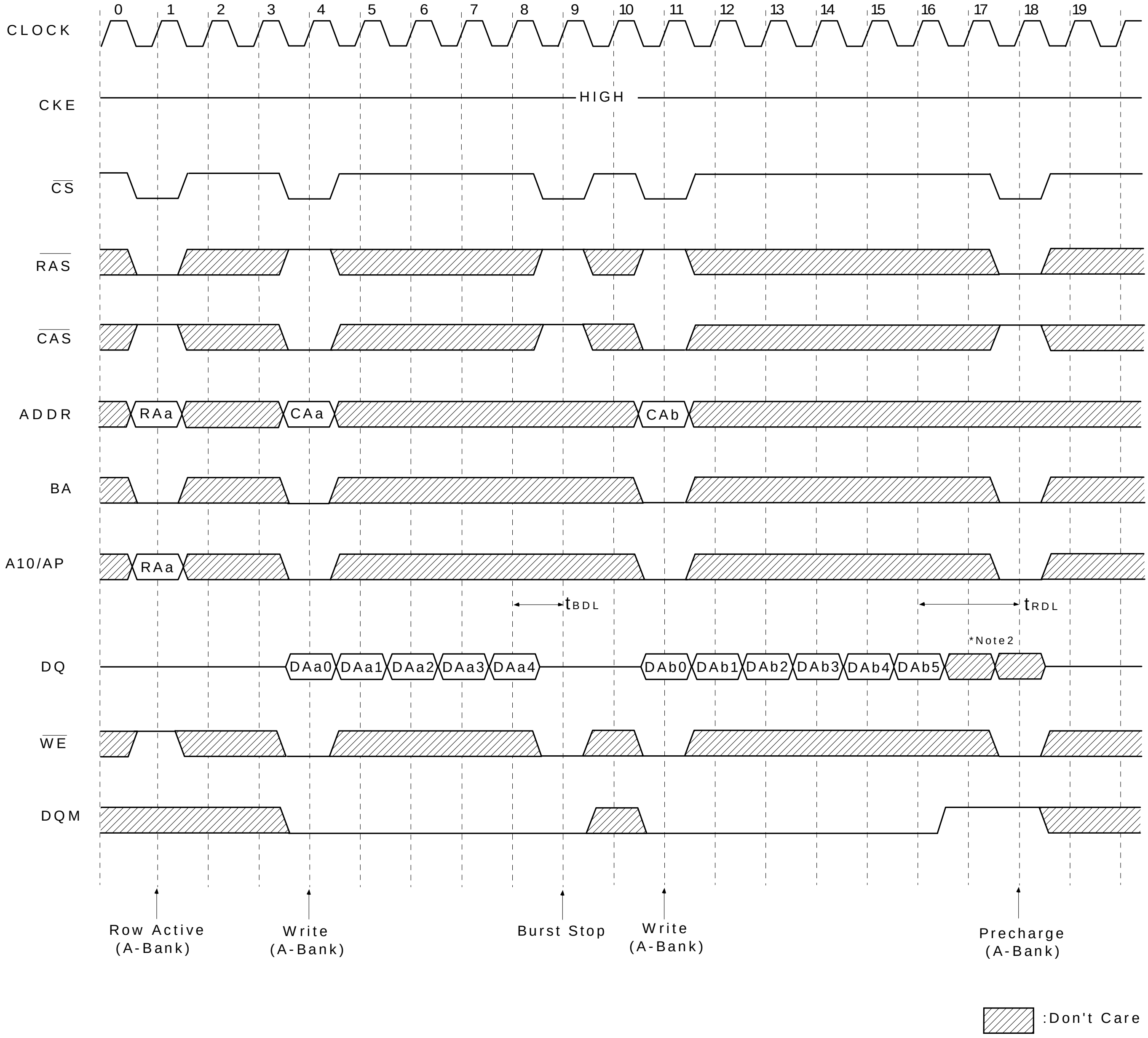
Both cases are illustrated above timing diagram. See the label 1, 2 on them.

But at burst write, burst stop and $\overline{RAS}$ interrupt should be compared carefully.

Refer the timing diagram of "Full page write burst stop cycle".

3.Burst stop is valid at every burst length.

Write Interrupted by Precharge Command & Write Burst stop Cycle @ Burst Length =Full page



*Note: 1. Burst can't end in full page mode, so auto precharge can't issue.

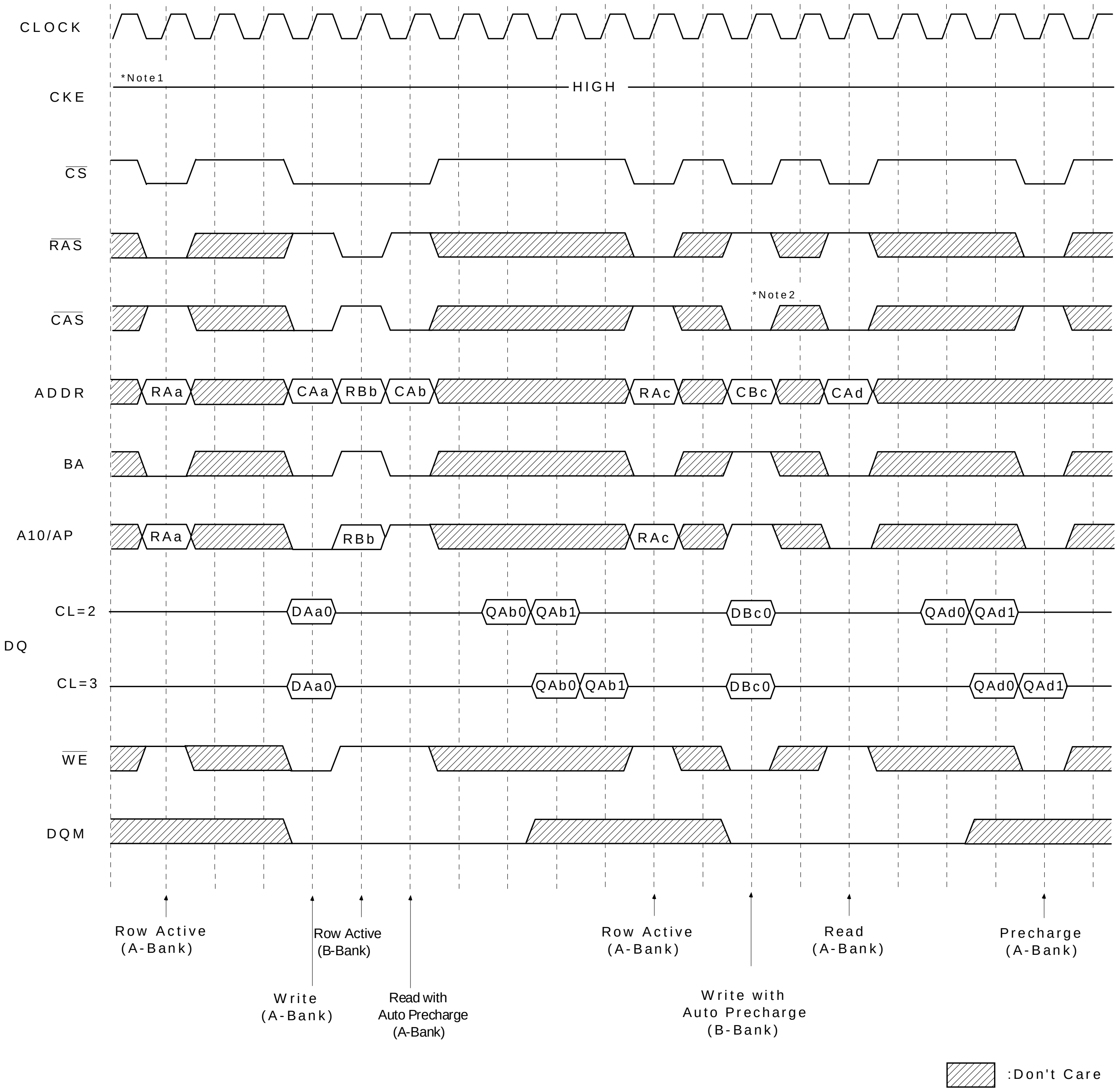
2.Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}.

DQM at write interrupted by precharge command is needed to prevent invalid write.

Input data after Row precharge cycle will be masked internally.

3.Burst stop is valid at every burst length.

Burst Read Single bit Write Cycle @ Burst Length=2



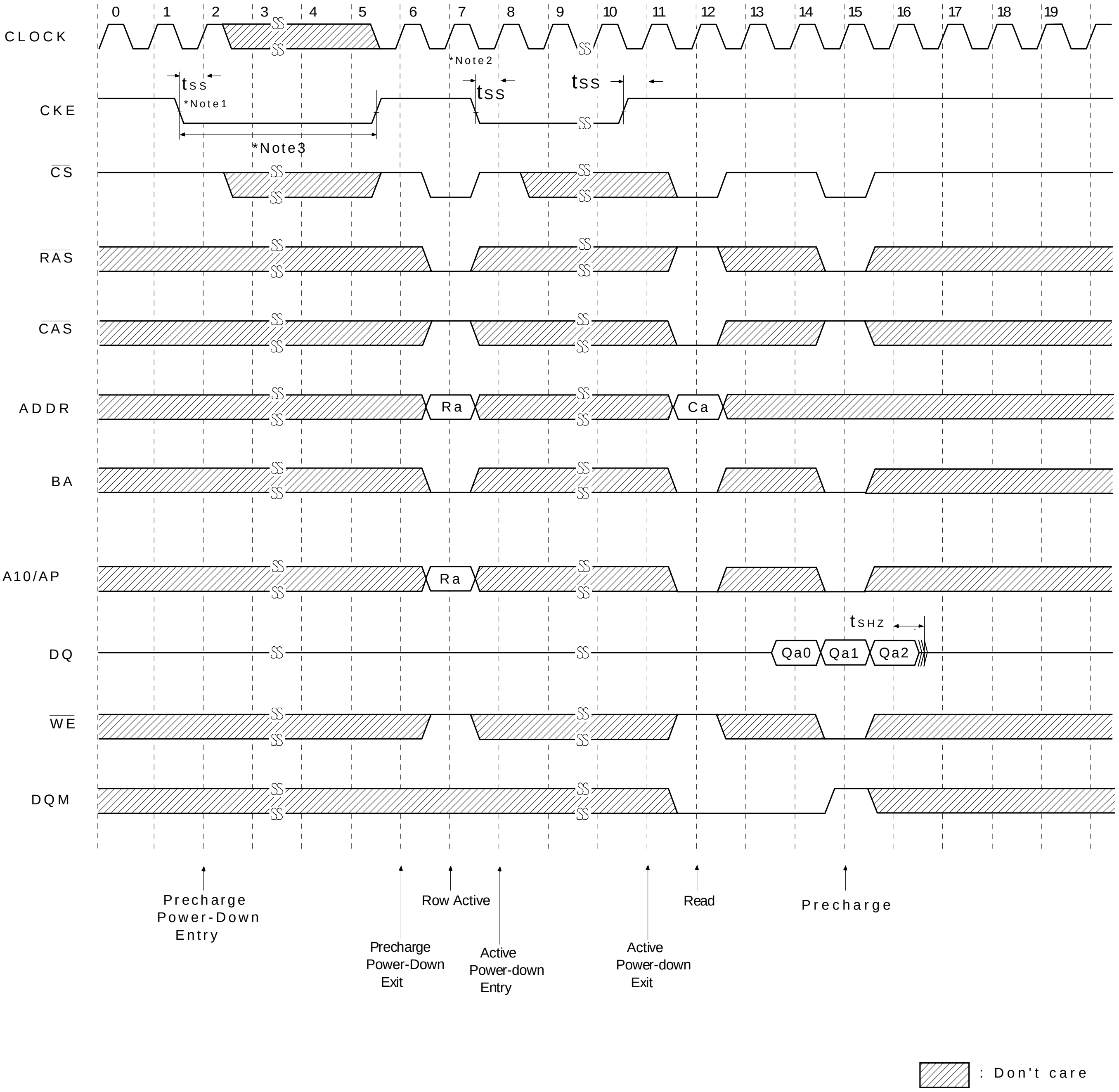
*Note: 1.BRSW modes is enabled by setting A9 “High” at MRS(Mode Register Set).

At the BRSW Mode, the burst length at write is fixed to “1” regardless of programmed burst length.

2.When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated.

Auto precharge is executed at the next cycle of burst-end, so in the case of BRSW write command, the precharge command will be issued after two clock cycles.

Active/Precharge Power Down Mode @ CAS Latency=2, Burst Length=4

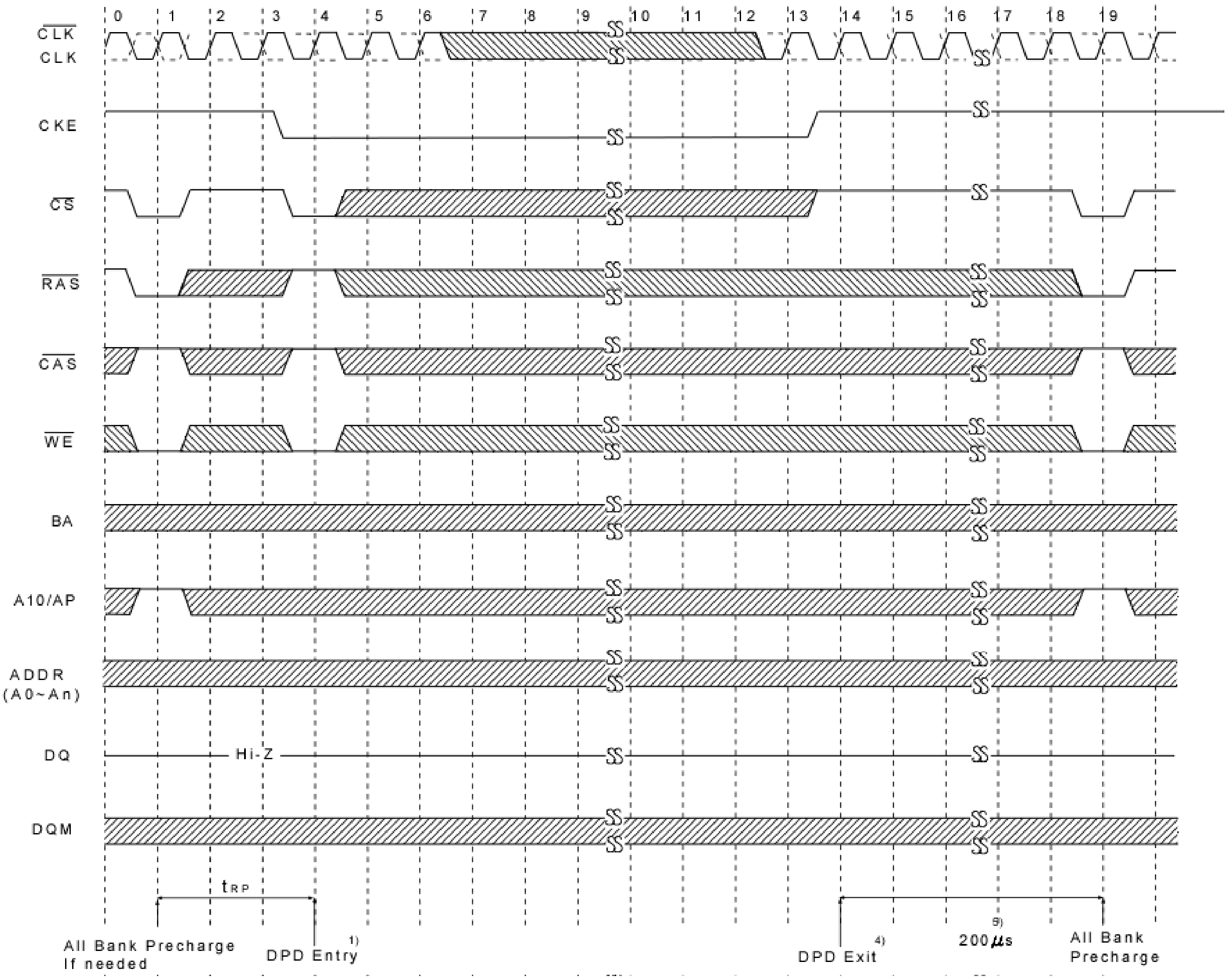


*Note: 1.Both banks should be in idle state prior to entering precharge power down mode.

2.CKE should be set high at least 1CLK+tss prior to Row active command.

3.Can not violate minimum refresh specification. (32ms)

Deep Power Down Mode Entry & Exit Cycle



Note:

DEFINITION OF DEEP POWER MODE FOR Mobile SDRAM:
Deep Power Down Mode is an operating mode to achieve maximum power reduction by cutting the power of the whole memory of the device. Once the device enters in Deep Power Down Mode, data will not be retained. Full initialization is required when the device exits from Deep Power Down Mode.

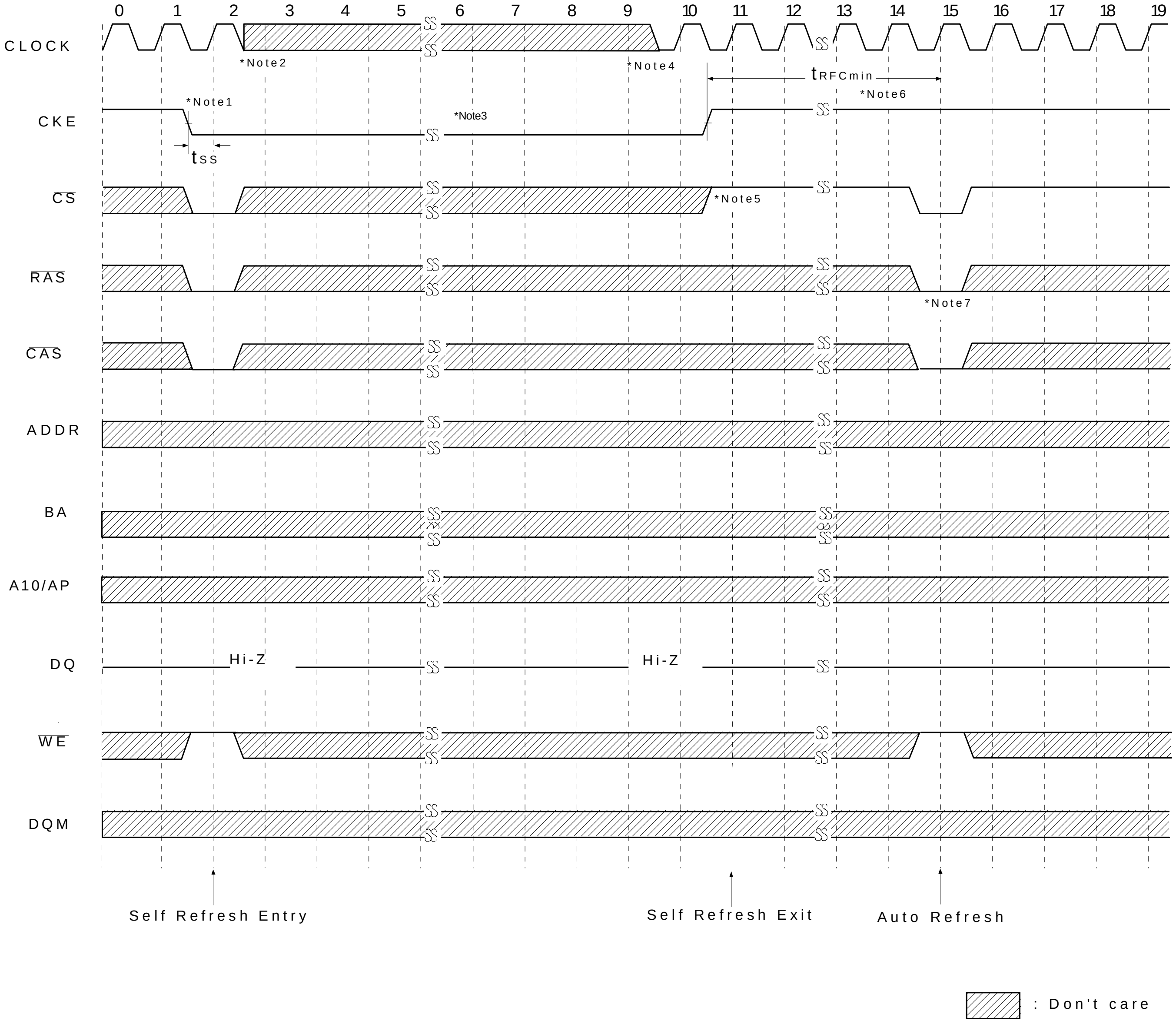
TO ENTER DEEP POWER DOWN MODE

1) The deep power down mode is entered by having $\overline{CS}$ and $\overline{WE}$ held low with $\overline{RAS}$ and $\overline{CAS}$ high at the rising edge of the clock. While CKE is low.
2) Clock must be stable before exited deep power down mode.
3) Device must be in the all banks idle state prior to entering Deep Power Down mode.

TO EXIT DEEP POWER DOWN MODE

4) The deep power down mode is exited by asserting CKE high.
5) 200μs wait time is required to exit from Deep Power Down.
6) Upon exiting deep power down an all bank precharge command must be issued followed by two auto refresh commands and a load mode register sequence.

Self Refresh Entry & Exit Cycle



*Note:

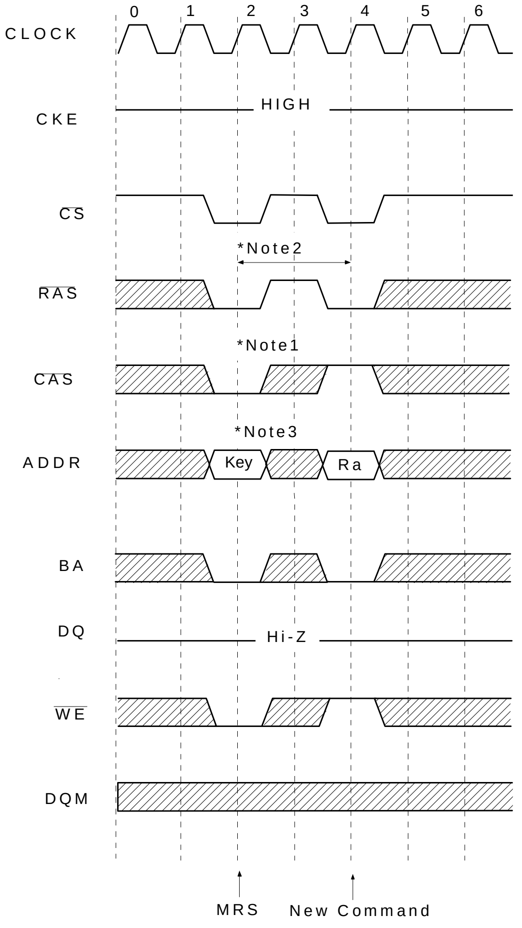
TO ENTER SELF REFRESH MODE

1. $\overline{CS}$, $\overline{RAS}$ & $\overline{CAS}$ with CKE should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "Low".
   cf.) Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

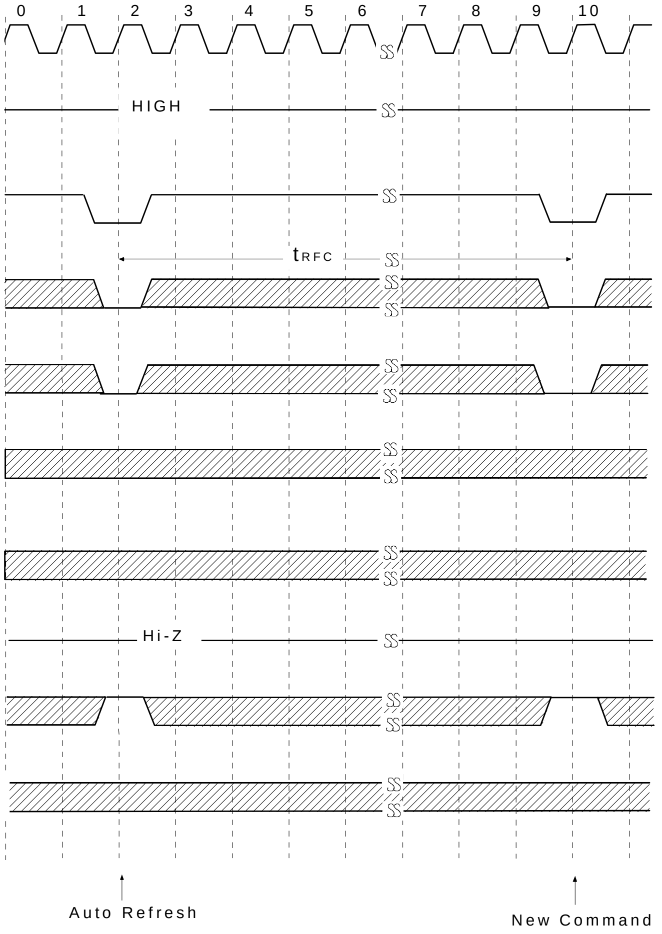
TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning CKE high.
5. $\overline{CS}$ Starts from high.
6. Minimum t_{RFC} is required after CKE going high to complete self refresh exit.
7. 2K cycles of burst auto refresh is required immediately before self refresh entry and immediately after self refresh exit.

Mode Register Set Cycle



Auto Refresh Cycle



▨ :Don't Care

*Both banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

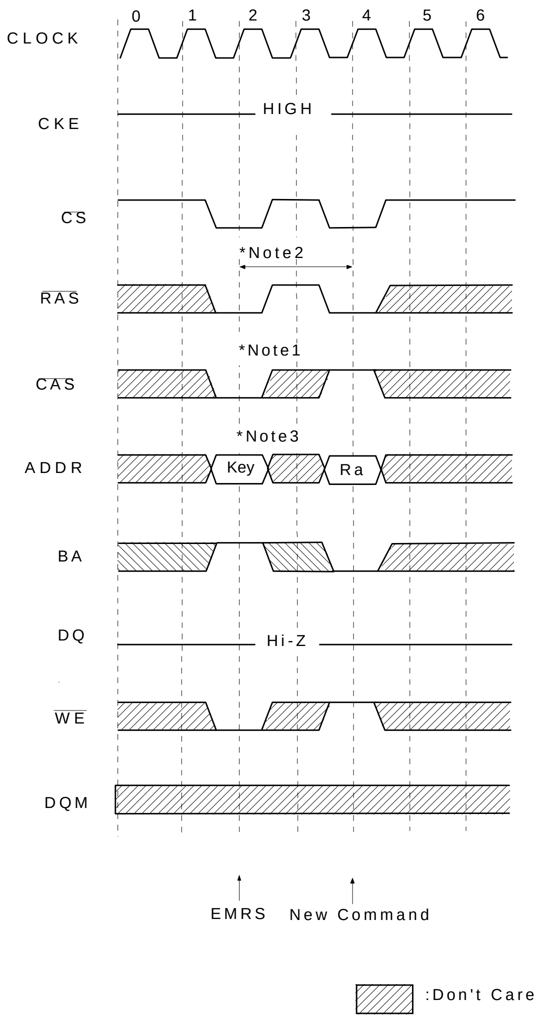
MODE REGISTER SET CYCLE

*Note: 1. $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ & $\overline{\text{WE}}$ activation at the same clock cycle with address key will set internal mode register.

2.Minimum 2 clock cycles should be met before new $\overline{\text{RAS}}$ activation.

3.Please refer to Mode Register Set table.

Extended Mode Register Set Cycle



*Both banks precharge should be completed before Extended Mode Register Set cycle.

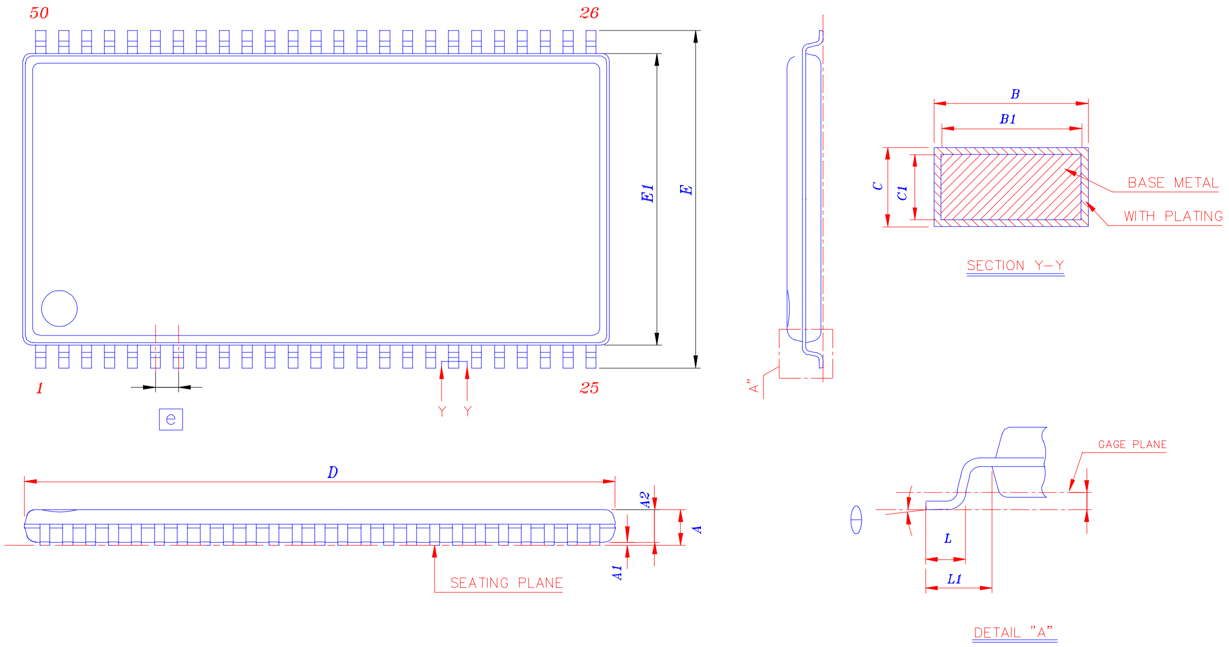
EXTENDED MODE REGISTER SET CYCLE

*Note: 1. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ & $\overline{WE}$ activation at the same clock cycle with address key will set internal extended mode register.

2.Minimum 2 clock cycles should be met before new $\overline{RAS}$ activation.

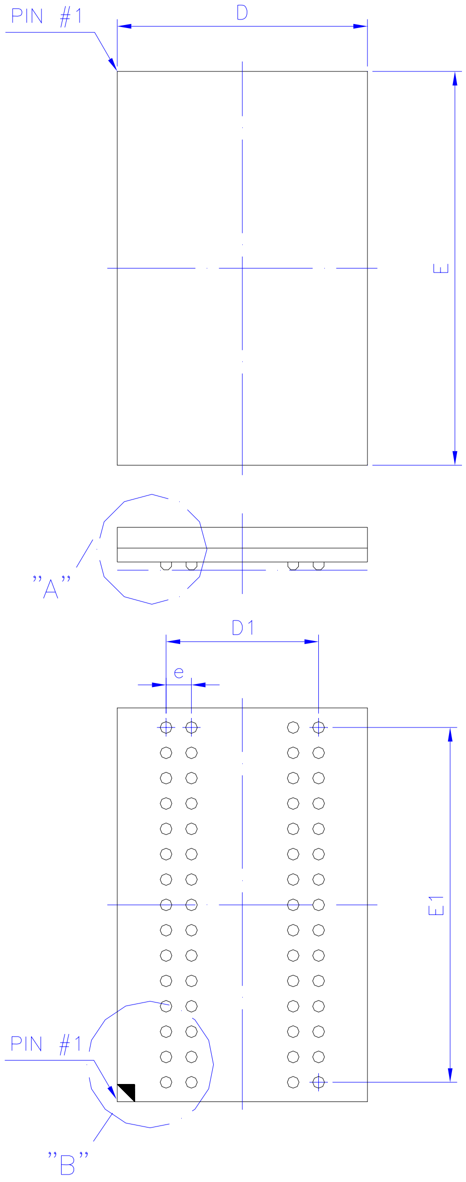
3.Please refer to Mode Register Set table.

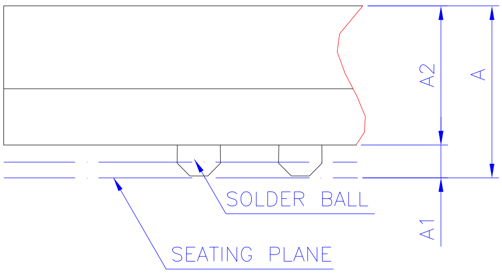
PACKAGE DIMENSIONS
50-LEAD TSOP(II) SDRAM(400mil)



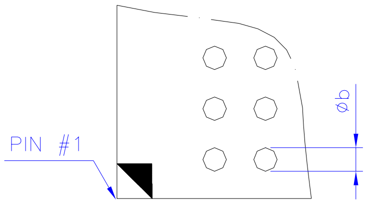
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.20	-	-	0.047
A1	0.051	0.127	0.203	0.002	0.005	0.008
A2	0.95	1.00	1.05	0.037	0.039	0.041
B	0.30	-	0.45	0.012	-	0.018
B1	0.30	0.35	0.40	0.012	0.014	0.016
C	0.12	-	0.21	0.005	-	0.008
C1	0.10	0.127	0.16	0.004	0.005	0.006
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.394	0.400	0.405
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.80 REF			0.031 REF		
e	0.80 BSC			0.031 BSC		
θ	0	-	8	0	-	8

PACKING DIMENSIONS
60-BALL SDRAM (6.4x10.1 mm)





DETAIL : "A"



DETAIL : "B"

Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A			1.00			0.039
A_1	0.20	0.25	0.30	0.008	0.010	0.012
A_2	0.61	0.66	0.71	0.024	0.026	0.028
Φ_b	0.30	0.35	0.40	0.012	0.014	0.016
D	6.30	6.40	6.50	0.248	0.252	0.256
E	10.00	10.10	10.20	0.394	0.398	0.402
D_1		3.90			0.154	
E_1		9.10			0.358	
e		0.65			0.026	

Controlling dimension : Millimeter.

Revision History

Revision	Date	Description
0.1	2008.05.15	Original
0.2	2008.10.03	1. Add t_{RFC} spec. 2. Modify t_{RP} and t_{RC} spec. 3. Modify the description about self refresh operation
1.0	2008.12.16	1. Delete "Preliminary" 2. Correct t_{RP} spec.
1.1	2009.09.03	1. Add -6 speed grade 2. Correct Power up Sequence for EMRS and add the chart of EMRS 3. Add the chart of Deep Power Down Mode

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