Freescale Semiconductor
Data Sheet: Advance Information

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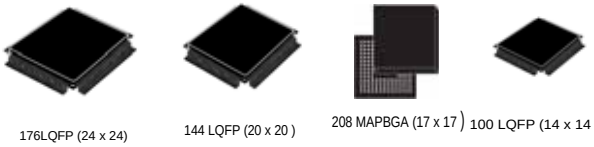
MPC5607B



MPC5607B Microcontroller Data Sheet

Features

- Single issue, 32-bit CPU core complex (e200z0h)
  - Compliant with the Power Architecture™ embedded category
  - Enhanced instruction set allowing variable length encoding (VLE) for code size footprint reduction. With the optional encoding of mixed 16-bit and 32-bit instructions, it is possible to achieve significant code size footprint reduction.
- Up to 1.5 Mbytes on-chip Flash supported with the Flash controller
- Up to 96 Kbytes on-chip SRAM
- Memory protection unit (MPU) with 8 region descriptors and 32-byte region granularity on certain family members
- Interrupt controller (INTC) capable of handling 204 selectable-priority interrupt sources
- Frequency modulated phase-locked loop (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, Flash, or RAM from multiple bus masters
- 16-channel eDMA controller with multiple transfer request sources using DMA multiplexer
- Boot assist module (BAM) supports internal Flash programming via a serial link (CAN or SCI)
- Timer supports I/O channels providing a range of 16-bit input capture, output compare, and pulse width modulation functions (eMIOS)
- 2 analog-to-digital converters (ADC): one 10-bit and one 12-bit
- Cross Trigger Unit to enable synchronization of ADC conversions with a timer event from the eMIOS or PIT
- Up to 6 serial peripheral interface (DSPI) modules
- Up to 10 serial communication interface (LINFlex) modules
- Up to 6 enhanced full CAN (FlexCAN) modules with configurable buffers
- 1 inter-integrated circuit (I^2C) interface module
- Up to 149 configurable general purpose pins supporting input and output operations (package dependent)
- Real-Time Counter (RTC)
  - Clock source from internal 128 kHz or 16 MHz oscillator supporting autonomous wakeup with 1 ms resolution with maximum timeout of 2 seconds
  - Optional support for RTC with clock source from external 32 kHz crystal oscillator, supporting wakeup with 1 sec resolution and maximum timeout of 1 hour
- Up to 8 periodic interrupt timers (PIT) with 32-bit counter resolution
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class Two Plus
- Device/board boundary scan testing supported per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator (VREG) for regulation of input supply for all internal levels

Table of Contents

1 General description

The MPC5607B is a new family of next generation microcontrollers built on the Power Architecture™ embedded category. This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device.

The MPC5607B family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of body electronics applications within the vehicle. The advanced and cost-efficient host processor core of the MPC5607B automotive controller family complies with the Power Architecture embedded category and only implements the VLE (variable-length encoding) APU (Auxillary Processor Unit), providing improved code density. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 1. MPC5607B Family Comparison[1]

Feature	MPC5605B			MPC5606B		MPC5607B	
Package	100 LQFP	144 LQFP	176 LQFP	144 LQFP	176 LQFP	176 LQFP	208 MAP BGA[2]
CPU	e200z0h						
Execution speed[3]	Up to 64 MHz						
Code Flash	768 KB			1 MB		1.5 MB	
Data Flash	64 (4 x 16) Kbyte						
RAM	64 KB			80 KB		96 KB	
MPU	8-entry						
DMA	16 ch						
10-bit ADC	Yes						
dedicated[4]	7 ch	15 ch	29 ch	15 ch	29 ch		
shared with 12-bit ADC	19 ch						
12-bit ADC	Yes						
dedicated[5]	5 ch						
shared with 10-bit ADC	19 ch						
Total timer I/O[6] eMIOS	37 ch, 16-bit	64 ch, 16-bit					
Counter / OPWM / ICOC[7]	10 ch						
O(I)PWM / OPWFMB / OPWMCB / ICOC[8]	7 ch						
O(I)PWM / ICOC[9]	7 ch	14 ch					
OPWM / ICOC[10]	13 ch	33 ch					
SCI (LINFlex)	4	6	8	6	8	10	
SPI (DSPI)	3	5	6	5	6		
CAN (FlexCAN)	6						

Table 1. MPC5607B Family Comparison[1] (continued)

Feature	MPC5605B			MPC5606B		MPC5607B	
I^2C	1						
32 kHz oscillator	Yes						
GPIO[11]	77	121	149	121	149	149	
Debug	JTAG						N2+

1 Feature set dependent on selected peripheral multiplexing; table shows example.
2 208 MAPBGA package is for debug use only.
3 Based on 105 °C ambient operating temperature.
4 Not shared with 12-bit ADC, but possibly shared with other alternate functions.
5 Not shared with 10-bit ADC, but possibly shared with other alternate functions.
6 Refer to eMIOS section of device reference manual for information on the channel configuration and functions.
7 Each channel supports a range of modes including Modulus counters, PWM generation, Input Capture, Output Compare.
8 Each channel supports a range of modes including PWM generation with dead time, Input Capture, Output Compare.
9 Each channel supports a range of modes including PWM generation, Input Capture, Output Compare, Period and Pulse width measurement.
10 Each channel supports a range of modes including PWM generation, Input Capture, and Output Compare.
11 Maximum I/O count based on multiplexing with peripherals.

1.1 Block diagram

Figure 1 shows a top-level block diagram of the MPC5607B.

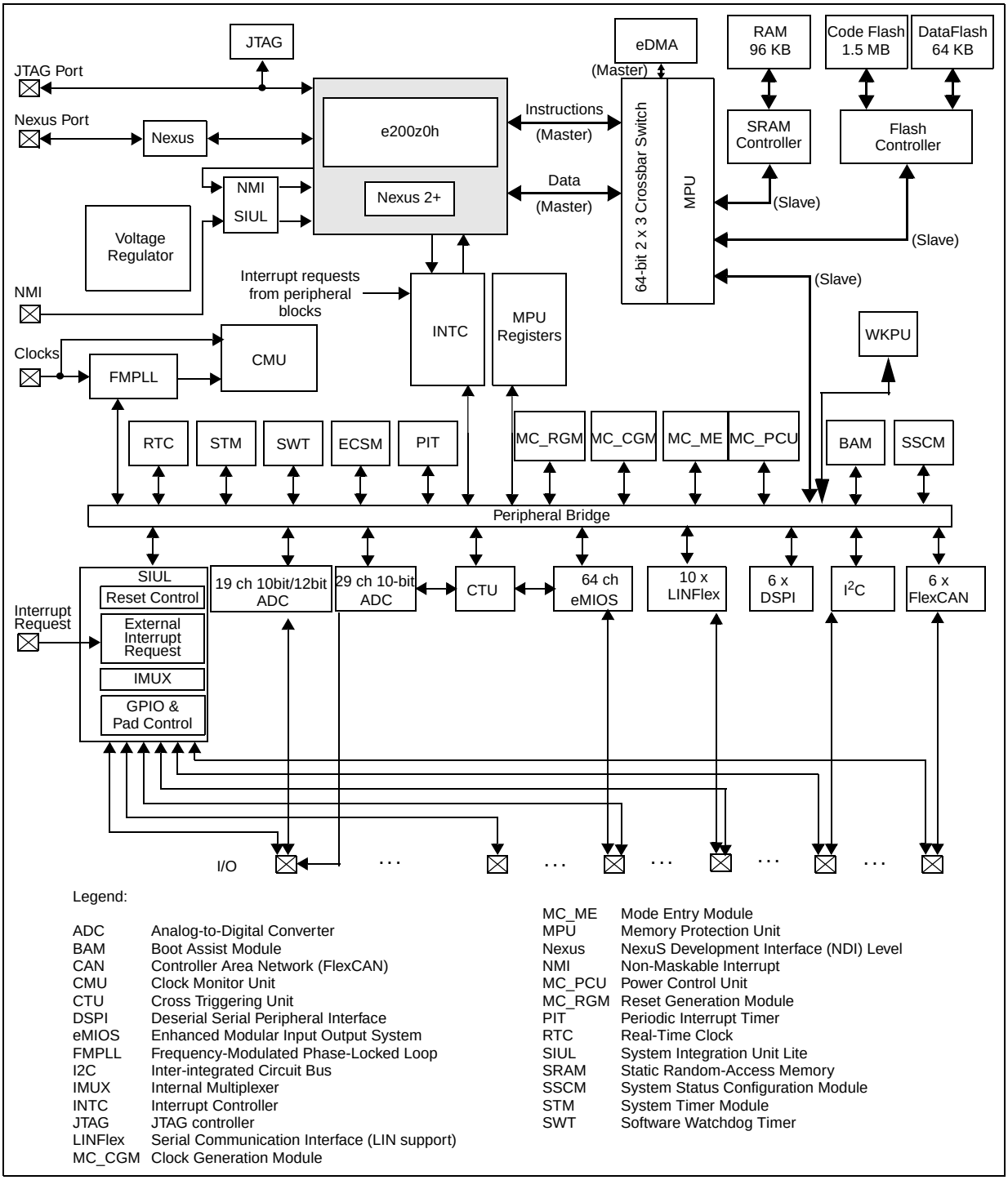


Figure 1. MPC5607B block diagram

Table 2 summarizes the functions of the blocks present on the MPC5607B.

Table 2. MPC5607B series block summary

Block	Function
Analog-to-digital converter (ADC)	Converts analog voltages to digital values
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Internal multiplexer (IMUX) SIU subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Inter-integrated circuit (I^2C™) bus	A two wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Memory protection unit (MPU)	Provides hardware access control for all memory references generated in a device
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Real-time counter (RTC)	A free running counter used for time keeping applications, the RTC can be configured to generate an interrupt at a predefined interval independent of the mode of operation (run mode or low-power mode)

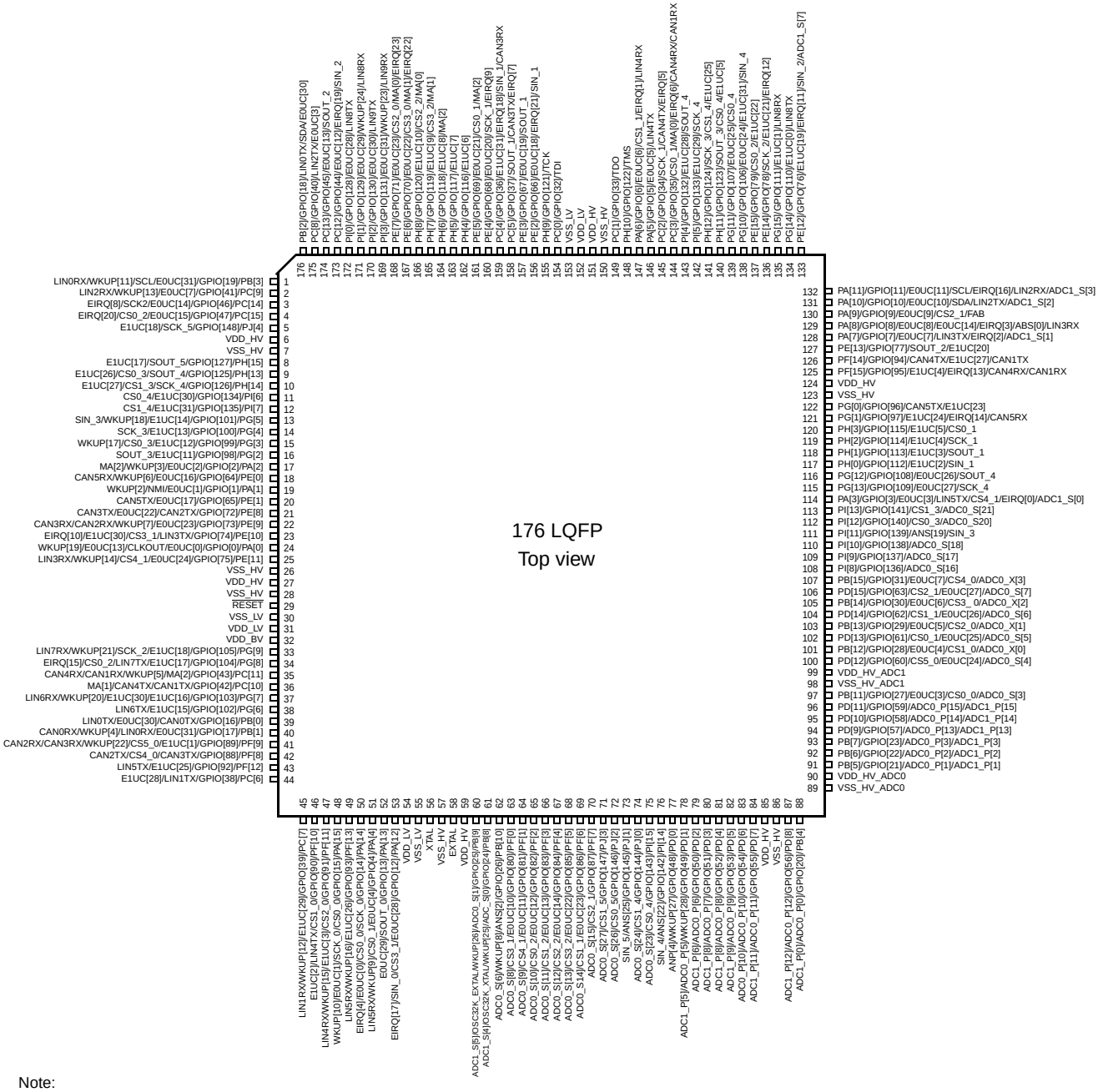
Table 2. MPC5607B series block summary (continued)

Block	Function
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System timer module (STM)	Provides a set of output compare events to support AutoSAR and operating system tasks

2 Package pinouts

The available LQFP pinouts and the 208 MAPBGA ballmap are provided in the following figures. For pin signal descriptions, please refer to the device reference manual.

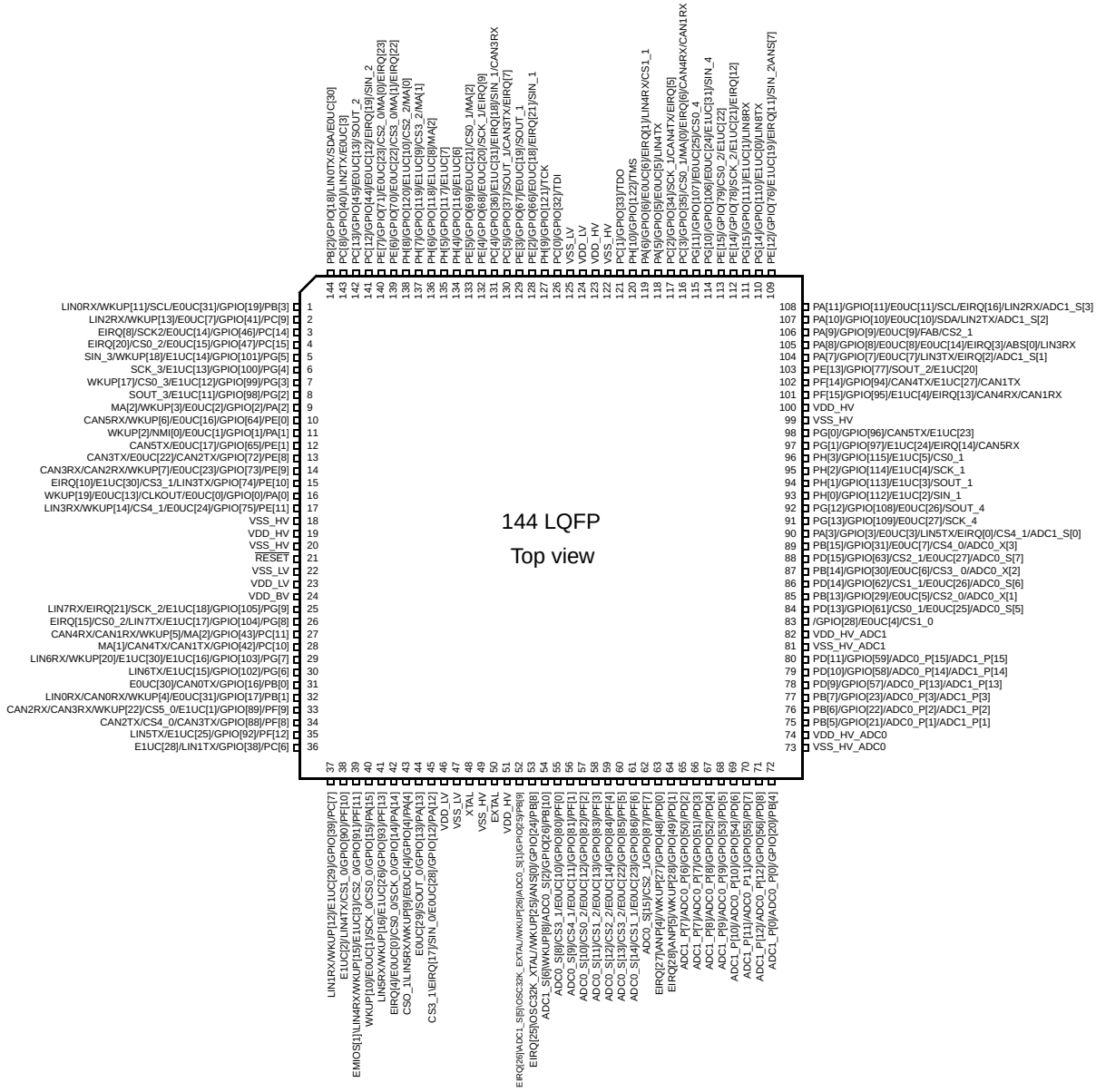
2.1 176LQFP pin configuration



Note:
Availability of port pin alternate functions depends on product selection.

Figure 2. 176 LQFP pin configuration (top view)

2.2 144LQFP pin configuration



Note:
Availability of port pin alternate functions depends on product selection.

Figure 3. 144 LQFP pin configuration (top view)

2.3 208MAPBGA pin configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	PC[8]	PC[13]	PH[15]	PJ[4]	PH[8]	PH[4]	PC[5]	PC[0]	PI[0]	PI[1]	PC[2]	PI[4]	PE[15]	PH[11]	NC	NC	A
B	PC[9]	PB[2]	PH[13]	PC[12]	PE[6]	PH[5]	PC[4]	PH[9]	PH[10]	PI[2]	PC[3]	PG[11]	PG[15]	PG[14]	PA[11]	PA[10]	B
C	PC[14]	VDD_HV	PB[3]	PE[7]	PH[7]	PE[5]	PE[3]	VSS_LV	PC[1]	PI[3]	PA[5]	PI[5]	PE[14]	PE[12]	PA[9]	PA[8]	C
D	PH[14]	PI[6]	PC[15]	PI[7]	PH[6]	PE[4]	PE[2]	VDD_LV	VDD_HV	NC	PA[6]	PH[12]	PG[10]	PF[14]	PE[13]	PA[7]	D
E	PG[4]	PG[5]	PG[3]	PG[2]									PG[1]	PG[0]	PF[15]	VDD_HV	E
F	PE[0]	PA[2]	PA[1]	PE[1]									PH[0]	PH[1]	PH[3]	PH[2]	F
G	PE[9]	PE[8]	PE[10]	PA[0]			VSS_HV	VSS_HV	VSS_HV	VSS_HV			VDD_HV	PI[12]	PI[13]	MSEO	G
H	VSS_HV	PE[11]	VDD_HV	NC			VSS_HV	VSS_HV	VSS_HV	VSS_HV			MDO3	MDO2	MDO0	MDO1	H
J	RESET	VSS_LV	NC	NC			VSS_HV	VSS_HV	VSS_HV	VSS_HV			PI[8]	PI[9]	PI[10]	PI[11]	J
K	EVTI	NC	VDD_BV	VDD_LV			VSS_HV	VSS_HV	VSS_HV	VSS_HV			VDD_HV_ADC1	PG[12]	PA[3]	PG[13]	K
L	PG[9]	PG[8]	NC	EVTO									PB[15]	PD[15]	PD[14]	PB[14]	L
M	PG[7]	PG[6]	PC[10]	PC[11]									PB[13]	PD[13]	PD[12]	PB[12]	M
N	PB[1]	PF[9]	PB[0]	VDD_HV	PJ[0]	PA[4]	VSS_LV	EXTAL	VDD_HV	PF[0]	PF[4]	VSS_HV_ADC1	PB[11]	PD[10]	PD[9]	PD[11]	N
P	PF[8]	PJ[3]	PC[7]	PJ[2]	PJ[1]	PA[14]	VDD_LV	XTAL	PB[10]	PF[1]	PF[5]	PD[0]	PD[3]	VDD_HV_ADC0	PB[6]	PB[7]	P
R	PF[12]	PC[6]	PF[10]	PF[11]	VDD_HV	PA[15]	PA[13]	PI[14]	XTAL	PF[3]	PF[7]	PD[2]	PD[4]	PD[7]	VSS_HV_ADC0	PB[5]	R
T	NC	NC	NC	MCKO	NC	PF[13]	PA[12]	PI[15]	EXTAL	PF[2]	PF[6]	PD[1]	PD[5]	PD[6]	PD[8]	PB[4]	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

NOTE: The 208 MAPBGA is available only as development package for Nexus 2+.

NC = Not connected

Figure 4. 208 MAPBGA configuration

3 Electrical characteristics

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

CAUTION

All of the following figures are indicative and must be confirmed during either silicon validation, silicon characterization or silicon reliability trial.

3.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 3 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 3. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 NVUSRO register

Portions of the device configuration, such as high voltage supply, oscillator margin, and watchdog enable/disable after reset are controlled via bit values in the Non-Volatile User Options Register (NVUSRO) register.

3.2.1 NVUSRO[PAD3V5V] field description

Table 4 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 4. PAD3V5V field description[1]

Value[2]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1 See the device reference manual for more information on the NVUSRO register.

2 '1' is delivery value. It is part of shadow Flash, thus programmable by customer.

The DC electrical characteristics are dependent on the PAD3V5V bit value.

3.2.2 NVUSRO[OSCILLATOR_MARGIN] field description

Table 5 shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 5. OSCILLATOR_MARGIN field description[1]

Value[2]	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

1 See the device reference manual for more information on the NVUSRO register.

2 '1' is delivery value. It is part of shadow Flash, thus programmable by customer.

The main external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value.

3.2.3 NVUSRO[WATCHDOG_EN] field description

Table 5 shows how NVUSRO[WATCHDOG_EN] controls the device configuration.

Table 6. WATCHDOG_EN field description[1]

Value[2]	Description
0	Disable after reset
1	Enable after reset

1 See the device reference manual for more information on the NVUSRO register.

2 '1' is delivery value. It is part of shadow Flash, thus programmable by customer.

3.3 Absolute maximum ratings

Table 7. Absolute maximum ratings

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	-0.3	6.0	V
V_{SS_LV}	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS}-0.1	V_{SS}+0.1	V
V_{DD_BV}	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	-0.3	6.0	V
			Relative to V_{DD}	-0.3	V_{DD}+0.3	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC 0, VSS_HV_ADC 1 (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS}-0.1	V_{SS}+0.1	V
V_{DD_ADC}	SR	Voltage on VSS_HV_ADC 0, VSS_HV_ADC 1 (ADC reference) with respect to ground (V_{SS})	—	-0.3	6.0	V
			Relative to V_{DD}	V_{DD} –0.3	V_{DD}+0.3	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	-0.3	6.0	V
			Relative to V_{DD}	V_{DD} –0.3	V_{DD}+0.3	

Table 7. Absolute maximum ratings (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	-10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	-50	50	
I_{AVGSEG}	SR	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		70	mA
			V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		64	
$T_{STORAGE}$	SR	Storage temperature	—	-55	150	°C

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

3.4 Recommended operating conditions

Table 8. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}[1]	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	3.0	3.6	V
V_{SS_LV}[2]	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS}–0.1	V_{SS}+0.1	V
V_{DD_BV}[3]	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	3.0	3.6	V
			Relative to V_{DD}	V_{DD}–0.1	V_{DD}+0.1	

Table 8. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS}–0.1	V_{SS}+0.1	V
V_{DD_ADC}[4]	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) with respect to ground (V_{SS})	—	3.0[5]	3.6	V
			Relative to V_{DD}	V_{DD}–0.1	V_{DD}+0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS}–0.1	—	V
			Relative to V_{DD}	—	V_{DD}+0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	V_{DD} slope to ensure correct power up[6]	—	—	0.25	V/µs
T_A	SR	Ambient temperature under bias	f_{CPU} < 64 MHz	–40	125	°C
T_J	SR	Junction temperature under bias	—	–40	150	

1 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair

2 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

3 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics).

4 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

5 Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL}, device is reset.

6 Guaranteed by device validation

Table 9. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}[1]	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
V_{SS_LV}[3]	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS}-0.1	V_{SS}+0.1	V
V_{DD_BV}[4]	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
			Relative to V_{DD}	V_{DD}-0.1	V_{DD}+0.1	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS}-0.1	V_{SS}+0.1	V

Table 9. Recommended operating conditions (5.0 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{DD_ADC}[5]	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
			Relative to V_{DD}	V_{DD}-0.1	V_{DD}+0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS}-0.1	-	V
			Relative to V_{DD}	-	V_{DD}+0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	-5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	-50	50	
TV_{DD}	SR	V_{DD} slope to ensure correct power up[6]	—	—	0.25	V/µs
			—	3	—	V/s
T_{A} C-Grade Part	SR	Ambient temperature under bias	f_{CPU} < 64 MHz	–40	85	°C
T_{J} C-Grade Part	SR	Junction temperature under bias	—	–40	110	
T_{A} V-Grade Part	SR	Ambient temperature under bias	f_{CPU} < 64 MHz	–40	105	
T_{J} V-Grade Part	SR	Junction temperature under bias	—	–40	130	
T_{A} M-Grade Part	SR	Ambient temperature under bias	f_{CPU} < 60 MHz	–40	125	
T_{J} M-Grade Part	SR	Junction temperature under bias	—	–40	150	

1 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair

2 Full device operation is guaranteed by design when the voltage drops below 4.5V down to 3.6V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.

3 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair

4 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics). This decoupling need to be increased as recommended in Section 3.5.1, “External ballast resistor recommendations incase external ballast resistor is planned to be used.

5 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair

6 Guaranteed by device validation

NOTE

RAM data retention is guaranteed wi‘th V_{DD_LV} not below 1.08 V.

3.5 Thermal characteristics

3.5.1 External ballast resistor recommendations

External ballast resistor on V_{DD_BV} pin helps in reducing the overall power dissipation inside the device. This resistor is required only when maximum power consumption exceeds the limit imposed by package thermal characteristics.

As stated in Table 10 LQFP thermal characteristics, considering thermal resistance of LQFP144 as 48.3 °C/W, at ambient T_A = 125 °C, the junction temp T_j will cross 150 °C if total power dissipation > (150 - 125)/48.3 = 517 mW. Therefore, total device current I_{DDMAX} at 125 °C/5.5V must not exceed 94.1 mA (i.e. PD/VDD). Assuming an average $I_{DD}(V_{DD\_HV})$ of 15-20 mA consumption typically during device RUN mode, the LV domain consumption $I_{DD}(V_{DD\_BV})$ is thus limited to I_{DDMAX} - $I_{DD}(V_{DD\_HV})$ i.e. 80 mA.

Therefore, respecting the maximum power allowed as explained in Section 3.5.2, “Package thermal characteristics, it is recommended to use this resistor only in the 125 °C/5.5V operating corner as per the following guidelines:

- If $I_{DD}(V_{DD\_BV})$ < 80 mA, then no resistor is required.
- If 80 mA < $I_{DD}(V_{DD\_BV})$ < 90 mA, then 4 Ohm resistor can be used along with 14.7 µf decoupling.
- If $I_{DD}(V_{DD\_BV})$ > 90 mA, then 8 Ohm resistor can be used along with 33 µf decoupling.

Using resistance in the range of 4-8 Ohm, the gain will be around 10-20% of total consumption on V_{DD_BV}. For example, if 8 Ohm resistor is used, then power consumption when $I_{DD}(V_{DD\_BV})$ is 110 mA is equivalent to power consumption when $I_{DD}(V_{DD\_BV})$ is 90 mA (approximately) when resistor not used.

3.5.2 Package thermal characteristics

Table 10. LQFP thermal characteristics[1]

Symbol		C	Parameter	Conditions[2]	Pin count	Value[3]			Unit
						Min	Typ	Max	
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection[4]	Single-layer board—1s	100	—	—	64	°C/W
					144	—	—	64	
					176	—	—	64	
				Four-layer board—2s2p	100	—	—	49.7	
					144	—	—	48.3	
					176	—	—	47.3	

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C.

3 All values need to be confirmed during device validation.

4 Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package. When Greek letters are not available, the symbols are typed as R_{thJA} and R_{thJMA}.

Table 11. 208 MAPBGA thermal characteristics[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	—	Thermal resistance, junction-to-ambient natural convection[2]	Single-layer board—1s	TBD	°C/W
				Four-layer board—2s2p		

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package. When Greek letters are not available, the symbols are typed as R_{thJA} and R_{thJMA}.

3.5.3 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using Equation 1:

$$T_J = T_A + (P_D \times R_{\theta JA}) \quad \textit{Eqn. 1}$$

Where:

T_A is the ambient temperature in °C.

$R_{\theta JA}$ is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$).

P_{INT} is the product of I_{DD} and V_{DD}, expressed in watts. This is the chip internal power.

$P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications, $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273\ °C) \quad \textit{Eqn. 2}$$

Therefore, solving equations 1 and 2:

$$K = P_D \times (T_A + 273\ °C) + R_{\theta JA} \times P_D^2 \quad \textit{Eqn. 3}$$

Where:

K is a constant for the particular part, which may be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations 1 and 2 iteratively for any value of T_A.

3.6 I/O pad electrical characteristics

3.6.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads - are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads - provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.

- Fast pads - provide maximum speed. These are used for improved Nexus debugging capability.
- Input only pads - are associated with ADC channels and 32 kHz low power external crystal oscillator providing low input leakage.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

3.6.2 I/O input DC characteristics

Table 12 provides input DC electrical characteristics as described in Figure 5.

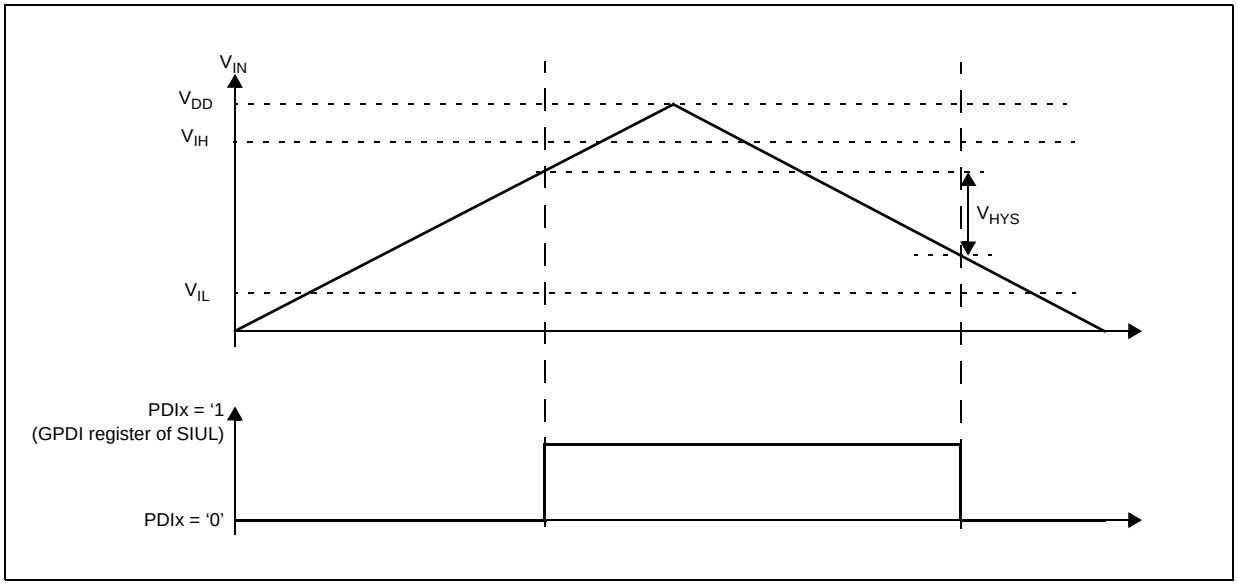


Figure 5. I/O input DC electrical characteristics definition

Table 12. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	$V_{DD}+0.4$	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—	–0.4	—	$0.35V_{DD}$	
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	

Table 12. I/O input DC electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
I_{LKG}	CC	P	Digital input leakage	No injection on adjacent pin	T_A = –40 °C	—	2	—	nA
		P			T_A = 25 °C	—	2	—	
		D			T_A = 105 °C	—	12	500	
		P			T_A = 125 °C	—	70	1000	
W_{FI}	SR	P	Width of input pulse surely filtered by analog filter[3]	—		—	—	40	ns
W_{NFI}	SR	P	Width of input pulse surely not filtered by analog filter[3]	—		1000	—	—	ns

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 Analog filters are available on all wakeup lines.

3.6.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 13 provides weak pull figures. Both pull-up and pull-down resistances are supported.
- Table 15 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 16 provides output driver characteristics for I/O pads when in MEDIUM configuration.
- Table 14 provides output driver characteristics for I/O pads when in FAST configuration.

Table 13. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$\|I_{WPU}\|$	CC	P	Weak pull-up current absolute value	$V_{IN} = V_{IL}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1[2]	10	—	250	
		P		$V_{IN} = V_{IL}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
$\|I_{WPD}\|$	CC	P	Weak pull-down current absolute value	$V_{IN} = V_{IH}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1	10	—	250	
		P		$V_{IN} = V_{IH}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 14. FAST configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level FAST configuration	Push Pull	I_{OH} = –14mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –7mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –11mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD}–0.8	—	—	
V_{OL}	CC	P	Output low level FAST configuration	Push Pull	I_{OL} = 14mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 7mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 11mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.6.4 Output pin transition times

Table 15. Output pin transition times

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
T_{tr}	CC	D	Output transition time output pin[3] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
T_{tr}	CC	D	Output transition time output pin[3] MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	

Table 15. Output pin transition times (continued)

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
T_{tr}	CC	D	Output transition time output pin[3] FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 C_L includes device and package capacitances (C_{PKG} < 5 pF).

3.6.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 16.

Table 17 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Table 16. I/O supply segments

Package	Supply segment							
	1	2	3	4	5	6	7	8
208 MAPBGA[1]	Equivalent to 176 LQFP segment pad distribution						MCKO	MDOn /MSEO
176 LQFP	pin7– pin27	pin28 – pin57	pin59 – pin85	pin86 – pin123			pin124 – pin150	pin151 – pin6
144 LQFP	pin20 – pin49	pin51 – pin99	pin100 – pin122	pin 123 – pin19	—	—	—	—
100 LQFP	pin16 – pin35	pin37 – pin69	pin70 – pin83	pin84 – pin15	—	—	—	—

1 208 MAPBGA available only as development package for Nexus2+

Table 17. I/O consumption

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
I_{DYNSEG}	SR	D	Sum of all the dynamic and static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	110	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	
I_{SWTSLW}[3]	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}[3]	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{SWTFST}[3]	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	

Table 17. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
I_{RMSSLW}	CC	D	Root medium square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	
I_{RMSMED}	CC	D	Root medium square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C_L = 25 pF, 40 MHz		—	—	13.4	
				C_L = 100 pF, 13 MHz		—	—	18.3	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C_L = 25 pF, 40 MHz		—	—	8.5	
				C_L = 100 pF, 13 MHz		—	—	11	

Table 17. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
I_{RMSFST}	CC	D	Root medium square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10 %, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

3.7 $\overline{\text{nRSTIN}}$ electrical characteristics

The device implements a dedicated bidirectional RESET pin.

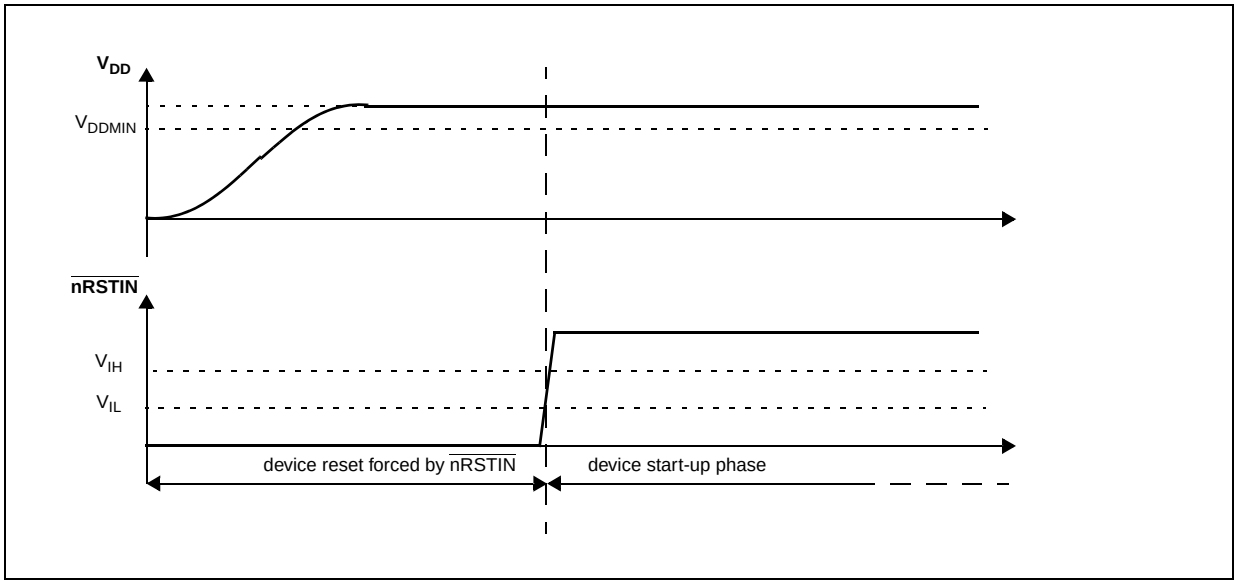


Figure 6. Start-up reset requirements

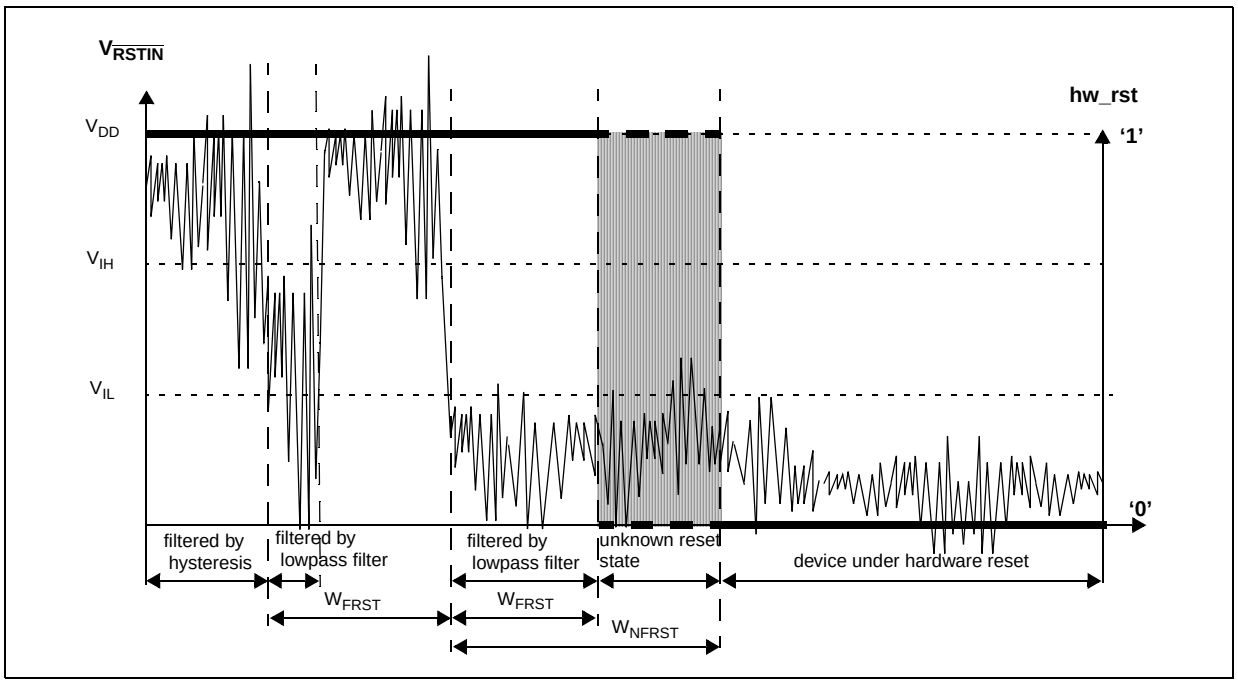


Figure 7. Noise filtering on reset signal

Table 18. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	$V_{DD}+0.4$	V
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
				Push Pull, I_{OL} = 1mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[3]	—	—	$0.1V_{DD}$	
				Push Pull, I_{OL} = 1mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
T_{tr}	CC	D	Output transition time output pin[4] MEDIUM configuration	C_L = 25pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{nRSTIN}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{nRSTIN}}$ input not filtered pulse	—	1000	—	—	ns
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[5]	10	—	250	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of the device reference manual).

4 C_L includes device and package capacitance (C_{PKG} < 5 pF).

5 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.8 Power management electrical characteristics

3.8.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply V_{DD_BV}. The regulator itself is supplied by the common I/O supply V_{DD}. The following supplies are involved:

- HV: High voltage external power supply for voltage regulator module. This must be provided externally through V_{DD} power pin.
- BV: High voltage external power supply for internal ballast module. This must be provided externally through V_{DD_BV} power pin. Voltage values should be aligned with V_{DD}.
- LV: Low voltage internal power supply for core, FMPLL and Flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
  - LV_COR: Low voltage supply for the core. It is also `used to provide supply for FMPLL through double bonding.
  - LV_CFLA: Low voltage supply for code Flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_DFLA: Low voltage supply for data Flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_PLL: Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

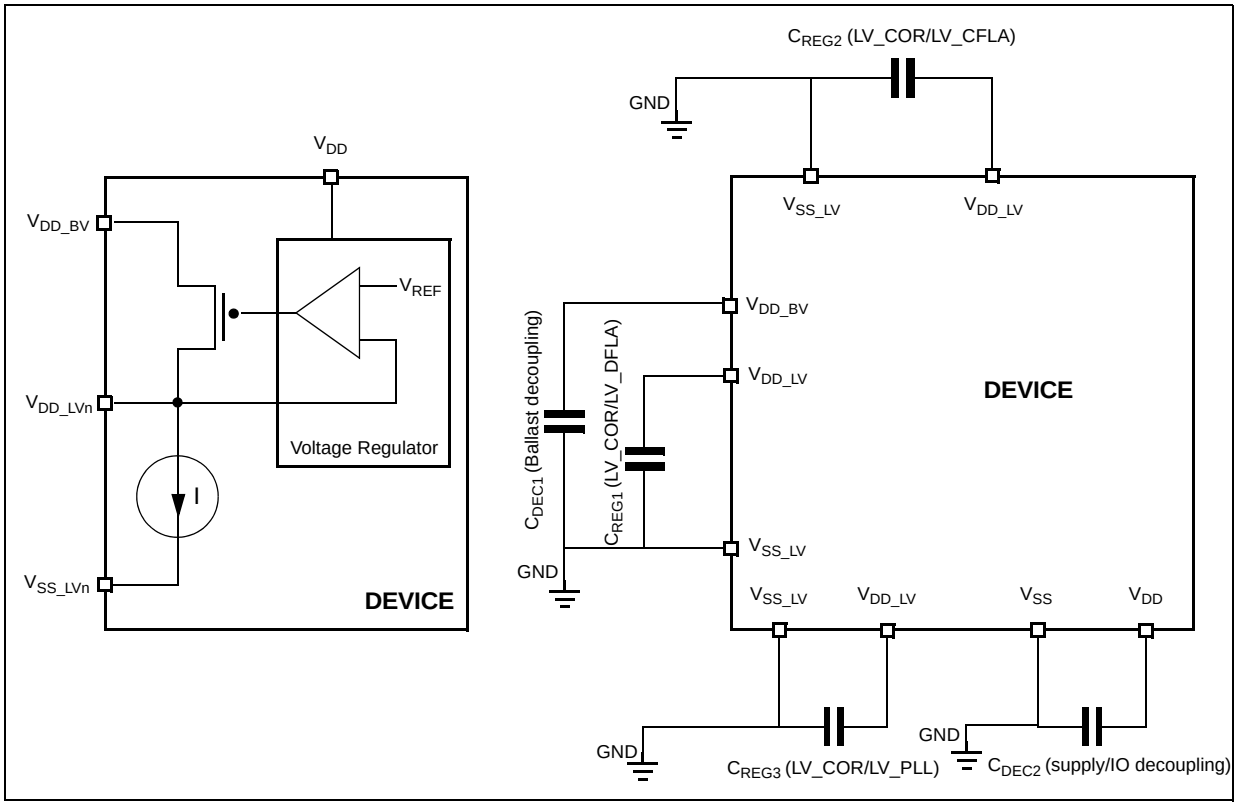


Figure 8. Voltage regulator capacitance connection

The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

Each decoupling capacitor must be placed between each of the three V_{DD_LV}/V_{SS_LV} supply pairs to ensure stable voltage (see Section 3.4, "Recommended operating conditions).

Table 19. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
C_{REGn}	SR	—	Internal voltage regulator external capacitance	—	200	—	330	nF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	—	—	—	0.2	W
C_{DEC1}	SR	—	Decoupling capacitance[3,4] ballast	V_{DD_BV}/V_{SS_LV} pair	400	470[5]	—	nF
C_{DEC2}	SR	—	Decoupling capacitance regulator supply	V_{DD}/V_{SS} pair	10	100	—	nF
V_{MREG}	CC	P	Main regulator output voltage	Before trimming	—	1.32	—	V
				After trimming	—	1.28	—	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	150	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low power regulator output voltage	After trimming	—	1.23	—	V
I_{LPREG}	SR	—	Low power regulator current provided to V_{DD_LV} domain	—	—	—	15	mA
$I_{LPREGINT}$	CC	D	Low power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	5	TBD	
V_{ULPREG}	CC	P	Ultra low power regulator output voltage	Post trimming	—	1.23	—	V
I_{ULPREG}	SR	—	Ultra low power regulator current provided to V_{DD_LV} domain	—	—	—	5	mA
$I_{ULPREGINT}$	CC	D	Ultra low power regulator module current consumption	I_{ULPREG} = 5 mA; T_A = 55 °C	—	—	100	µA
				I_{ULPREG} = 0 mA; T_A = 55 °C	—	2	TBD	
$I_{VREGREF}$	CC	D	Main LVDs and reference current consumption (low power and main regulator switched off)	T_A = 55 °C	—	17	—	µA
$I_{VREDLVD12}$	CC	D	Main LVD current consumption (switch-off during standby)	T_A = 55 °C	—	2	TBD	µA
I_{DD_BV}	CC	D	In-rush current on V_{DD_BV} during power-up	—	—	—	400[6]	mA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

[3] This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.

[4] In case external ballast resistor is planned to be used, then to avoid a LVD reset during standby mode exit, the following configuration need to be respected.
- for 8 ohm ballast resistor, decoupling cap of 33 µf is required.
- for 4 ohm ballast resistor, decoupling cap of 14.7µf is required.

These values are only after preliminary validation and are subject to change.

[5] External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in operating range.

[6] In-rush current is seen only for short time during power-up and on standby exit (max 20µs, depending on external capacitances to be load)

3.8.2 Voltage monitor electrical characteristics

The device implements a Power-on Reset module to ensure correct power-up initialization, as well as four low voltage detectors to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV3B monitors VDD_BV to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10% range
- LVDLVCOR monitors power domain No. 1
- LVDLVBKP monitors power domain No. 0

NOTE

When enabled, power domain No. 2 is monitored through LVD_DIGBKP.

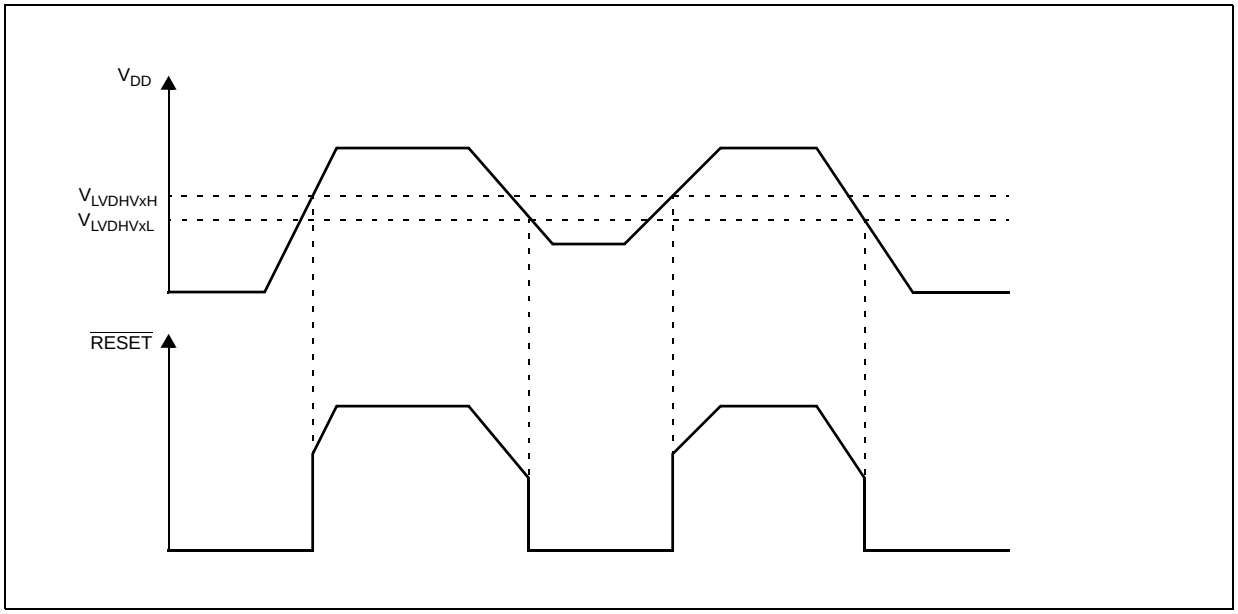


Figure 9. Low voltage monitor vs reset

Table 20. Low voltage monitor electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit	Symbol
V_{PORUP}	SR	P	Supply for functional POR module	T_A = 25 °C, after trimming	1.0	—	5.5	V	V_{PORUP}
V_{PORH}	CC	P	Power-on reset threshold		1.5	—	2.6		V_{PORH}
$V_{LVDHV3H}$	CC	T	LVDHV3 low voltage detector high threshold		—	—	2.95		$V_{LVDHV3H}$
$V_{LVDHV3L}$	CC	P	LVDHV3 low voltage detector low threshold		2.7	—	2.9		$V_{LVDHV3L}$
$V_{LVDHV3BH}$	CC	P	LVDHV3B low voltage detector high threshold		—	—	2.95		$V_{LVDHV3BH}$
$V_{LVDHV3BL}$	CC	P	LVDHV3B L low voltage detector low threshold		2.7	—	2.9		$V_{LVDHV3BL}$
$V_{LVDHV5H}$	CC	T	LVDHV5 low voltage detector high threshold		—	—	4.5		$V_{LVDHV5H}$
$V_{LVDHV5L}$	CC	P	LVDHV5 low voltage detector low threshold		3.8	—	4.4		$V_{LVDHV5L}$
$V_{LVDLVCORL}$	CC	P	LVDLVCOR low voltage detector low threshold		1.07	—	1.11		$V_{LVDLVCORL}$

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

[2] All values need to be confirmed during device validation.

3.9 Low voltage domain power consumption

Table 21 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 21. Low voltage power domain electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{DDMAX}[2]	CC	D	RUN mode maximum average current	—		—	115	140[3]	mA
I_{DDRUN}[4]	CC	T	RUN mode typical average current[5]	—		—	80	100	mA
		P		—		—	TBD	TBD	
I_{DDHALT}	CC	P	HALT mode current[6]	—		—	8	TBD	mA
I_{DDSTOP}	CC	P	STOP mode current[7]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	350	900[8]	µA
		D			T_A = 55 °C	—	750	—	
		D			T_A = 85 °C	—	2	—	mA
		D			T_A = 105 °C	—	4	—	
		P			T_A = 125 °C	—	9	TBD[8]	
$I_{DDSTDBY2}$	CC	P	STANDBY 2 mode current[9]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	30	100	µA
		D			T_A = 55 °C	—	TBD	—	
		D			T_A = 85 °C	—		—	
		D			T_A = 105 °C	—		—	
		P			T_A = 125 °C	—		TBD	

Table 21. Low voltage power domain electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$I_{DDSTDBY1}$	CC	T	STANDBY 1 mode current[10]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	20	60	µA
		D			T_A = 55 °C	—	TBD	—	
		D			T_A = 85 °C	—		—	
		D			T_A = 105 °C	—		—	
		D			T_A = 125 °C	—	280	TBD	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 Running consumption is given on voltage regulator supply (V_{DDREG}). It does not include consumption linked to I/Os toggling. This value is **highly** dependent on the application. The given value is thought to be a **worst case value** with all peripherals running, and code fetched from code flash while modify operation on-going on data flash. It is to be noticed that this value can be significantly reduced by application: switch-off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.

3 Higher current may be sinked by device during power-up and standby exit. please refer to in rush current on Table 19.

4 RUN current measured with typical application with accesses on both flash and RAM.

5 Only for the “P” classification: Code fetched from RAM: Serial IPs CAN and LIN in loop back mode, DSPi as Master, PLL as system Clock (4 x Multiplier) peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled.

6 Data Flash Power Down. Code Flash in Low Power. RC-osc128kHz & RC-OSC 16MHz on. 10MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but not reception or transmission), instances: 4, 5, 6 clock gated. LINFlex: instances: 0, 1, 2 ON (clocked but not reception or transmission), instance: 3 clock gated. eMIOS: instance: 0 ON (16 channels on PA[0]-PA[11] and PC[12]-PC[15]) with PWM 20KHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication). RTC/API ON.PIT ON. STM ON. ADC ON but not conversion except 2 analogue watchdog

7 Only for the “P” classification: No clock, RC 16MHz off, RC128kHz on, PLL off, HPvreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.

8 When going from RUN to STOP mode and the core consumption is > 6 mA , it is normal operation for the main regulator module to be kept on by the on-chip current monitoring circuit. This is most likely to occur with junction temperatures exceeding 125 °C and under these circumstances , it is possible for the current to initially exceed the maximum STOP specification by up to 2 mA. After entering stop, the application junction temperature will reduce to the ambient level and the main regulator will be automatically switched off when the load current is below 6 mA.

9 Only for the “P” classification: ULPreg on, HP/LPVreg off, 32 KB RAM on, device configured for minimum consumption, all possible modules switched-off.

10 ULPreg on, HP/LPVreg off, 8KB RAM on, device configured for minimum consumption, all possible modules switched-off.

3.10 Flash memory electrical characteristics

3.10.1 Program/Erase characteristics

Table 22 shows the program and erase characteristics.

Table 22. Program and erase specifications

Symbol		C	Parameter	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$T_{dwprogram}$	CC	C	Double word (64 bits) program time[4]	—	22	TBD	500	µs
$T_{16Kpperase}$			16 KB block pre-program and erase time	—	300	500	5000	ms
$T_{32Kpperase}$			32 KB block pre-program and erase time	—	400	600	5000	ms
$T_{128Kpperase}$			128 KB block pre-program and erase time	—	800	1300	7500	ms

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

Table 23. Flash module life

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Typ	
P/E	CC	C	Number of program/erase cycles per block for 16 Kbyte blocks over the operating temperature range (T_J)	—	100,000	—	cycles
P/E	CC	C	Number of program/erase cycles per block for 32 Kbyte blocks over the operating temperature range (T_J)	—	10,000	100,000[1]	cycles
P/E	CC	C	Number of program/erase cycles per block for 128 Kbyte blocks over the operating temperature range (T_J)	—	1,000	100,000[1]	cycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature[2]	Blocks with 0–1,000 P/E cycles	20	—	years
				Blocks with 10,000 P/E cycles	10	—	years
				Blocks with 100,000 P/E cycles	5	—	years

1 To be confirmed

2 Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 24. Flash read access timing

Symbol		C	Parameter	Conditions[1]	Max	Unit
f_{READ}	CC	P	Maximum frequency for Flash reading	2 wait states	64	MHz
		C		1 wait state	40	
		C		0 wait states	20	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

3.10.2 Flash power supply DC characteristics

Table 25 shows the power supply DC characteristics on external supply.

Table 25. Flash power supply DC electrical characteristics

Symbol		Parameter	Conditions[1]		Value[2]			Unit
					Min	Typ	Max	
I_{CFREAD}[3]	CC	Sum of the current consumption on V_{DDHV} and V_{DDBV} on read access	Flash module read f_{CPU} = 64 MHz[4]	Code Flash			33	mA
I_{DFREAD}[3]				Data Flash			33	
I_{CFMOD}[3]	CC	Sum of the current consumption on V_{DDHV} and V_{DDBV} on matrix modification (program/erase)	Program/ Erase on-going while reading Flash registers f_{CPU} = 64 MHz[4]	Code Flash			52	mA
I_{DFMOD}[3]				Data Flash			33	
I_{CFLPW}[3]	CC	Sum of the current consumption on V_{DDHV} and V_{DDBV} during Flash low power mode		Code Flash			1.1	mA
I_{DFLPW}[3]				Data Flash			900	µA
I_{CFPWD}[3]	CC	Sum of the current consumption on V_{DDHV} and V_{DDBV} during Flash power down mode		Code Flash			150	µA
I_{DFPWD}[3]				Data Flash			150	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 / 125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 Data based on characterization results, not tested in production

4 f_{CPU} 64 MHz can be achieved only at up to 105 °C

3.10.3 Start-up/Switch-off timings

Table 26. Start-up time/Switch-off time

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$T_{FLARSTEXIT}$	CC	T	Delay for Flash module to exit reset mode	—	—	—	125	µs
$T_{FLALPEXIT}$	CC	T	Delay for Flash module to exit low-power mode	—	—	—	0.5	
$T_{FLAPDEXIT}$	CC	T	Delay for Flash module to exit power-down mode	—	—	—	30	
$T_{FLALPENTRY}$	CC	T	Delay for Flash module to enter low-power mode	—	—	—	0.5	
$T_{FLAPDENTRY}$	CC	T	Delay for Flash module to enter power-down mode	—	—	—	1.5	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

3.11 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

3.11.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for the application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:
  - Corrupted program counter

— Unexpected reset
— Critical data corruption (control registers...)

- Prequalification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

3.11.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC61967-1 standard, which specifies the general conditions for EMI measurements.

Table 27. EMI radiated emission measurement[1,2]

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
—	SR	—	Scan range	—		0.150		1000	MHz
f_{CPU}	SR	—	Operating frequency	—		—	64	—	MHz
V_{DD_LV}	SR	—	LV operating voltages	—		—	1.28	—	V
S_{EMI}	CC	T	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP144 package Test conforming to IEC 61967-2, f_{OSC} = 8 MHz/f_{CPU} = 64 MHz	No PLL frequency modulation	—	—	18	dBµV
					± 2% PLL frequency modulation	—	—	14[3]	dBµV

1 EMI testing and I/O port waveforms per IEC 61967-1, -2, -4

2 For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

3 All values need to be confirmed during device validation

3.11.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

3.11.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts×(n+1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 28. ESD absolute maximum ratings[1,2]

Symbol	Ratings	Conditions	Class	Max value[3]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	
				750 (corners)	

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3 Data based on characterization results, not tested in production

3.11.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 29. Latch-up results

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.12 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. Figure describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 30 provides the parameter description of 4 MHz to 16 MHz crystals used for the design simulations.

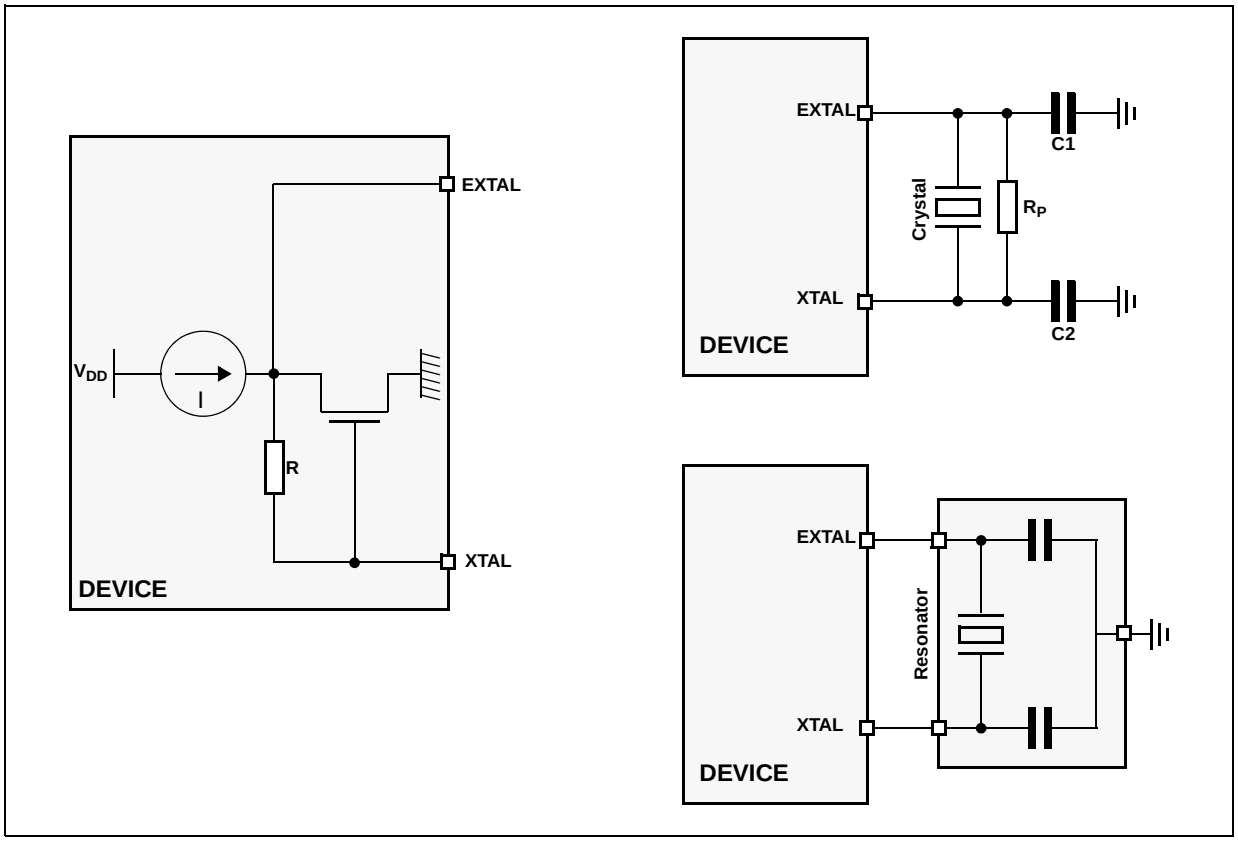


Figure 10. Crystal oscillator and resonator connection scheme

NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

Table 30. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance ESR Ω	Crystal motional capacitance (C_m) fF	Crystal motional inductance (L_m) mH	Load on xtalin/xtalout C1 = C2 (pF)[1]	Shunt capacitance between xtalout and xtalin C0[2] (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00

1 The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.

2 The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

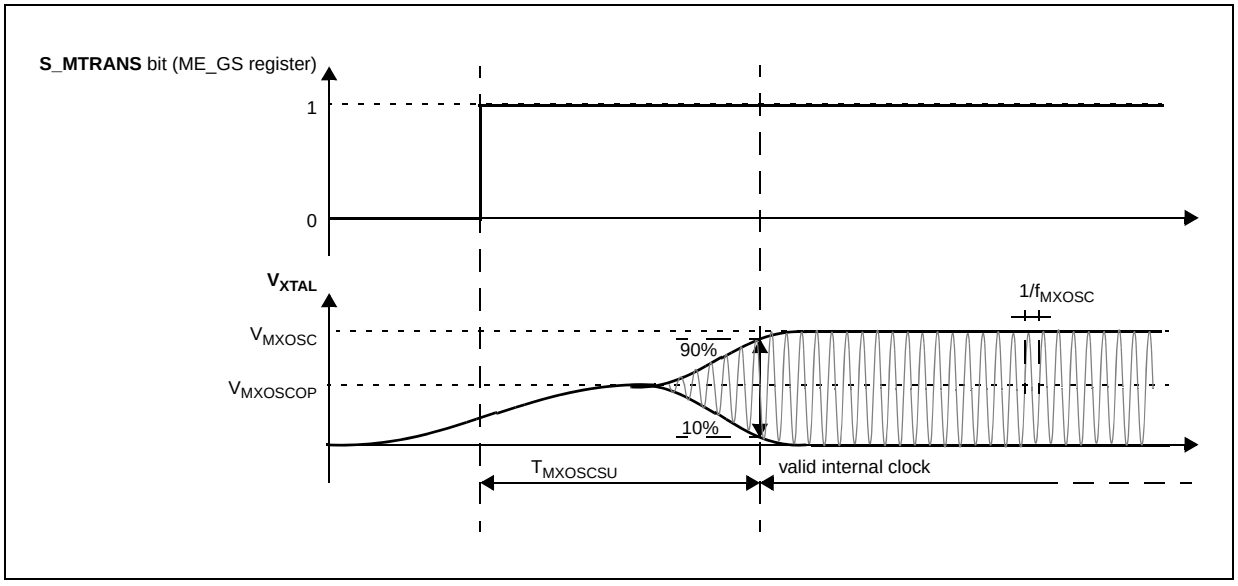


Figure 11. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

Table 31. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{FXOSC}	SR	—	Fast external crystal oscillator frequency	—	4.0	—	16.0	MHz
g_{mFXOSC}	CC	C	Fast external crystal oscillator transconductance	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 0	2.2	—	8.2	mA/V
	CC	P		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 0	2.0	—	7.4	
	CC	C		V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 1	2.7	—	9.7	
	CC	C		V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 1	2.5	—	9.2	
V_{FXOSC}	CC	T	Oscillation amplitude at EXTAL	f_{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	1.3	—	—	V
				f_{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	1.3	—	—	
$V_{FXOSCOP}$	CC	P	Oscillation operating point	—	—	0.95		V
I_{FXOSC},[3]	CC	T	Fast external crystal oscillator consumption	—	—	2	3	mA

Table 31. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
$T_{FXOSCSU}$	CC	T	Fast external crystal oscillator start-up time	f_{OSC} = 4 MHz, OSCILLATOR_MARGIN = 0	—	—	6	ms
				f_{OSC} = 16 MHz, OSCILLATOR_MARGIN = 1	—	—	1.8	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	Oscillator bypass mode	$0.65V_{DD}$	—	V_{DD}+0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	Oscillator bypass mode	–0.4	—	$0.35V_{DD}$	V

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals)

3.13 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.

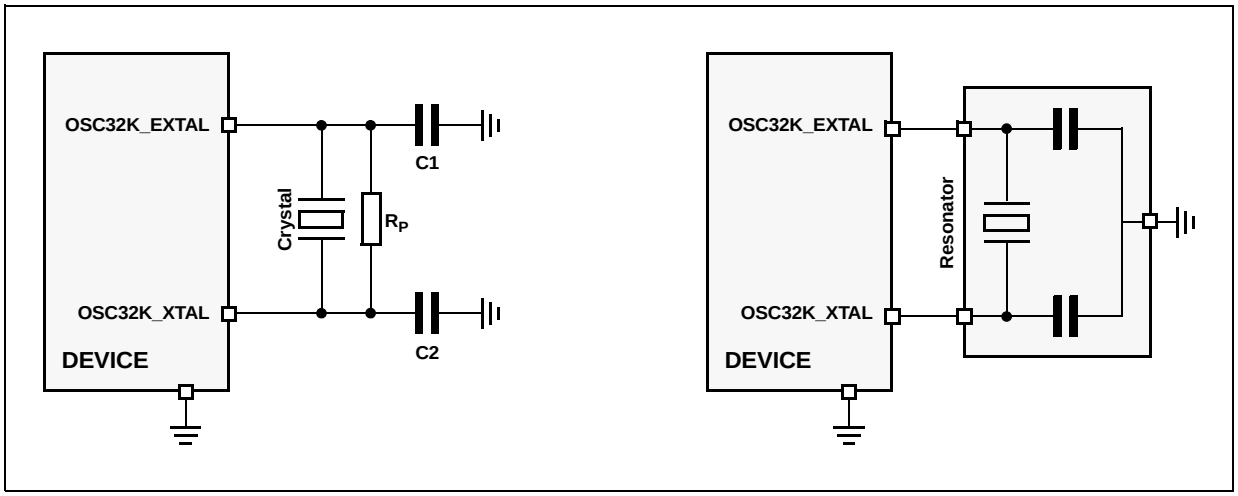


Figure 12. Crystal oscillator and resonator connection scheme

NOTE

OSC32K_XTAL/OSC32K_EXTAL must not be directly used to drive external circuits.

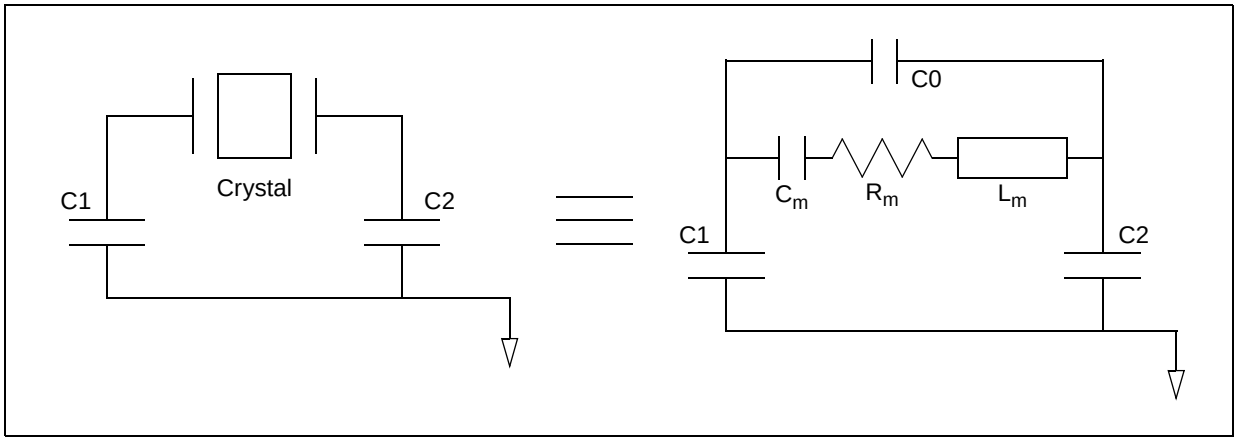


Figure 13. Equivalent circuit of a quartz crystal

Table 32. Crystal motional characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
L_m	Motional inductance	—	—	11.796	—	KH
C_m	Motional capacitance	—	—	2	—	fF
C1/C2	Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground[2]	—	18	—	28	pF
R_m[3]	Motional resistance	AC coupled @ C0 = 2.85 pF[4]	—	—	65	kW
		AC coupled @ C0 = 4.9 pF[4]	—	—	50	
		AC coupled @ C0 = 7.0 pF[4]	—	—	35	
		AC coupled @ C0 = 9.0 pF[4]	—	—	30	

1 The crystal used is Epson Toyocom MC306.

2 This is the recommended range of load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.

3 Maximum ESR (R_m) of the crystal is 50 kΩ

4 C0 Includes a parasitic capacitance of 2.0 pF between OSC32K_XTAL and OSC32K_EXTAL pins

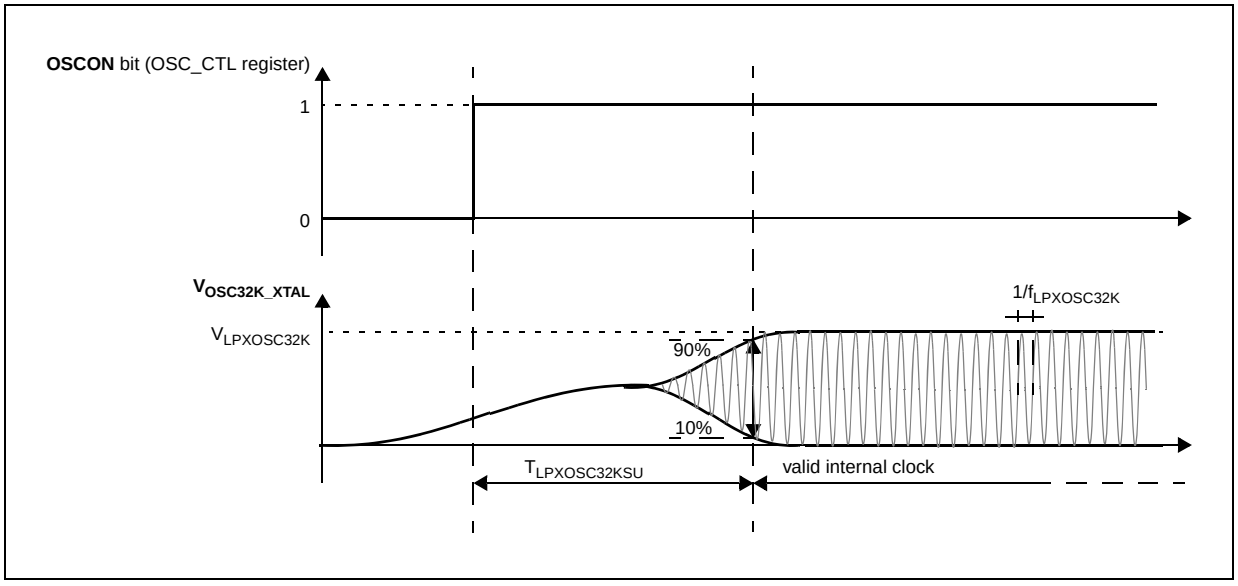


Figure 14. Slow external crystal oscillator (32 kHz) electrical characteristics

Table 33. Slow external crystal oscillator (32 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{SXOSC}	SR	—	Slow external crystal oscillator frequency	—	32	32.768	40	kHz
g_{mSXOSC}	CC	—	Slow external crystal oscillator transconductance	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	TBD			mA/V
				V_{DD} = 5.0 V ± 10% PAD3V5V = 0	TBD			
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	TBD			
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	TBD			
V_{SXOSC}	CC	T	Oscillation amplitude	—	—	2.1	—	V
$I_{SXOSCBIAS}$	CC	T	Oscillation bias current	—	TBD			µA
I_{SXOSC}	CC	T	Slow external crystal oscillator consumption	—	—	—	8	µA
$T_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	—	2[3]	s

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 All values need to be confirmed during device validation.

3 Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal

3.14 FMPLL electrical characteristics

The device provides a frequency modulated phase locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Table 34. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[3]	—	4	—	64	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle[3]	—	40	—	60	%
f_{PLLOUT}	CC	P	FMPLL output clock frequency	—	16	—	64	MHz
f_{CPU}	SR	—	System clock frequency	—	—	—	64[4]	MHz
f_{FREE}	CC	P	Free-running frequency	—	20	—	150	MHz
t_{LOCK}	CC	P	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)		40	100	µs
Δt_{LTJIT}	CC	—	FMPLL long term jitter	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} @ 64 MHz, 4000 cycles	—	—	10	ns
I_{PLL}	CC	C	FMPLL consumption	T_A = 25 °C	—	—	4	mA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 All values need to be confirmed during device validation.

3 PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.

4 f_{CPU} 64 MHz can be achieved only at up to 105 °C

3.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz main internal RC oscillator. This is used as the default clock at the power-up of the device.

Table 35. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed	—	16	—	MHz
	SR	—		—	12		20	
$I_{FIRCRUN}$[3],	CC	T	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed	—	—	200	µA
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 25 °C	—	TBD	10	µA
		—		T_A = 55 °C	—	TBD	TBD	

Table 35. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value[2]			Unit
						Min	Typ	Max	
$I_{FIRCSTOP}$	CC	T	Fast internal RC oscillator high frequency and system clock current in stop mode	T_A = 25 °C	sysclk = off	—	500	—	µA
					sysclk = 2 MHz	—	600	—	
					sysclk = 4 MHz	—	700	—	
					sysclk = 8 MHz	—	900	—	
					sysclk = 16 MHz	—	1250	—	
T_{FIRCSU}	CC	C	Fast internal RC oscillator start-up time	T_A = 55 °C	V_{DD} = 5.0 V ± 10%	—	1.1	2.0	µs
		—			V_{DD} = 3.3 V ± 10%	—	1.2	TBD	
		—		T_A = 125 °C	V_{DD} = 5.0 V ± 10%	—	—	2.0	
		—			V_{DD} = 3.3 V ± 10%	—	—	TBD	
$\Delta_{FIRCPRE}$	CC	C	Fast internal RC oscillator precision after software trimming of f_{FIRC}	T_A = 25 °C		–1	—	+1	%
$\Delta_{FIRCTRIM}$	CC	C	Fast internal RC oscillator trimming step	T_A = 25 °C		—	1.6		%
$\Delta_{FIRCVAR}$	CC	C	Fast internal RC oscillator variation over temperature and supply with respect to f_{FIRC} at T_A = 25 °C in high-frequency configuration	—		–5	—	+5	%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 All values need to be confirmed during device validation.

3 This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

3.16 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz low power internal RC oscillator. This can be used as the reference clock for the RTC module.

Table 36. Slow internal RC oscillator (128 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
f_{SIRC}	CC	P	Slow internal RC oscillator low frequency	T_A = 25 °C, trimmed	—	128	—	kHz
	SR	—		—	100	—	150	
I_{SIRC}[3],	CC	C	Slow internal RC oscillator low frequency current	T_A = 25 °C, trimmed	—	—	5	µA

Table 36. Slow internal RC oscillator (128 kHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value[2]			Unit
					Min	Typ	Max	
T_{SIRCSU}	CC	P	Slow internal RC oscillator start-up time	T_A = 25 °C, V_{DD} = 5.0 V ± 10%	—	8	12	µs
$\Delta_{SIRCPRE}$	CC	C	Slow internal RC oscillator precision after software trimming of f_{SIRC}	T_A = 25 °C	–2	—	+2	%
$\Delta_{SIRCTRIM}$	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	
$\Delta_{SIRCVAR}$	CC	C	Slow internal RC oscillator variation in temperature and supply with respect to f_{SIRC} at T_A = 55 °C in high frequency configuration	High frequency configuration	–10	—	+10	%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 All values need to be confirmed during device validation.

3 This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

3.17 ADC electrical characteristics

3.17.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit and 12-bit).

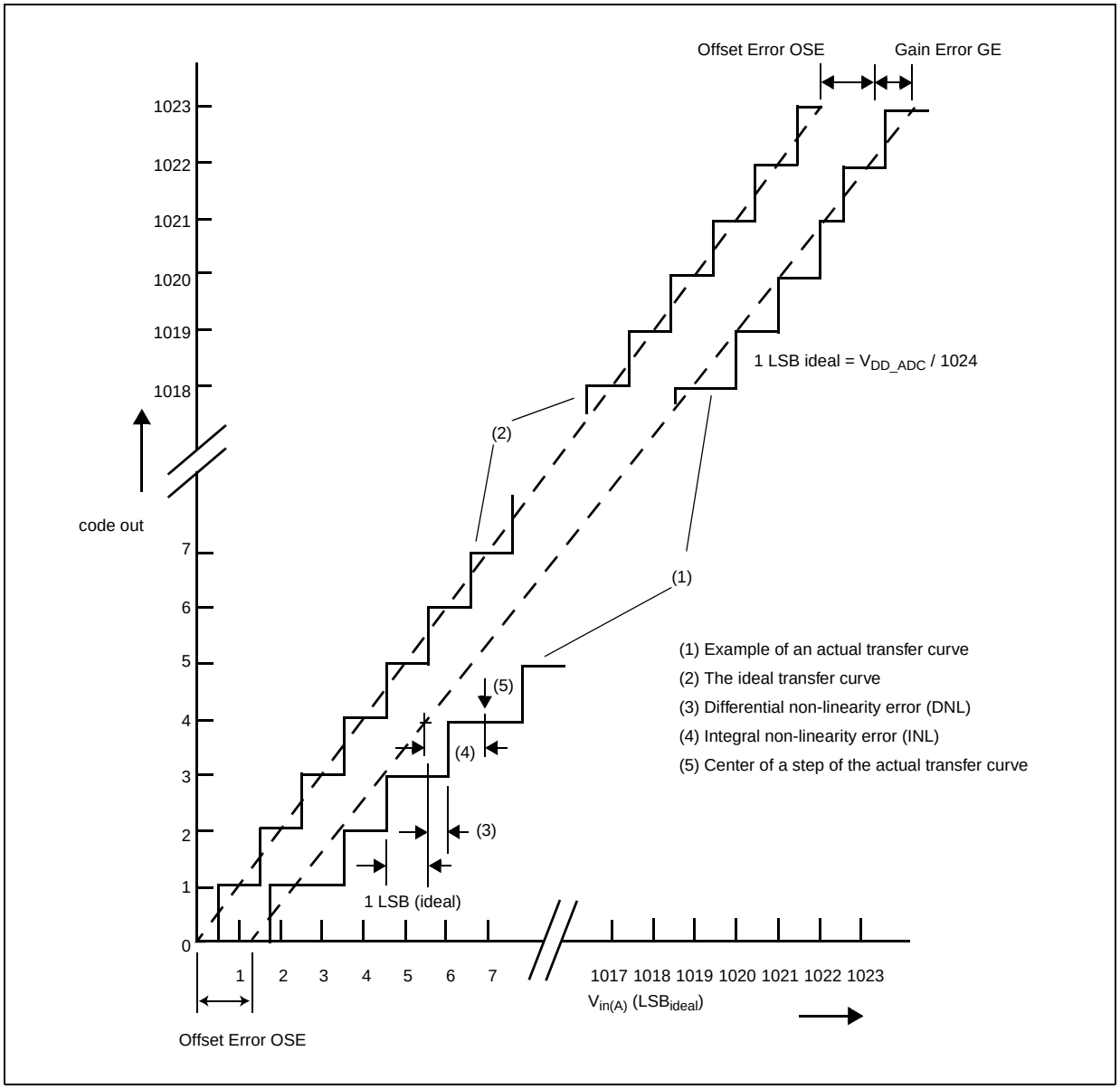


Figure 15. ADC0 characteristic and error definitions

3.17.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330 kΩ is obtained (R_{EQ} = 1 / (fc*C_S), where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the Equation 4:

Eqn. 4

$$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

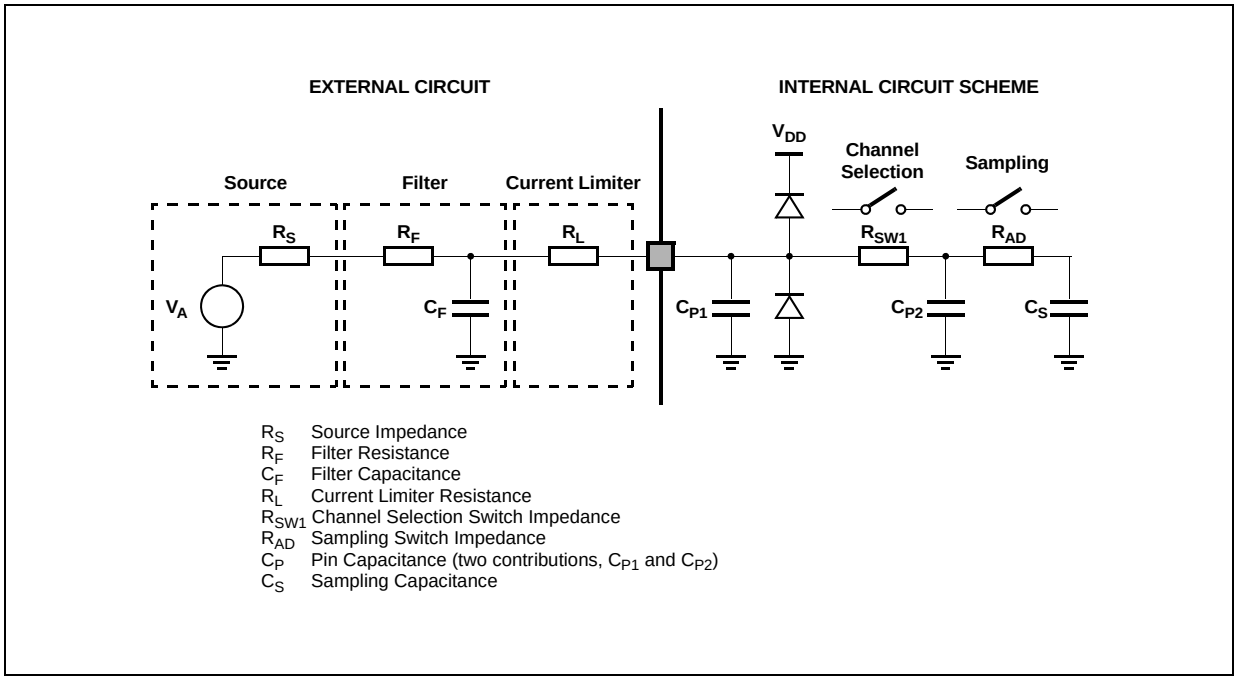


Figure 16. Input equivalent circuit (precise channels)

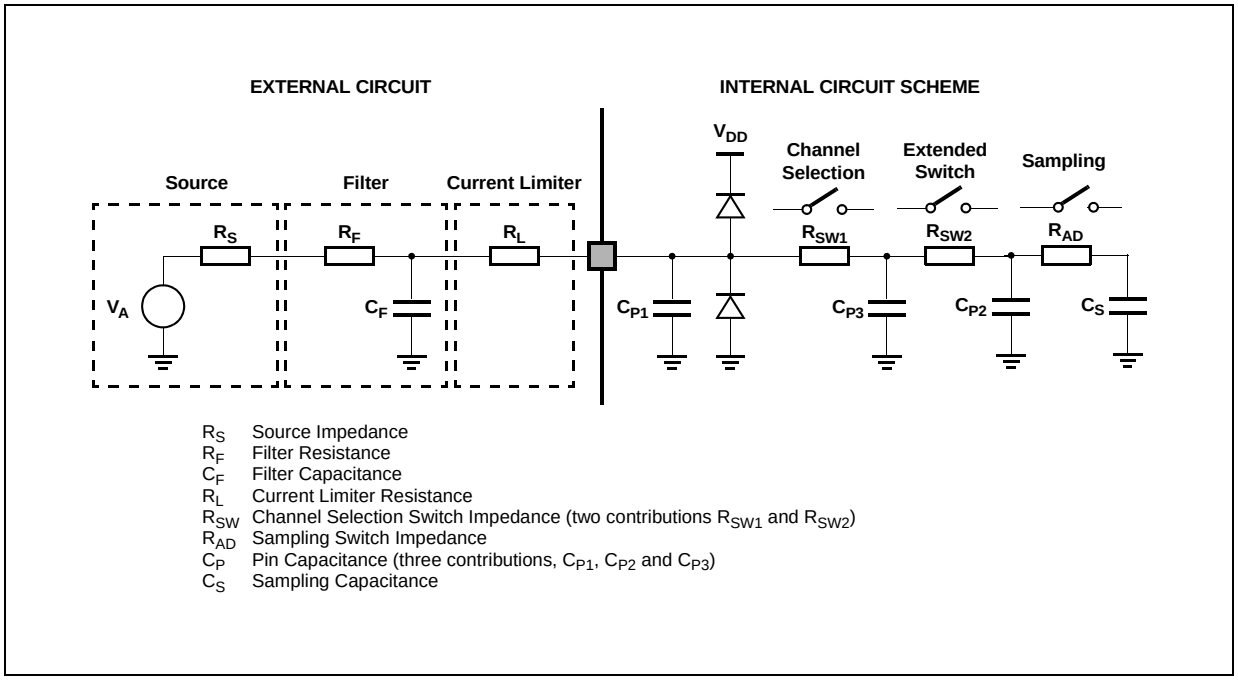


Figure 17. Input equivalent circuit (extended channels)

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 16): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

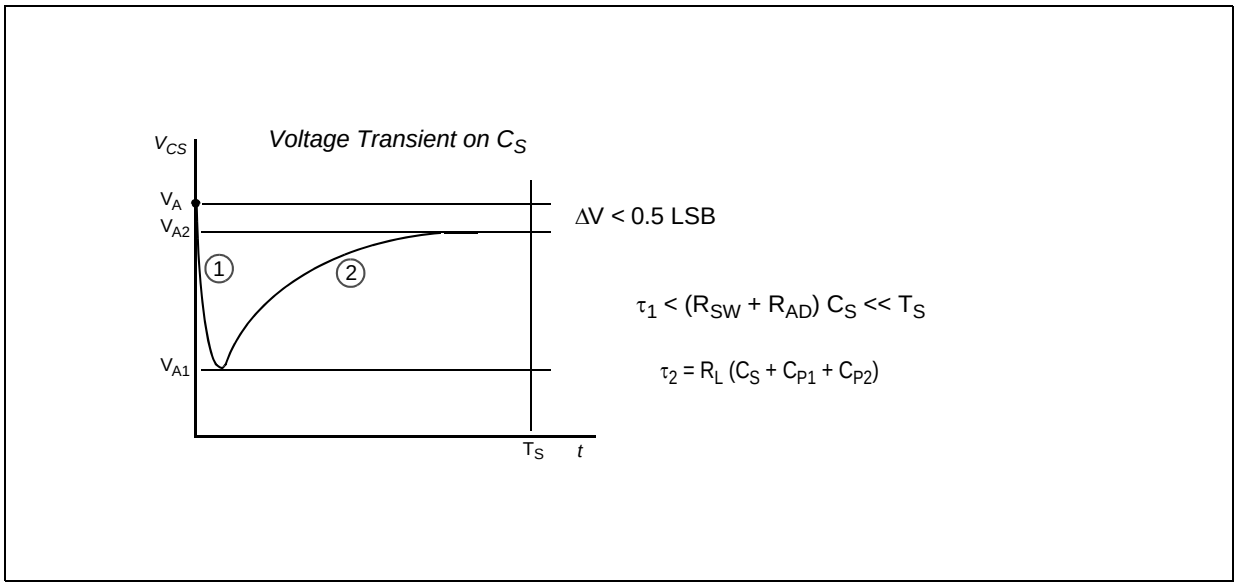


Figure 18. Transient behavior during sampling phase

In particular two different transient periods can be distinguished:

1. A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Eqn. 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

Eqn. 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

2. A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Eqn. 9

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 10 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 10

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

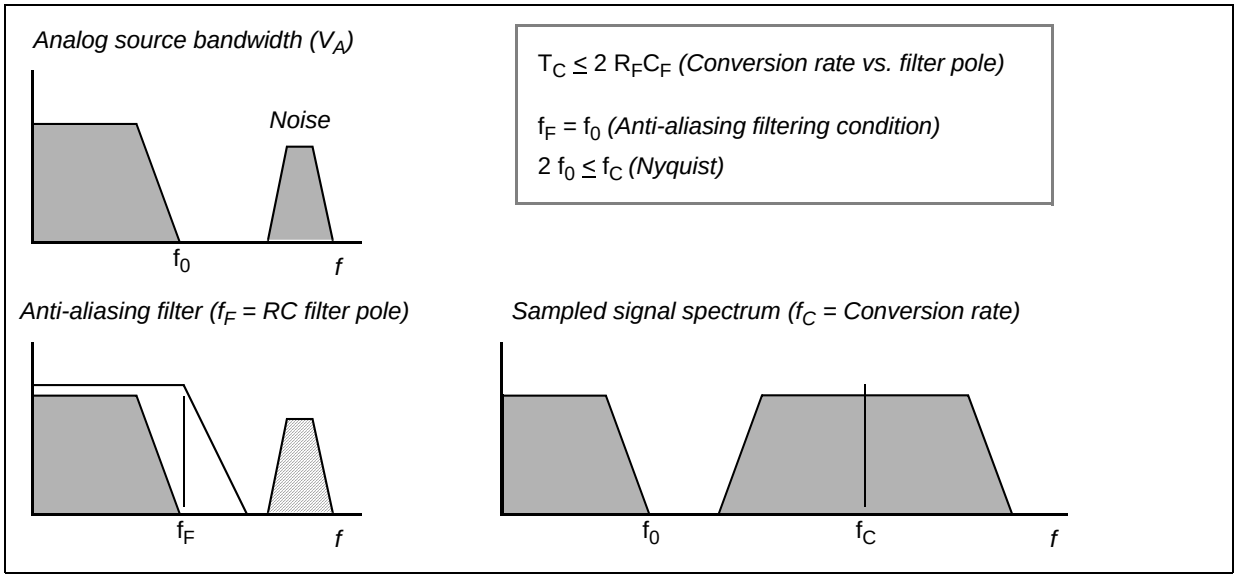


Figure 19. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on C_S:

Eqn. 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

ADC0 (10-bit) ***Eqn. 12***

$$C_F > 2048 \bullet C_S$$

ADC1 (12-bit) ***Eqn. 13***

$$C_F > 8192 \bullet C_S$$

3.17.3 ADC electrical characteristics

Table 37. ADC input leakage current

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
I_{LKG}	CC	C	Input leakage current	T_A = –40 °C	No current injection on adjacent pin	—	1	—	nA
		C		T_A = 25 °C		—	1	—	
		C		T_A = 105 °C		—	8	200	
		P		T_A = 125 °C		—	45	400	

Table 38. ADC conversion characteristics (10-bit ADC0)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC0}	SR	—	Voltage on VSS_HV_ADC0 (ADC0 reference) pin with respect to ground (V_{SS})[2]	—	–0.1	—	0.1	V
V_{DD_ADC0}	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	V_{DD}–0.1	—	V_{DD}+0.1	V
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC0} –0.1	—	V_{DD_ADC0} +0.1	V
f_{ADC0}	SR	—	ADC0 analog frequency	—	6	—	32 + 4%	MHz
Δ_{ADC0_SYS}	SR	—	ADC0 digital clock duty cycle (ipg_clk)	ADCLKSEL = 1[4]	45	—	55	%
t_{ADC0_PU}	SR	—	ADC0 power up delay	—	—	—	1.5	µs

Table 38. ADC conversion characteristics (continued)(10-bit ADC0)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{ADC0_S}	CC	T	Sample time[5]	f_{ADC} = 32 MHz, ADC0_conf_sample_input = 17		0.5	—		µs
				f_{ADC} = 6 MHz, INPSAMP = 255			—	42	
t_{ADC0_C}	CC	P	Conversion time[6]	f_{ADC} = 32 MHz, ADC_conf_comp = 2		0.625	—		µs
C_S	CC	D	ADC0 input sampling capacitance	—		—	—	3	pF
C_{P1}	CC	D	ADC0 input pin capacitance 1	—		—	—	3	pF
C_{P2}	CC	D	ADC0 input pin capacitance 2	—		—	—	1	pF
C_{P3}	CC	D	ADC0 input pin capacitance 3	—		—	—	1	pF
R_{SW1}	CC	D	Internal resistance of analog source	—		—	—	3	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—		—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—		—	—	2	kΩ
I_{INJ}	SR	—	Input current Injection	Current injection on one ADC0 input, different from the converted one	V_{DD} = 3.3 V ± 10%	–5	—	5	mA
					V_{DD} = 5.0 V ± 10%	–5	—	5	

Table 38. ADC conversion characteristics (continued)(10-bit ADC0)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
| INL |	CC	T	Absolute value for integral non-linearity	No overload	—	0.5	1.5	LSB
| DNL |	CC	T	Absolute differential non-linearity	No overload	—	0.5	1.0	LSB
| OFS |	CC	T	Absolute offset error	—	—	0.5	—	LSB
| GNE |	CC	T	Absolute gain error	—	—	0.6	—	LSB
TUEP	CC	P	Total unadjusted error[7] for precise channels, input only pins	Without current injection	–2	0.6	2	LSB
		T		With current injection	–3		3	
TUEX	CC	T	Total unadjusted error[7] for extended channel	Without current injection	–3	1	3	LSB
		T		With current injection	–4		4	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 Analog and digital V_{SS} **must** be common (to be tied together externally).

3 V_{AINx} may exceed V_{SS_ADC0} and V_{DD_ADC0} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.

4 Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.

5 During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC0_S}. After the end of the sample time t_{ADC0_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC0_S} depend on programming.

6 This parameter does not include the sample time t_{ADC0_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.

7 Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

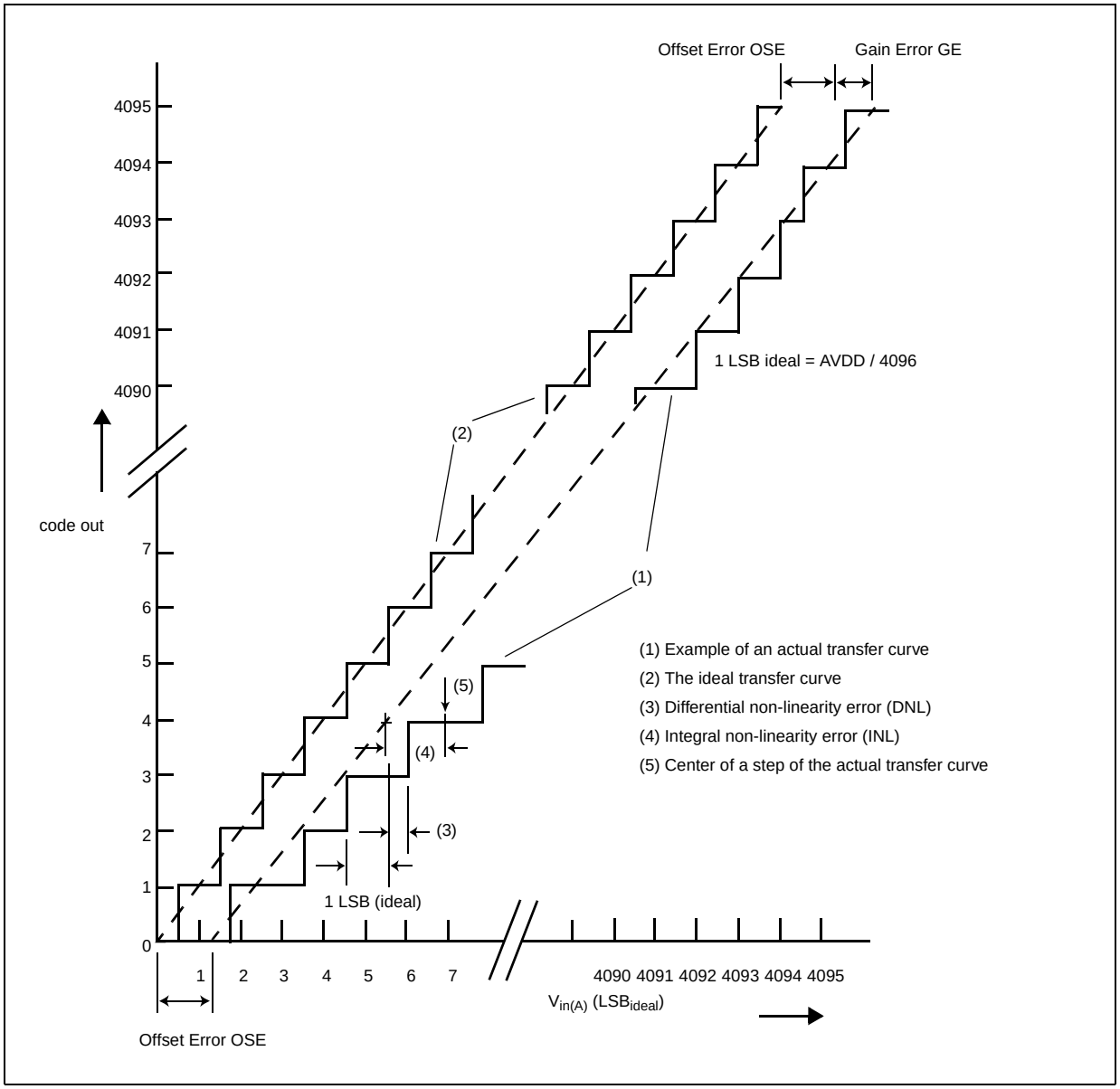


Figure 20. ADC1 characteristic and error definitions

Table 39. Conversion characteristics (12-bit ADC1)

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
V_{SS_ADC1}	SR	Voltage on VSS_HV_ADC1 (ADC1 reference) pin with respect to ground (V_{SS})[2]	—	-0.1		0.1	V
V_{DD_ADC1}	SR	Voltage on VDD_HV_ADC1 pin (ADC1 reference) with respect to ground (V_{SS})	—	V_{DD}-0.1		V_{DD}+0.1	V
V_{AINx}	SR	Analog input voltage[3]	—	V_{SS_ADC1}-0.1		V_{DD_ADC1}+0.1	V
f_{ADC1}	SR	ADC1 analog frequency	—	32 + 3%	32 + 4%		MHz
t_{ADC1_PU}	SR	ADC1 power up delay	—	1.5			µs
t_{ADC1_S}	CC	Sample time[4] VDD=3.3 V	f_{ADC1}= 32 MHz, ADC1_conf_sample_input = 20	600			ns
		Sample time[4] VDD =5.0 V	f_{ADC1}= 32 MHz, ADC1_conf_sample_input = 17	500			
		Sample time[4] VDD=3.3 V	f_{ADC1}= 3.33 MHz, ADC1_conf_sample_input = 255			76.2	µs
		Sample time[4] VDD =5.0 V	f_{ADC1}= 3.33 MHz, ADC1_conf_sample_input = 255			76.2	

Table 39. Conversion characteristics (12-bit ADC1) (continued)

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
t_{ADC1_C}	CC	Conversion time[5] VDD=3.3 V	f_{ADC1} = 20MHz, ADC1_conf_comp = 0	2.4			µs
		Conversion time[5] VDD =5.0 V	$f_{ADC\ 1}$= 13.33 MHz, ADC1_conf_comp = 0	1.5			µs
		Conversion time[5] VDD=3.3 V	$f_{ADC\ 1}$= 13.33 MHz, ADC1_conf_comp = 0	3.6			µs
		Conversion time[5] VDD =5.0 V	f_{ADC1} = 32 MHz, ADC1_conf_comp = 0	3.6			µs
Δ_{ADC0_SYS}	SR	ADC1 digital clock duty cycle (ipg_clk)	ADCLKSEL = 1[6]	45	—	55	%
C_S	CC	ADC1 input sampling capacitance	—		5		pF
C_{P1}	CC	ADC1 input pin capacitance 1	—		3		pF
C_{P2}	CC	ADC1 input pin capacitance 2	—		1		pF
C_{P3}	CC	ADC1 input pin capacitance 3	—		1.5		pF
R_{SW1}	CC	Internal resistance of analog source	—			1	kΩ
R_{SW2}	CC	Internal resistance of analog source	—			2	kΩ
R_{AD}	CC	Internal resistance of analog source	—			0.3	kΩ

Table 39. Conversion characteristics (12-bit ADC1) (continued)

Symbol		Parameter	Conditions[1]		Value			Unit
					Min	Typ	Max	
I_{INJ}	SR	Input current Injection	Current injection on one ADC1 input, different from the converted one	V_{DD} = 3.3 V ± 10%	-5	—	5	mA
				V_{DD} = 5.0 V ± 10%	-5	—	5	
INLP	CC	Absolute Integral non-linearity-Precise channels	No overload			1	3	LSB
INLX	CC	Absolute Integral non-linearity-Extended channels	No overload			1.5	5	LSB
DNL	CC	Absolute Differential non-linearity	No overload			0.5	1	LSB
OFS	CC	Absolute Offset error	—			2		LSB
GNE	CC	Absolute Gain error	—			2		LSB
TUEP[7]	CC	Total Unadjusted Error for precise channels, input only pins						
			Without current injection		-6		6	
			With current injection		-8		8	
TUEX[7]	CC	Total Unadjusted Error for extended channel						
			Without current injection		-10		10	LSB
			With current injection		-12		12	LSB

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 / 125 °C, unless otherwise specified.

2 Analog and digital V_{SS} **must** be common (to be tied together externally).

3 V_{AINx} may exceed V_{SS_ADC1} and V_{DD_ADC1} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0xFFF.

4 During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC1_S}. After the end of the sample time t_{ADC1_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC1_S} depend on programming.

5 This parameter does not include the sample time t_{ADC1_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.

6 Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.

7 Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

3.18 On-chip peripherals

3.18.1 Current consumption

Table 40. On-chip peripherals current consumption[1]

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
$I_{DD\_BV(CAN)}$	CC	T	CAN (FlexCAN) supply current on V_{DD_BV}	500 Kbps	Total (static + dynamic) consumption: • FlexCAN in loop-back mode • XTAL@8 MHz used as CAN engine clock source • Message sending period is 580 µs	7.652 * f_{periph} + 84.73			µA
				125 Kbps		8.0743 * f_{periph} + 26.757			
$I_{DD\_BV(eMIOS)}$	CC	T	eMIOS supply current on V_{DD_BV}	Static consumption: • eMIOS channel OFF • Global prescaler enabled		28.7 * f_{periph}			
				Dynamic consumption: • It does not change varying the frequency (0.003 mA)		3			
$I_{DD\_BV(SCI)}$	CC	T	SCI (LINFlex) supply current on V_{DD_BV}	Total (static + dynamic) consumption: • LIN mode • Baudrate: 20 Kbps		4.7804 * f_{periph} + 30.946			
$I_{DD\_BV(SPI)}$	CC	T	SPI (DSPI) supply current on V_{DD_BV}	Ballast static consumption (only clocked)		1			
				Ballast dynamic consumption (continuus communication): • Baudrate: 2 Mbit • Trasmission every 8 µs • Frame: 16 bits		16.3 * f_{periph}			

Table 40. On-chip peripherals current consumption[1] (continued)

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
$I_{DD\_BV(ADC)}$	CC	T	ADC supply current on V_{DD_BV}	V_{DD} = 5.5 V	Ballast static consumption (no conversion)	0.0409 * f_{periph}			mA
				V_{DD} = 5.5 V	Ballast dynamic consumption (continuus conversion)	0.0049 * f_{periph}			
$I_{DD\_HV\_ADC(ADC)}$	CC	T	ADC supply current on $V_{DD\_HV\_ADC}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	0.0017 * f_{periph}			
				V_{DD} = 5.5 V	Analog dynamic consumption (continuus conversion)	0.075 * f_{periph} + 0.032			
$I_{DD\_HV(FLASH)}$	CC	T	CFlash + DFlash supply current on $V_{DD\_HV\_ADC}$	V_{DD} = 5.5 V	-	13.25			
$I_{DD\_HV(PLL)}$	CC	T	PLL supply current on V_{DD_HV}	V_{DD} = 5.5 V	-	0.0031 * f_{periph}			

1 Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 64 MHz

3.18.2 DSPI characteristics

Table 41. DSPI characteristics

No.	Symbol		C	Parameter		Value			Unit
						Min	Typ	Max	
1	t_{SCK}	SR	D	SCK cycle time		64	—	—	ns
—	f_{DSPI}	SR	D	DSPI digital controller frequency		—	—	f_{CPU}	MHz
—	Δt_{CSC}	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode		—	—	120[1]	ns
2	t_{CSCext}[2]	CC	D	CS to SCK delay	Master mode	$t_{CSCext} = t_{CSC} + \Delta t_{CSC}$			ns
		SR	D		Slave mode	32	—	—	
3	t_{ASCext}[3]	CC	D	After SCK delay	Master mode	$t_{ASCext} = t_{ASC} + \Delta t_{CSC}$			ns
		SR	D		Slave mode	$1/f_{DSPI} + 5$ ns	—	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	Master mode	—	$t_{SCK/2}$	—	ns
		SR	D		Slave mode	$t_{SCK/2}$	—	—	
5	t_A	SR	D	Slave access time	—	27	—	—	ns
6	t_{DI}	SR	D	Slave SOUT disable time	—	0	—	—	ns
7	t_{SUI}	SR	D	Data setup time for inputs	Master (MTFE = 0)	35	—	—	ns
					Slave	5	—	—	
					Master (MTFE = 1)	35	—	—	
8	t_{HI}	SR	D	Data hold time for inputs	Master (MTFE = 0)	0	—	—	ns
					Slave	2[4]	—	—	
					Master (MTFE = 1)	0	—	—	

Table 41. DSPI characteristics (continued)

No.	Symbol		C	Parameter		Value			Unit
						Min	Typ	Max	
9	t_{SUO}[5]	CC	D	Data valid after SCK edge	Master (MTFE = 0)	—	—	32	ns
					Slave	—	—	34	
					Master (MTFE = 1)	—	—	32	
10	t_{HO}[5]	CC	D	Data hold time for outputs	Master (MTFE = 0)	2	—	—	ns
					Slave	5.5	—	—	
					Master (MTFE = 1)	2	—	—	

1 Maximum is reached when CSn pad is configured as SLOW pad while SCK pad is configured as MEDIUM pad.

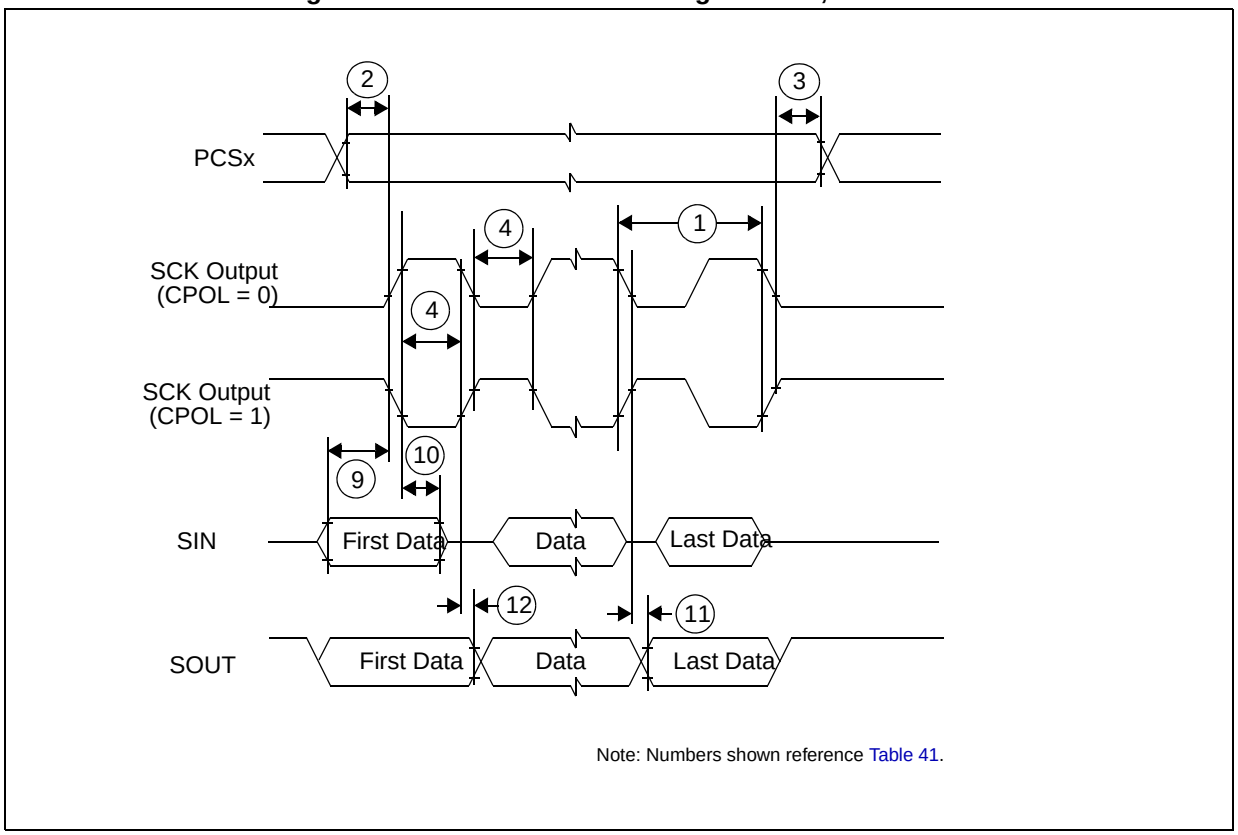
2 The t_{CSC} delay value is configurable through a register. When configuring t_{CSC} (using PCSSCK and CSSCK fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{CSC} to ensure positive t_{CSCext}.

3 The t_{ASC} delay value is configurable through a register. When configuring t_{ASC} (using PASC and ASC fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{ASC} to ensure positive t_{ASCext}.

4 This delay value corresponds to SMPL_PT = 00b which is bit field 9 and 8 of DSPI_MCR register.

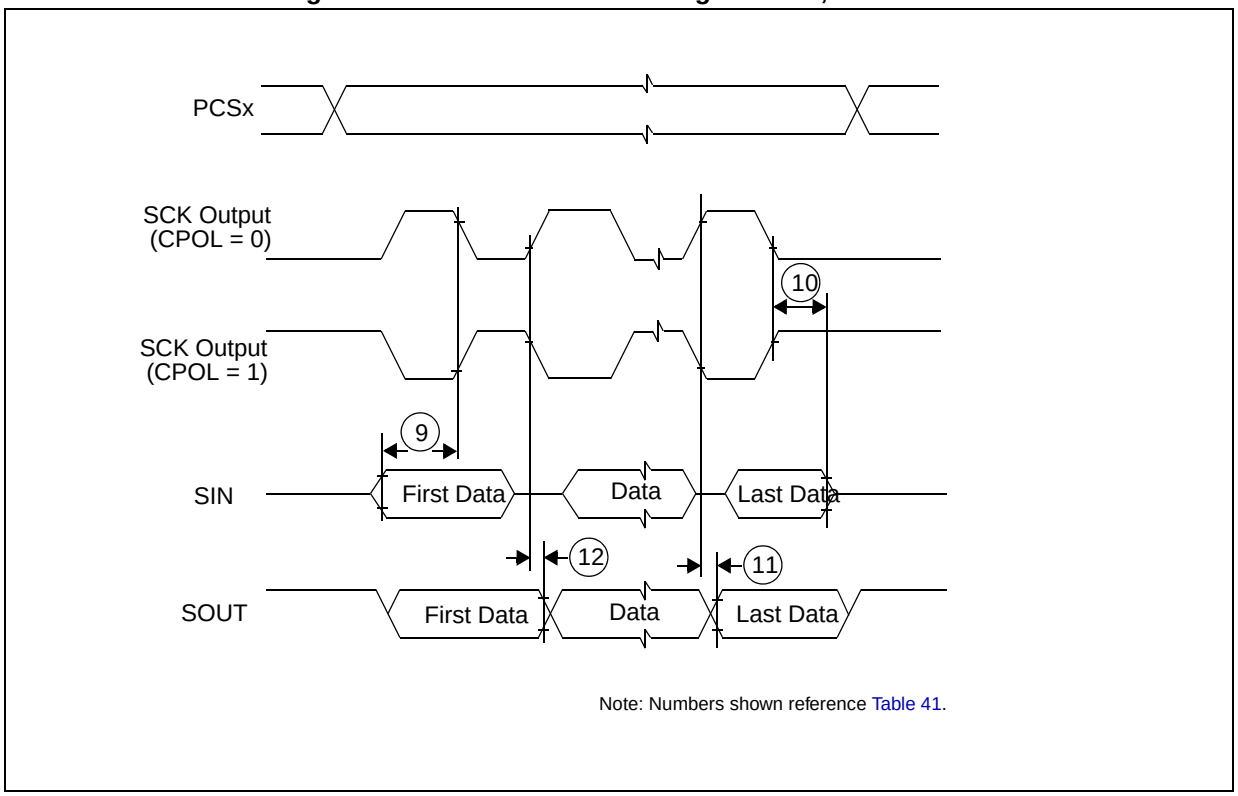
5 SCK and SOUT configured as MEDIUM pad

Figure 21. DSPI classic SPI timing - master, CPHA = 0



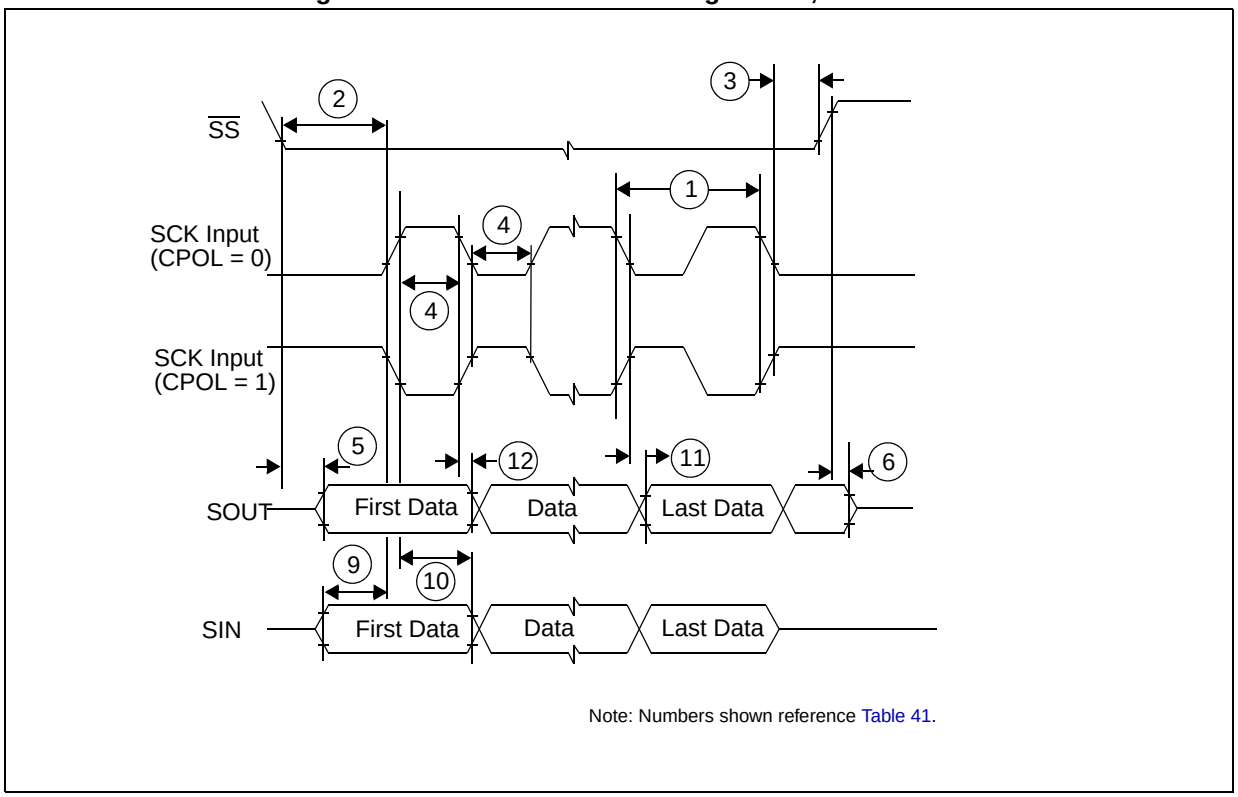
Note: Numbers shown reference Table 41.

Figure 22. DSPI classic SPI timing - master, CPHA = 1



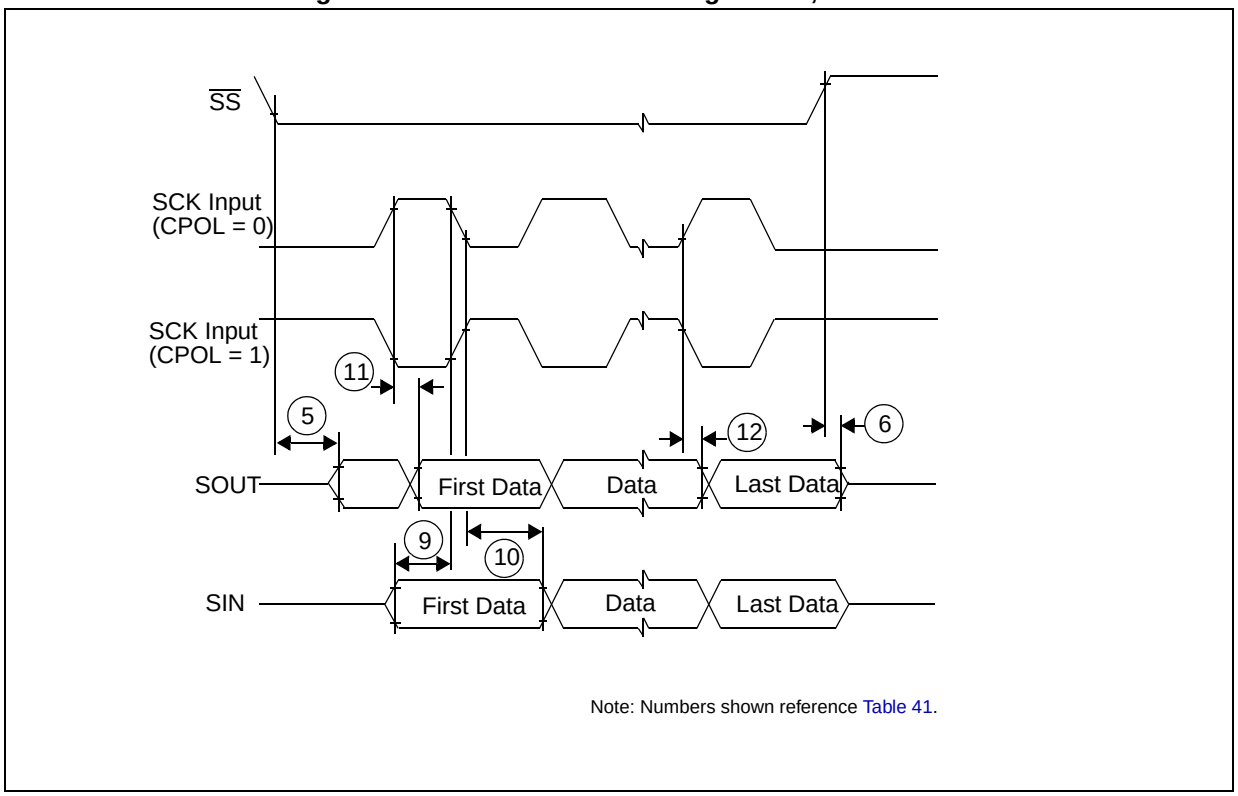
Note: Numbers shown reference Table 41.

Figure 23. DSPI classic SPI timing - slave, CPHA = 0



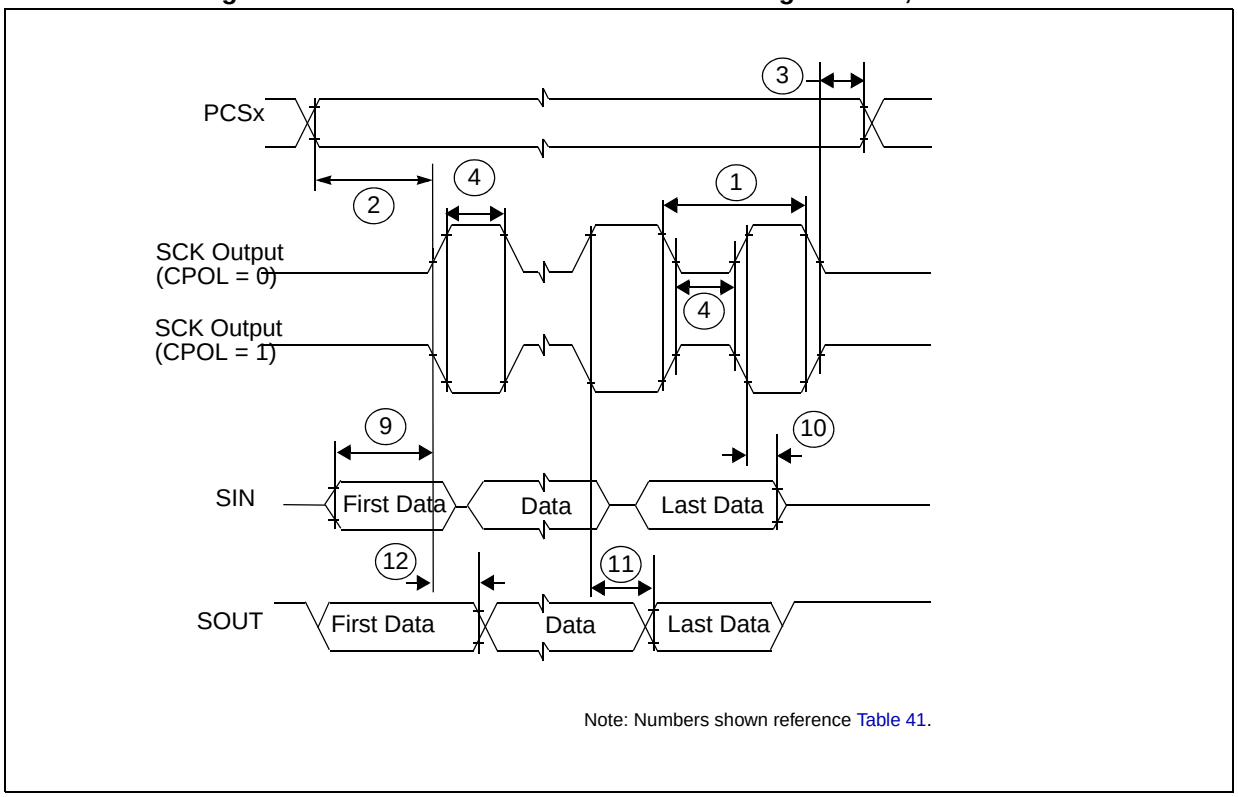
Note: Numbers shown reference Table 41.

Figure 24. DSPI classic SPI timing - slave, CPHA = 1



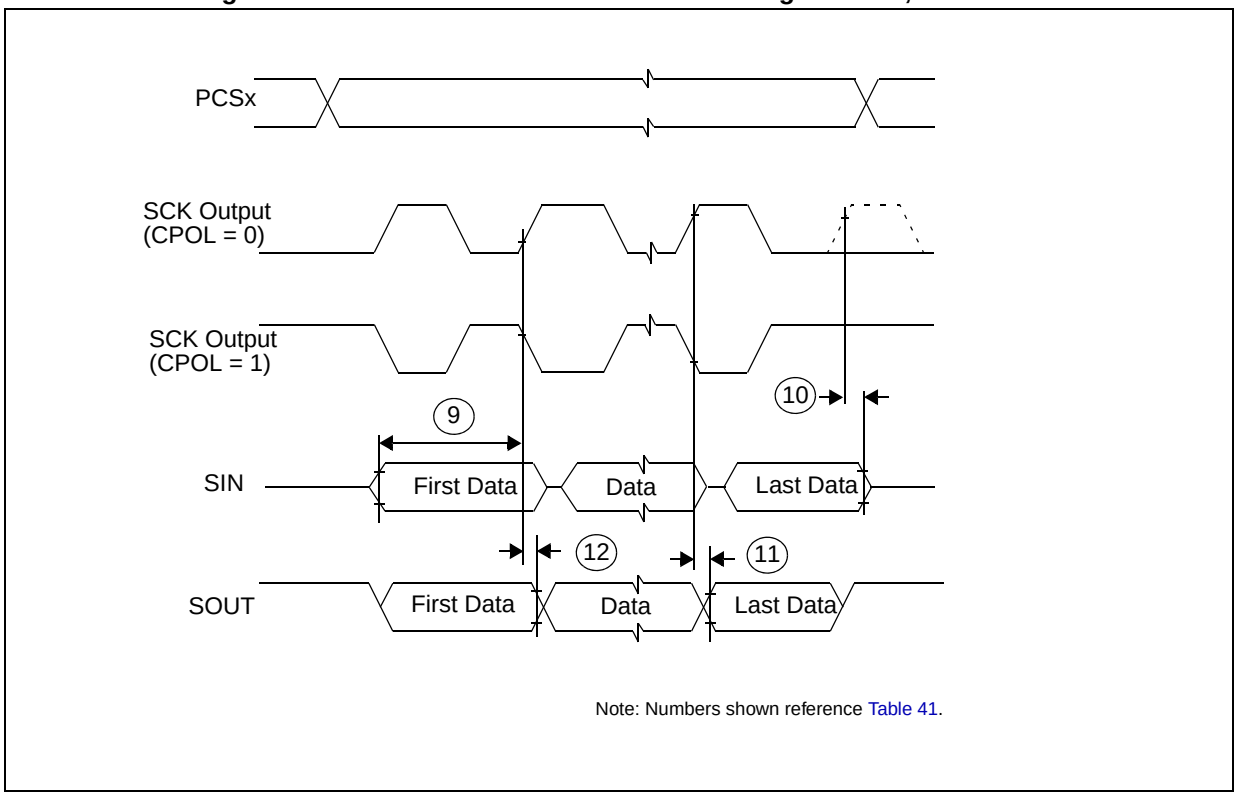
Note: Numbers shown reference Table 41.

Figure 25. DSPI modified transfer format timing - master, CPHA = 0



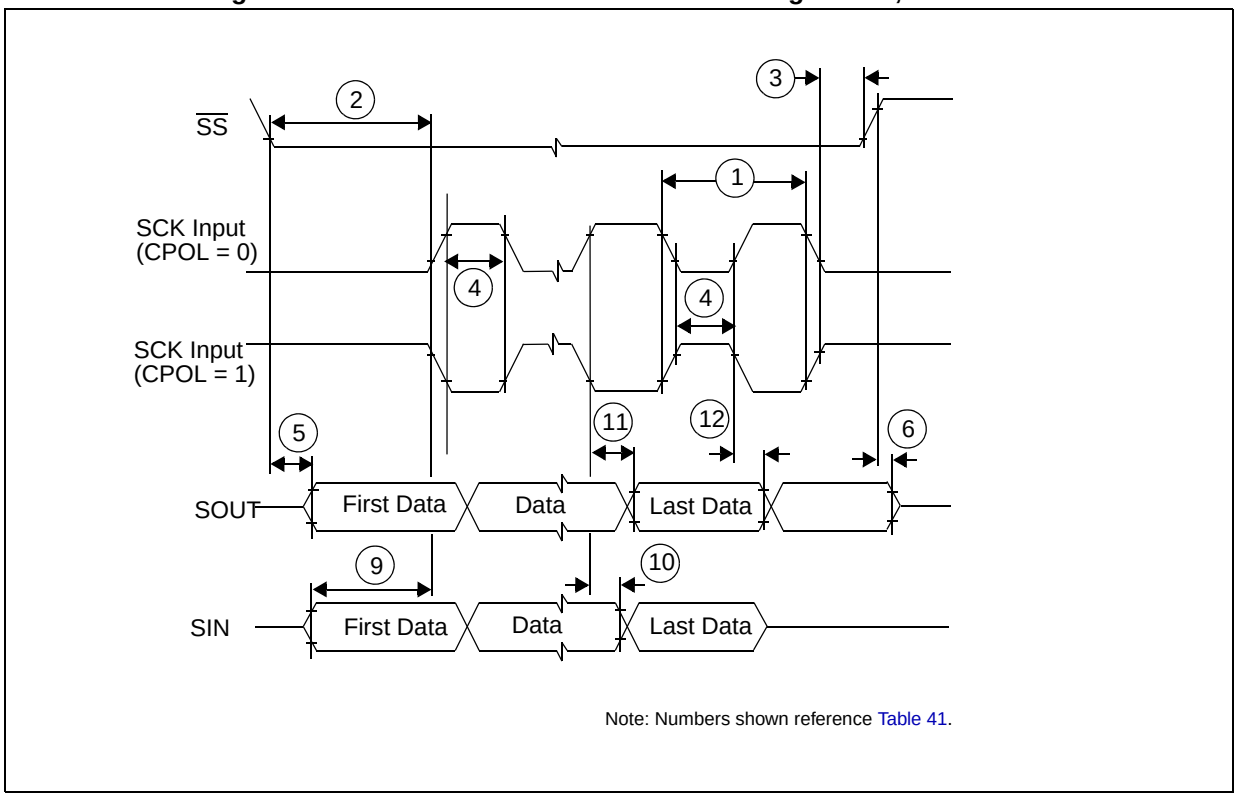
Note: Numbers shown reference Table 41.

Figure 26. DSPI modified transfer format timing - master, CPHA = 1



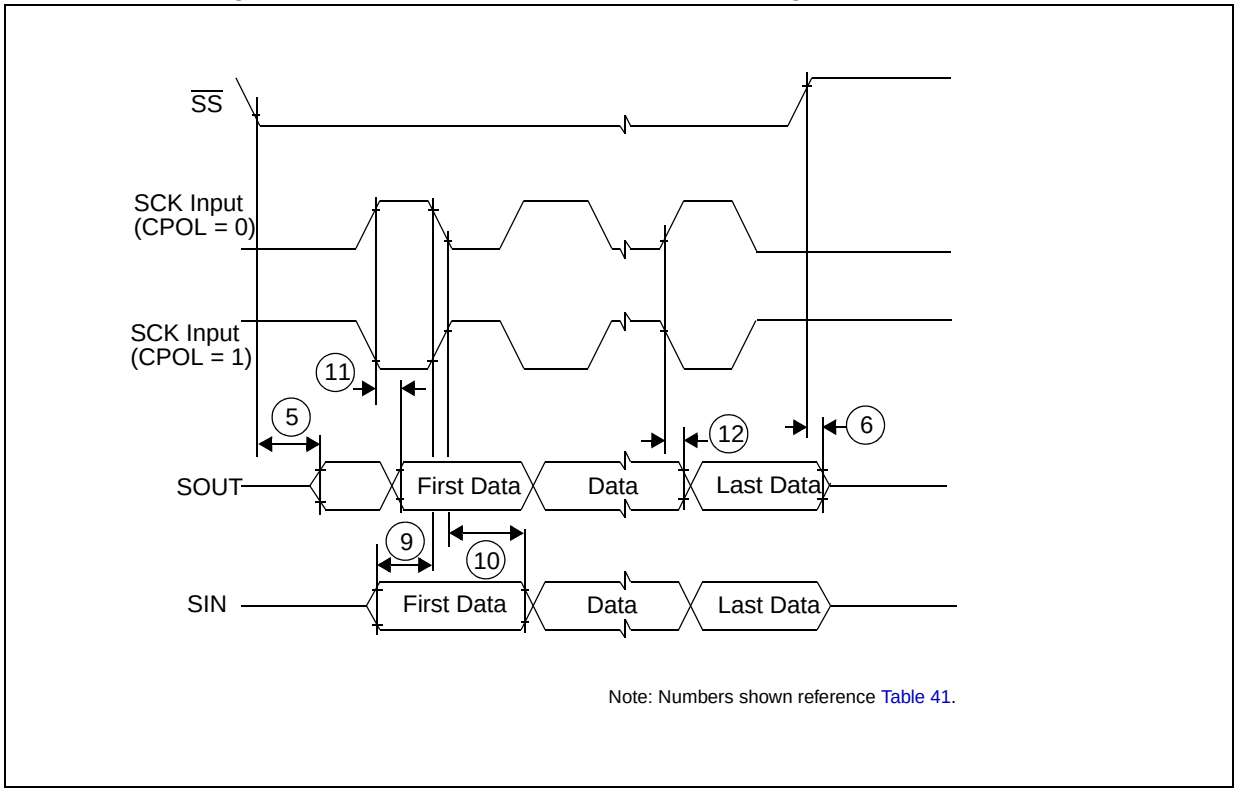
Note: Numbers shown reference Table 41.

Figure 27. DSPI modified transfer format timing - slave, CPHA = 0



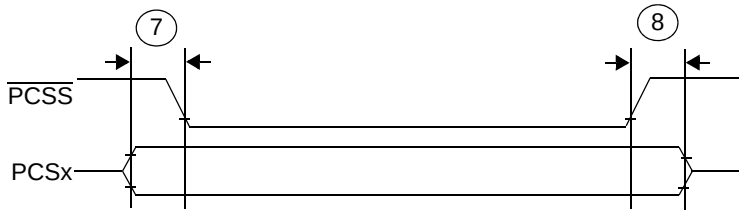
Note: Numbers shown reference Table 41.

Figure 28. DSPI modified transfer format timing - slave, CPHA = 1



Note: Numbers shown reference Table 41.

Figure 29. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing



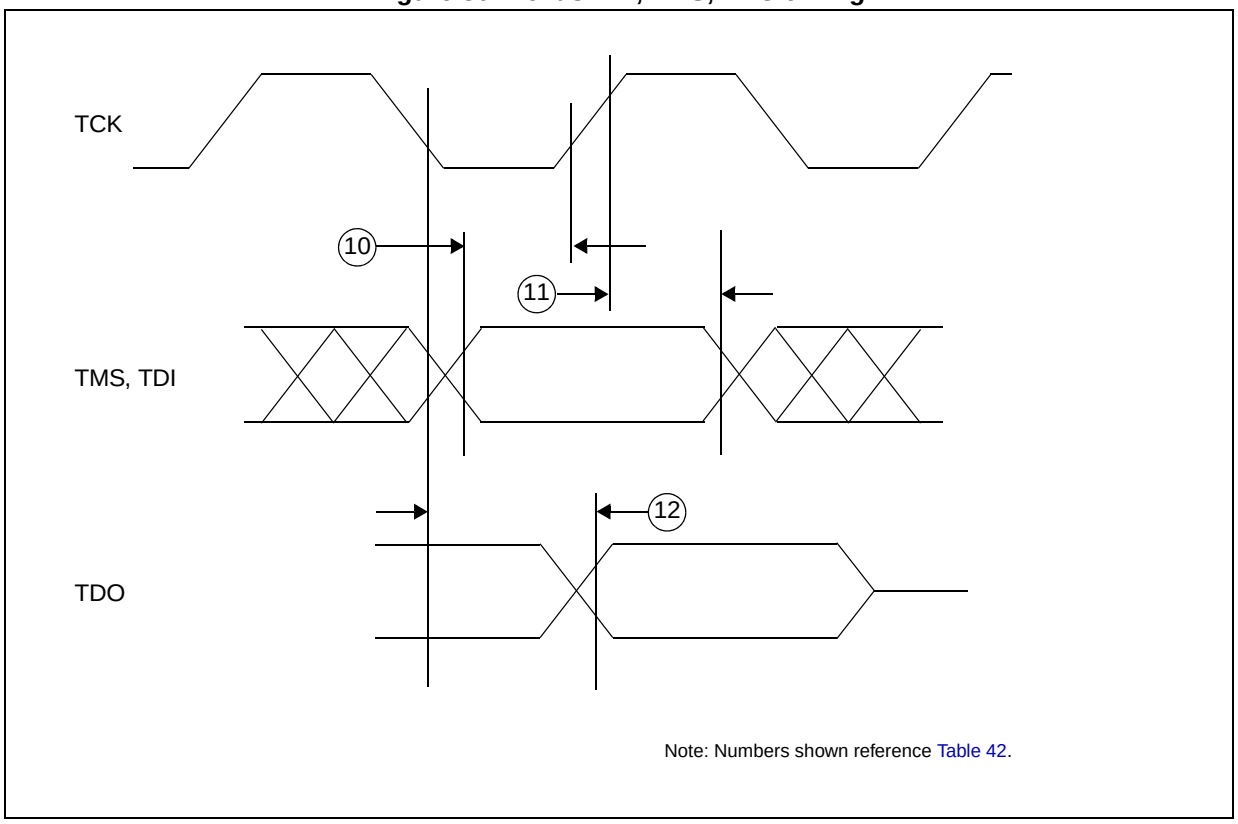
Note: Numbers shown reference Table 41.

3.18.3 Nexus characteristics

Table 42. Nexus characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{TCYC}	CC	D	TCK cycle time	64	—	—	ns
2	t_{MCYC}	CC	D	MCKO cycle time	32	—	—	ns
3	t_{MDOV}	CC	D	MCKO low to MDO data valid	—	—	8	ns
4	t_{MSEOV}	CC	D	MCKO low to MSEO_b data valid	—	—	8	ns
5	t_{EVTOV}	CC	D	MCKO low to EVTO data valid	—	—	8	ns
6	t_{NTDIS}	CC	D	TDI data setup time	15	—	—	ns
	t_{NTMSS}	CC	D	TMS data setup time	15	—	—	ns
7	t_{NTDIH}	CC	D	TDI data hold time	5	—	—	ns
	t_{NTMSH}	CC	D	TMS data hold time	5	—	—	ns
8	t_{TDOV}	CC	D	TCK low to TDO data valid	35	—	—	ns
9	t_{TDOI}	CC	D	TCK low to TDO data invalid	6	—	—	ns

Figure 30. Nexus TDI, TMS, TDO timing



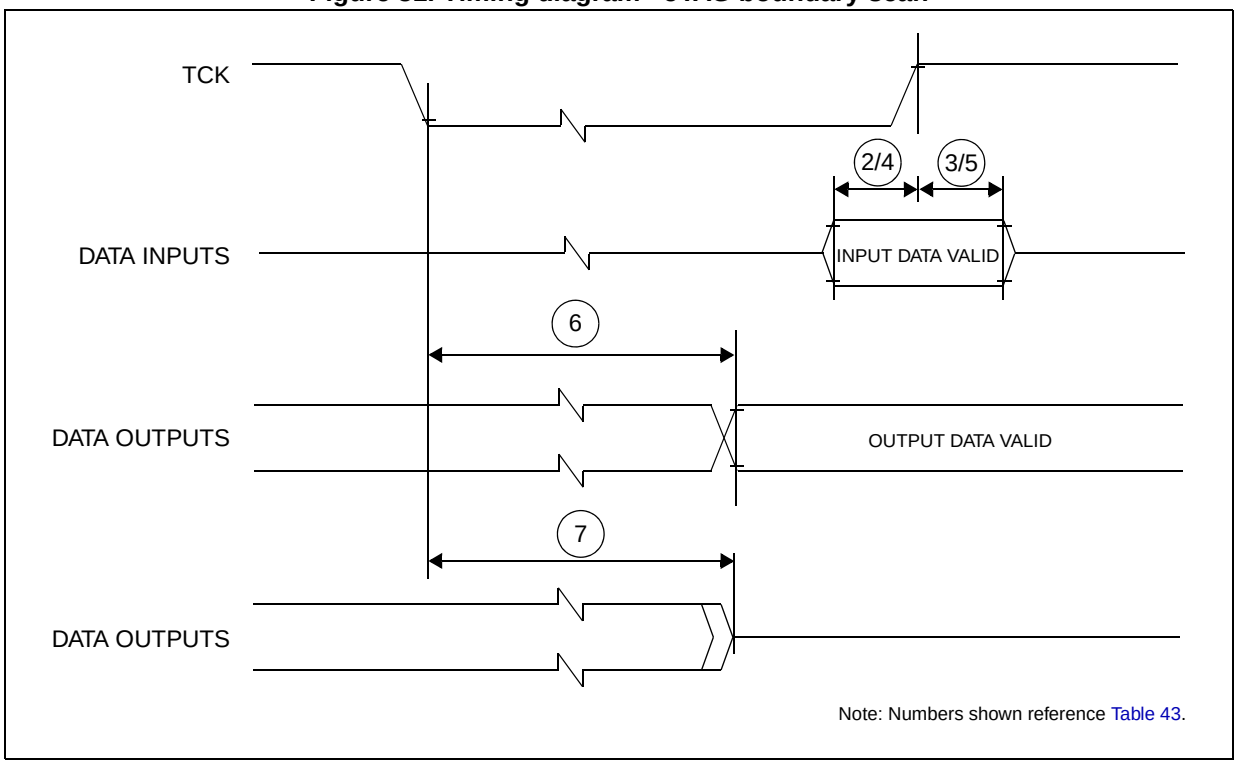
Note: Numbers shown reference Table 42.

3.18.4 JTAG characteristics

Table 43. JTAG characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{JCYC}	CC	D	TCK cycle time	64	—	—	ns
2	t_{TDIS}	CC	D	TDI setup time	15	—	—	ns
3	t_{TDIH}	CC	D	TDI hold time	5	—	—	ns
4	t_{TMSS}	CC	D	TMS setup time	15	—	—	ns
5	t_{TMSH}	CC	D	TMS hold time	5	—	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO valid		—	33	ns
7	t_{TDOI}	CC	D	TCK low to TDO invalid	6	—	—	ns

Figure 31. Timing diagram - JTAG boundary scan



4 Package characteristics

4.1 Package mechanical data

4.1.1 176 LQFP

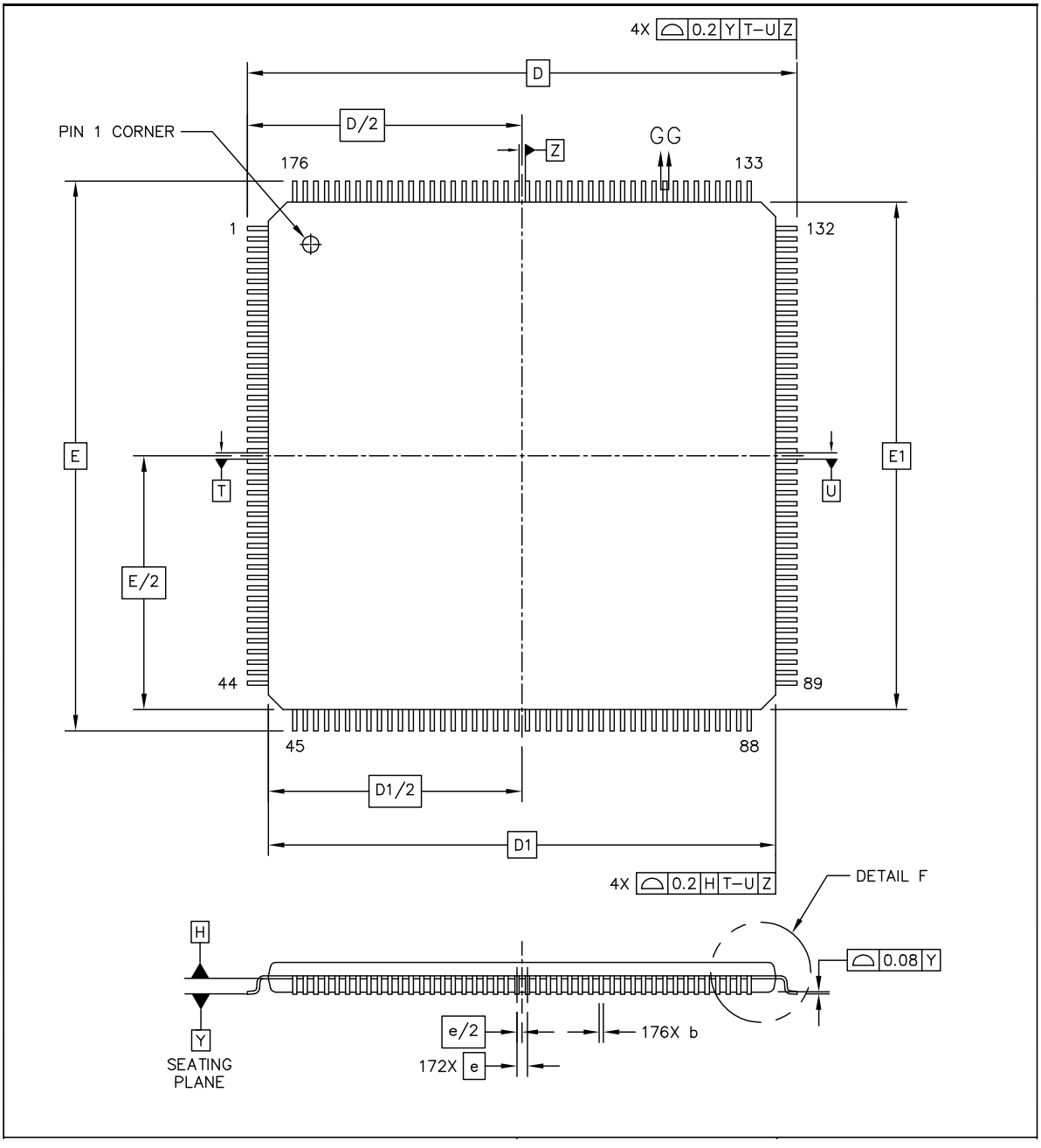


Figure 32. 176 LQFP package mechanical drawing (Part 1 of 3)

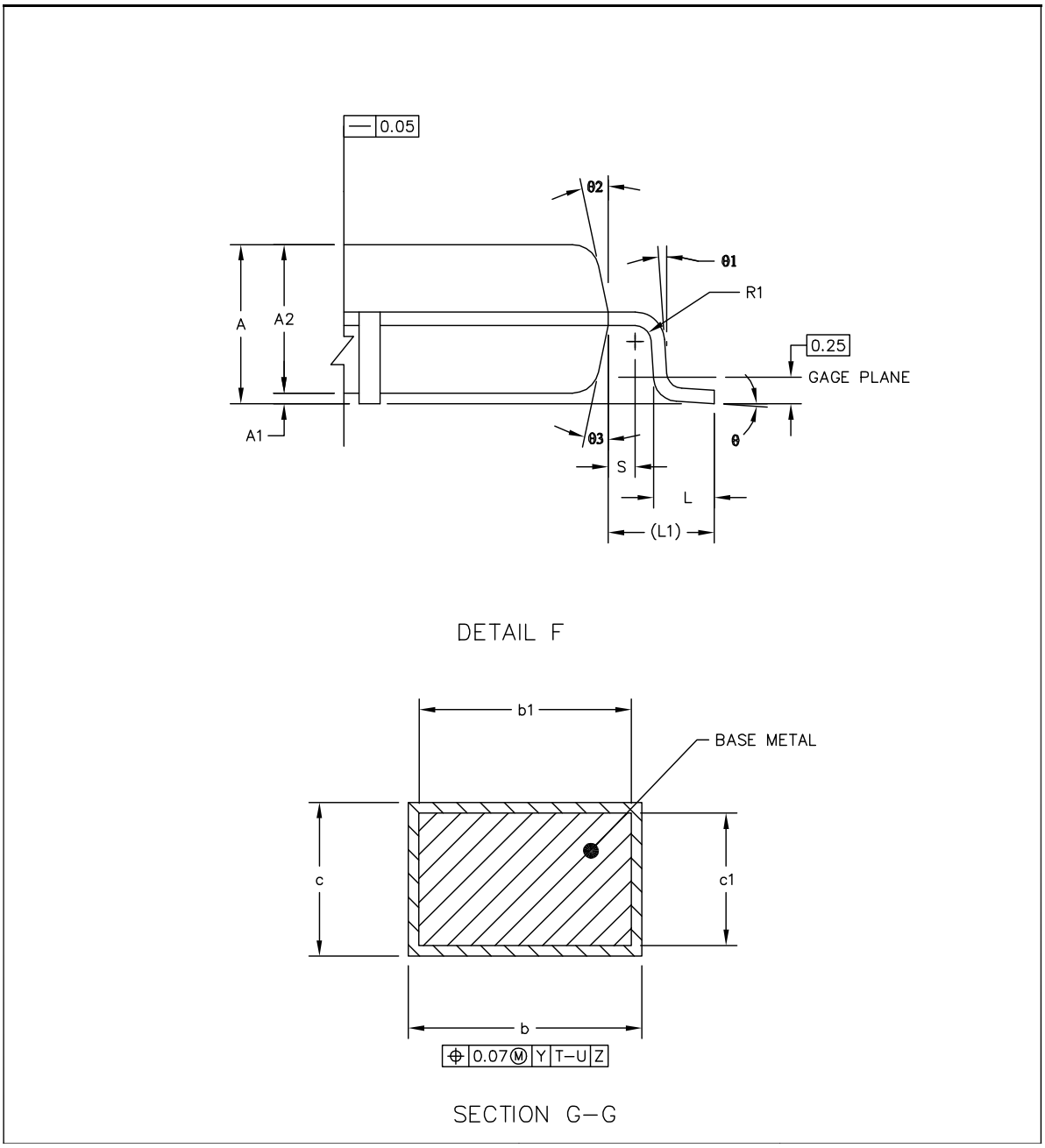


Figure 33. 176 LQFP package mechanical drawing (Part 2 of 3)

NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THEN 0.08MM. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07MM FOR 0.4MM AND 0.5MM PITCH PACKAGES.

DIM	MIN	NOM	MAX
A	---		1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
b	0.17	0.22	0.27
b1	0.17	0.2	0.23
c	0.09		0.2
c1	0.09		0.16
D		26 BSC	
D1		24 BSC	
e		0.5 BSC	
E		26 BSC	
E1		24 BSC	
L	0.45	0.6	0.75

DIM	MIN	NOM	MAX
L1		1 REF	
R1	0.08		---
R2	0.08		0.2
S		0.2 REF	
θ	0°	3.5°	7°
θ1	0°		---
θ2	11°	12°	13°
θ3	11°	12°	13°

DIM	MIN	NOM	MAX

UNIT	DIMENSION AND TOLERANCES	REFERANCE DOCUMENT
MM	ASME Y14.5M	64-06-280-1392

Figure 34. 176 LQFP package mechanical drawing (Part 3 of 3)

Table 44. LQFP176 mechanical data[1]

Symbol	mm			inches[2]		
	Min	Typ	Max	Min	Typ	Max
A	1.400		1.600			0.063
A1	0.050		0.150	0.002		
A2	1.350		1.450	0.053		0.057
b	0.170		0.270	0.007		0.011
C	0.090		0.200	0.004		0.008
D	23.900		24.100	0.941		0.949
E	23.900		24.100	0.941		0.949
e		0.500			0.020	
HD	25.900		26.100	1.020		1.028
HE	25.900		26.100	1.020		1.028
L[3]	0.450		0.750	0.018		0.030
L1		1.000			0.039	
ZD		1.250			0.049	
ZE		1.250			0.049	
q	0 °		7 °	0 °		7 °
Tolerance	mm			inches		
ccc	0.080			0.0031		

1 Controlling dimension: millimeter

2 Values in inches are converted from mm and rounded to 4 decimal digits.

3 L dimension is measured at gauge plane at 0.25 mm above the seating plane

4.1.2 144 LQFP

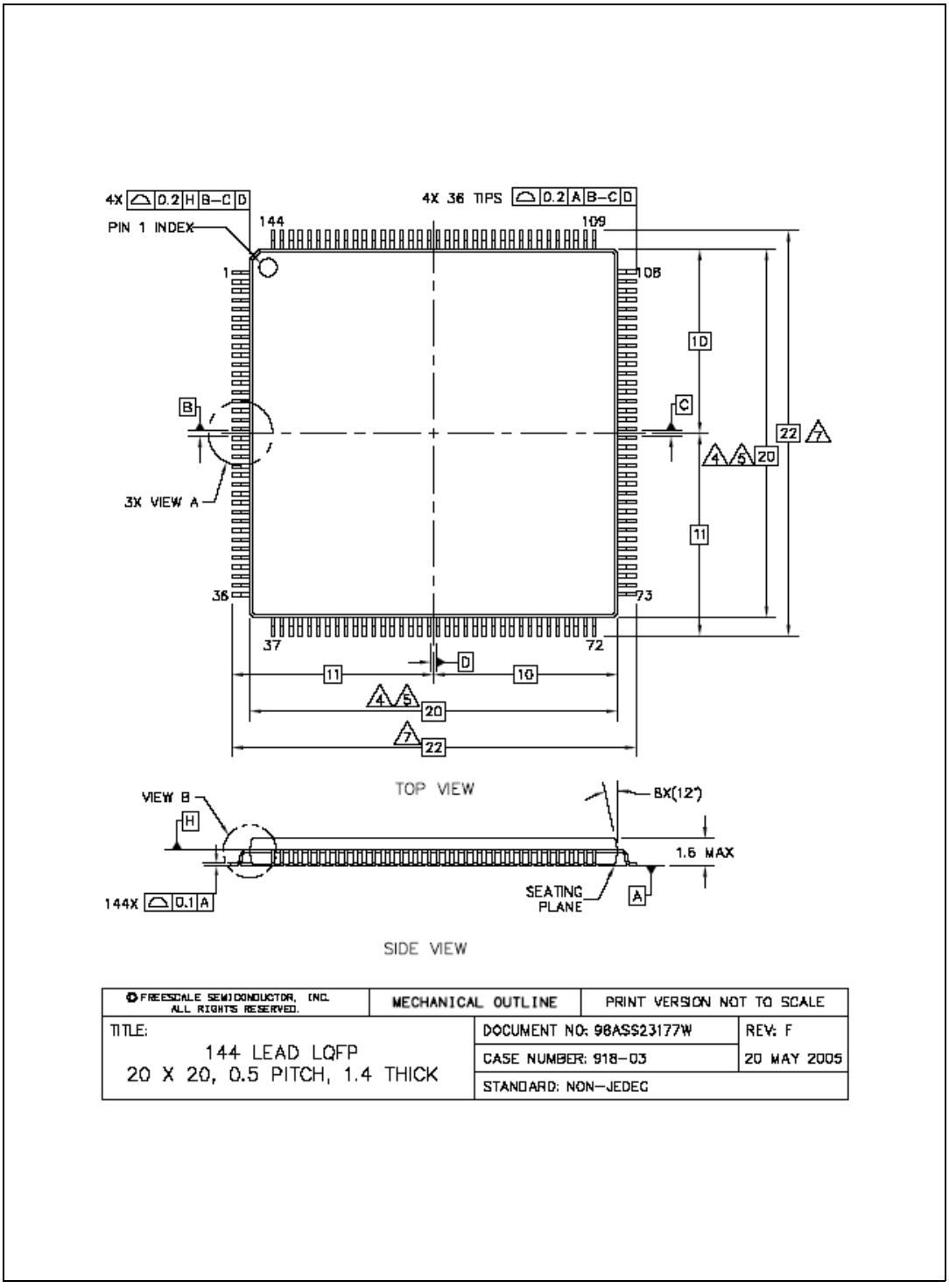


Figure 35. 144 LQFP package mechanical drawing (Part 1 of 2)

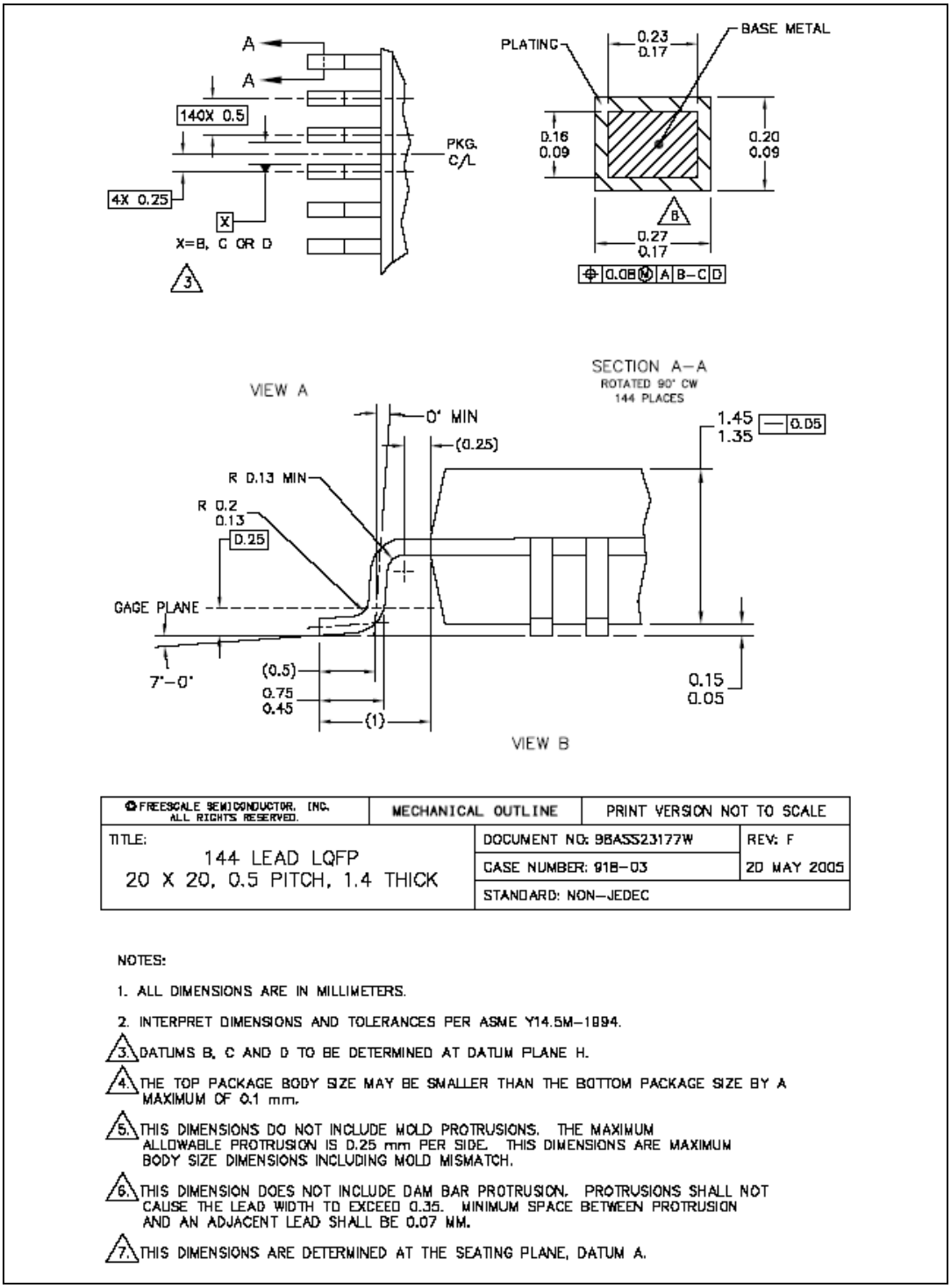


Figure 36. 144 LQFP package mechanical drawing (Part 2 of 2)

Table 45. LQFP144 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3		17.500			0.6890	
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3		17.500			0.6890	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0.0 °	3.5 °	7.0°	3.5 °	0.0 °	7.0 °
Tolerance	mm			inches		
ccc	0.080			0.0031		

[1] Values in inches are converted from mm and rounded to 4 decimal digits.

4.1.3 100 LQFP

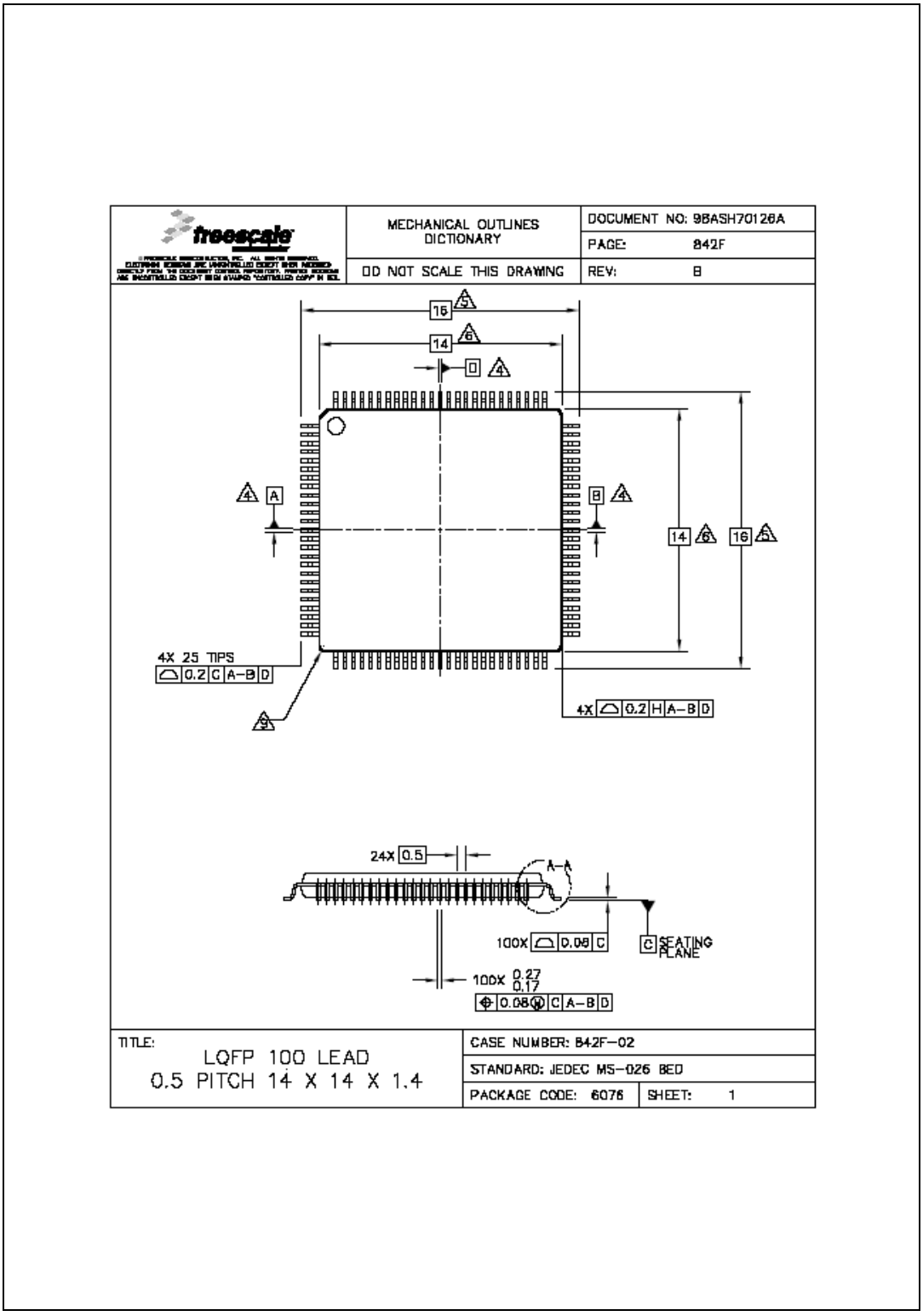
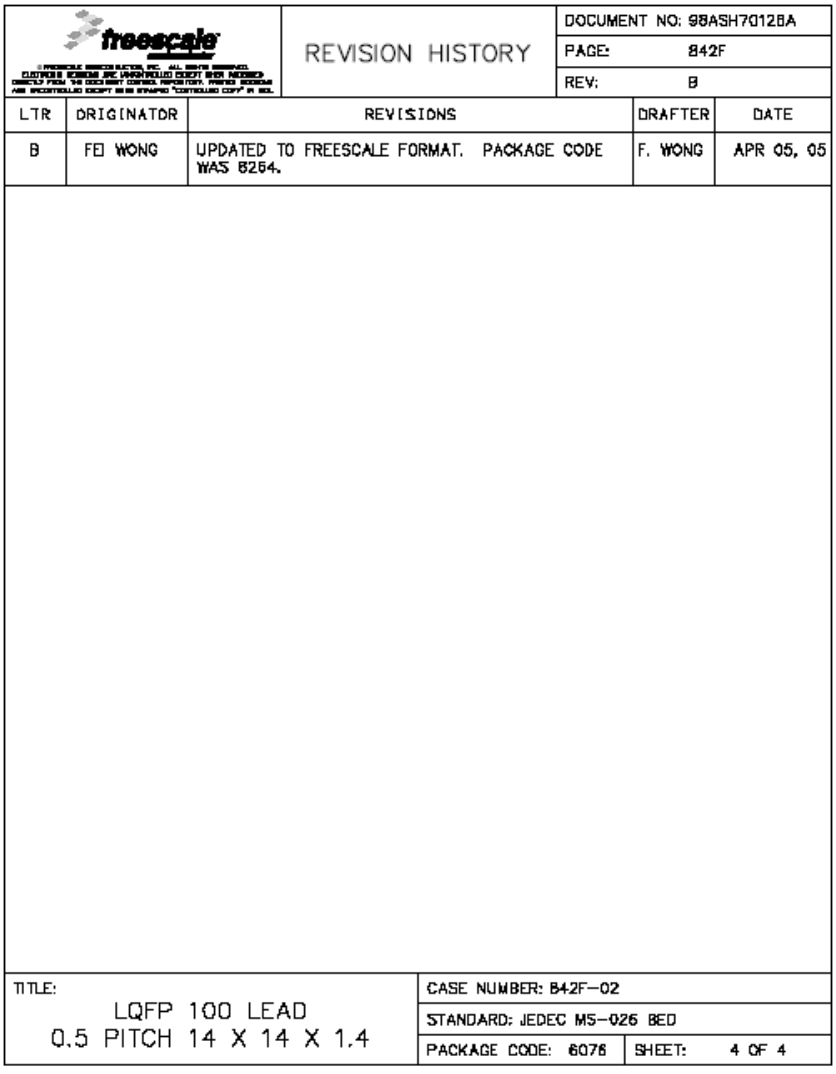


Figure 37. 100 LQFP package mechanical drawing (Part 1 of 3)



freescale	REVISION HISTORY	DOCUMENT NO: 98ASH70126A
		PAGE: 842F
		REV: B

LTR	ORIGINATOR	REVISIONS	DRAFTER	DATE
B	FEI WONG	UPDATED TO FREESCALE FORMAT. PACKAGE CODE WAS 8254.	F. WONG	APR 05, 05

TITLE: LQFP 100 LEAD 0.5 PITCH 14 X 14 X 1.4	CASE NUMBER: 842F-02	
	STANDARD: JEDEC MS-026 BED	
	PACKAGE CODE: 6076	SHEET: 4 OF 4

Figure 38. 100 LQFP package mechanical drawing (Part 2 of 3)

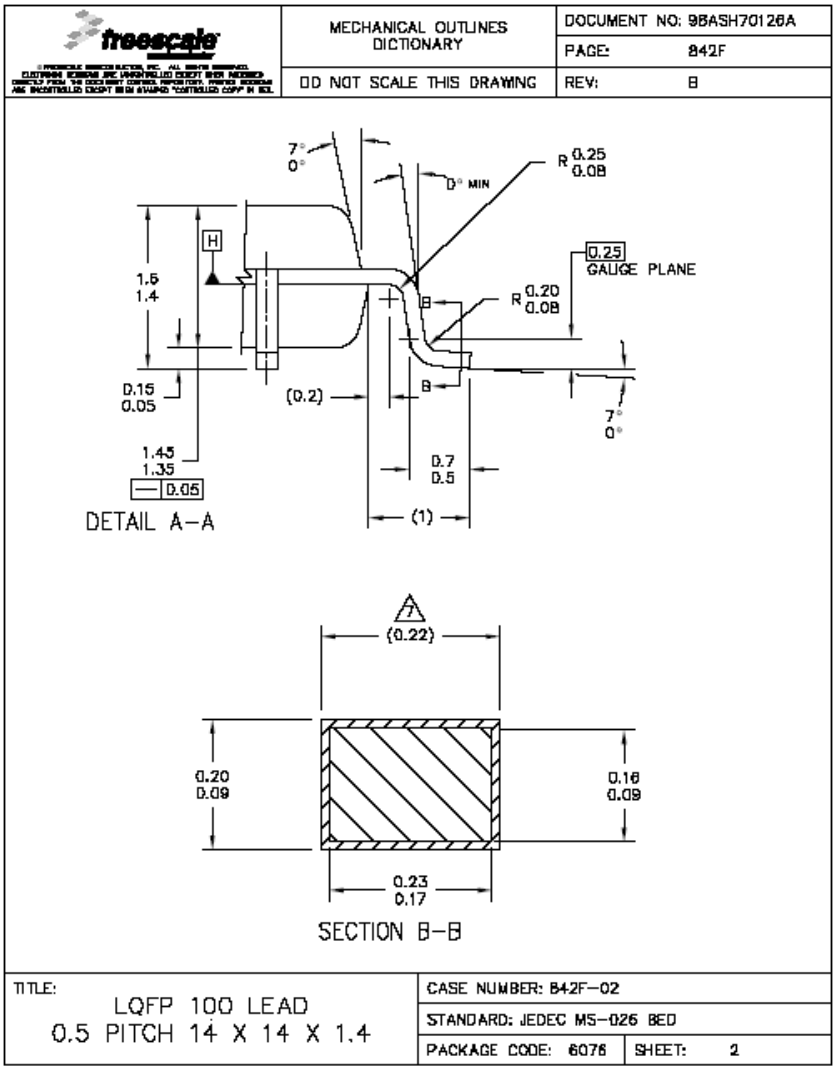


Figure 39. 100 LQFP package mechanical drawing (Part 3 of 3)

Table 46. LQFP100 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3		12.000			0.4724	
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3		12.000			0.4724	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °
Tolerance	**mm**			**inches**		
ccc	0.080			0.0031		

[1] Values in inches are converted from mm and rounded to 4 decimal digits.

4.1.4 208MAPBGA

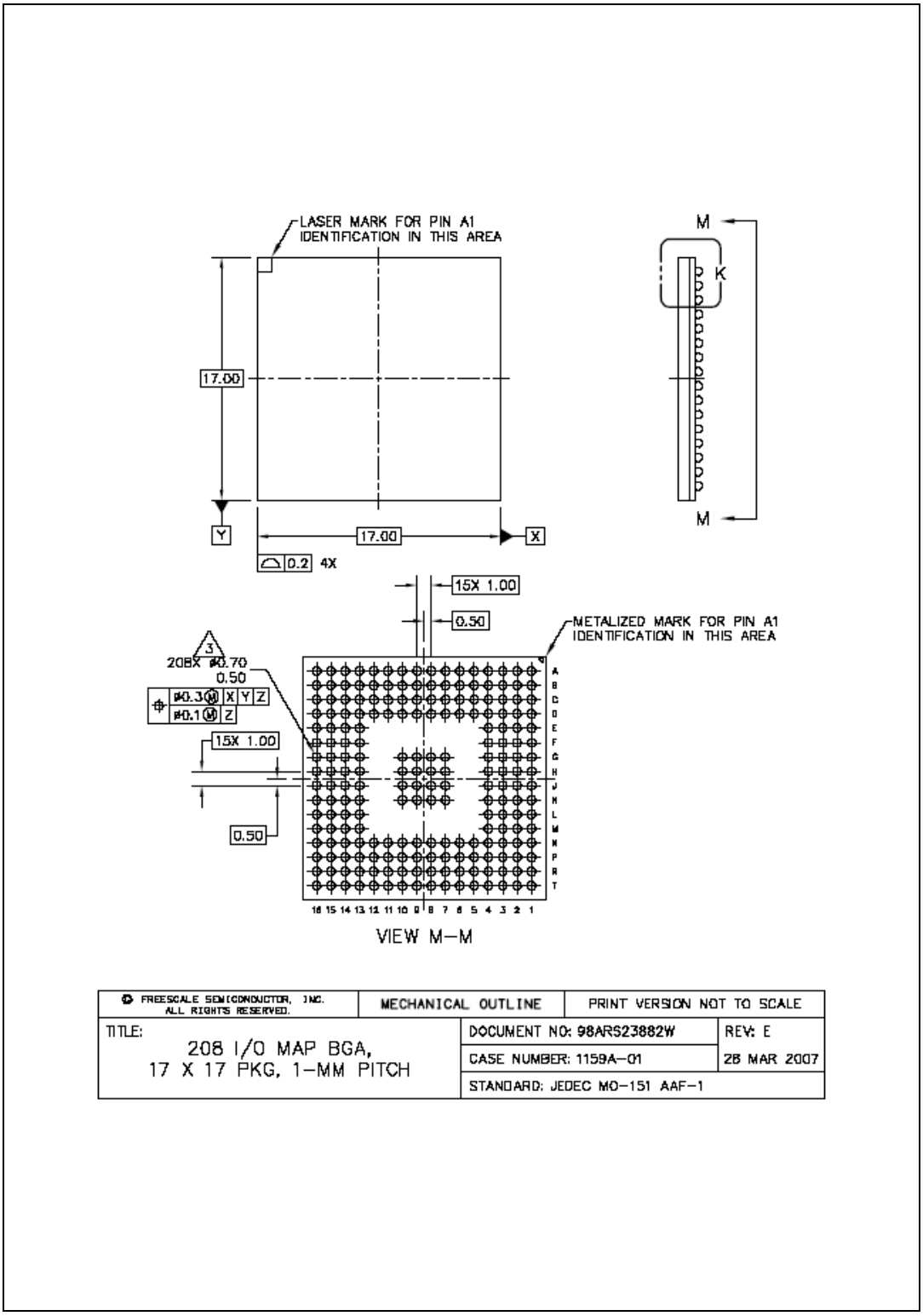


Figure 40. 208 MAPBGA package mechanical drawing (Part 1 of 2)

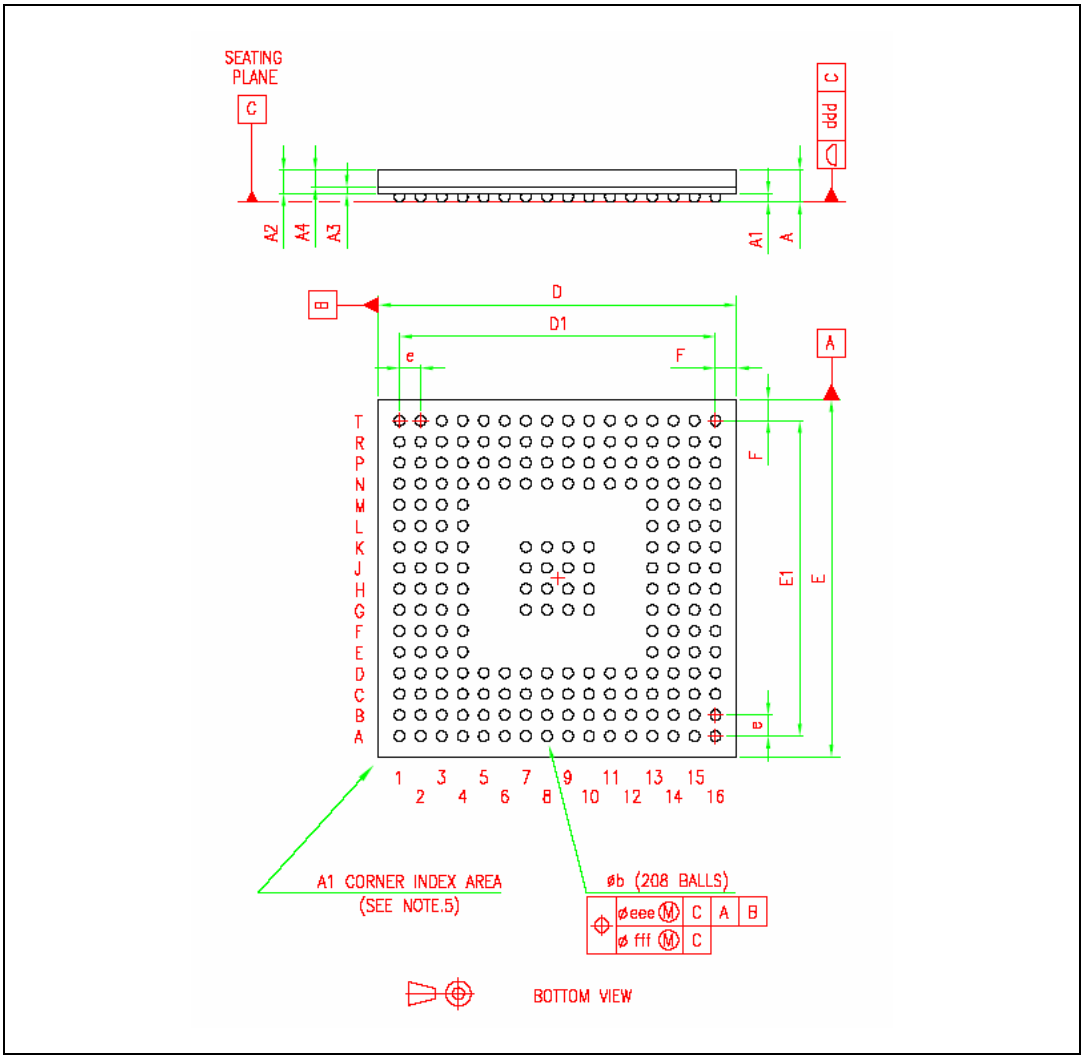


Figure 41. 208 MAPBGA package mechanical drawing (Part 2 of 2)

Table 47. LBGA208 mechanical data

Symbol	mm			inches[1]			Notes
	Min	Typ	Max	Min	Typ	Max	
A			1.70			0.0669	2
A1	0.30			0.0118			
A2		1.085			0.0427		
A3		0.30			0.0118		
A4			0.80			0.0315	
b	0.50	0.60	0.70	0.0197	0.0236	0.0276	3

Table 47. LBGA208 mechanical data (continued)

Symbol	mm			inches[1]			Notes
	Min	Typ	Max	Min	Typ	Max	
D	16.80	17.00	17.20	0.6614	0.6693	0.6772	
D1		15.00			0.5906		
E	16.80	17.00	17.20	0.6614	0.6693	0.6772	
E1		15.00			0.5906		
e		1.00			0.0394		
F		1.00			0.0394		
ddd			0.20			0.0079	
eee			0.25			0.0098	4
fff			0.10			0.0039	5

1 Values in inches are converted from mm and rounded to 4 decimal digits.

2 LBGA stands for **L**ow profile **B**all **G**rid **A**rray.
- Low profile: The total profile height (Dim A) is measured from the seating plane to the top of the component
- The maximum total package height is calculated by the following methodology:
A2 Typ+A1 Typ +√ ($A1^2$+$A3^2$+$A4^2$ tolerance values)
- Low profile: 1.20mm < A ≤ 1.70mm

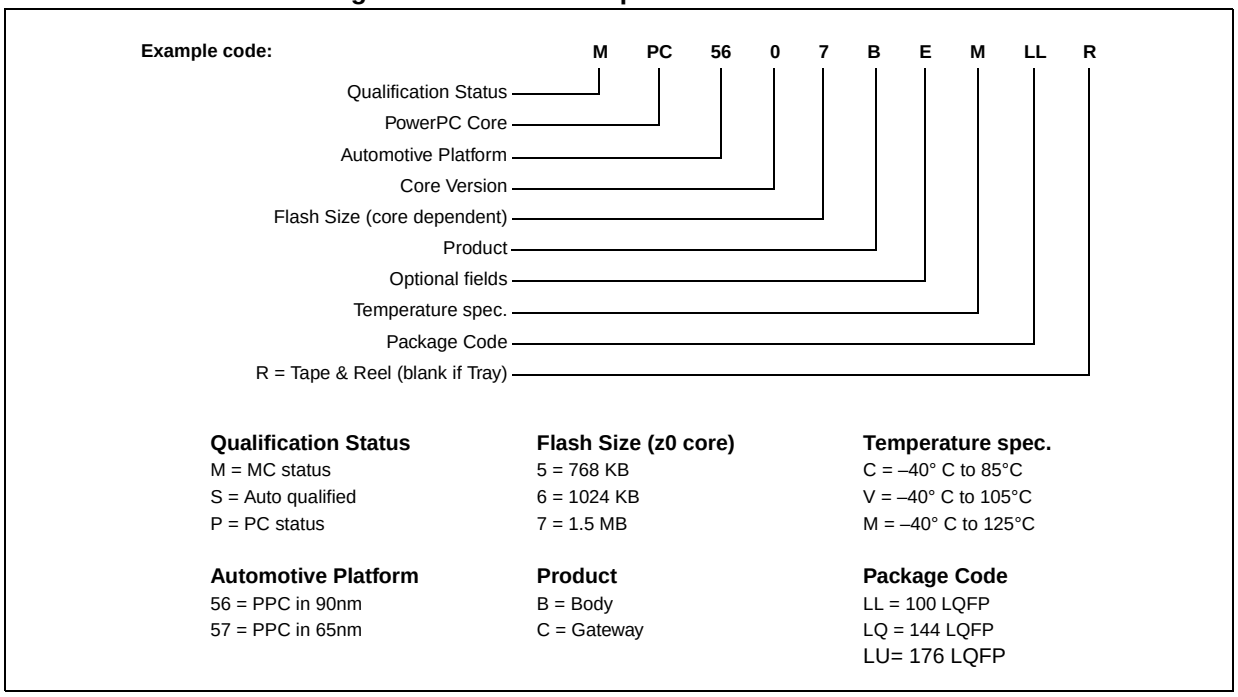
3 The typical ball diameter before mounting is 0.60mm.

4 The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.

5 The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

5 Ordering information

Figure 42. Commercial product code structure



[1] 208 MAPBGA available only as development package for Nexus2+

6 Revision history

Table 48 summarizes revisions to this document.

Table 48. Revision history

Revision	Date	Substantive changes
1	12-Jan-2009	Initial release
2	09 Nov-2009	Updated Features -Replaced 27 IRQs in place of 23 -ADC features -External Ballast resistor support conditions -updated device summary-added 208 BGA details -updated block diagram to include WKUP -updated block diagram to include 5 ch ADC 12 -bit -updated Block summary table -updated LQFP 144, 176 and 100 pinouts. Applied new naming convention for ADC signals as ADCx_P[x] and ADCx_S[x] Section 1, “General description -updated Bolero 1.5M device comparison table -updated block diagram-aligned with 512k -updated block summary-aligned with 512k Section 2, “Package pinouts -updated 100,144,176,208 packages according to cut2.0 changes Added Section 3.5.1, “External ballast resistor recommendations Added NVUSRO [WATCHDOG_EN] field description updated Absolute maximum ratings updated LQFP thermal characteristics updated I/O supply segments updated Voltage regulator capacitance connection updated Low voltage monitor electrical characteristics updated Low voltage power domain electrical characteristics updated DC electrical characteristics updated Program/Erase specifications updated Conversion characteristics (10 bit ADC) updated FMPLL electrical characteristics updated Fast RC oscillator electrical characteristics-aligned with Bolero 512K updated On-chip peripherals current consumption updated ADC characteristics and error definitions diagram updated ADC conversion characteristics (10 bit and 12 bit) Added ADC characteristics and error definitions diagram for 12 bit ADC
3	25 Jan-2010	Updated Features Updated block diagram to connect peripherals to pad I/O Updated block summary to include ADC 12-bit Updated 144, 176 and 100 pinouts to adjust format issues Table 26 Flash module life-retention value changed from 1-5 to 5 yrs Minor editing changes

Appendix A
Abbreviations

Table 49 lists abbreviations used but not defined elsewhere in this document.

Table 49. Abbreviations

Abbreviation	Meaning
CMOS	Complementary metal–oxide–semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
EVTO	Event out
LED	Light emitting diode
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select

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