VC-707

LVPECL, LVDS Crystal Oscillator Data Sheet

Previous Vectron Model VCC6

Description

Vectron's VC-707 Crystal Oscillator is a quartz stabilized, differential output oscillator, operating off 3.3 volt supply, hermetically sealed 5x7 ceramic package.

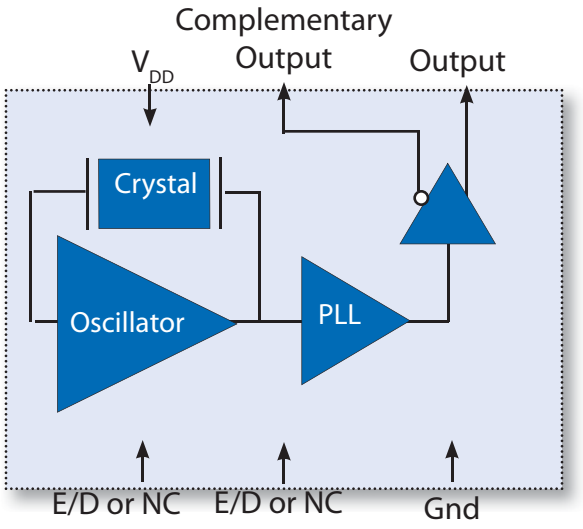
Features

- 3.3V Operation
- Output Frequencies to 800MHz
- Differential Output
- Enable/Disable
- -10/70°C or -40/85°C Operation
- Hermetically Sealed 5x7 Ceramic Package
- Product is compliant to RoHS directive and fully compatible with lead free assembly

Applications

- Storage Area Networking
- Telecom
- Ethernet, GE, SynchE
- Fiber Channel
- PON
- Driving A/D's, D/A's, FPGA's
- Test and Measurement
- Medical
- COTS

Block Diagram



Performance Specifications

Table 1. Electrical Performance, LVPECL Option					
Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage[1]	V_{DD}	3.15	3.3	3.45	V
Current (No Load)	I_{DD}			100	mA
Frequency					
Nominal Frequency[2]	f_N	270		800	MHz
Stability[2,3] (Ordering Options)		±20, ±25, ±32, ±50, ±100			ppm
Outputs					
Output Logic Levels[4], -10/70°C Output Logic High Output Logic Low	 V_{OH} V_{OL}	 V_{DD}-1.025 V_{DD}-1.810		 V_{DD}-0.880 V_{DD}-1.620	V
Output Logic Levels[4], -40/85°C Output Logic High Output Logic Low	 V_{OH} V_{OL}	 V_{DD}-1.085 V_{DD}-1.830		 V_{DD}-0.880 V_{DD}-1.555	V
Output Rise and Fall Time[4] Rise Time Fall Time	t_R/t_F			 600 600	 ps ps
Output Load		50 ohms to V_{DD}-1.3V			
Duty Cycle[5]		45	50	55	%
Jitter (12 kHz - 20 MHz BW)155.52MHz[6]	ϕJ		2		ps
Period Jitter[7] RMS P/P	ϕJ		 4 30		 ps ps
Enable/Disable					
Output Enabled[8] Output Disabled	V_{IH} V_{IL}	0.7*V_{DD}		 0.3*V_{DD}	V V
Enable/Disable Leakage Current				±200	uA
Start-Up Time	t_{SU}			10	ms
Operating Temp. (Ordering Option)	T_{OP}	-10/70 or -40/85			°C
Package Size		5.0 x 7.0 x 1.8 or 5.08x7.5x2.2			mm

1. The VC-707 power supply pin should be filtered, eg, a 0.1 and 0.01uf capacitor.
2. See Standard Frequencies and Ordering Information for more information.
3. Includes calibration tolerance, operating temperature, supply voltage variations,, aging and IR reflow.
4. Figure 2 defines these parameters and Figure 1 defines the test circuit.
5. Duty Cycle is defines as the On/Time Period.
6. Measured using an Agilent E5052, 155.520MHz. Please see "Typical Phase Noise and Jitter Report for the VC-706 series".
7. Measured using a LeCroy 8600, 25K samples.
8. Outputs will be Enabled if Enable/Disable is left open.

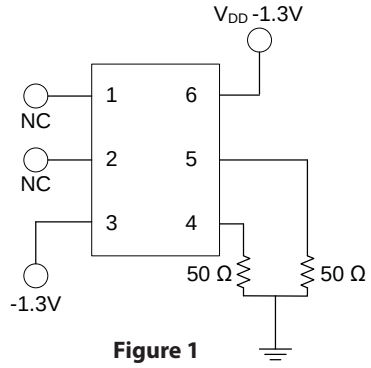


Figure 1

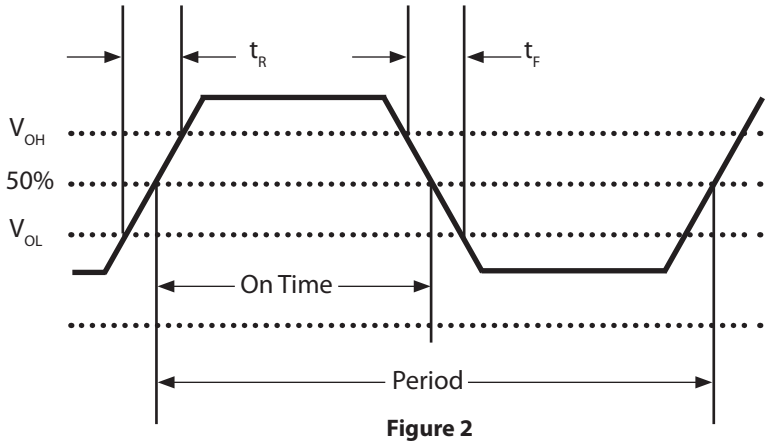


Figure 2

Performance Specifications

Table 2. Electrical Performance, LVDS Option

Parameter	Symbol	Min	Typical	Maximum	Units
Supply					
Voltage[1]	V_{DD}	3.15	3.3	3.45	V
Current (No Load)	I_{DD}			60	mA
Frequency					
Nominal Frequency[2]	f_N	260		800.000	MHz
Stability[2,3,] (Ordering Options)		±20, ±25, ±32, ±50, ±100			ppm
Outputs					
Output Logic Levels[4] Output Logic High Output Logic Low	 V_{OH} V_{OL}	 0.9	 1.40 1.10	 1.6	V
Differential Output		247	330	454	mV
Differential Output Error				50	mV
Offset Voltage		1.125	1.25	1.375	V
Offset Voltage Error				50	mV
Output Leakage Current				10	uA
Output Load		100 ohms differential			
Output Rise and Fall Time[4] Rise Time Fall Time	t_R/t_F			 600 600	 ps ps
Duty Cycle[5]		45	50	55	%
Jitter (12 kHz - 20 MHz BW)155.52MHz[6]	ϕJ		2		ps
Period Jitter[7] RMS P/P	ϕJ		 4 30		 ps ps
Enable/Disable					
Output Enabled[8] Output Disabled	V_{IH} V_{IL}	0.7*V_{DD}		 0.3*V_{DD}	V V
Enable/Disable Leakage Current				±200	uA
Start-Up Time	t_{SU}			10	ms
Operating Temp. (Ordering Option)	T_{OP}	-10/70 or -40/85			°C
Package Size		5.0 x 7.0 x 1.8 or 5.08x7.5x2.2			mm

1. The VC-707 power supply pin should be filtered, eg, a 0.1 and 0.01uf capacitor.
2. See Standard Frequencies and Ordering Information for more information.
3. Includes calibration tolerance, operating temperature, supply voltage variations,, aging and IR reflow.
4. Figure 2 defines these parameters and Figure 3 defines the test circuit.
5. Duty Cycle is defines as the On/Time Period.
6. Measured using an Agilent E5052, 155.520MHz. Please see "Typical Phase Noise and Jitter Report for the VCC6 series".
7. Measured using a LeCroy 8600, 25K samples.
8. Outputs will be Enabled if Enable/Disable is left open.

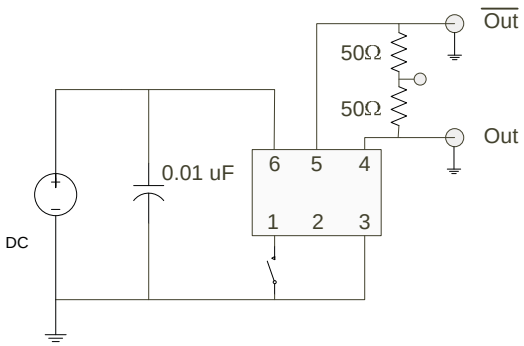


Figure 3

Package and Pinout

Table 3. Pinout		
Pin #	Symbol	Function
1	E/D or NC	Enable Disable or No Connection
2	E/D or NC	Enable Disable or No Connection
3	GND	Electrical and Lid Ground
4	f_O	Output Frequency
5	Cf_O	Complementary Output Frequency
6	V_{DD}	Supply Voltage

The Enable/Disable function is set at the factory on either pin 1 or pin 2 and is an ordering option

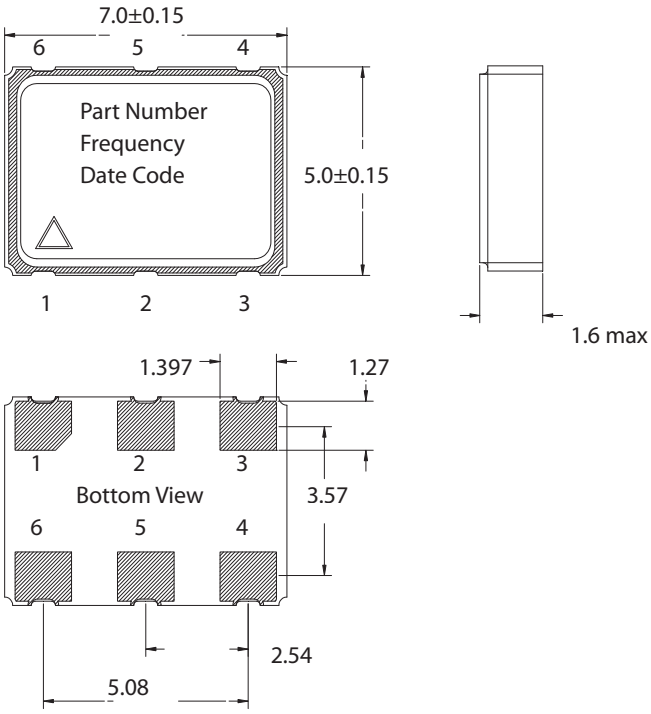


Figure 4 Package A Outline Drawing

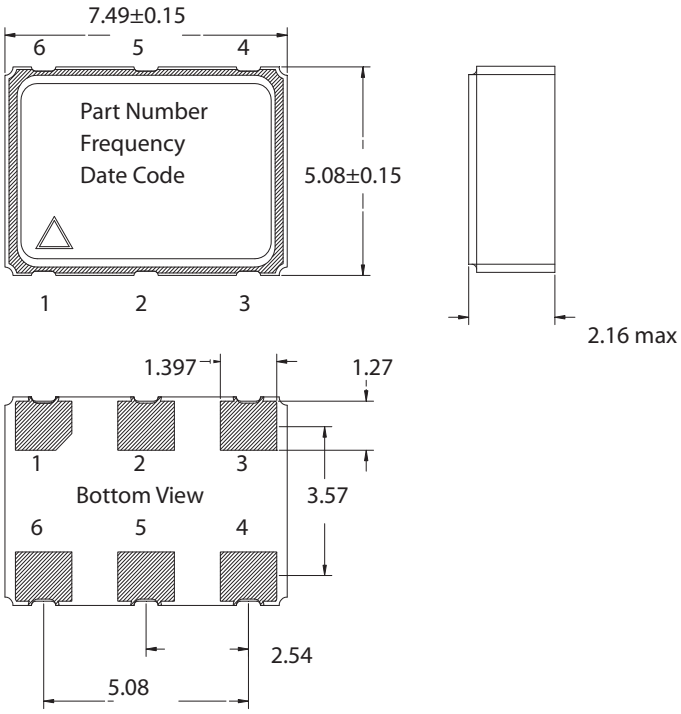


Figure 5 Optional Package Outline Drawing

The VC-707 can be supplied in one of two package options and Figure 4 shows the primary package used. The pad layout and dimesnions are identical and a reel would include only 1 of the two options

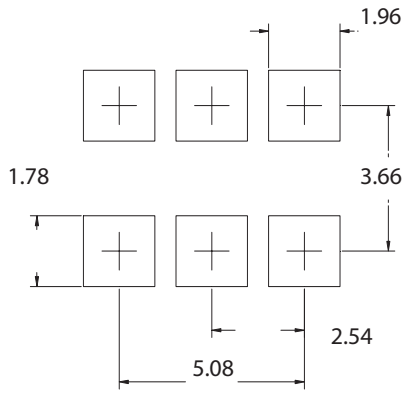


Figure 6 Pad Layout

LVPECL Application Diagrams

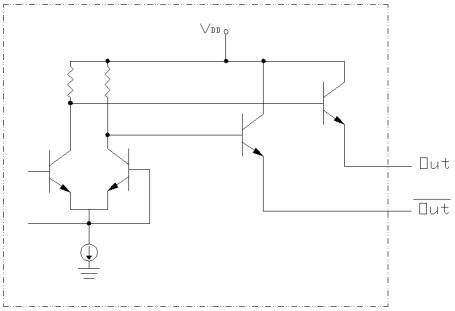


Figure 7 Standard PECL Output Configuration

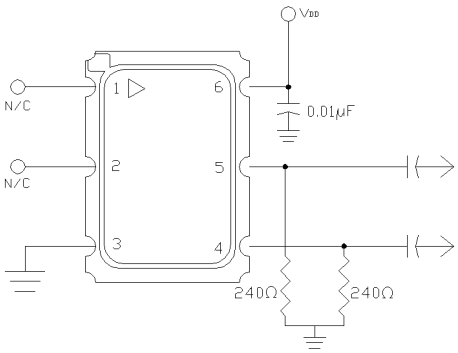


Figure 8 Single Resistor Termination Scheme
Resistor values are typically 120 to 240 ohms for 3.3V operation.
Resistor values are typically 82 to 120 ohms for 2.5V operation.

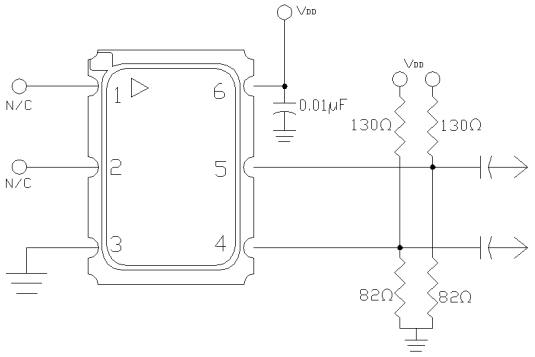


Figure 9 Pull-Up Pull Down Termination
Resistor values are typically for 3.3V operation
For 2.5V operation, the resistor to ground is 62 ohms and the resistor to supply is 240 ohms

The VC-707 incorporates a standard PECL output scheme, which are un-terminated emitters as shown in Figure 7. There are numerous application notes on terminating and interfacing PECL logic and the two most common methods are a single resistor to ground, Figure 8, and a pull-up/pull-down scheme as shown in Figure 9. An AC coupling capacitor is optional, depending on the application and the input logic requirements of the next stage.

LVDS Application Diagrams

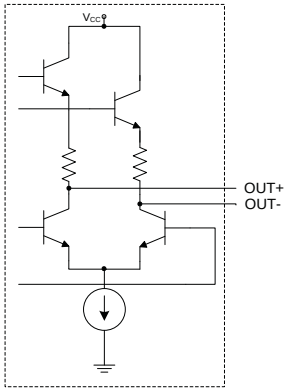


Figure 10 Standard LVDS Output Configuration

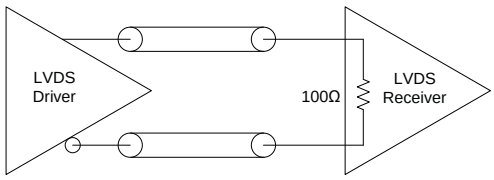


Figure 11 LVDS to LVDS Connection, Internal 100ohm
Some LVDS structures have an internal 100 ohm resistor on the input and do not need additional components.

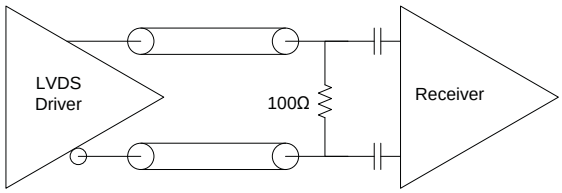


Figure 12 LVDS to LVDS Connection External 100ohm and AC blocking caps
Some input structures may not have an internal 100 ohm resistor on the input and will need an external 100ohm resistor for impedance matching. Also, the input may have an internal DC bias which may not be compatible with LVDS levels, AC blocking capacitors can be used.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left un-terminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50 ohm impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

Environmental and IR Compliance

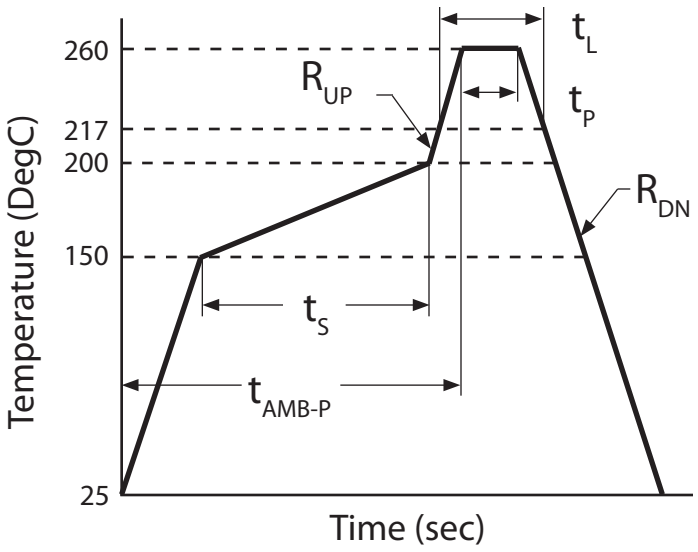
Table 4. Environmental Compliance	
Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002
Mechanical Vibration	MIL-STD-883 Method 2007
Temperature Cycle	MIL-STD-883 Method 1010
Solderability	MIL-STD-883 Method 2003
Fine and Gross Leak	MIL-STD-883 Method 1014
Resistance to Solvents	MIL-STD-883 Method 2015
Moisture Sensitivity Level	MSL1
Contact Pads	Gold over Nickel

IR Compliance

Suggested IR Profile

Devices are built using lead free epoxy and can be subjected to standard lead free IR reflow conditions shown in Table 5. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220C.

Table 5. Reflow Profile		
Parameter	Symbol	Value
PreHeat Time	ts	200 sec Max
Ramp Up	R_{UP}	3°C/sec Max
Time above 217°C	tL	150 sec Max
Time to Peak Temperature	tAMB-P	480 sec Max
Time at 260°C	tP	10 sec Max
Time at 240°C	tP2	60 sec Max
Ramp down	R_{DN}	6°C/sec Max



Maximum Ratings, Tape & Reel

Absolute Maximum Ratings and Handling Precautions

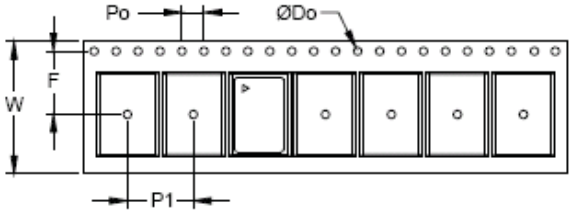
Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied or any other excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

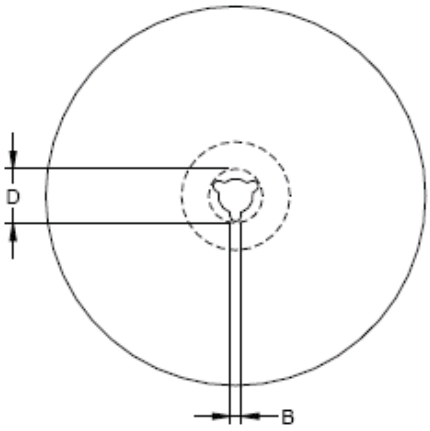
Although ESD protection circuitry has been designed into the VC-707, proper precautions should be taken when handling and mounting, VI employs a Human Body Model and Charged Device Model for ESD susceptibility testing and design evaluation.
ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM a standard resistance of 1.5kOhms and capacitance of 100pF is widely used and therefor can be used for comparison purposes.

Table 6. Maximum Ratings			
Parameter	Symbol	Rating	Unit
Storage Temperature	T_{STORE}	-55/125	°C
Supply Voltage		-0.5 to 5.0	V
Enable Disable Voltage		-0.5 to V_{DD}+0.5	
ESD, Human Body Model		1000	V
ESD, Charged Device Model		1000	V

Table 7. Tape and Reel Information

Tape Dimensions (mm)					Reel Dimensions (mm)							
W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#/Reel
16	7.5	1.5	4	8	180	2	13	21	50	17	21	200





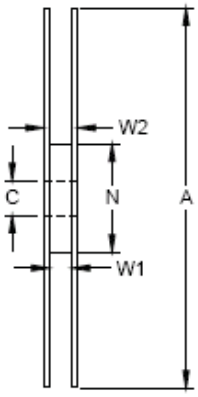


Table 8. Standard Frequencies (MHz)									
311.040	312.000	312.500	320.000	322.2656	332.000	333.000	350.000	400.000	446.000
472.000	500.000	600.000	622.080	625.000	644.5313	657.4219	666.5413	669.3236	669.3265
693.4829	693.750	700.000	779.5686						

Ordering Information

VC-707- E C E - K A A N - xxxMxxxxxx

Product
XO

Package
5x7

Voltage Options
E: +3.3 Vdc ±5%
H: +2.5 Vdc ±5%

Output
C: LVPECL
D: LVDS

Temp Range
W: -10/70°C
E: -40/85°C

Stability
E: ±20ppm
F: ±25ppm
K: ±50ppm
S: ±100ppm

Enable/Disable Logic
A: Enable High

Enable/Disable Pin
A: Pin 1
B: Pin 2

Other (Future Use)
N: Standard

Frequency in MHz

**Note: not all combination of options are available.*
Other specifications may be available upon request.

Example: VC-707-ECE-KAAN-622M080000

For Additional Information, Please Contact

USA:
Vectron International
267 Lowell Road
Hudson, NH 03051
Tel: 1.888.328.7661
Fax: 1.888.329.8328

Europe:
Vectron International
Landstrasse, D-74924
Neckarbischofsheim, Germany
Tel: +49 (0) 3328.4784.17
Fax: +49 (0) 3328.4784.30

Asia:
Vectron International
1F-2F, No 8 Workshop, No 308 Fenju Road
WaiGaoQiao Free Trade Zone
Pudong, Shanghai, China 200131
Tel: 86.21.5048.0777
Fax: 86.21.5048.1881

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