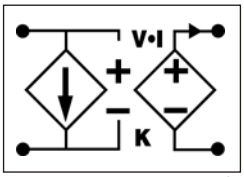
# B048F096T24
# B048F096M24

RoHS

# BCM™
# Bus Converter

- 48 V to 9.6 V V•I Chip™ Converter
- 240 Watt (360 Watt for 1 ms)
- High density – 813 W/in³
- Small footprint – 210 W/in²
- Low weight – 0.5 oz (15 g)
- ZVS / ZCS isolated Sine Amplitude Converter
- Typical efficiency 96%
- 125°C operation ($T_J$)
- <1 µs transient response
- 3.5 million hours MTBF
- No output filtering required




©

**Vin = 38 - 55 V**
**Vout = 7.60 - 11.0 V**
**Iout = 25 A**
**K = 1/5**
**Rout = 12.0 mΩ max**

## Product Description

The V•I Chip Bus Converter Module is a high efficiency (>96%), narrow input range Sine Amplitude Converter (SAC) operating from a 38 to 55 Vdc primary bus to deliver an isolated 7.60 V to 11.0 V secondary. The BCM may be used to power non-isolated POL converters or as an independent 7.60 – 11.0 V source. Due to the fast response time and low noise of the BCM, the need for limited life aluminum electrolytic or tantalum capacitors at the load is reduced—or eliminated—resulting in savings of board area, materials and total system cost.

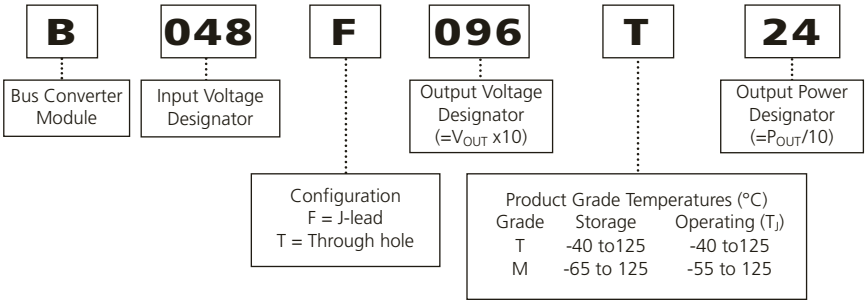
The BCM achieves a power density of 813 W/in³ in a V•I Chip package compatible with standard pick-and-place and surface mount assembly process. The V•I Chip package provides flexible thermal management through its low junction-to-board and junction-to-case thermal resistance. Owing to its high conversion efficiency and safe operating temperature range, the BCM does not require a discrete heat sink in typical applications. Low junction-to-case and junction-to-lead thermal impedances assure low junction temperatures and long life in the harshest environments.

## Absolute Maximum Ratings

| Parameter | Values | Unit | Notes |
|---|---|---|---|
| +In to -In | -1.0 to 60 | Vdc | |
| +In to -In | 100 | Vdc | For 100 ms |
| PC to -In | -0.3 to 7.0 | Vdc | |
| +Out to -Out | -0.5 to 16 | Vdc | |
| Isolation voltage | 2,250 | Vdc | Input to output |
| Output current | 31.5 | A | Continuous |
| Peak output current | 37.5 | A | For 1 ms |
| Output power | 240 | W | Continuous |
| Peak output power | 360 | W | For 1 ms |
| Case temperature | 225 | °C | During reflow MSL 5 |
| Operating junction temperature (1) | -40 to 125 | °C | T-Grade |
| | -55 to 125 | °C | M-Grade |
| Storage temperature | -40 to 125 | °C | T-Grade |
| | -65 to 125 | °C | M-Grade |

**Note:**
(1) The referenced junction is defined as the semiconductor having the highest temperature. This temperature is monitored by a shutdown comparator.

## Part Numbering



## Input (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

| Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|
| Input voltage range | 38 | 48 | 55 | Vdc | |
| Input dV/dt | | | 1 | V/µs | |
| Input undervoltage turn-on | | | 38.0 | Vdc | |
| Input undervoltage turn-off | 32.0 | | | Vdc | |
| Input overvoltage turn-on | 55.0 | | | Vdc | |
| Input overvoltage turn-off | | | 59.5 | Vdc | |
| Input quiescent current | | 2.5 | | mA | PC low |
| Inrush current overshoot | | 5.3 | | A | Using test circuit in Figure 20; See Figure 1 |
| Input current | | | 5.4 | Adc | |
| Input reflected ripple current | | 140 | | mA p-p | Using test circuit in Figure 20; See Figure 4 |
| No load power dissipation | | 3.1 | 4.1 | W | |
| Internal input capacitance | | 4.0 | | µF | |
| Internal input inductance | | 5 | | nH | |
| Recommended external input capacitance | | 47 | | µF | 200 nH maximum source inductance; See Figure 20 |

## Input Waveforms

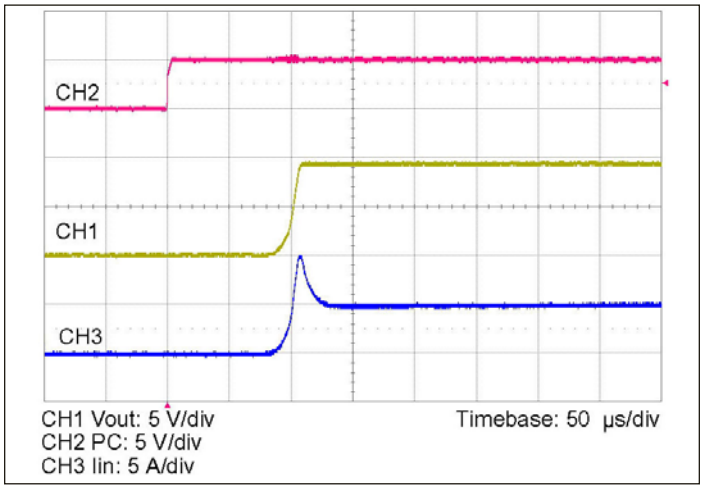



***Figure 1*** *— Inrush transient current at full load and 48 Vin with PC enabled*

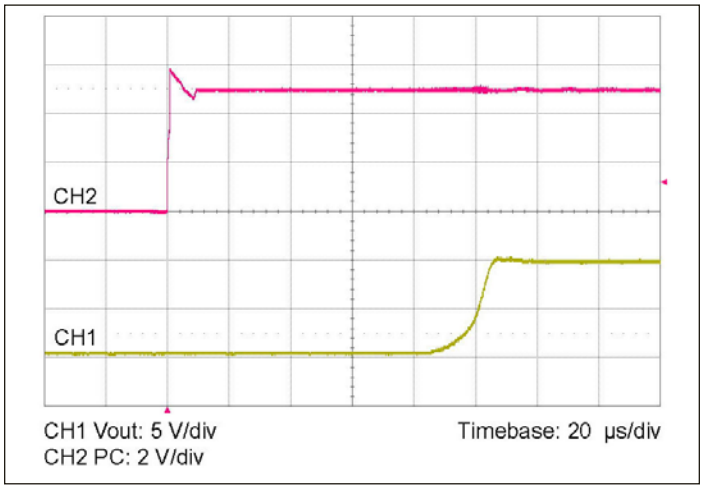



***Figure 2*** *— Output voltage turn-on waveform with PC enabled at full load and 48 Vin*

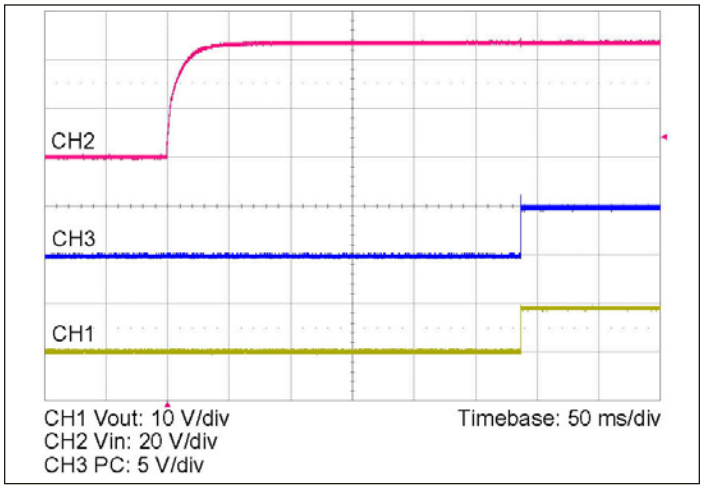



***Figure 3*** *— Output voltage turn-on waveform with input turn-on at full load and 48 Vin*

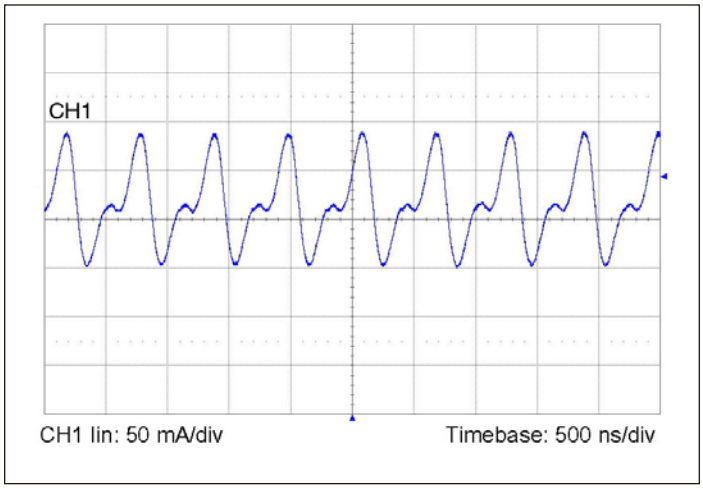



***Figure 4*** *— Input reflected ripple current at full load and 48 Vin*

## Output (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

| Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|
| Output voltage | 7.60 | | 11.0 | Vdc | No load |
| | 7.30 | | 10.7 | Vdc | Full load |
| Output power | 0 | | 240 | W | 40 - 55 $V_{IN}$ |
| | 0 | | 227 | W | 38 - 55 $V_{IN}$ |
| Rated DC current | 0 | | 31.5 | Adc | $P_{OUT} \leq 240$ W |
| Peak repetitive power | | | 360 | W | Max pulse width 1ms, max duty cycle 10%, baseline power 50% |
| Current share accuracy | | 5 | 10 | % | See Parallel Operation on Page 10 |
| Efficiency | | | | | |
| Half load | 95.5 | 96.2 | | % | See Figure 5 |
| Full load | 95.5 | 96.2 | | % | See Figure 5 |
| Internal output inductance | | 1.6 | | nH | |
| Internal output capacitance | | 55 | | µF | Effective value |
| Load capacitance | | | 1,600 | µF | |
| Output overvoltage setpoint | 11.0 | | | Vdc | Module will shut down |
| Output ripple voltage | | | | | |
| No external bypass | | 176 | 200 | mVp-p | See Figures 7 and 9 |
| 10 µF bypass capacitor | | 17 | | mVp-p | See Figure 8 |
| Short circuit protection set point | 33 | | | Adc | Module will shut down |
| Average short circuit current | | 0.43 | | A | |
| Effective switching frequency | 3.0 | 3.1 | 3.4 | MHz | Fixed, 1.6 MHz per phase |
| Line regulation | | | | | |
| K | 0.1980 | 1/5 | 0.2020 | | $V_{OUT} = K \bullet V_{IN}$ at no load |
| Load regulation | | | | | |
| $R_{OUT}$ | | 8.9 | 12.0 | mΩ | |
| Transient response | | | | | |
| Voltage overshoot | | 92 | | mV | 100% load step; See Figures 10 and 11 |
| Response time | | 200 | | ns | See Figures 10 and 11 |
| Recovery time | | 1 | | µs | See Figures 10 and 11 |
| Output overshoot | | | | | |
| Input turn-on | | 0 | | mV | No output filter; See Figure 3 |
| PC enable | | 0 | | mV | No output filter; See Figure 2 |
| Output turn-on delay | | | | | |
| From application of power | | 288 | | ms | No output filter; See Figure 3 |
| From release of PC pin | | 70 | | ms | No output filter |

## Output Waveforms

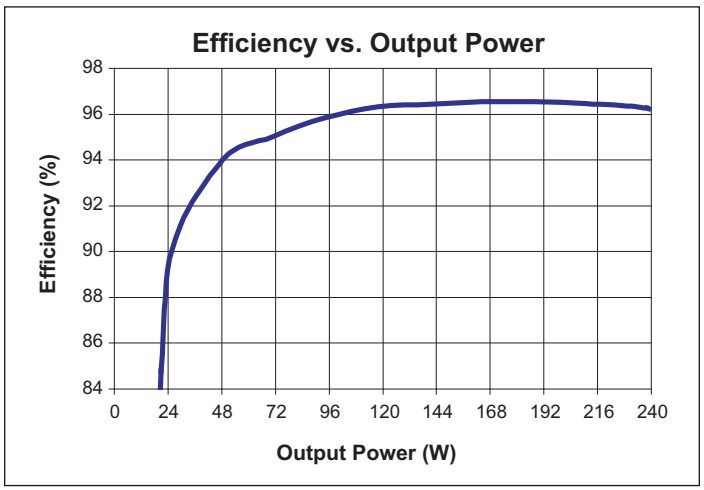



***Figure 5*** *— Efficiency vs. output power*

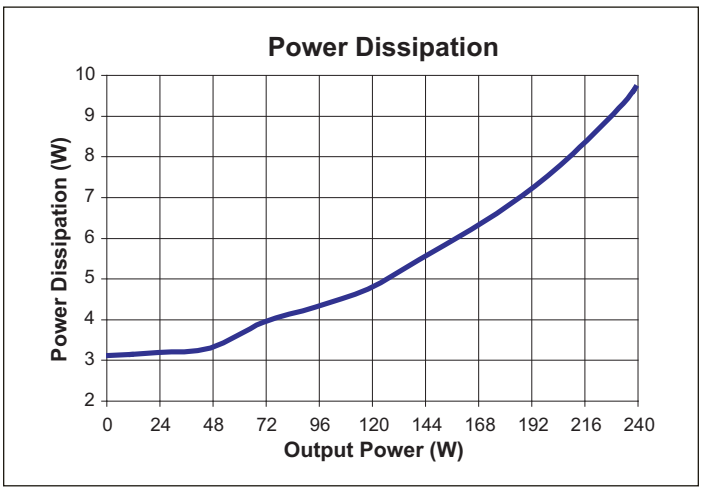



***Figure 6*** *— Power dissipation as a function of output power*

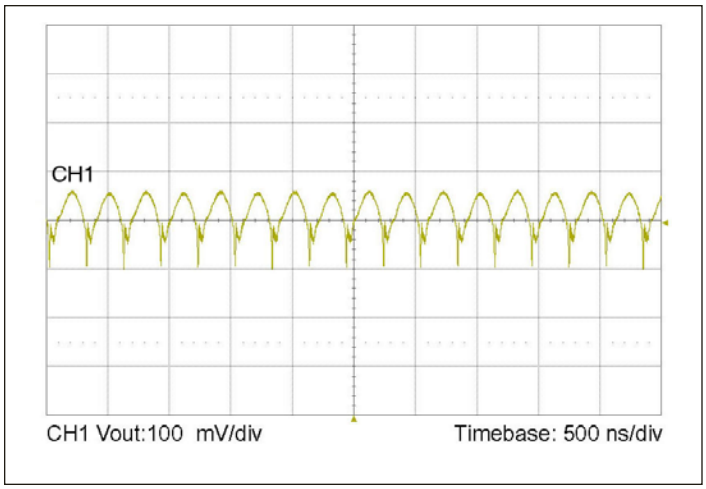



***Figure 7*** *— Output voltage ripple at full load and 48 Vin without any external bypass capacitor.*

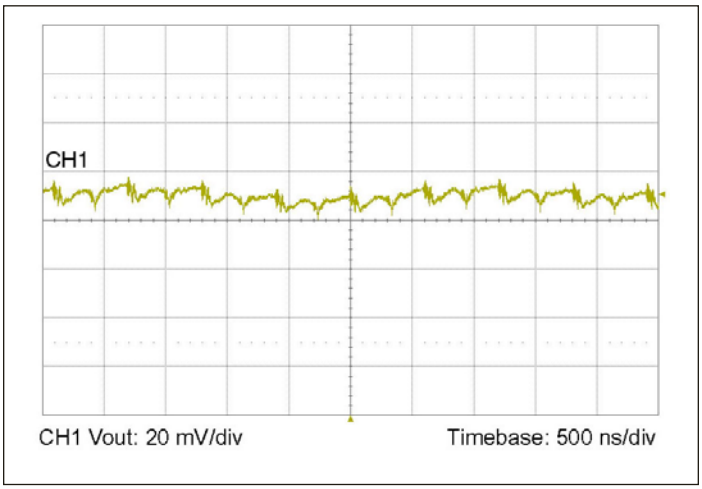



***Figure 8*** *— Output voltage ripple at full load and 48 Vin with 10 µF ceramic external bypass capacitor and 20 nH of distribution inductance.*

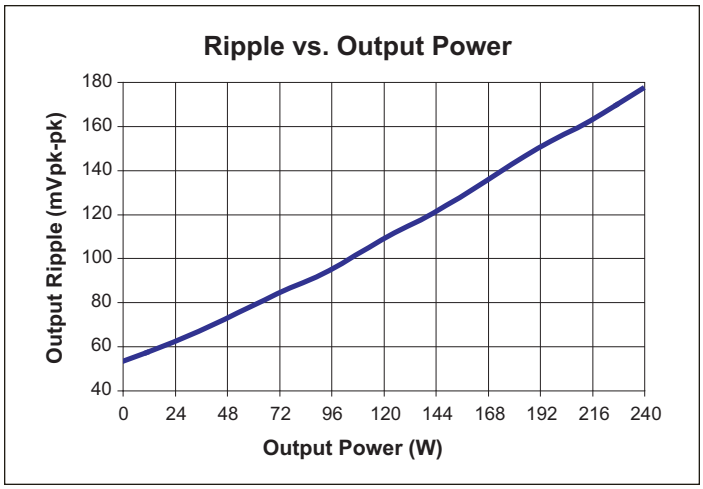



***Figure 9*** *— Output voltage ripple vs. output power at 48 Vin without any external bypass capacitor.*

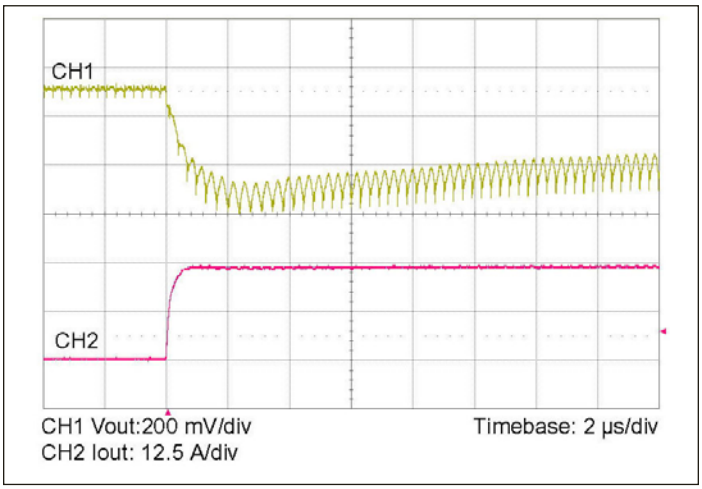



***Figure 10*** *— 0-25 A load step with 100 µF input capacitor and no output capacitor.*

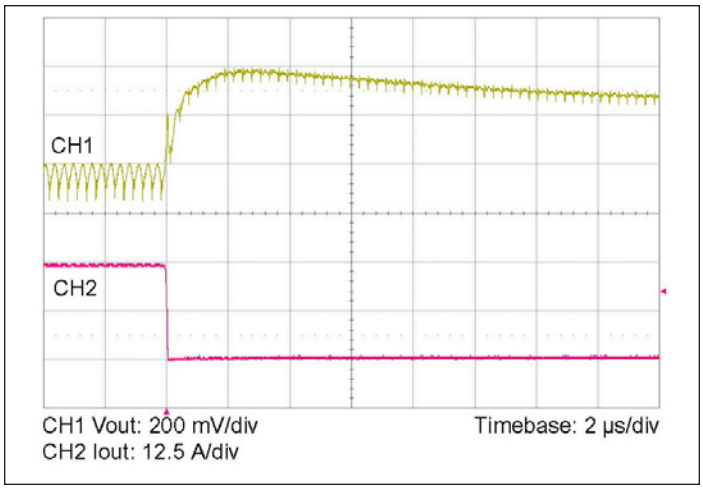



***Figure 11*** *— 25-0 A load step with 100 µF input capacitor and no output capacitor.*

## General

| Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|
| MTBF | | | | | |
| MIL-HDBK-217F | | 3.5 | | Mhrs | 25°C, GB |
| Isolation specifications | | | | | |
| Voltage | 2,250 | | | Vdc | Input to output |
| Capacitance | | 3,000 | | pF | Input to output |
| Resistance | 10 | | | MΩ | Input to output |
| Agency approvals | | cTÜVus | | | UL/CSA 60950-1, EN 60950-1 |
| | | CE Mark | | | Low voltage directive |
| | | RoHS | | | |
| Mechanical | | | | | See Mechanical Drawings, Figures 15 – 18 |
| Weight | | 0.53/15 | | oz/g | |
| Dimensions | | | | | |
| Length | | 1.28/32,5 | | in/mm | |
| Width | | 0.87/22 | | in/mm | |
| Height | | 0.265/6,73 | | in/mm | |
| Thermal | | | | | |
| Over temperature shutdown | 125 | 130 | 135 | °C | Junction temperature |
| Thermal capacity | | 9.3 | | Ws/°C | |
| Junction-to-case thermal impedance ($R_{\theta JC}$) | | 1.1 | | °C/W | |
| Junction-to-board thermal impedance ($R_{\theta JB}$) | | 2.1 | | °C/W | |

## Auxiliary Pins (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

| Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|
| Primary control (PC) | | | | | |
| DC voltage | 4.8 | 5.0 | 5.2 | Vdc | |
| Module disable voltage | 2.4 | 2.5 | | Vdc | |
| Module enable voltage | | 2.5 | 2.6 | Vdc | |
| Current limit | 2.4 | 2.5 | 2.9 | mA | Source only |
| Enable delay time | | 70 | | ms | |
| Disable delay time | | 20 | | µs | See Figure 12, time from PC low to output low |

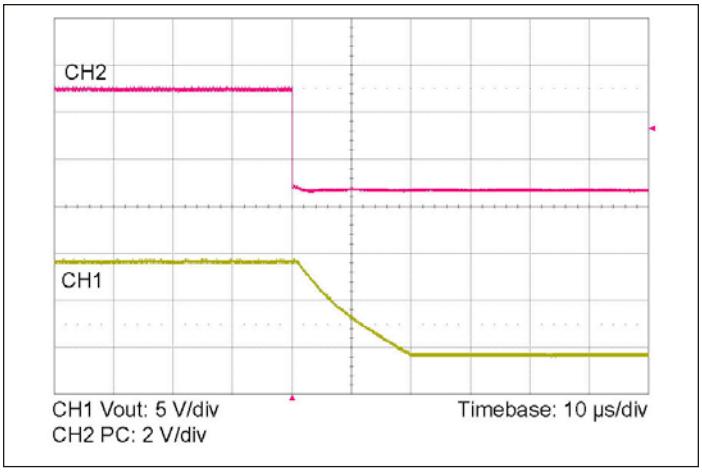



***Figure 12*** — *$V_{OUT}$ at full load vs. PC disable*

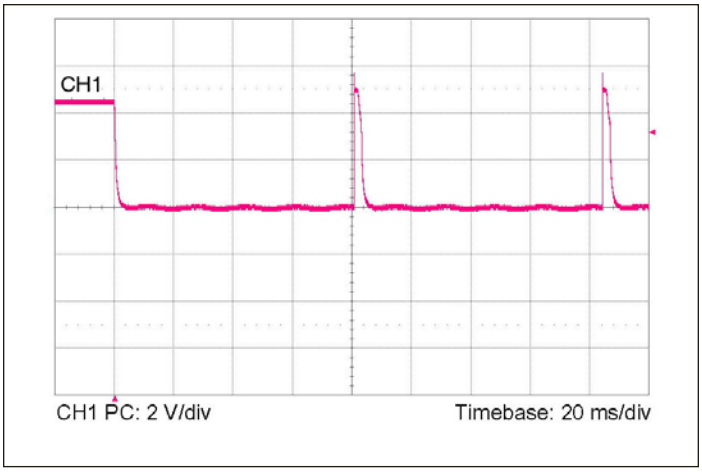



***Figure 13*** — *PC signal during fault*

**+In / -In – DC Voltage Input Ports**

The V•I Chip input voltage range should not be exceeded. An internal under / over voltage lockout function prevents operation outside of the normal operating input range. The BCM turns on within an input voltage window bounded by the "Input under-voltage turn-on" and "Input over-voltage turn-off" levels, as specified. The V•I Chip may be protected against accidental application of a reverse input voltage by the addition of a rectifier in series with the positive input, or a reverse rectifier in shunt with the positive input located on the load side of the input fuse.

The connection of the V•I Chip to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100 nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200 nH, the RC damper may be 47 µF in series with 0.3Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

**PC – Primary Control**

The Primary Control port is a multifunction node that provides the following functions:

Enable / Disable – If the PC port is left floating, the BCM output is enabled. Once this port is pulled lower than 2.4 Vdc with respect to –In, the output is disabled. This action can be realized by employing a relay, opto-coupler, or open collector transistor. Refer to Figures 1-3, 12 and 13 for the typical enable / disable characteristics. This port should not be toggled at a rate higher than 1 Hz. The PC port should also not be driven by or pulled up to an external voltage source.

Primary Auxiliary Supply – The PC port can source up to 2.4 mA at 5.0 Vdc. The PC port should never be used to sink current.

Alarm – The BCM contains circuitry that monitors output overload, input over voltage or under voltage, and internal junction temperatures. In response to an abnormal condition in any of the monitored parameters, the PC port will toggle. Refer to Figure 13 for PC alarm characteristics.

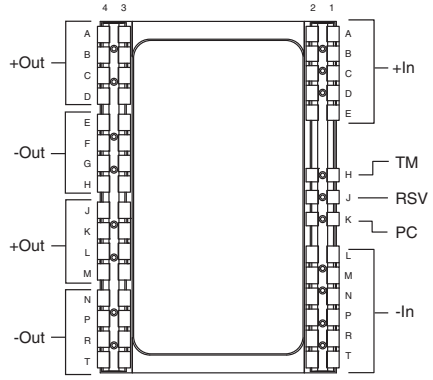
**TM and RSV – Reserved for factory use.**

**+Out / -Out – DC Voltage Output Ports**

Two sets of contacts are provided for the +Out port. They must be connected in parallel with low interconnect resistance. Similarly, two sets of contacts are provided for the –Out port. They must be connected in parallel with low interconnect resistance. Within the specified operating range, the average output voltage is defined by the Level 1 DC behavioral model of Figure 21. The current source capability of the BCM is rated in the specifications section of this document.

The low output impedance of the BCM reduces or eliminates the need for limited life aluminum electrolytic or tantalum capacitors at the input of POL converters.

Total load capacitance at the output of the BCM should not exceed the specified maximum. Owing to the wide bandwidth and low output impedance of the BCM, low frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the input of the BCM.




| Signal Name | Designation |
|---|---|
| +In | A1-E1, A2-E2 |
| –In | L1-T1, L2-T2 |
| TM | H1, H2 |
| RSV | J1, J2 |
| PC | K1, K2 |
| +Out | A3-D3, A4-D4, J3-M3, J4-M4 |
| –Out | E3-H3, E4-H4, N3-T3, N4-T4 |

***Figure 14*** *— BCM pin configuration*

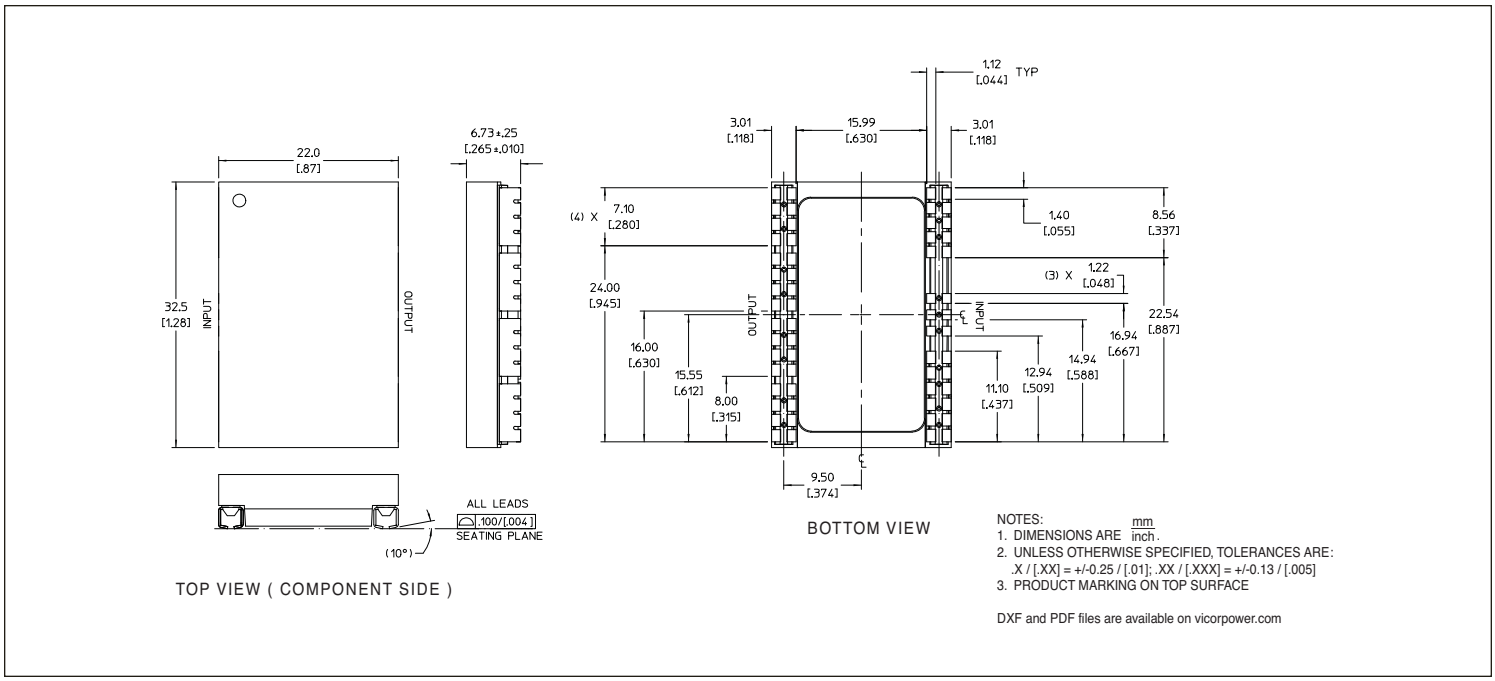



***Figure 15*** *— BCM J-Lead mechanical outline; Onboard mounting*

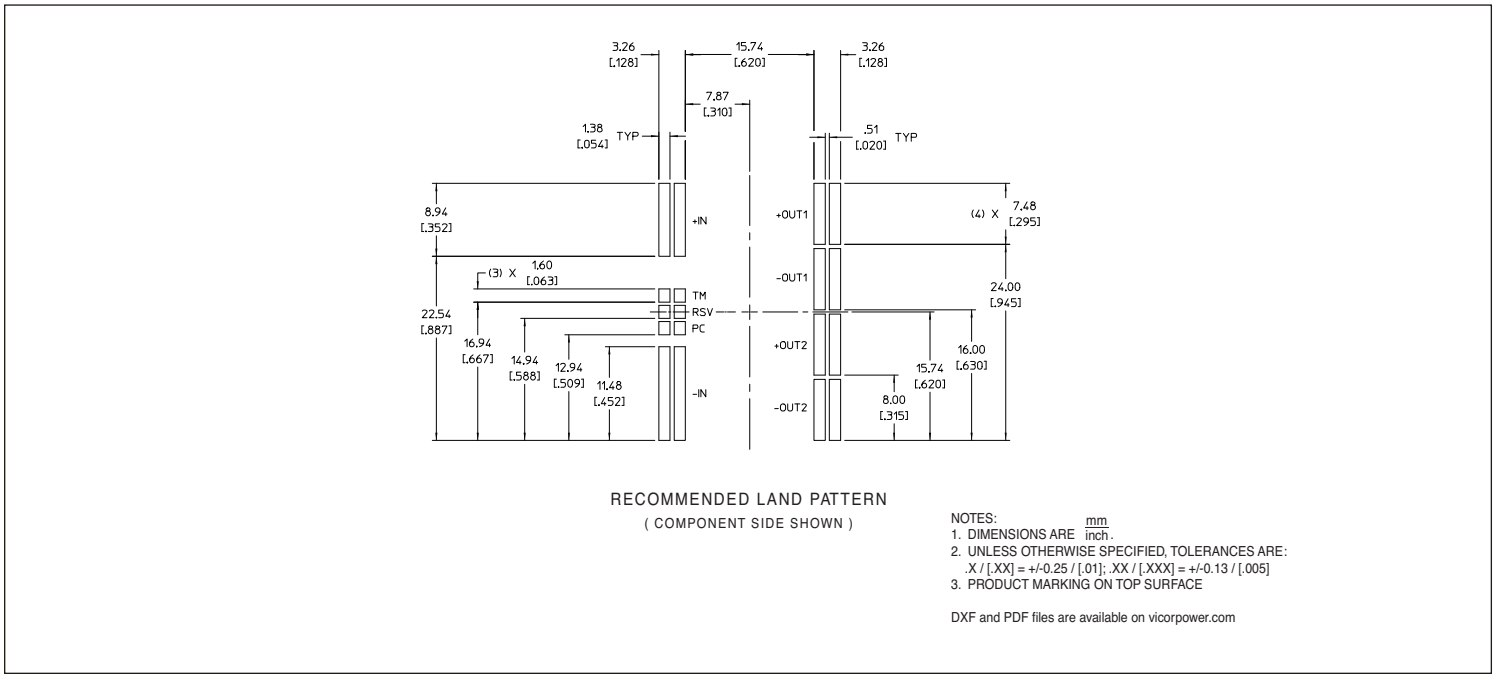



***Figure 16*** *— BCM PCB land layout information*

## Mechanical Drawings (continued)

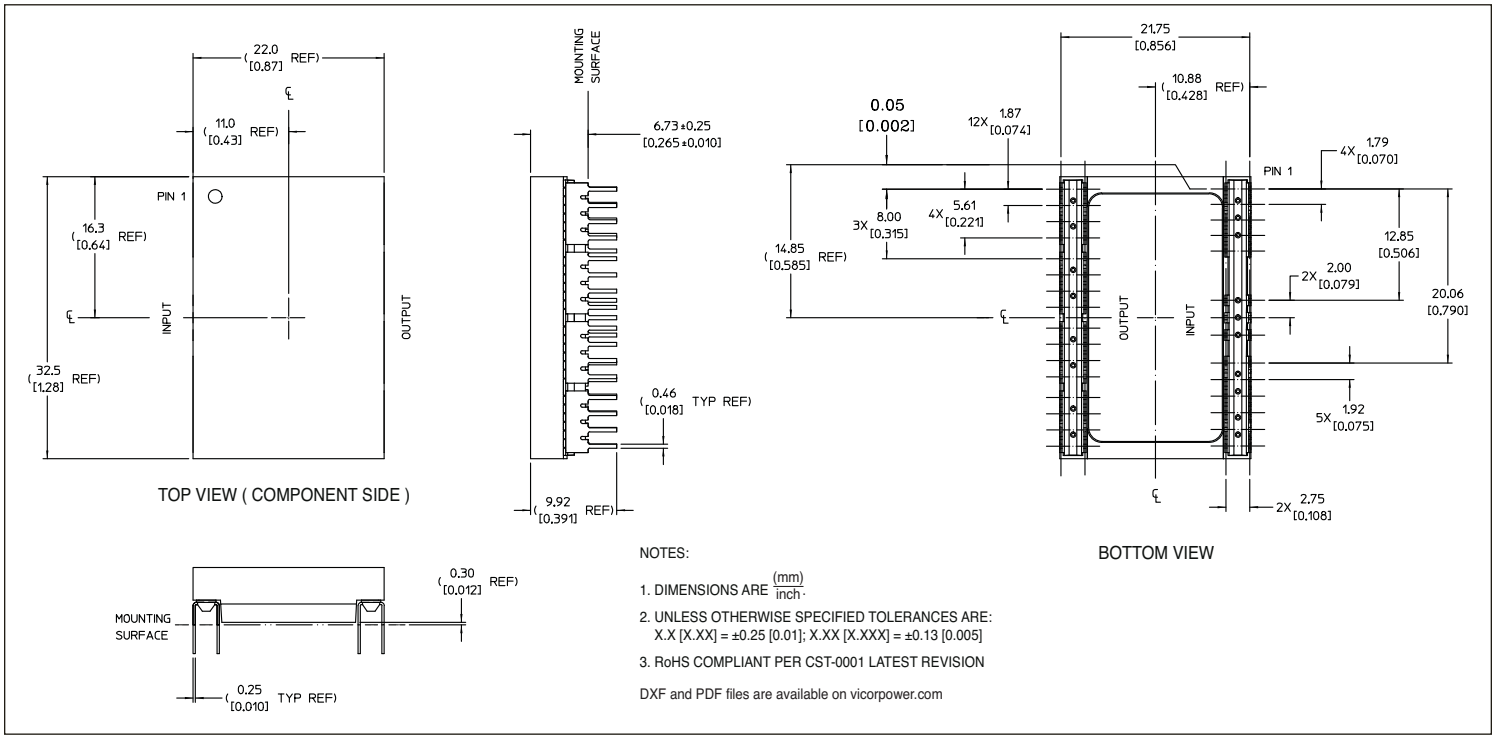



***Figure 17*** *— BCM through-hole mechanical outline*

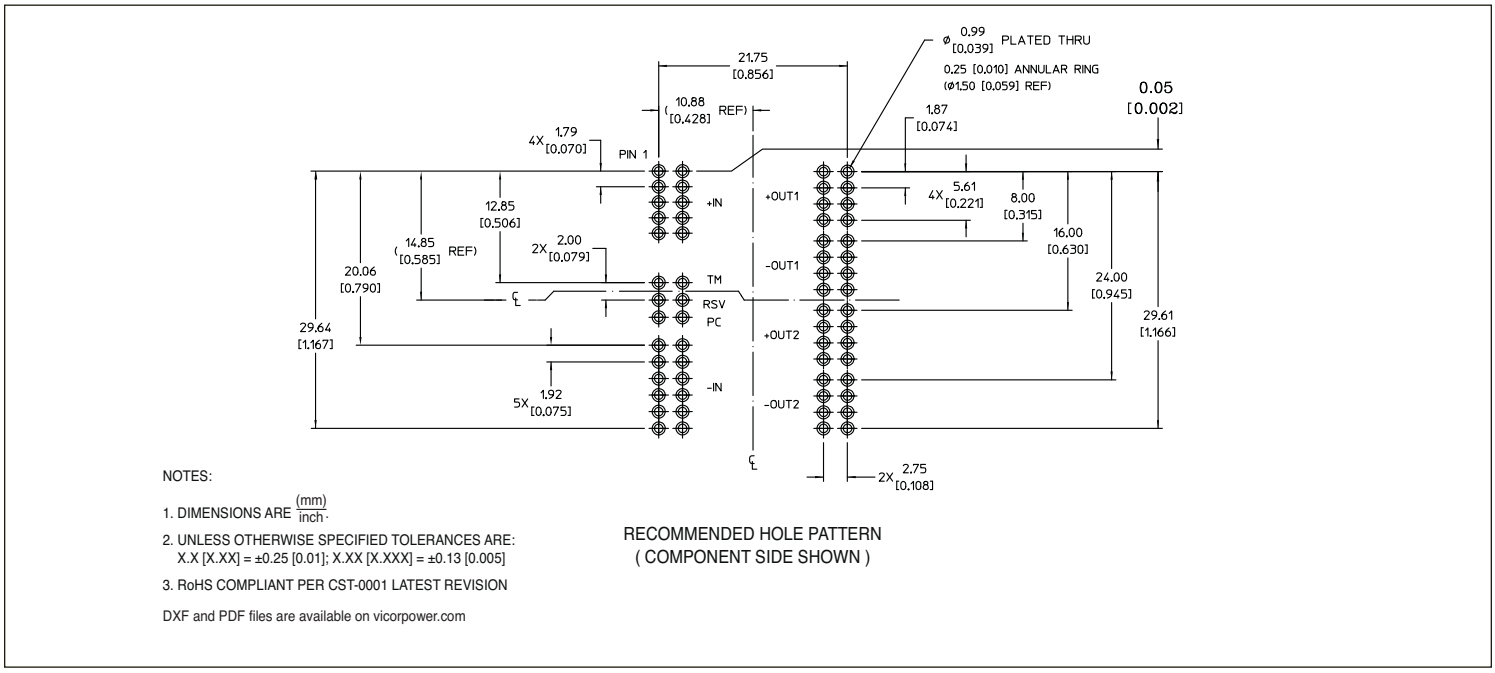
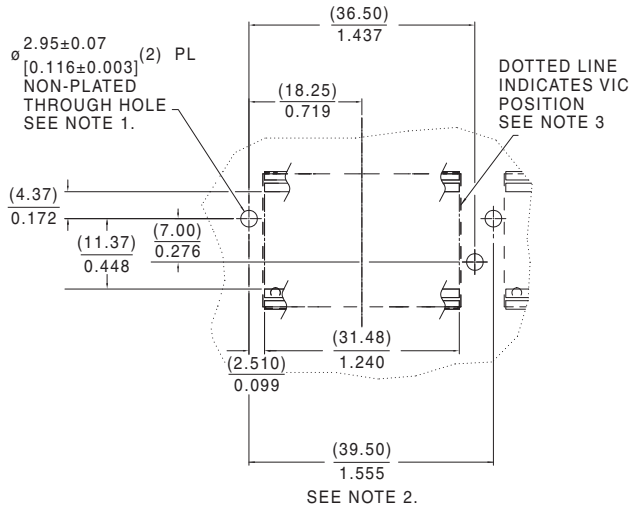



***Figure 18*** *— BCM through-hole PCB layout information*

NOTES:

1. MAINTAIN 3.5/[0.138] DIA. KEEP OUT ZONE FREE OF COPPER. ALL PCB LAYERS.
2. MINIMUM RECOMMENDED PITCH IS 39.50/[1.555]. THIS PROVIDES 7.00/[0.276] COMPONENT EDGE-TO-EDGE SPACING. AND 0.50/[0.020] CLEARANCE BETWEEN VICOR HEAT SINKS.
3. V•I CHIP LAND PATTERN SHOWN FOR REFERENCE ONLY; ACTUAL LAND PATTERN MAY DIFFER. DIMENSIONS FROM EDGES OF LAND PATTERN TO PUSH-PIN HOLES WILL BE THE SAME FOR ALL FULL SIZE V•I CHIPS.
4. DIMENSION ARE (mm) / inch.




HEAT SINK PUSH-PIN HOLE PATTERN
( TOP SIDE SHOWN )
SEE NOTE 3

***Figure 19*** *— Hole location for push pin heat sink relative to V•I Chip*

### Parallel Operation

The BCM will inherently current share when operated in an array. Arrays may be used for higher power or redundancy in an application.

Current sharing accuracy is maximized when the source and load impedance presented to each BCM within an array are equal. The recommended method to achieve matched impedances is to dedicate common copper planes within the PCB to deliver and return the current to the array, rather than rely upon traces of varying lengths. In typical applications the current being delivered to the load is larger than that sourced from the input, allowing traces to be utilized on the input side if necessary. The use of dedicated power planes is, however, preferable.

The BCM power train and control architecture allow bi-directional power transfer, including reverse power processing from the BCM output to its input. Reverse power transfer is enabled if the BCM input is within its operating range and the BCM is otherwise enabled. The BCM's ability to process power in reverse improves the BCM transient response to an output load dump.

### Input Impedance Recommendations

To take full advantage of the BCM capabilities, the impedance presented to its input terminals must be low from DC to approximately 5 MHz. The source should exhibit low inductance (less than 100 nH) and should have a critically damped response. If the interconnect inductance exceeds 100 nH, the BCM input pins should be bypassed with an RC damper (e.g., 47 µF in series with 0.3 ohm) to retain low source impedance and stable operations. Given the wide bandwidth of the BCM, the source response is generally the limiting factor in the overall system response.

Anomalies in the response of the source will appear at the output of the BCM multiplied by its K factor. The DC resistance of the source should be kept as low as possible to minimize voltage deviations. This is especially important if the BCM is operated near low or high line as the over/under voltage detection circuitry could be activated.

### Input Fuse Recommendations

V•I Chips are not internally fused in order to provide flexibility in configuring power systems. However, input line fusing of V•I Chips must always be incorporated within the power system. A fast acting fuse should be placed in series with the +In port.

### Application Notes

For BCM and V•I Chip application notes on soldering, thermal management, board layout, and system design click on the link below:

http://www.vicorpower.com/technical_library/application_information/chips/

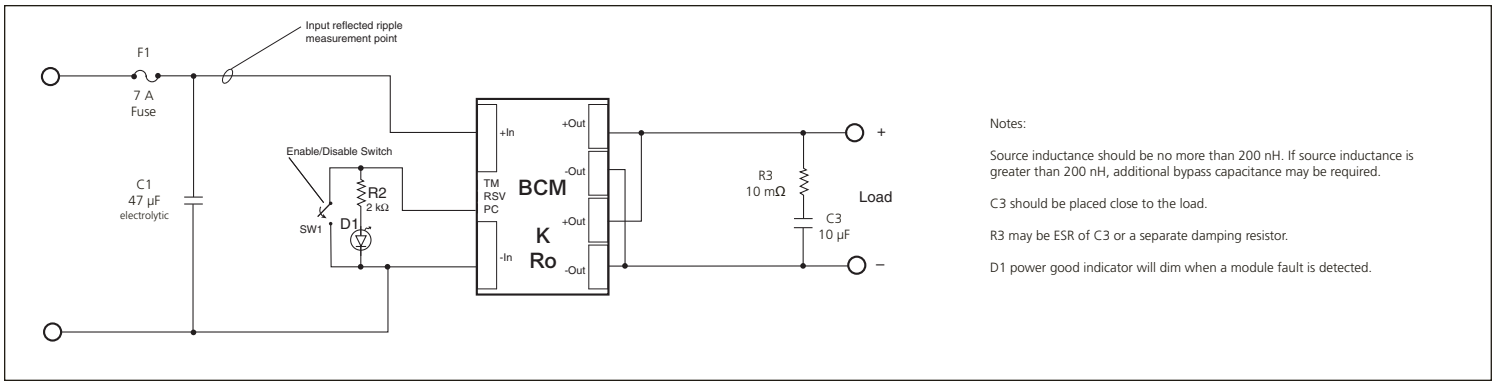



***Figure 20*** *— BCM test circuit*

## V•I Chip Bus Converter Level 1 DC Behavioral Model for 48 V to 9.6 V, 240 W

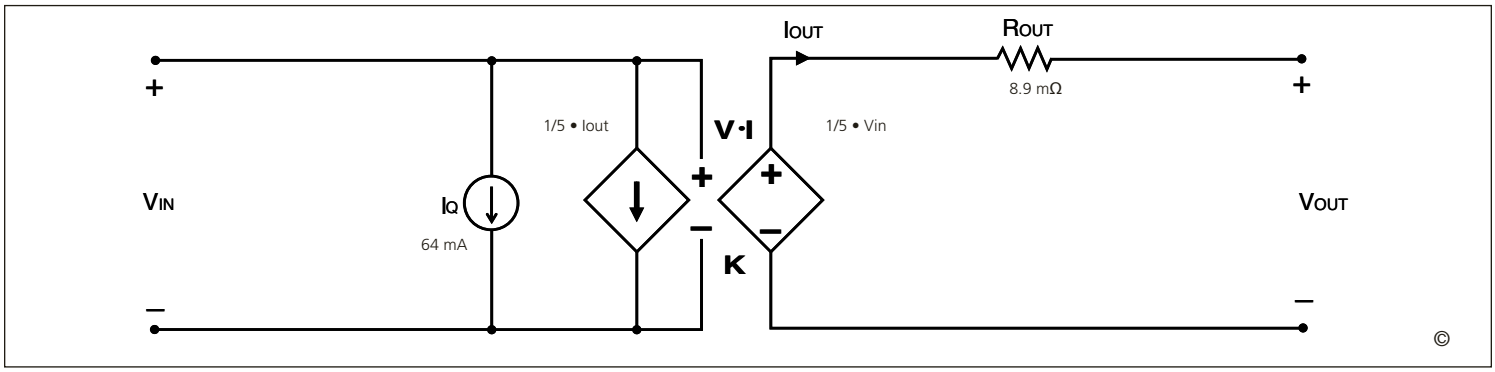



***Figure 21*** *— This model characterizes the DC operation of the V•I Chip bus converter, including the converter transfer function and its losses. The model enables estimates or simulations of output voltage as a function of input voltage and output load, as well as total converter power dissipation or heat generation.*

## V•I Chip Bus Converter Level 2 Transient Behavioral Model for 48 V to 9.6 V, 240 W

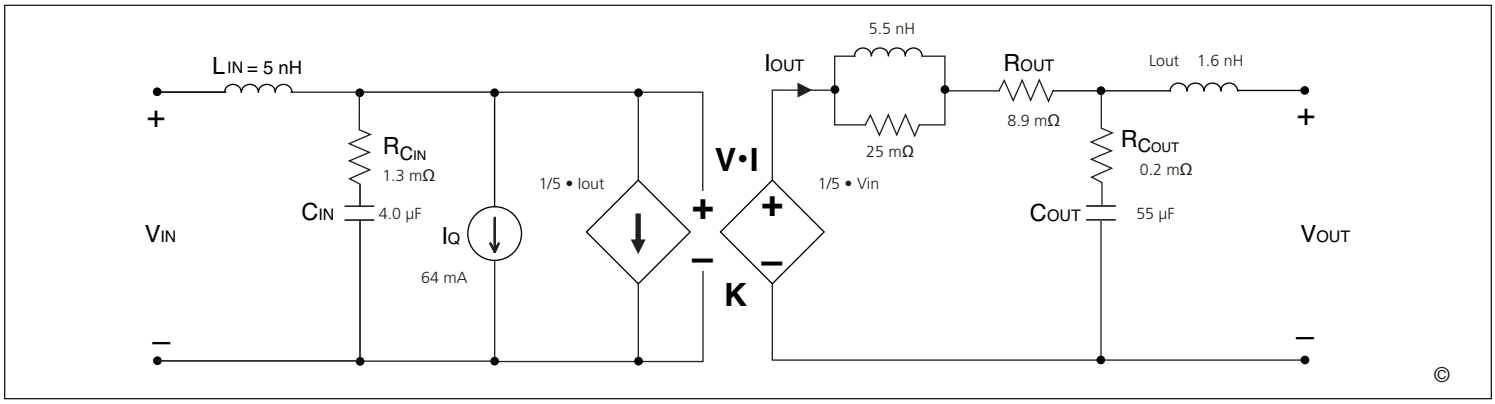



***Figure 22*** *— This model characterizes the AC operation of the V•I Chip bus converter including response to output load or input voltage transients or steady state modulations. The model enables estimates or simulations of input and output voltages under transient conditions, including response to a stepped load with or without external filtering elements.*

## Warranty

Vicor products are guaranteed for two years from date of shipment against defects in material or workmanship when in normal use and service. This warranty does not extend to products subjected to misuse, accident, or improper application or maintenance. Vicor shall not be liable for collateral or consequential damage. This warranty is extended to the original purchaser only.

EXCEPT FOR THE FOREGOING EXPRESS WARRANTY, VICOR MAKES NO WARRANTY, EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

Vicor will repair or replace defective products in accordance with its own best judgement. For service under this warranty, the buyer must contact Vicor to obtain a Return Material Authorization (RMA) number and shipping instructions. Products returned without prior authorization will be returned to the buyer. The buyer will pay all charges incurred in returning the product to the factory. Vicor will pay all reshipment charges if the product was defective within the terms of this warranty.

Information published by Vicor has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. Vicor reserves the right to make changes to any products without further notice to improve reliability, function, or design. Vicor does not assume any liability arising out of the application or use of any product or circuit; neither does it convey any license under its patent rights nor the rights of others. Vicor general policy does not recommend the use of its components in life support applications wherein a failure or malfunction may directly threaten life or injury. Per Vicor Terms and Conditions of Sale, the user of Vicor components in life support applications assumes all risks of such use and indemnifies Vicor against all damages.

## Vicor's comprehensive line of power solutions includes high density AC-DC and DC-DC modules and accessory components, fully configurable AC-DC and DC-DC power supplies, and complete custom power systems.

Information furnished by Vicor is believed to be accurate and reliable. However, no responsibility is assumed by Vicor for its use. Vicor components are not designed to be used in applications, such as life support systems, wherein a failure or malfunction could result in injury or death. All sales are subject to Vicor's Terms and Conditions of Sale, which are available upon request.

## Specifications are subject to change without notice.

## Intellectual Property Notice

Vicor and its subsidiaries own Intellectual Property (including issued U.S. and Foreign Patents and pending patent applications) relating to the products described in this data sheet. Interested parties should contact Vicor's Intellectual Property Department.

The products described on this data sheet are protected by the following U.S. Patents Numbers:
5,945,130; 6,403,009; 6,710,257; 6,911,848; 6,930,893; 6,934,166; 6,940,013; 6,969,909; 7,038,917; 7,166,898; 7,187,263; 7,361,844; D496,906; D505,114; D506,438; D509,472 and for use under 6,975,098 and 6,984,965

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