

Silicon PNP Power Transistors

2SB1419

DESCRIPTION

- With TO-3PL package
- Wide area of safe operation
- Low collector saturation voltage

APPLICATIONS

- For low frequency and high power amplifier applications

PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector;connected to mounting base
3	Base

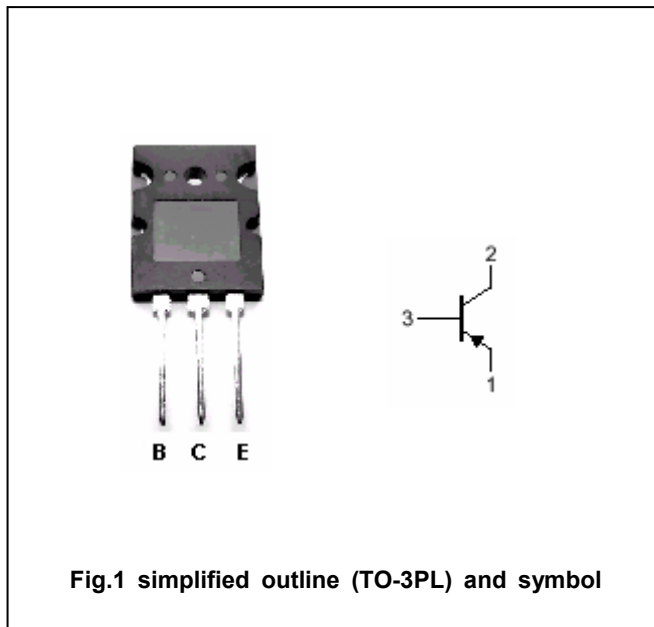


Fig.1 simplified outline (TO-3PL) and symbol

Absolute maximum ratings(Ta=25°C)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	Open emitter	-160	V
V _{CEO}	Collector-emitter voltage	Open base	-160	V
V _{EBO}	Emitter-base voltage	Open collector	-5	V
I _C	Collector current		-12	A
I _{CM}	Collector current-peak		-20	A
P _C	Collector power dissipation	T _C =25°C	120	W
T _j	Junction temperature		150	°C
T _{stg}	Storage temperature		-55~150	°C

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CHARACTERISTICS

T_j=25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-50mA ; I _B =0	-160			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-8A ; I _B =-0.8A			-1.8	V
V _{BE}	Base-emitter voltage	I _C =-8A ; V _{CE} =-5V			-1.8	V
I _{CBO}	Collector cut-off current	V _{CB} =-160V ; I _E =0			-50	μA
I _{EBO}	Emitter cut-off current	V _{EB} =-5V ; I _C =0			-50	μA
h _{FE-1}	DC current gain	I _C =-20mA ; V _{CE} =-5V	20			
h _{FE-2}	DC current gain	I _C =-1A ; V _{CE} =-5V	60		200	
h _{FE-3}	DC current gain	I _C =-8A ; V _{CE} =-5V	20			

◆ h_{FE-2} classifications

Q	S	P
60-120	80-160	100-200

