

## H5N2001LD, H5N2001LS, H5N2001LM

Silicon N Channel MOS FET  
High Speed Power Switching

REJ03G1339-0600

Rev.6.00

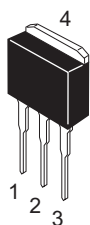
Jul 14, 2006

### Features

- Low on-resistance
- Low leakage current
- High speed switching

### Outline

RENESAS Package code: PRSS0004AE-A  
(Package name: LDKPAK (L) )



H5N2001LD

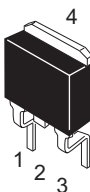
RENESAS Package code: PRSS0004AE-B  
(Package name: LDKPAK (S)-(1) )



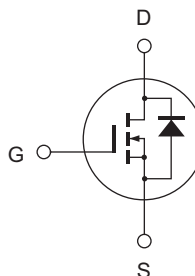
H5N2001LS

1. Gate
2. Drain
3. Source
4. Drain

RENESAS Package code: PRSS0004AE-C  
(Package name: LDKPAK (S)-(2) )



H5N2001LM



## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V <sub>DSS</sub>	200	V
Gate to source voltage	V <sub>GSS</sub>	±30	V
Drain current	I <sub>D</sub>	20	A
Drain peak current	I <sub>D (pulse)</sub> <sup>Note 1</sup>	80	A
Body to drain diode reverse drain current	I <sub>DR</sub>	20	A
Body to drain diode reverse drain peak current	I <sub>DR (pulse)</sub> <sup>Note 1</sup>	80	A
Avalanche current	I <sub>AP</sub> <sup>Note 3</sup>	20	A
Channel dissipation	P <sub>ch</sub> <sup>Note 2</sup>	75	W
Channel to case Thermal Impedance	θ <sub>ch-c</sub>	1.67	°C/W
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C

- Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%  
 2. Value at T<sub>c</sub> = 25°C  
 3. T<sub>ch</sub> ≤ 150°C

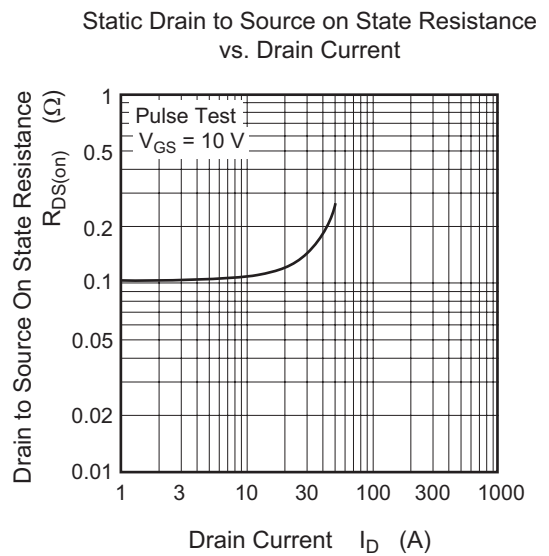
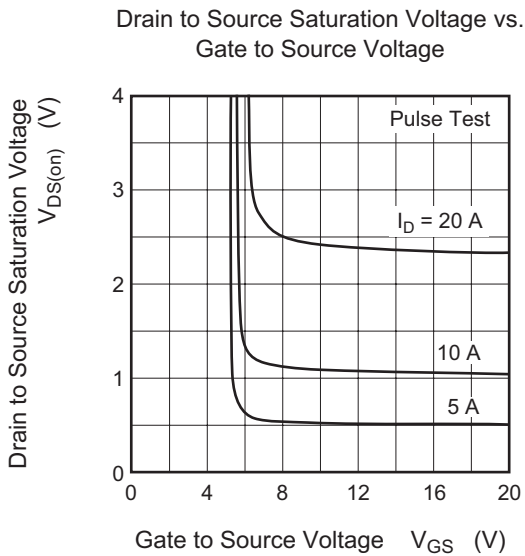
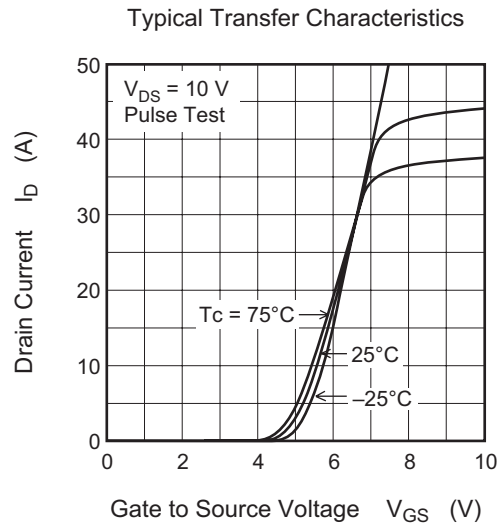
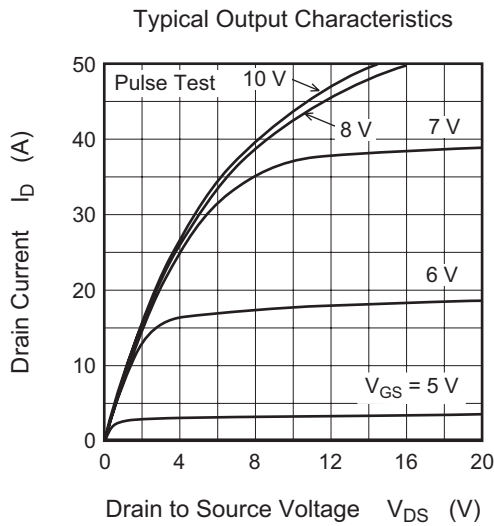
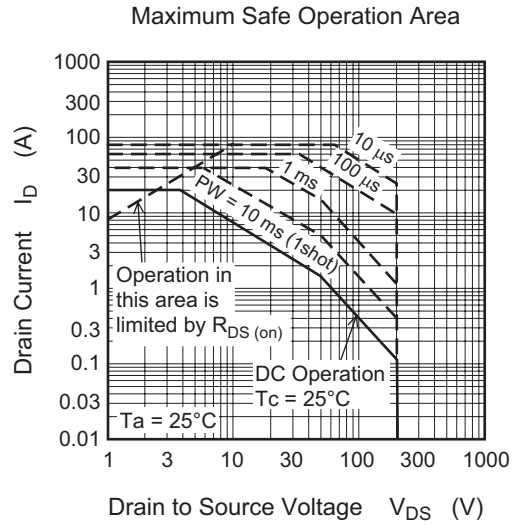
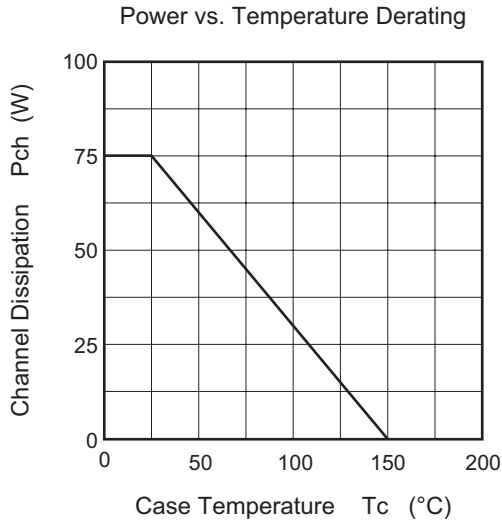
## Electrical Characteristics

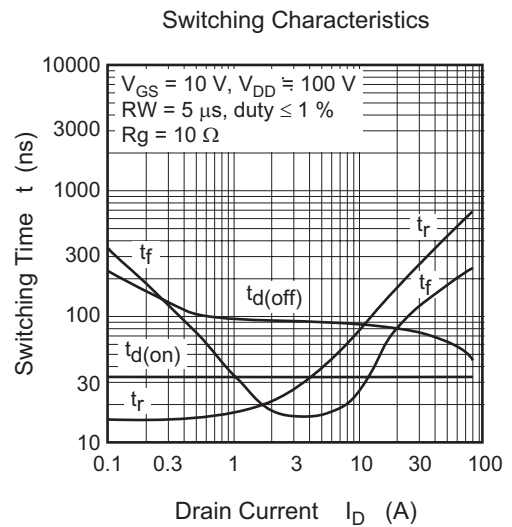
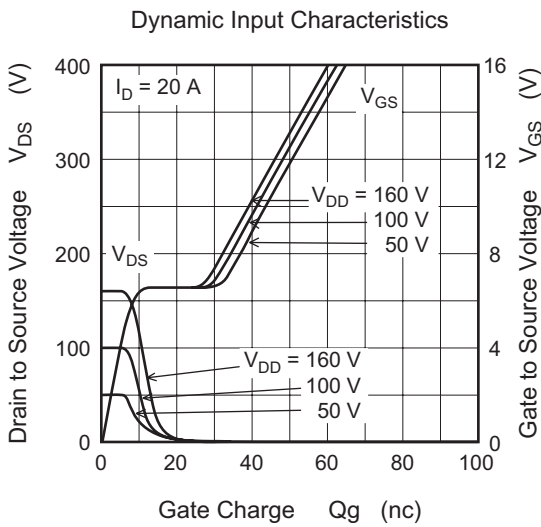
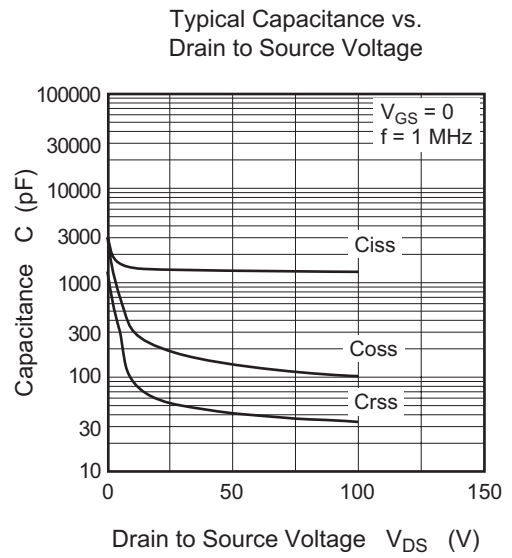
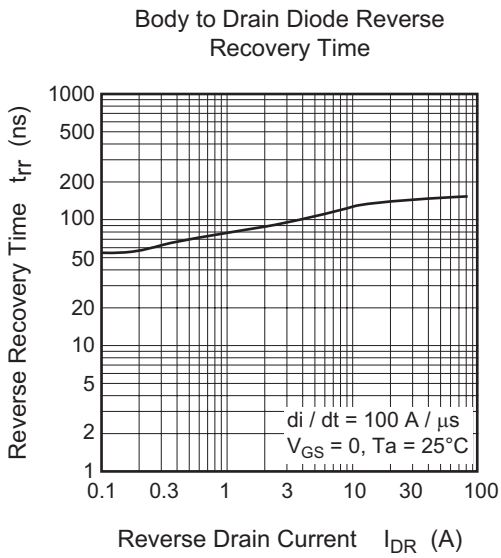
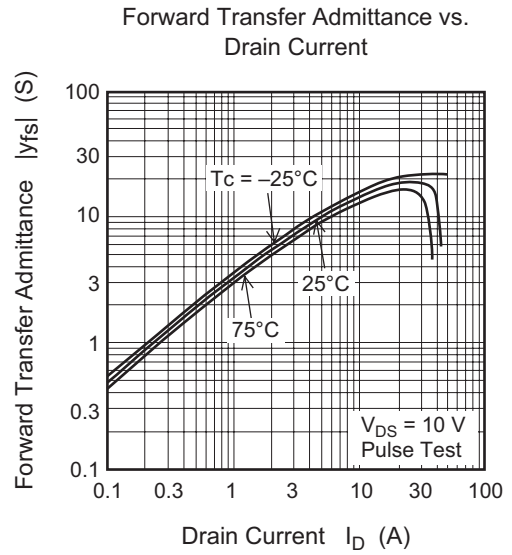
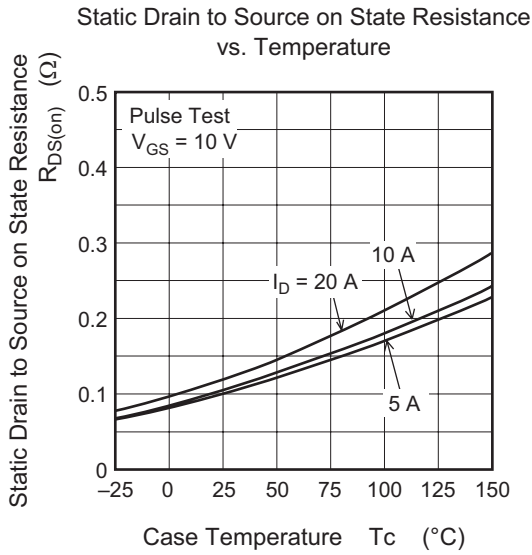
(Ta = 25°C)

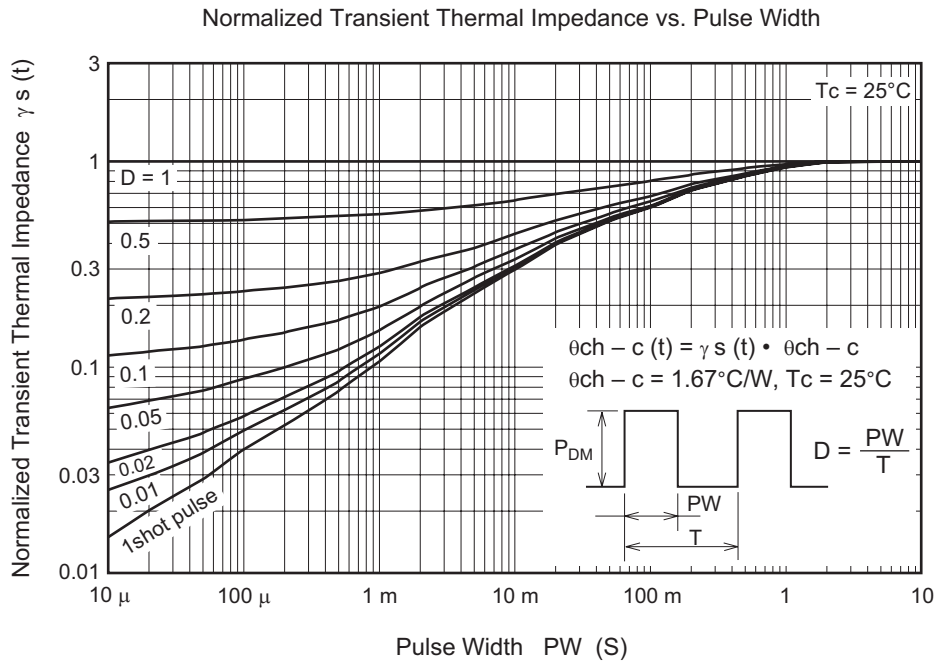
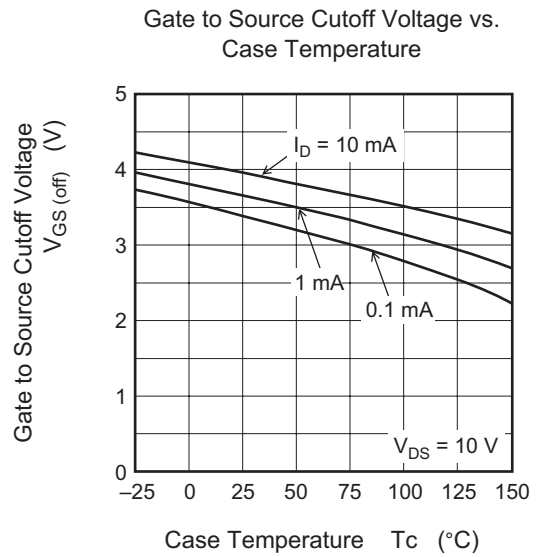
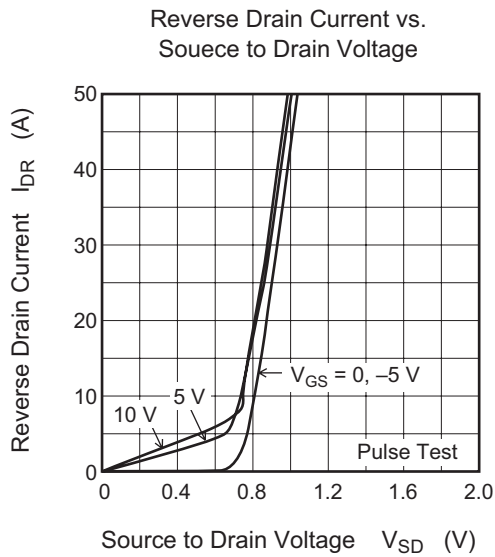
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V <sub>(BR)DSS</sub>	200	—	—	V	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0
Gate to source leak current	I <sub>GSS</sub>	—	—	±0.1	μA	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0
Zero gate voltage drain current	I <sub>DSS</sub>	—	—	1	μA	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0
Gate to source cutoff voltage	V <sub>GS (off)</sub>	3.0	—	4.5	V	I <sub>D</sub> = 1 mA, V <sub>DS</sub> = 10 V
Static drain to source on state resistance	R <sub>DS (on)</sub>	—	0.100	0.125	Ω	I <sub>D</sub> = 10 A, V <sub>GS</sub> = 10 V <sup>Note 4</sup>
Forward transfer admittance	y <sub>fs</sub>	8	14	—	S	I <sub>D</sub> = 10 A, V <sub>DS</sub> = 10 V <sup>Note 4</sup>
Input capacitance	C <sub>iss</sub>	—	1350	—	pF	V <sub>DS</sub> = 25 V
Output capacitance	C <sub>oss</sub>	—	180	—	pF	V <sub>GS</sub> = 0
Reverse transfer capacitance	C <sub>rss</sub>	—	55	—	pF	f = 1 MHz
Turn-on delay time	t <sub>d (on)</sub>	—	35	—	ns	I <sub>D</sub> = 10 A
Rise time	t <sub>r</sub>	—	70	—	ns	R <sub>L</sub> = 10 Ω
Turn-off delay time	t <sub>d (off)</sub>	—	85	—	ns	V <sub>GS</sub> = 10 V
Fall time	t <sub>f</sub>	—	20	—	ns	R <sub>g</sub> = 10 Ω
Total gate charge	Q <sub>g</sub>	—	44	—	nC	V <sub>DD</sub> = 160 V
Gate to source charge	Q <sub>gs</sub>	—	8	—	nC	V <sub>GS</sub> = 10 V
Gate to drain charge	Q <sub>gd</sub>	—	22	—	nC	I <sub>D</sub> = 20 A
Body to drain diode forward voltage	V <sub>DF</sub>	—	0.9	1.4	V	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0 <sup>Note4</sup>
Body to drain diode reverse recovery time	t <sub>rr</sub>	—	140	—	ns	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0
Body to drain diode reverse recovery charge	Q <sub>rr</sub>	—	0.7	—	μC	di <sub>F</sub> /dt = 100 A/μs

- Note: 4. Pulse test

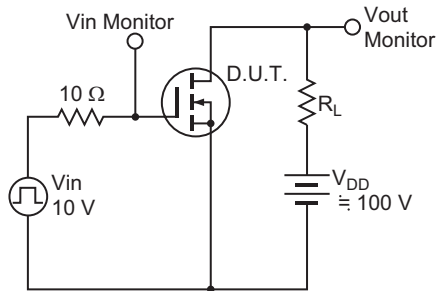
Main Characteristics



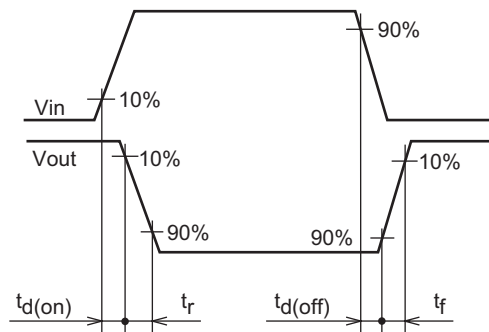




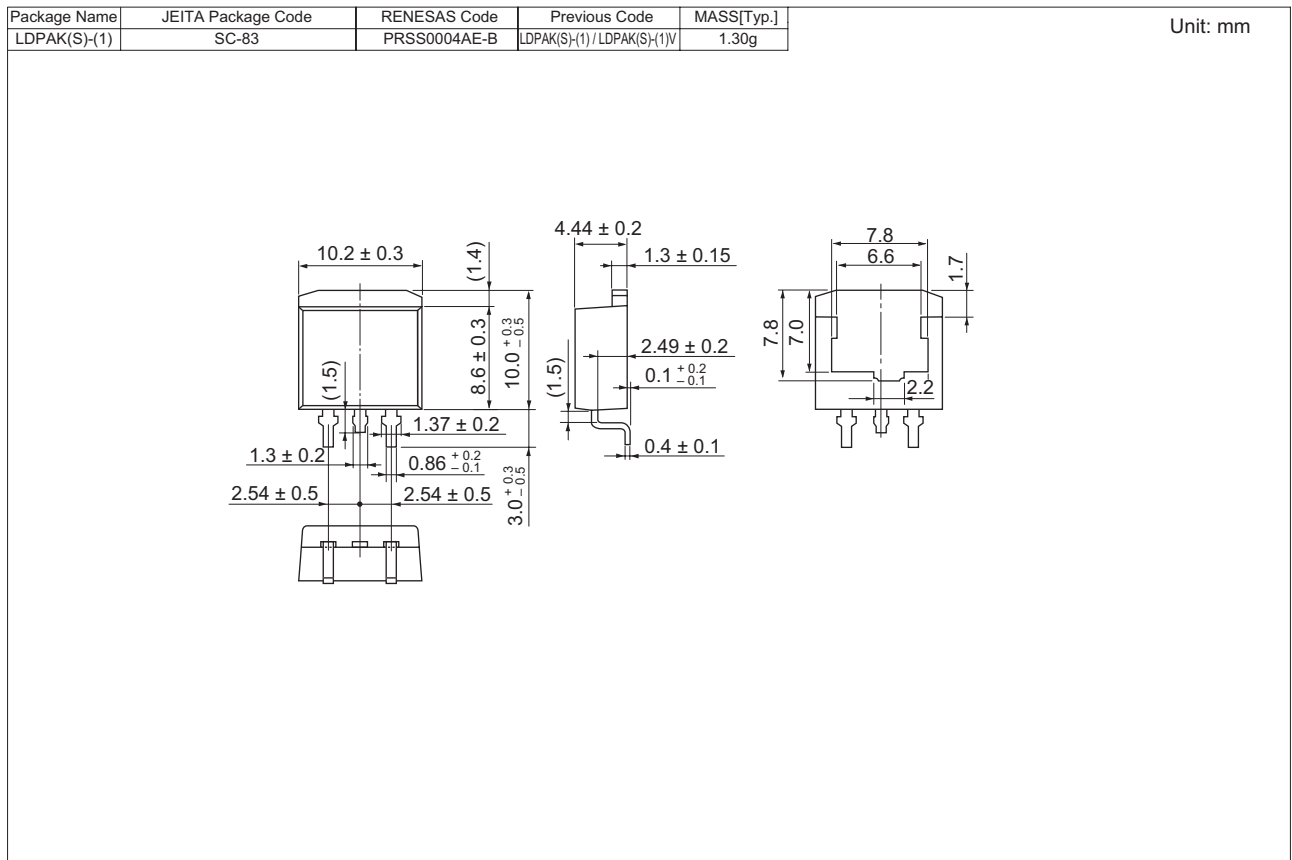
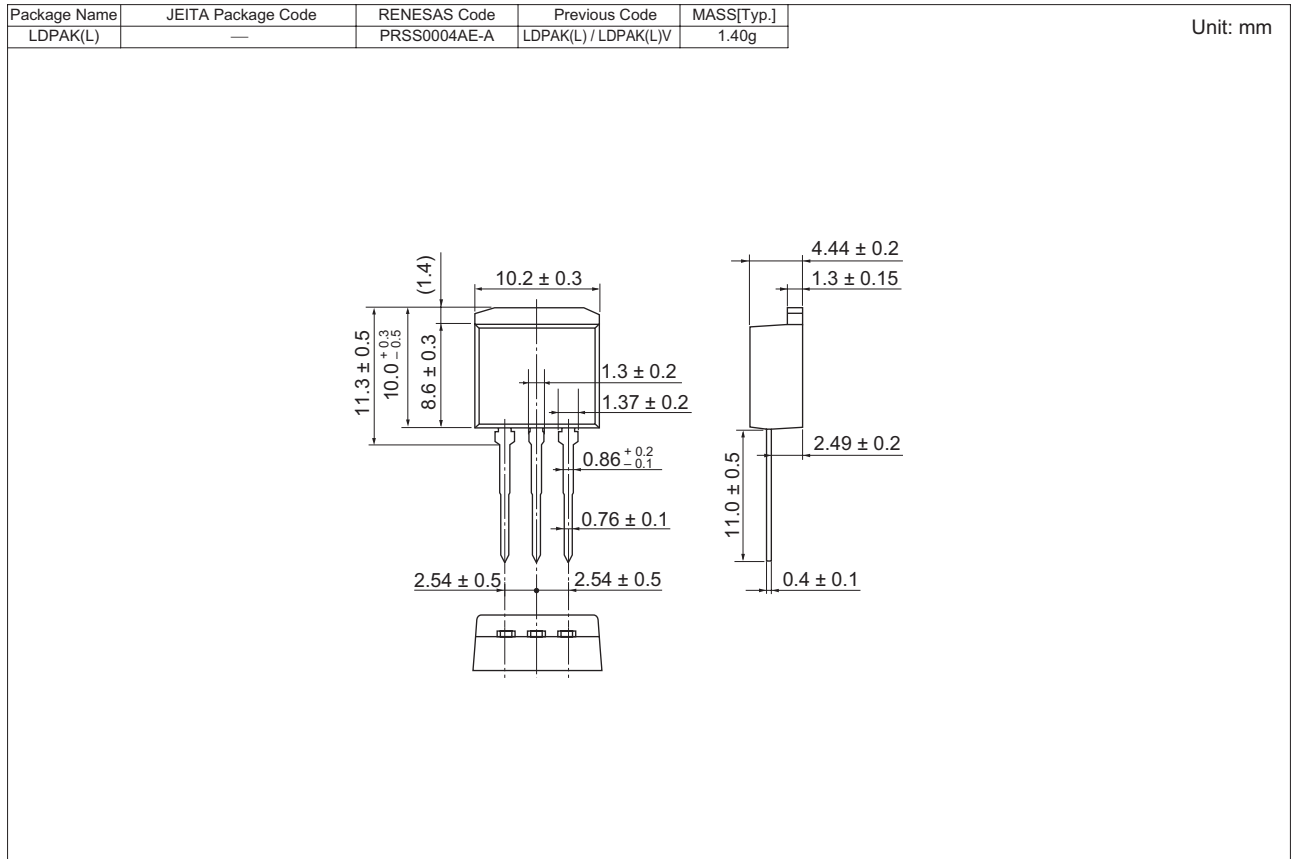
Switching Time Test Circuit



Switching Time Waveform



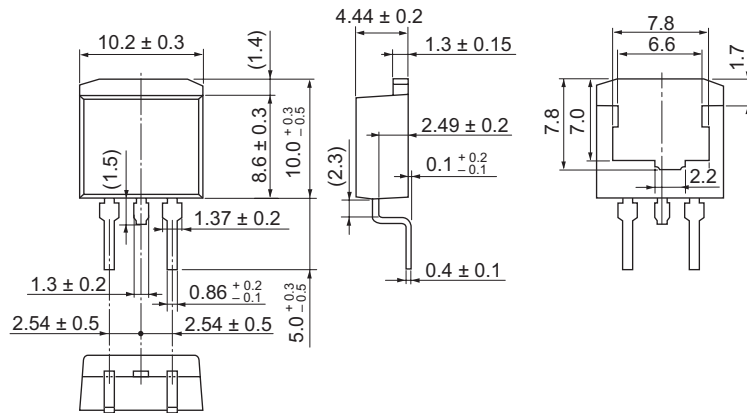
Package Dimensions



## H5N2001LD, H5N2001LS, H5N2001LM

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDBPAK(S)-(2)	—	PRSS0004AE-C	LDBPAK(S)-(2) / LDBPAK(S)-(2)V	1.35g

Unit: mm



## Ordering Information

Part Name	Quantity	Shipping Container
H5N2001LD-E	500 pcs	Box (Conductive Sack)
H5N2001LSTL-E	1000 pcs	Taping
H5N2001LMTL-E	1000 pcs	Taping

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